



A New Direction in Mixed-Signal

October 2013

ANP-41

Powering the Zynq-7000 All Programmable SoC with XRP7714

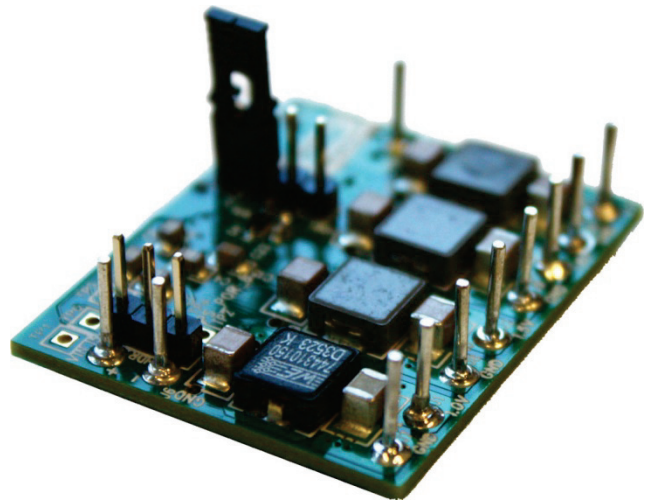
Rev. 2.0.0

GENERAL DESCRIPTION

This reference design is a complete four output power system designed to power a Xilinx Zynq-7000 All Programmable (AP) SoC and associated DDR3 memory. The power system provides 1.0V, 1.5V, 0.75V, 1.8V, and 2.5V in a 1.5" x 1.25" solution. The order and ramp rates for each supply are programmed to accommodate Zynq-7000 AP SoC sequencing requirements. All power supply operations can be controlled over an I²C interface. Faults, output voltages and currents can also be monitored. Four GPIO signals are available and can be programmed to provide the status of power good signals, enables, and faults. Unused GPIO pins can be programmed for use as I/O expansion. The board is supported by PowerArchitect™ 4.x and connects to the Exar Communications Module (XRP77XXEVB-XCM).

FEATURES

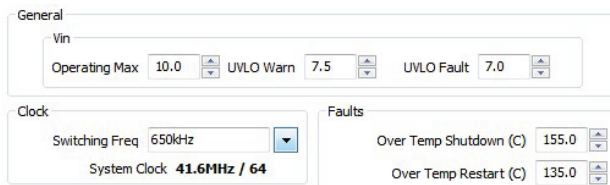
- **Xilinx Zynq-7000 All Programmable SoC Power System**
 - 4 Channel Power System using XRP7714 Programmable Digital PWM Switching Controller
- **Validated in actual end system**
- **I²C Interface**
 - Programming
 - Monitoring
 - Control



ZYNQ-7000 AP SOC POWER SOLUTION

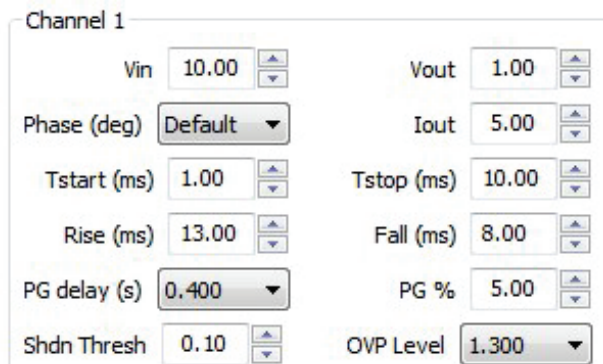
The Zynq-7000 AP SoC power reference design provides 4 output voltages. The order and ramp rates for each output are programmed to accommodate Zynq-7000 AP SoC sequencing requirements.

The power system was designed to operate at 650kHz as a good trade-off between space and efficiency.



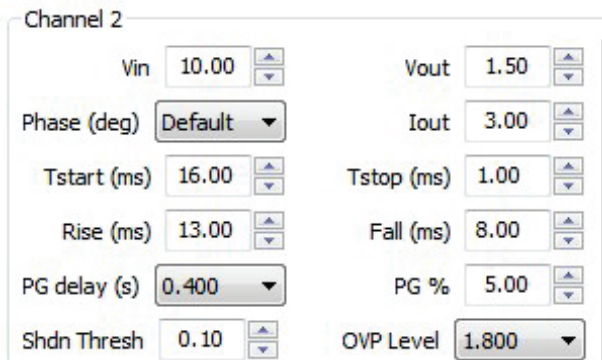
Output 1/Channel 1 Configuration

Channel 1 is designed to provide 1V to VCCINT, VCCBRAM and VCCPINT Zynq-7000 AP SoC rails at 5A.



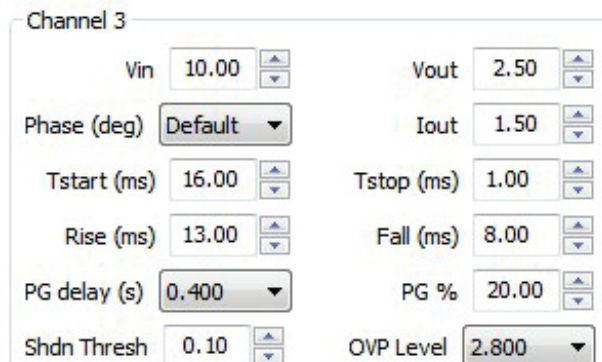
Output 2/Channel 2 Configuration

Channel 2 provides 1.5V to the DDR3 SDRAM subsystem as well as the DDR3 block inside the Zynq-7000 AP SoC. In addition, it sources the XRP2997 DDR Bus Termination Regulator which provides termination voltage for the DDR3 SDRAM signals. The channel is designed to support a 3A load.



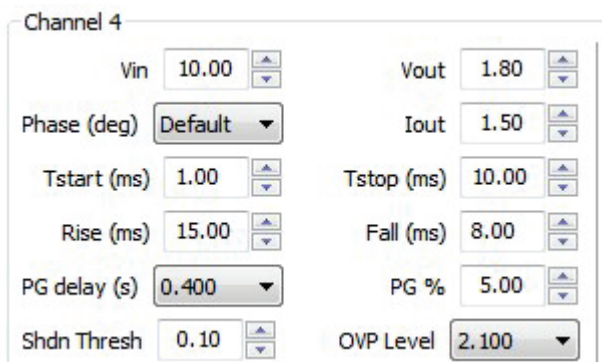
Output 3/Channel 3 Configuration

Channel 3 provides 2.5V to Zynq-7000 AP SoC IO banks (VCCO) and peripherals in the system. It is designed to support a 1.5A load.



Output 4/Channel 4 Configuration

Channel 4 is designed to provide 1.8V to VCCAUX and VCCPLL Zynq-7000 AP SoC rails at 1.5A.



LDOOUT

LDOOUT is routed to XRP2997 control pin enabling the device.

CHANNEL SEQUENCING

The XRP7714 sequencing has been designed to meet the Zynq-7000 AP SoC power up sequencing requirements.

Power-On Sequencing

- 1. 1.0V** supply with 0.077V/msec ramp rate
- 2. 1.8V** supply with 0.12V/msec ramp rate
- 3. 1.5V and 2.5V supplies** - the 1.5V supply with 0.115V/msec ramp rate reaching the target level at the same time as the 2.5V supply with 0.192V/msec ramp rate.



Power-Down Sequencing

- 1. 1.5V and 2.5V supplies** - the 1.5V supply following 0.1875V/msec ramp down rate; the 2.5V supply following 0.3125V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.
- 2. 1.0V and 1.8V supplies** - the 1.0V supply following 0.125V/msec ramp down rate; the 1.8V supply following 0.225V/msec ramp down rate. Both channels regulate down to the shutdown threshold of 100mV before switching stops.

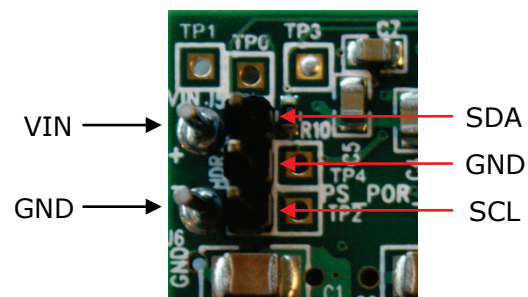


ZYNQ-7000 AP SoC POWER ON RESET

XRP7714 will generate a power on reset signal on GPIO3 to the Zynq-7000 AP SoC 400ms after the last rail is in regulation.

POWERING UP THE BOARD

The board hardware is provided capable of supporting an input voltage range of 5.5V to 20V with power connected directly to J5 (VIN) and J6 (GND). Putting a jumper on HDR1 allows the board to be powered from an input voltage of 5V±5%.



I²C Interface

The Zynq-7000 AP SoC power reference design schematic shows an I²C interface connector (HDR2) to connect the Exar Communications Module (XRP77XXEVB-XCM which has it's own users guide available). This provides an interface with PowerArchitect™ 4.x allowing programming of the board.

Powering the Zynq-7000 All Programmable SoC with XRP7714

Ensure the XCM is configured to use the on board pull-up resistors (check jumper settings).

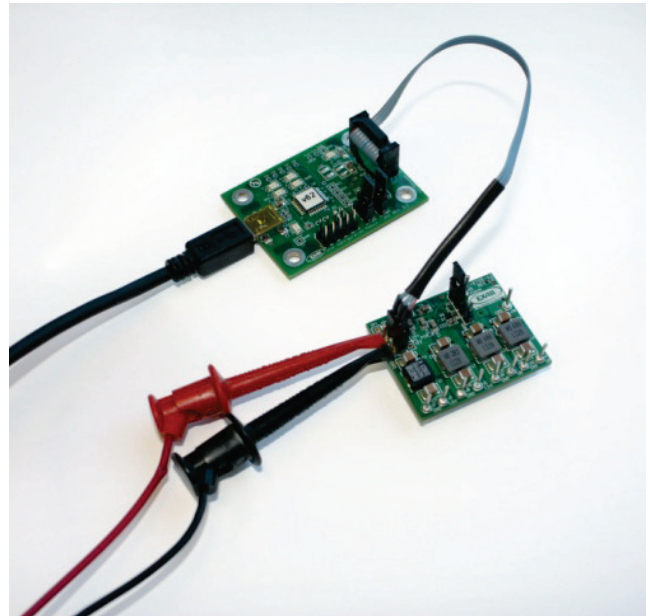
If communication between Zynq-7000 AP SoC and XRP7714 is desired, ensure that the Zynq-7000 AP SoC system board has pull-up resistors installed.

For more information how to implement power subsystem control and monitoring via I²C bus refer to ANP-31.

Configuring the Board

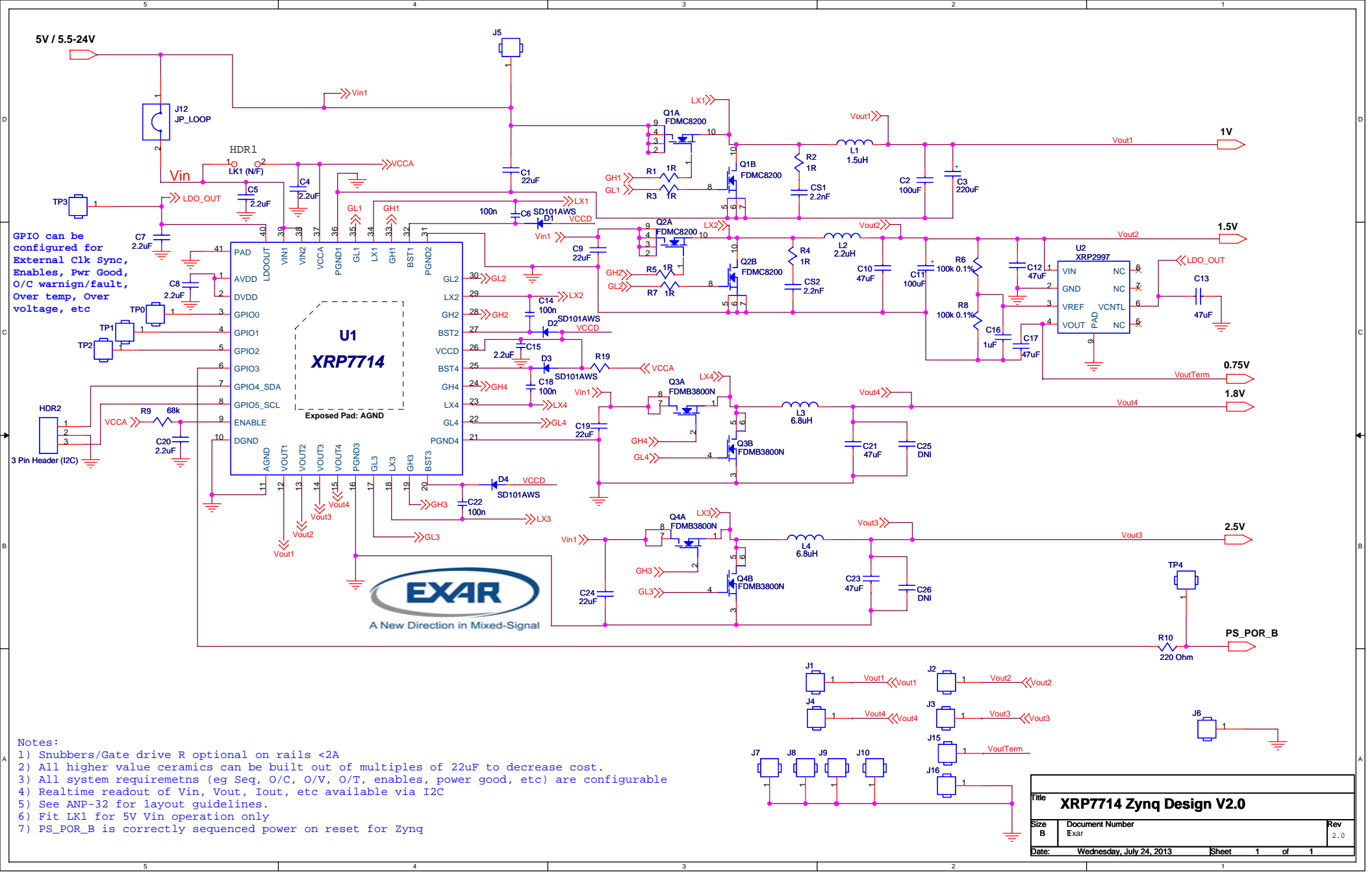
The board is typically delivered with a XRP7714 which has not yet had its OTP memory burned with a specific configuration. This allows the user to select a different VIO voltage or DDR memory voltage than the one used in the default configuration file available from Exar's web site.

<http://www.exar.com/power-management/power-conversion/switching-regulators/step-down-regulators/zynq-evb>



5V / 5.5-24V

GPIO can be configured for External Clk Sync, Enables, Pwr Good, O/C warnign/fault, Over temp, Over voltage, etc



- Notes:
- 1) Snubbers/Gate drive R optional on rails <2A
 - 2) All higher value ceramics can be built out of multiples of 22uF to decrease cost.
 - 3) All system requiremetns (eg Seq, O/C, O/V, O/T, enables, power good, etc) are configurable
 - 4) Realtime readout of Vin, Vout, Iout, etc available via I2C
 - 5) See ANP-32 for layout guidelines.
 - 6) Fit LK1 for 5V Vin operation only
 - 7) PS_POR_B is correctly sequenced power on reset for Zynq

Title		
XRP7714 Zynq Design V2.0		
Size B	Document Number	Rev
	Exar	2.0
Date:	Wednesday, July 24, 2013	Sheet 1 of 1



A New Direction in Mixed-Signal

Powering the Zynq-7000 All Programmable SoC with XRP7714

BILL OF MATERIAL

Ref.	Qty	Manufacturer	Part Number	Size	Component
U1	1	EXAR	XRP7714ILB-F	40-TQFN	XRP7714 PWM Step-Down DC/DC Controller
U2	1	EXAR	XRP2997	8-SOIC	2A DDR I/II/III Bus Termination Regulator
Q1,Q2	1	Fairchild	FDMC8200	Power 33	Dual N-Channel PowerTrench MOSFET 30V, 9.5mOhm & 20mOhm
Q3,Q4	3	Fairchild	FDMB3800N	MicroFET 3x1.9	Dual N-Channel PowerTrench MOSFET 30V, 4.8A, 40mOhm
D1,D2,D3,D4	4	Vishay	SD101AWS-V-GS08	SOD323	Small Signal Schottky Diode 60V, 30mA
L1	1	Würth Elektronik	744310150	7.3x6.8mm	Inductor 1.5uH, 12.7mOhm, 7.5A
L2	1	Würth Elektronik	74437346022	7.3x6.8mm	Inductor 2.2uH, 20mOhm, 6.5A
L3, L4	2	Würth Elektronik	74437346068	7.3x6.8mm	Inductor 6.8uH, 60mOhm, 3.4A
C1,C9,C19,C24	4	Murata	GRM32ER71E226KE15L	1210	Capacitor Ceramic 22uF, 25V, X7R
C2	1	Murata	GRM32ER60J107ME20L	1210	Capacitor Ceramic 100uF, 6.3V, X5R
C3	1	SANYO/Panasonic	EEF-SX0E221R	7343	Capacitor POSCAP, 220uF
C4,C5,C7,C8,C15,C20	6	Murata	GRM21BR71E225KA73L	0805	Capacitor Ceramic 2.2uF, 25V, X7R
C6,C14,C18,C22	4	Murata	GRM188R71H104KA93D	0603	Capacitor Ceramic 0.1uF, 50V, X7R
C10,C21,C23	3	Murata	GRM32ER71A476KE15L	1210	Capacitor Ceramic, 47uF, 10V, X7R
C11	1	SANYO/Panasonic	EEF-SX0G101R	7343	Capacitor POSCAP, 100uF
C12,C13,C17	3	Murata	GRM31CR60J476KE19L	1206	Capacitor Ceramic 47uF, 6.3V, X5R
C16	1	Murata	GRM21BR71H105KA12L	0805	Capacitor Ceramic, 1uF, 50V, X7R
CS1, CS2	2	Murata	GRM188R71H222KA01D	0603	Capacitor Ceramic 2200pF, 50V, X7R
R1,R2,R3,R4,R5,R7	6	Panasonic	ERJ-3RQF1R0V	0603	Chip Resistor 1 Ohm, 1%, 1/10W
R6,R8	2	Panasonic	ERA-3EAB104V	0603	Chip Resistor 100K Ohm, 1/10w, 0.1%
R9	1	Panasonic	ERJ-3EKF6802V	0603	Chip Resistor 68K Ohm, 1/10w, 1%
R10	1	Panasonic	ERJ-3EKF2200V	0603	Chip Resistor 220 Ohm, 1/10W, 1%
R19	1	Panasonic	ERJ-3EKF10R0V	0603	Chip Resistor 10 Ohm, 1/10W, 1%
HDR1, J12	2	Würth Elektronik	61300211121	0.1"	2 Pin Header
HDR2	1	Würth Elektronik	61300311121	0.1"	3 Pin Header
J1-J10,J15,J16	12	Vector Elektronik	K30C/M	.042" Hole	PCB Pin



A New Direction in Mixed-Signal

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	04/09/2013	Initial release of document
1.0.1	05/08/2013	Changed the document name
2.0.0	10/18/2013	Changes to the schematics, configuration and bill of materials. Clarification on power up procedure. Added web link for config file.

FOR FURTHER ASSISTANCE

Email:

powertechsupport@exar.com

customersupport@exar.com

Exar Technical Documentation:

[http://www.exar.com/TechDoc/default.aspx?](http://www.exar.com/TechDoc/default.aspx)



A New Direction in Mixed-Signal

EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road

Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000

Fax: +1 (510) 668-7030

www.exar.com

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.