



# **XR21B14xx, XR21V14xx USB UARTs**

## Design Guide

## Revision History

Document No.	Release Date	Change Description
202DGR00	4/20/20	Initial release.
202DGR01	5/4/20	Minor typo correction in the Introduction.

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## Introduction

The XR21B14xx and XR21V14xx Design Guide provides a helpful checklist of schematic design and PCB layout tips to aid in applying a XR21B14xx or XR21V14xx USB UART to your PCB design. The XR21B1420/2/4 Family and XR21V14xx Family with 1, 2 or 4 UARTs have a USB 2.0 interface fully compliant to Full Speed (12Mbps), while the XR21B1421 UART has an HID class USB interface. The XR21B14xx Family has an on-chip One-Time Programmable (OTP) memory.

Please refer to the respective XR21B14xx or XR21V14xx Data Sheet for more information.

## Reference Documentation

[XR21B1411](#) Data Sheet

[XR21B1420](#) Data Sheet

[XR21B1421](#) Data Sheet

[XR21B1422](#) Data Sheet

[XR21B1424](#) Data Sheet

[XR21V1410](#) Data Sheet

[XR21V1412](#) Data Sheet

[XR21V1414](#) Data Sheet

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## Pin Groups

The tables below are arranged by the following pin groups:

- USB
- USB UART "Special Handling" Device Pins
- Voltage Rails
- General PCB Layout

## Design and Layout Recommendations

**Table 1: USB**

Schematic Design Recommendations
Ensure there are no external components on <b>USBD+ / USB-</b> unless tested in compliance with the USB 2.0 spec. For example, no series resistance, inductance or capacitance. No shunt capacitance. Exceptions are ESD protection diodes, EMI filters that have demonstrated compliance with USB 2.0 high speed signaling.
Layout Recommendations
<b>USBD+ / USB-</b> are full speed USB signaling at 12MHz. Ensure 90Ω differential impedance.
<b>USBD+ / USB-</b> should not be routed over a split reference plane.
<b>USBD+ / USB-</b> should be length matched, ideally to within ±50 mils.
<b>USBD+ / USB-</b> should have no stubs on these traces greater than 200 mils, for example to test points.

**Table 2: USB UART "Special Handling" Device Pins**

Schematic Design Recommendations
Connect <b>VBUS_SENSE</b> , using pin description in the Data Sheet to VBUS power input. Required for proper operation in self-powered USB designs. (Note that as XR21V141x devices are 3.3V $V_{CC}$ , they do not have a VBUS_SENSE pin. Refer to AN-202 for self-powered designs using XR21V141x devices). For XR21B142x designs, use a tantalum capacitor on the VBUS input to the VBUS_SENSE pin.
For XR21B142x devices, decouple <b>3V3_OUT</b> with a minimum of 4.7uF and connect to CAP1 and CAP2 pins.
For USB suspend mode power compliance, use the <b>LOW_PWR# (USB_STAT</b> in XR21B142x devices) output to power down other devices powered by USB VBUS.
Layout Recommendations
Connect <b>XTAL</b> pins with short traces isolated from other high frequency nets.
Connect <b>CNTR_PAD</b> (QFN packages) with multiple thermal vias to power plane for electrical performance.

**Table 3: Voltage Rails**

Schematic Design Recommendations
An in-rush current limiting circuit is recommended (refer to USB UART Evaluation board schematics) to meet USB compliance.
All decoupling capacitors should be implemented without traces to power or ground rails if possible.
Bulk decoupling:
USB requires between 1 and 10uF of bulk capacitance on the VBUS power rail from the USB host. We recommend 4.7uF. In general if no in-rush current limiting circuit is used, a tantalum capacitor is recommended except for embedded applications or applications where no external USB cable will be used. For all other voltage rails (including any external $V_{CC}$ supply voltages to the XR21xxxx device in self-powered mode) a minimum of 10uF of bulk decoupling should be used.
High frequency decoupling:
For all designs, a 100nF high frequency decoupling capacitor is recommended on each power pin, located as close as possible to the device power pin.

**Table 4: General PCB Layout**

Layout Recommendations
A minimum of a 4 layer PCB is critical with 5V or 3.3V power and ground reference planes (2 and 3) and microstrip signal layers (layers 1 and 4).



MaxLinear, Inc.  
5966 La Place Court, Suite 100  
Carlsbad, CA 92008  
760.692.0711 p.  
760.444.8598 f.  
[www.maxlinear.com](http://www.maxlinear.com)

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