GENERAL DESCRIPTION

The XRP6668 is a dual channel synchronous current mode PWM step down (buck) converter capable of delivering up to 1 Amp of current per channel and optimized for portable battery-operated applications.

Based on a current mode 1.5MHz constant frequency PWM control scheme, the XRP6668 reduces the overall component count and solution footprint as well as provides a low output voltage ripple and excellent line and load regulation. It also implements a PFM mode to improve light load efficiency as well as a 100% duty cycle LDO mode. Output voltage is adjustable to as low as 0.6V with a better than 3% accuracy while a low quiescent current supports the most stringent battery operating conditions.

Built-in over temperature and under voltage lock-out protections insure safe operations under abnormal operating conditions.

The XRP6668 is offered in a RoHS compliant, "green"/halogen free 8-pin exposed pad SOIC package.

APPLICATIONS

- **Portable Equipments**
- **Battery Operated Equipments**
- **Audio-Video Equipments**
- **Networking & Telecom Equipments**

FEATURES

- **Dual Channel Step Down Converter**
- **Guaranteed 1A / 1A Output Current**
  - Input Voltage: 2.5V to 5.5V
- **1.5MHz PWM Current Mode Control**
  - PFM Mode Operations at Light Load
  - 100% Duty Cycle LDO Mode Operations
- **Adjustable Output Voltage Range**
  - As Low as 0.6V with ±3% Accuracy
- **Internal Compensation Network**
- **30µA Quiescent Current**
- **Over Temperature & UVLO Protections**
- **RoHS Compliant "Green" / Halogen Free 8-Pin Exposed Pad SOIC Package**

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TYPICAL APPLICATION DIAGRAM

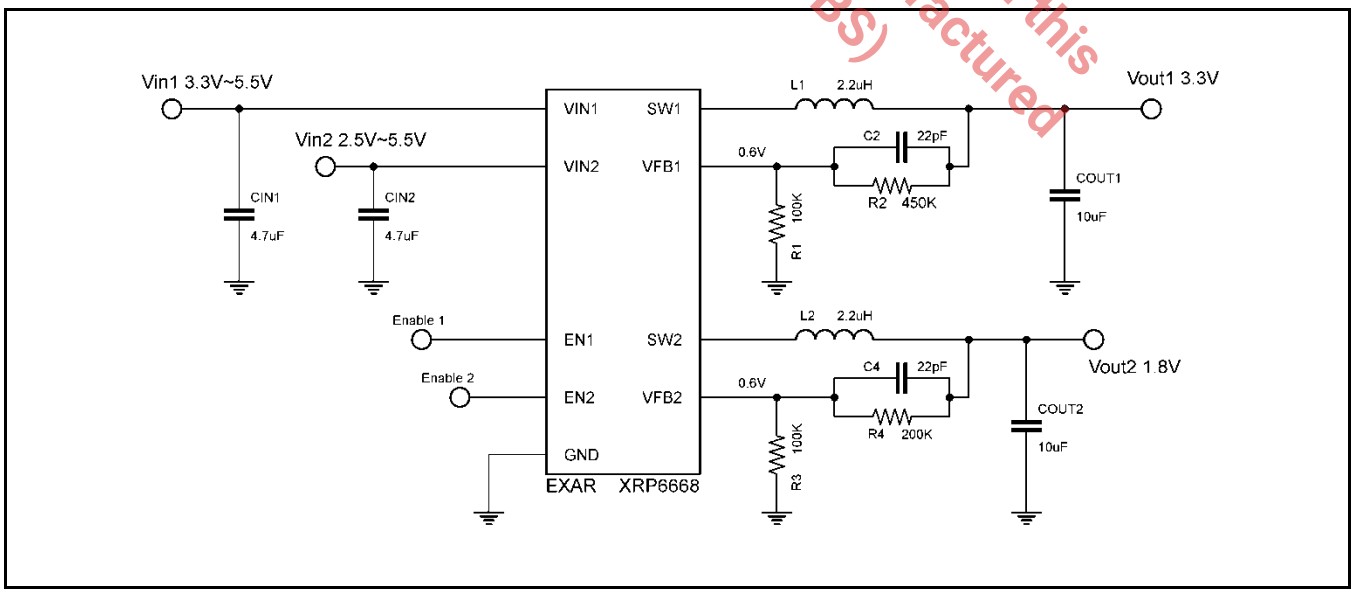


Fig. 1: XRP6668 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage V_{IN} ..... -0.3V to 6.0V
EN, V_{FB} Voltages ..... -0.3V to V_{IN}
SW Voltage ..... -0.3V to (V_{IN} + 0.3V)
Storage Temperature ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
ESD Rating (HBM - Human Body Model) 2kV
ESD Rating (MM - Machine Model) 200V
Junction Temperature (Notes 1, 3) ..... 150°C

OPERATING RATINGS

Input Voltage Range V_{IN} ..... 2.5V to 5.5V
Junction Temperature Range ..... -40°C to 125°C
Thermal Resistance .....
θ_{JA} (8 Pin HSOIC) ..... 42°C/W
θ_{JC} (8 Pin HSOIC) ..... 10°C/W

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ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Ambient Temperature of T_A = 25°C only; limits applying over the full Operating Ambient Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 3.6V, T_A= 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Voltage Range	2.5		5.5	V		
Feedback Current			±100	nA		
Regulated Feedback Voltage	0.588	0.600	0.612	V		
Output Voltage Accuracy	-3		+3	%		I_{OUT}=100mA, V_{IN} = 2.5V to 3.0V
Output Voltage Accuracy	-3		+3	%	•	I_{OUT}=100mA, V_{IN} = 3.0V to 5.5V
Reference Voltage Line Regulation			1	%/V		V_{IN} = 3V to 5.5V
Output Voltage Line Regulation			1	%/V	•	V_{IN} = 3V to 5.5V
Peak Inductor Current	1.5	2.3		A		V_{FB} = 0.5V or V_{OUT} = 90%
PWM Quiescent Current (Note 2)		376		µA		V_{FB} = 0.5V or V_{OUT} = 90%, dual channel
PFM Quiescent Current		30		µA		V_{FB} = 0.65V or V_{OUT} = 108%, dual channel
Shutdown		0.1	1	µA		V_{RUN} = 0V, V_{IN} = 4.2V, dual channel
Oscillator Frequency	1.2	1.5	1.8	MHz	•	V_{FB} = 0.6V or V_{OUT} = 100%
Short-Circuit Oscillator Frequency		900		kHz	•	V_{FB} = 0V or V_{OUT} = 0V
$R_{DS(ON)}$ of PMOS		0.24		Ω		I_{SW} = 100mA
$R_{DS(ON)}$ of NMOS		0.21		Ω		I_{SW} = –100mA
Under Voltage Lock Out		1.8		V		
SW Leakage			±1	µA		V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V
Enable Threshold			1.2	V	•	
Shutdown Threshold	0.4			V	•	
RUN Leakage Current			±1	µA	•	

Note 1: T_J is a function of the ambient temperature T_A and power dissipation P_D: (T_J = T_A + (P_D * θ_{JA}))
Note 2: Dynamic quiescent current is higher due to the gate charge being delivered at the switching frequency.
Note 3: This IC has built-in over-temperature protection to avoid damage from overload conditions.
Note 4: θ_{JA} is measured in the natural convection at TA=25℃ on a high effective thermal conductivity test board (4 layers, 2S2P) of JEDEC 51-5 thermal measurement standard.
Note 5: θ_{JC} represents the resistance to the heat flows the chip to package top case.

BLOCK DIAGRAM

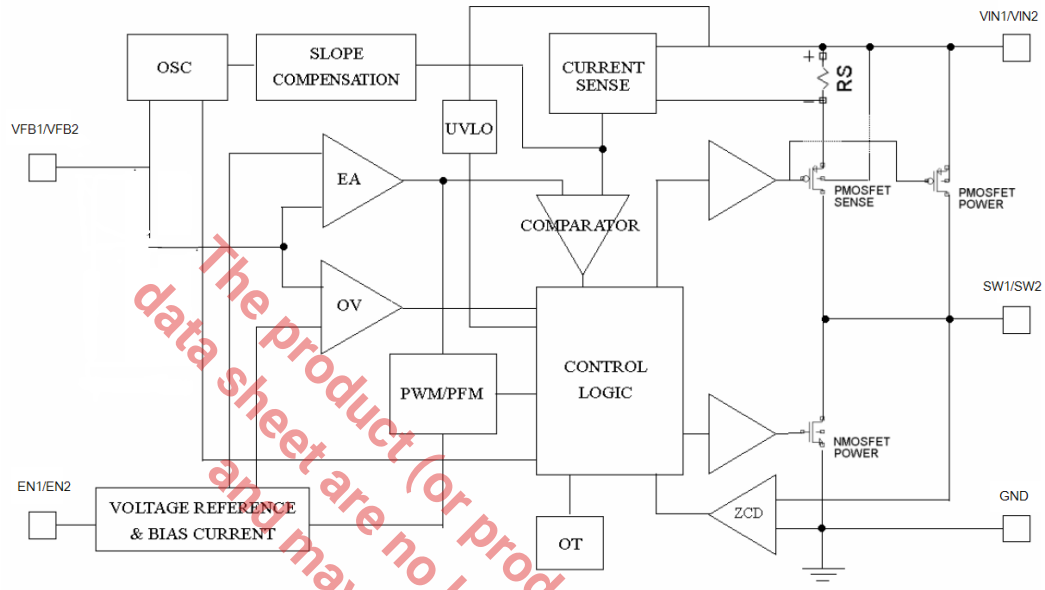


Fig. 2: XRP6668 Block Diagram (One Channel Shown)

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PIN ASSIGNMENT

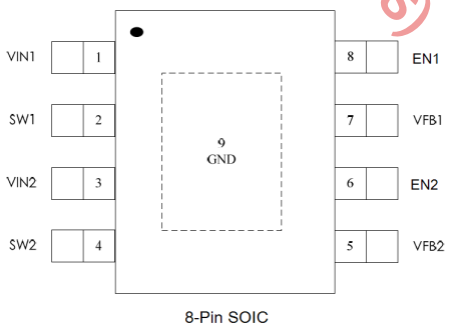


Fig. 3: XRP6668 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
VIN1	1	Channel 1 Power Input Pin. Must be closely decoupled to GND pin with a 4.7µF or greater ceramic capacitor.
SW1	2	Channel 1 Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VIN2	3	Channel 2 Power Input Pin. Must be closely decoupled to GND pin with a 4.7µF or greater ceramic capacitor.
SW2	4	Channel 2 Switch Pin. Must be connected to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
VFB2	5	Channel 2 Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
EN2	6	Channel 2 Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shutdown the device.
VFB1	7	Channel 1 Feedback Pin. Receives the feedback voltage from an external resistive divider across the output.
EN1	8	Channel 1 Enable Pin. Minimum 1.2V to enable the device. Maximum 0.4V to shutdown the device.
GND	Exposed Pad	Connect to GND.

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method
XRP6668IDBTR-F	-40°C ≤ T_J ≤ +125°C	Yes(2)	8-Pin HSOIC	Tape & Reel
XRP6668EVB	XRP6668 Evaluation Board			

NOTE:

1. Refer to www.exar.com/XRP6668 for most up-to-date Ordering Information
2. Visit www.exar.com for additional information on Environmental Rating.

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TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 3.6V, T_J = T_A = 25°C and apply to each individual channel unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

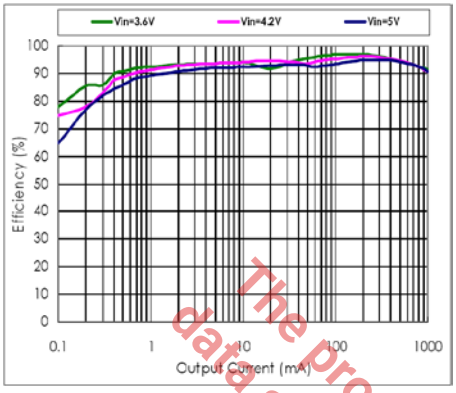


Fig. 4: Efficiency vs Output Current (V_{OUT}=3.3V)

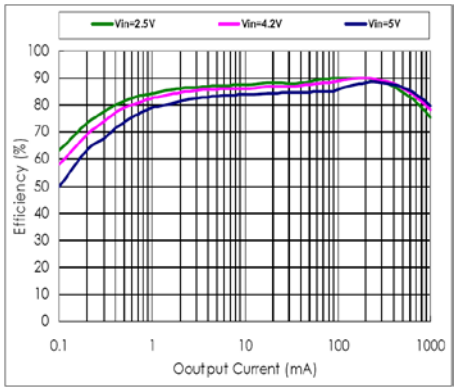


Fig. 5: Efficiency vs Output Current (V_{OUT}=1.2V)

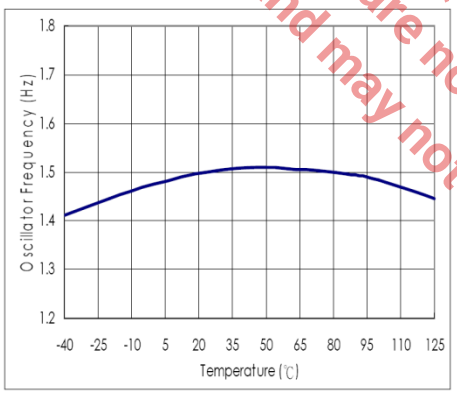


Fig. 6: Oscillator Frequency vs Temperature

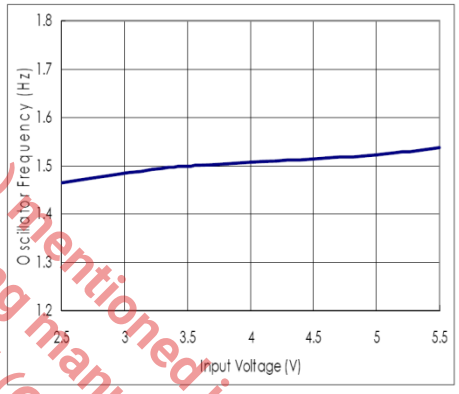


Fig. 7: Oscillator Frequency vs Supply Voltage

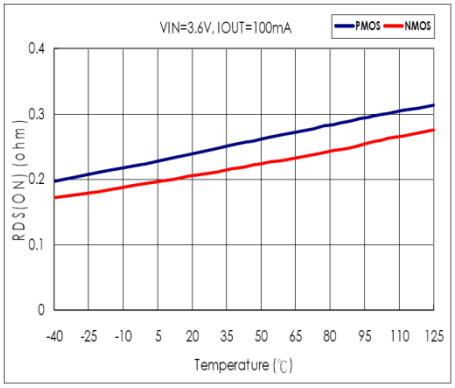


Fig. 8: $R_{DS(ON)}$ vs Temperature

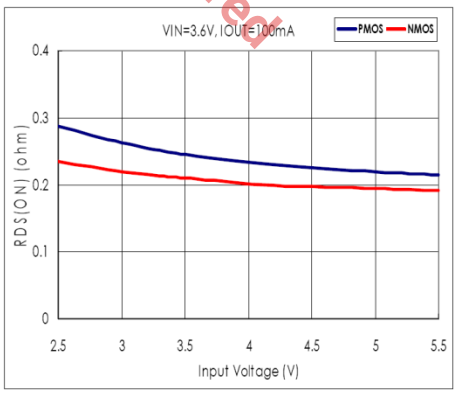


Fig. 9: $R_{DS(ON)}$ vs Input Voltage

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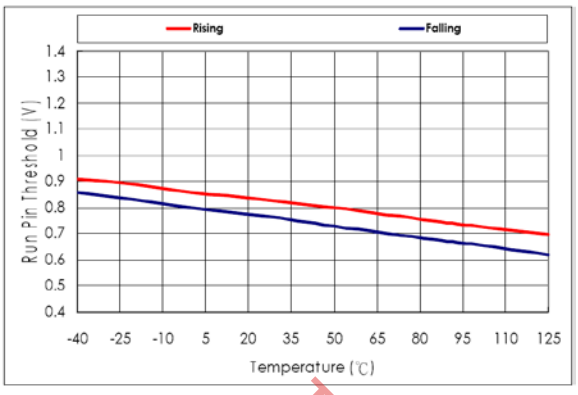


Fig. 10: EN Pin Threshold vs Temperature

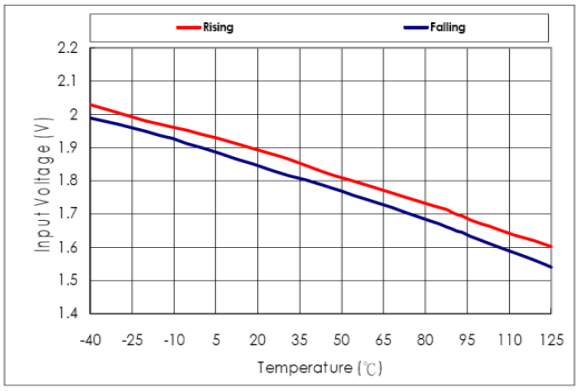


Fig. 11: UVLO Threshold vs Temperature

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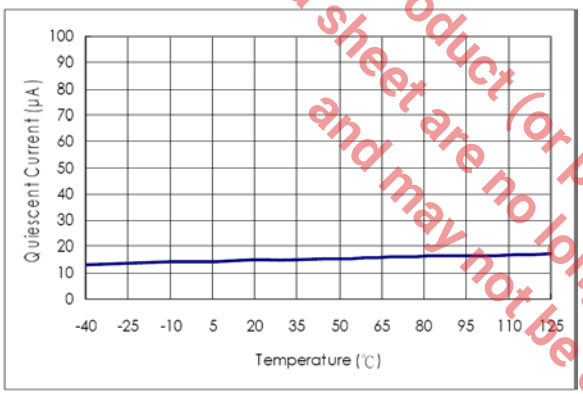


Fig. 12: Quiescent Current vs Temperature (PFM Mode)

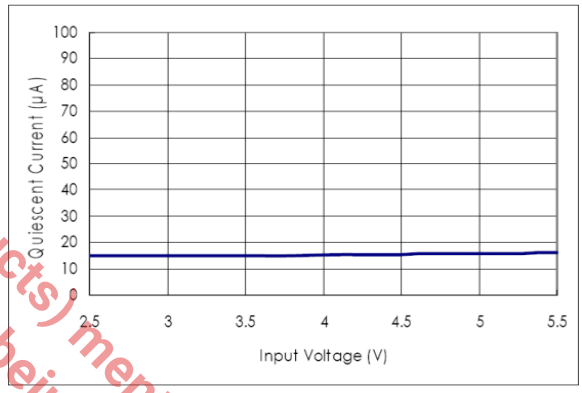


Fig. 13: Quiescent Current vs Input Voltage (PFM Mode)

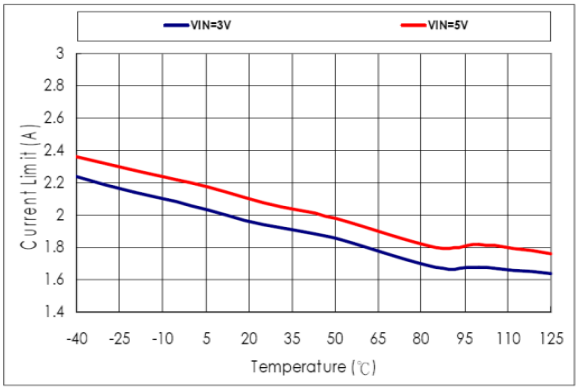


Fig. 14: Current Limit vs Temperature (V_{OUT}=1.2V)

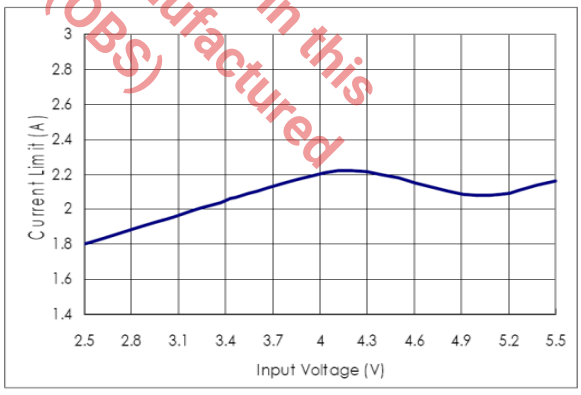


Fig. 15: Current Limit vs Input Voltage (V_{OUT}=1.2V)

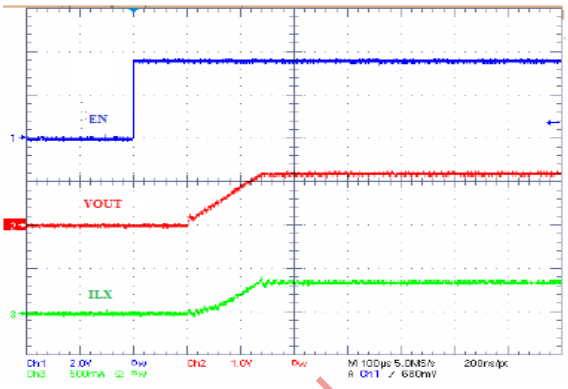


Fig. 16: Power On From EN Pin (I_{OUT}=1A)

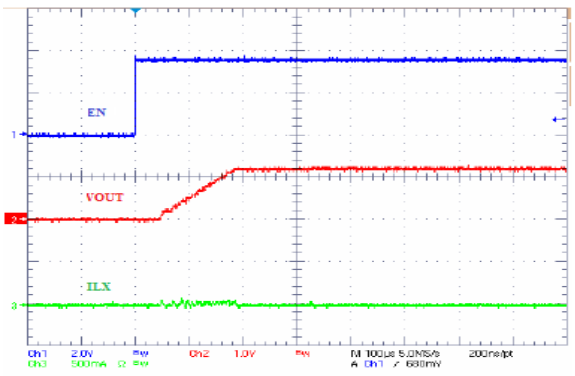


Fig. 17: Power On From EN Pin (I_{OUT}=10mA)

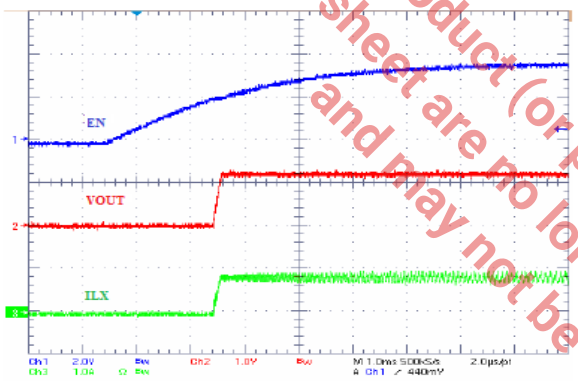


Fig. 18: Power On From V_{IN} (I_{OUT}=1A)

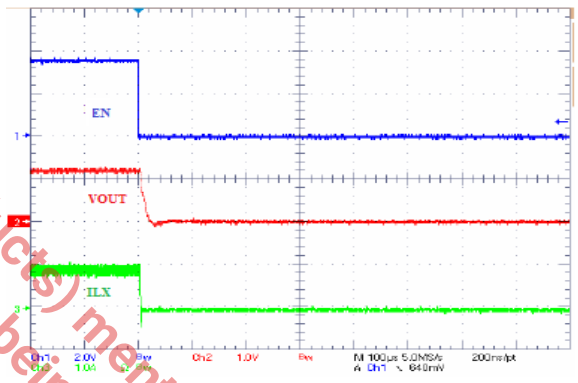


Fig. 19: Power Off From EN (I_{OUT}=1A)

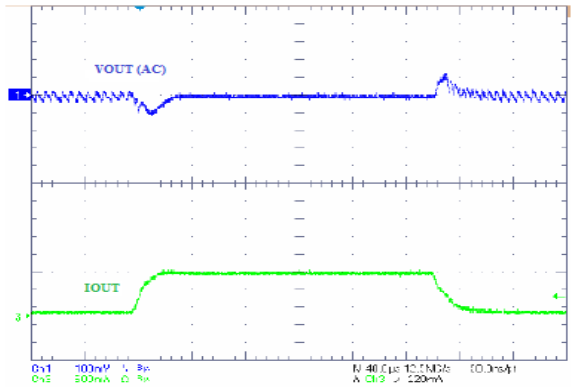


Fig. 20: Load Step Response
V_{OUT}=1.2V, I_{OUT} From 50mA to 500mA

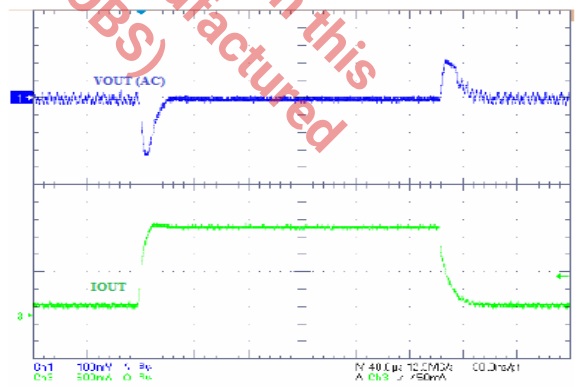


Fig. 21: Load Step Response
V_{OUT}=1.2V, I_{OUT} From 50mA to 1A

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THEORY OF OPERATION

The typical application circuit of adjustable version is shown in figure 22.

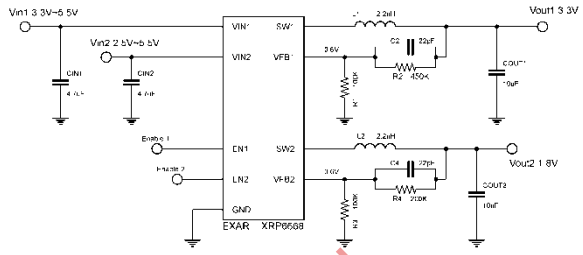


Fig. 22: Typical Application

All explanation below pertaining to one channel of the XRP6668 and can be extrapolated to apply to the second channel.

INDUCTOR SELECTION

Inductor ripple current and saturation current rating are two factors to be considered when selecting the inductor value. A low DCR inductor is preferred.

The inductor value L can be calculated from the following equation:

$$L = (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN}}\right) x \left(\frac{1}{f}\right) x \left(\frac{1}{\Delta IL}\right)$$

CIN AND COUT SELECTION

A low ESR input capacitor can minimize the input voltage ripple. Voltage rating of the capacitor should be at least 50% higher than the input voltage. The RMS current of the input capacitor is required to be larger than the I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The ESR value is an important parameter to consider when selecting an output capacitor C_{OUT}. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \times f \times C_{OUT}}\right)$$

The output capacitor's value can be optimized for very low output voltage ripple and small circuit size. Voltage rating of the capacitor should be at least 50% higher than the output voltage. Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications.

It is recommended to use X5R or X7R ceramic capacitors as they have the best temperature and voltage characteristics.

OUTPUT VOLTAGE SELECTION

The output voltage is adjustable via the external resistor network R1 and R2 in the first channel and R3 and R4 in the second channel as per the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R2}{R1}\right)$$

where, V_{REF} is the reference voltage at 0.6V.

The feedback resistors must be chosen such that power dissipation of the resistor network is minimal. R1 (R3 for channel 2) can be fixed at 100kΩ and R2 (R4 for channel 2) is selected based on the above equation.

THERMAL CONSIDERATIONS

Although thermal shutdown is built-in in XRP6668 to protect the device from thermal damage, the total power dissipation that XRP6668 can sustain is based on the package thermal capability. The formula to ensure safe operation is shown in Note 1. To avoid XRP6668 from exceeding the maximum junction temperature, thermal analysis is required.

GUIDELINES FOR PCB LAYOUT

To ensure proper operation of the XRP6668, please note the following PCB layout guidelines:

1. The GND, SWx and VINx traces should be kept short, direct and wide.

2. VFBx pin must be connected directly to the feedback resistors. Resistive divider R1/R2 and R3/R4 must be connected in parallel to the output capacitor C_{OUTx}.

3. The input capacitor C_{INx} must be as close as possible to pin VINx.

4. Keep SWx node away from the sensitive VFB node since SWx signal experiences high frequency voltage swings.

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APPLICATIONS

Typical Schematic

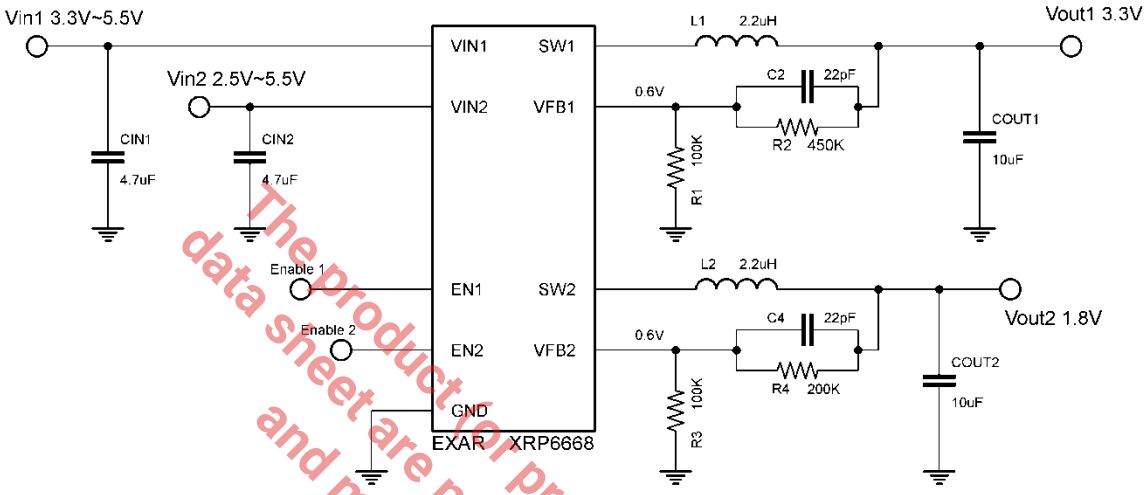
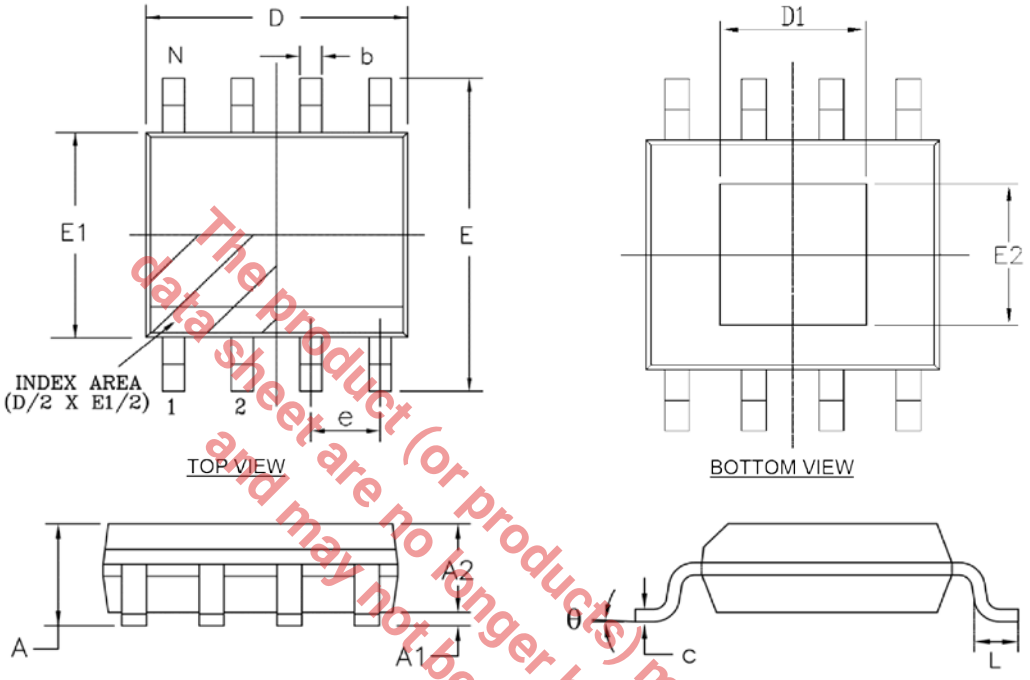


Fig. 23: XRP6668 5V to 3.3V and 1.8V Conversions

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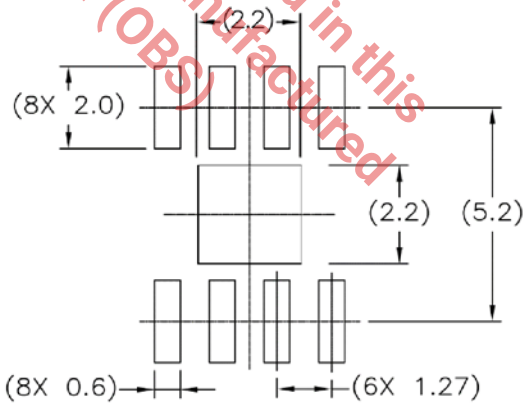
PACKAGE SPECIFICATION

EXPOSED PAD 8-PIN SOIC



8 Pin HSOICN JEDEC MS-012 Variation BA			
SYMBOLS	DIMENSIONS IN MM		
	MIN	NOM	MAX
A	1.35		1.75
A1	0.05		0.15
A2			1.50
b		0.4 BSC	
c	0.17		0.25
D	4.80		5.00
D1		2.0 REF	
E	5.80		6.20
E1	3.80		4.00
E2		2.0 REF	
e		1.27 BSC	
L	0.40		1.27
θ	0°		8°
N		8	

TERMINAL DETAILS



LAND PATTERN RECOMMENDED

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES

Drawing No. : POD - 00000123

Revision: A.1

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REVISION HISTORY

Revision	Date	Description
1.0.0	09/16/2010	Initial release of datasheet
1.1.0	11/15/2010	Corrected ΔV_{OUT} equation: changed V_{OUT} to C_{OUT}. Updated 'Output Voltage selection' section.
1.2.0	01/14/2011	Added specific test conditions and data in Electrical Specification Table for output voltage accuracy for operations below 3V.
1.2.1	10/30/2017	Corrected temperature range to -40°C ≤ T_J ≤ 125°C. Update to MaxLinear logo. Update format and ordering information.

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Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

High Performance Analog:
1060 Rincon circle
San Jose, CA 95131
Tel.: +1 (669) 265-6100
Fax: +1 (669) 265-6101
Email: powertechsupport@exar.com
www.exar.com

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