## GENERAL DESCRIPTION

The XRA1200/1200P is an 8-bit GPIO expander with an I²C/SMBus interface. After power-up, the XRA1200 has internal 100K ohm pull-up resistors on each I/O pin that can be individually enabled. The XRA1200P have the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

In addition, the GPIOs on the XRA1200/1200P can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The XRA1200/1200P are enhanced versions of other 8-bit GPIO expanders with an I²C/SMBus interface. The XRA1200 is pin and software compatible with the CAT9534 and PCA9534. The XRA1200P is pin and software compatible with the CAT9554 and PCA9554. The XRA1200/1200P are also pin compatible with the PCA9554A and TCA9554A.

The XRA1200/1200P are available in 16-pin QFN and 16-pin TSSOP packages.

TSSOP-16 versions available,
QFN-16 versions obsolete

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

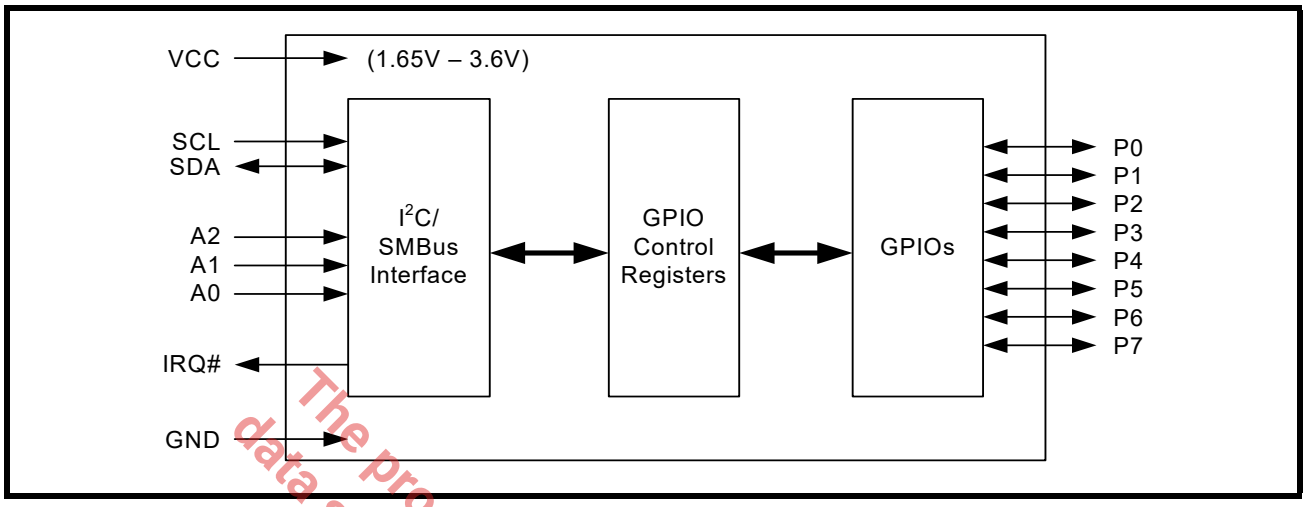
### *FEATURES*

- 1.65V to 3.6V operating voltage
- 8 General Purpose I/Os (GPIOs)
- 5V tolerant inputs
- Maximum stand-by current of 1uA at +1.8V
- I²C/SMBus bus interface
- I²C clock frequency up to 400kHz
- Noise filter on SDA and SCL inputs
- Up to 32 I²C Slave Addresses
- Individually programmable inputs
- Internal pull-up resistors
- Polarity inversion
- Individual interrupt enable
- Rising edge and/or Falling edge interrupt
- Input filter
- Individually programmable outputs
- Output Level Control
- Output Three-State Control
- Open-drain active low interrupt output
- Pin and software compatible with CAT9534, CAT9554, PCA9534, and PCA9554
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

### *APPLICATIONS*

- Personal Digital Assistants (PDA)
- Cellular Phones/Data Devices
- Battery-Operated Devices
- Global Positioning System (GPS)
- Bluetooth

**FIGURE 1. XRA1200 BLOCK DIAGRAM**



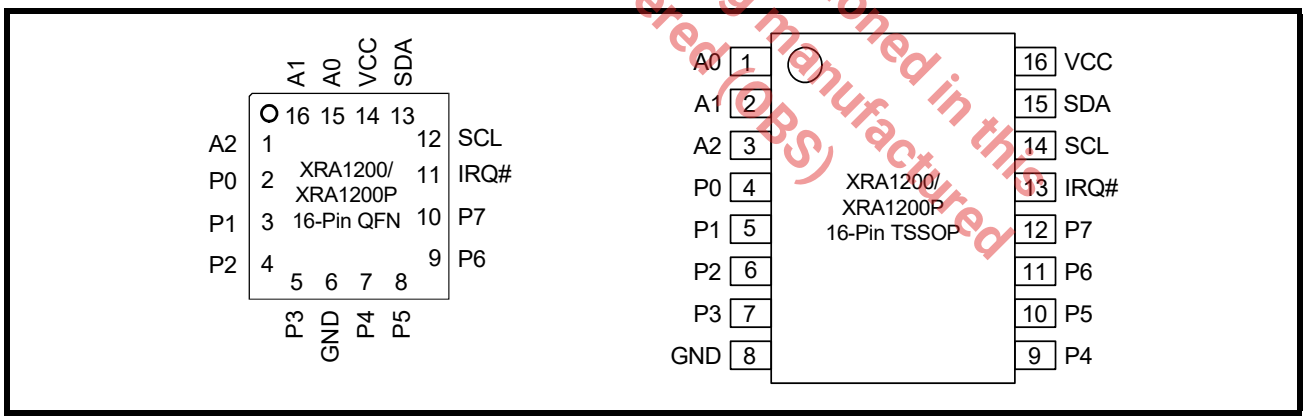

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## *ORDERING INFORMATION*

| PART NUMBER | NUMBER OF GPIOS | OPERATING TEMPERATURE RANGE | PACKAGE | PACKAGE METHOD | LEAD-FREE |
|---|---|---|---|---|---|
| XRA1200IG16TR-F | 8 | -40°C to +85°C | TSSOP-16 | Tape and Reel | Yes |
| XRA1200PIG16TR-F | 8 | -40°C to +85°C | TSSOP-16 | Tape and Reel | Yes |

***NOTE:*** *For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/XRA1200 and www.maxlinear.com/XRA1200P.*

**FIGURE 2. PIN OUT ASSIGNMENTS TSSOP-16 VERSIONS AVAILABLE, QFN-16 VERSIONS OBSOLETE**



## PIN DESCRIPTIONS

**Pin Description TSSOP-16 versions available, QFN-16 versions obsolete**

| NAME | QFN-16 PIN# | TSSOP-16 PIN# | TYPE | DESCRIPTION |
|---|---|---|---|---|
| **I2C INTERFACE** | | | | |
| SDA | 13 | 15 | I/O | I2C-bus data input/output (open-drain). |
| SCL | 12 | 14 | I | I2C-bus serial input clock. |
| IRQ# | 11 | 13 | OD | Interrupt output (open-drain, active LOW). |
| A0 | 15 | 1 | I | These pins select the I2C slave address. See Table 1. |
| A1 | 16 | 2 | I | |
| A2 | 1 | 3 | I | |
| **GPIOs** | | | | |
| P0 | 2 | 4 | I/O | General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up. After power-up, the internal pull-up resistors are enabled for the XRA1200P. The internal pull-up resistors are disabled for the XRA1200. |
| P1 | 3 | 5 | I/O | |
| P2 | 4 | 6 | I/O | |
| P3 | 5 | 7 | I/O | |
| P4 | 7 | 9 | I/O | |
| P5 | 8 | 10 | I/O | |
| P6 | 9 | 11 | I/O | |
| P7 | 10 | 12 | I/O | |
| **ANCILLARY SIGNALS** | | | | |
| VCC | 14 | 16 | Pwr | 1.65V to 3.6V VCC supply voltage. |
| GND | 6 | 8 | Pwr | Power supply common, ground. |
| GND | Center Pad | - | Pwr | The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential. |

**Pin type: I=Input, O=Output, I/O= Input/output, OD=Output Open Drain.**

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (obs).

## 1.0 FUNCTIONAL DESCRIPTIONS

### 1.1 I²C-bus Interface

The I²C-bus interface is compliant with the Standard-mode and Fast-mode I²C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the Standard-mode, the serial clock and serial data can go up to 100 kbps and in the Fast-mode, the serial clock and serial data can go up to 400 kbps.

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The XRA120x responds to each write with an acknowledge (SDA driven LOW by XRA1200/1200P for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figures 3 - 5 below. For complete details, see the I²C-bus specifications.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**FIGURE 3. I²C START AND STOP CONDITIONS**

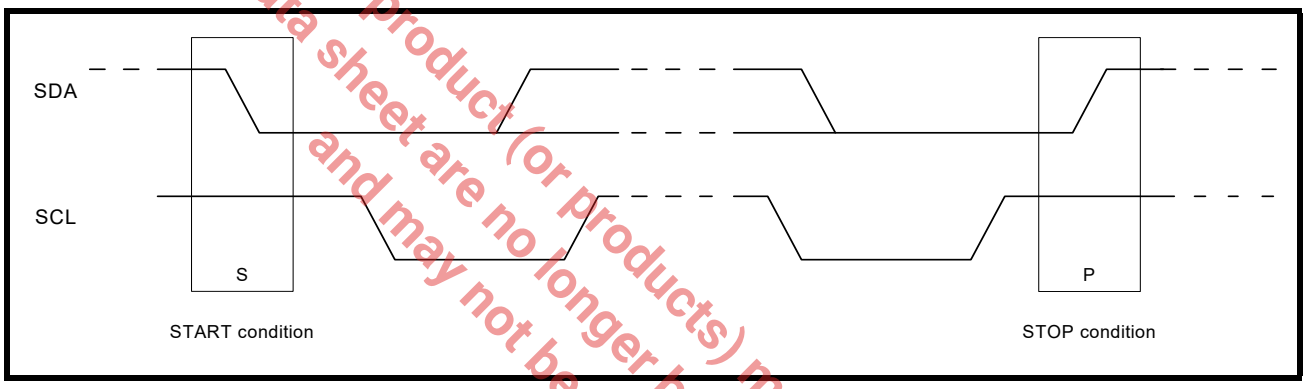



**FIGURE 4. MASTER WRITES TO SLAVE**

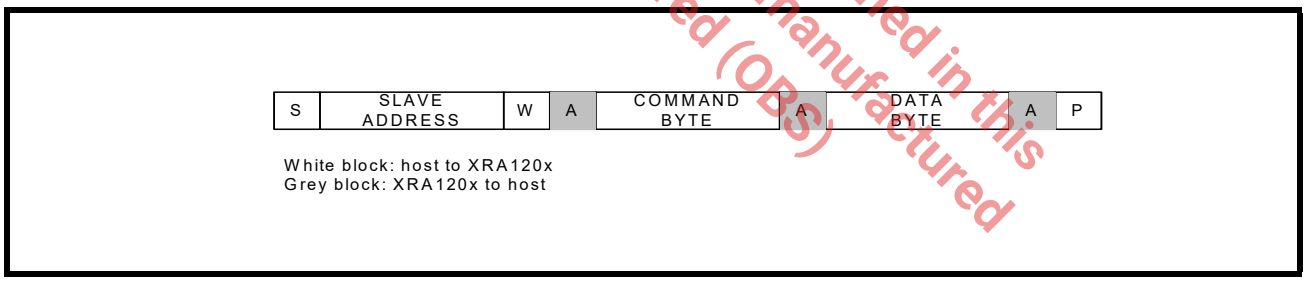
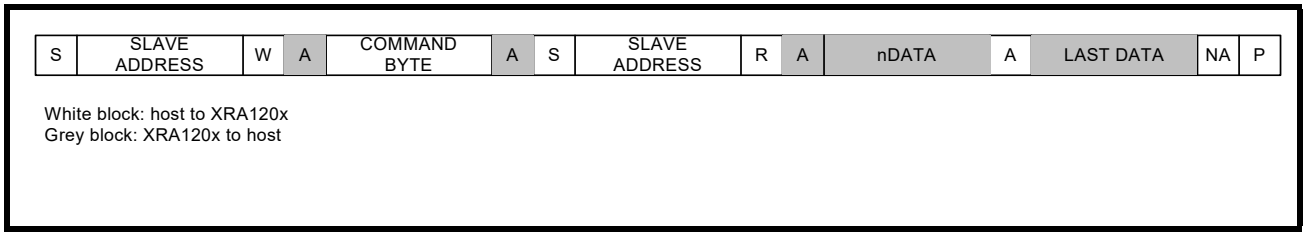



**FIGURE 5. MASTER READS FROM SLAVE**



### 1.1.1 I²C-bus Addressing

There could be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the XRA1200/1200P has up to 32 I²C slave addresses using the A2-A0 address lines. Table 1 below shows the different addresses that can be selected.

**TABLE 1: I²C ADDRESS MAP**

| A2 | A1 | A0 | I²C ADDRESS |
|---|---|---|---|
| GND | SCL | GND | 0x20 (0010 000X) |
| GND | SCL | VCC | 0x22 (0010 001X) |
| GND | SDA | GND | 0x24 (0010 010X) |
| GND | SDA | VCC | 0x26 (0010 011X) |
| VCC | SCL | GND | 0x28 (0010 100X) |
| VCC | SCL | VCC | 0x2A (0010 101X) |
| VCC | SDA | GND | 0x2C (0010 110X) |
| VCC | SDA | VCC | 0x2E (0010 111X) |
| GND | SCL | SCL | 0x30 (0011 000X) |
| GND | SCL | SDA | 0x32 (0011 001X) |
| GND | SDA | SCL | 0x34 (0011 010X) |
| GND | SDA | SDA | 0x36 (0011 011X) |
| VCC | SCL | SCL | 0x38 (0011 100X) |
| VCC | SCL | SDA | 0x3A (0011 101X) |
| VCC | SDA | SCL | 0x3C (0011 110X) |
| VCC | SDA | SDA | 0x3E (0011 111X) |
| GND | GND | GND | 0x40 (0100 000X) |
| GND | GND | VCC | 0x42 (0100 001X) |
| GND | VCC | GND | 0x44 (0100 010X) |
| GND | VCC | VCC | 0x46 (0100 011X) |
| VCC | GND | GND | 0x48 (0100 100X) |
| VCC | GND | VCC | 0x4A (0100 101X) |
| VCC | VCC | GND | 0x4C (0100 110X) |
| VCC | VCC | VCC | 0x4E (0100 111X) |
| GND | GND | SCL | 0x50 (0101 000X) |
| GND | GND | SDA | 0x52 (0101 001X) |
| GND | VCC | SCL | 0x54 (0101 010X) |
| GND | VCC | SDA | 0x56 (0101 011X) |
| VCC | GND | SCL | 0x58 (0101 100X) |
| VCC | GND | SDA | 0x5A (0101 101X) |
| VCC | VCC | SCL | 0x5C (0101 110X) |
| VCC | VCC | SDA | 0x5E (0101 111X) |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 1.1.2 I²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is '0', then it is a write transaction. If bit-0 is '1', then it is a read transaction.

### 1.1.3 I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that will be accessed. Table 2 below lists the command bytes for each register.

**TABLE 2: I²C COMMAND BYTE (REGISTER ADDRESS)**

| COMMAND BYTE | REGISTER NAME DESCRIPTION | READ/WRITE | DEFAULT VALUES |
|---|---|---|---|
| 0x00 | GSR - GPIO State | Read-Only | 0xXX |
| 0x01 | OCR - Output Control | Read/Write | 0xFF |
| 0x02 | PIR - Input Polarity Inversion | Read/Write | 0x00 |
| 0x03 | GCR - GPIO Configuration | Read/Write | 0xFF |
| 0x04 | PUR - Input Internal Pull-up Resistor Enable/Disable | Read/Write | 0x00 (XRA1200)<br>0xFF (XRA1200P) |
| 0x05 | IER - Input Interrupt Enable | Read/Write | 0x00 |
| 0x06 | TSCR - Output Three-State Control | Read/Write | 0x00 |
| 0x07 | ISR - Input Interrupt Status | Read | 0x00 |
| 0x08 | REIR - Input Rising Edge Interrupt Enable | Read/Write | 0x00 |
| 0x09 | FEIR - Input Falling Edge Interrupt Enable | Read/Write | 0x00 |
| 0x0A | IFR - Input Filter Enable/Disable | Read/Write | 0xFF |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### *1.2 Interrupts*

The table below summarizes the interrupt behavior of the different register settings for the XRA1200/1200P.

**TABLE 3: INTERRUPT GENERATION AND CLEARING**

| GCR BIT | IER BIT | REIR BIT | FEIR BIT | IFR BIT | INTERRUPT GENERATED BY: | INTERRUPT CLEARED BY: |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | No interrupts enabled (default) | N/A |
| 1 | 1 | 0 | 0 | 0 | A rising or falling edge on the input | Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR) |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 1 | 1 | 1 | 0 | 0 | A rising edge on the input | Reading the GSR register |
| | | | | 1 | A rising edge on the input and remains high for more than 1075ns | |
| 1 | 1 | 0 | 1 | 0 | A falling edge on the input | Reading the GSR register |
| | | | | 1 | A falling edge on the input and remains low for more than 1075ns | |
| 1 | 1 | 1 | 1 | 0 | A rising or falling edge on the input | Reading the GSR register |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns | |
| 0 | x | x | x | x | No interrupts in output mode | N/A |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

## 2.0 REGISTER DESCRIPTION

### *2.1 GPIO State Register (GSR) - Read-Only*

The status of P7 - P0 can be read via this register. A read will show the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register will clear an input interrupt (see Table 3 for complete details). Reading this register will also return the last value written to the OCR register for any pins that are configured as outputs (ie. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.2 Output Control Register (OCR) - Read/Write*

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register will return the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.3 Input Polarity Inversion Register (PIR) - Read/Write*

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to '1', the value of this bit in the GSR Register will be the inverted value of the input pin. If the corresponding bit in this register is set to '0', the value of this bit in the GSR Register will be the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.4 GPIO Configuration Register (GCR) - Read/Write*

This register configures the GPIOs as inputs or outputs. After power-up, the GPIOs are inputs. Setting these bits to '0' will enable the GPIOs as outputs. Setting these bits to '1' will enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.5 Input Internal Pull-up Enable/Disable Register (PUR) - Read/Write*

This register enables/disables the internal pull-up resistors for an input. After power-up, the internal pull-up resistors are disabled for the XRA1200. Writing a '1' to these bits will enable the internal pull-up resistors. After power-up, the internal pull-up resistors are enabled for the XRA1200P. Writing a '0' to these bits will disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.6 Input Interrupt Enable Register (IER) - Read/Write*

This register enables/disables the interrupts for an input. After power-up, the interrupts are disabled. Writing a '1' to these bits will enable the interrupt for the corresponding input pins. See Table 3 for complete details of the interrupt behavior for various register settings. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.7 Output Three-State Control Register (TSCR) - Read/Write*

This register can enable/disable the three-state mode of an output. Writing a '1' to these bits will enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### *2.8 Input Interrupt Status Register (ISR) - Read-Only*

This register reports the input pins that have generated an interrupt. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

### 2.9 Input Rising Edge Interrupt Enable Register (REIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the rising edge. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.10 Input Falling Edge Interrupt Enable Register (FEIR) - Read/Write

Writing a '1' to these bits will enable the corresponding input to generate an interrupt on the falling edge. Writing a '1' to these bits will make that input generate an interrupt on the rising edge only. See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

### 2.11 Input Filter Enable Register (IFR) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns will generate an interrupt (if enabled). Pulses that are less than 225ns will be filtered and will not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a '0' to these bits will disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs will generate an interrupt (if enabled). See Table 3 for complete details of the interrupt behavior for various register settings. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

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## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | 3.6 Volts |
| Supply current | 160 mA |
| Ground current | 200 mA |
| External current limit of each GPIO | 25 mA |
| Total current limit for GPIO[7:0] | 100 mA |
| Total supply current sourced by all GPIOs | 160 mA |
| Operating Temperature | -40° to +85°C |
| Storage Temperature | -65° to +150°C |
| Power Dissipation | 200 mW |

## TYPICAL PACKAGE THERMAL RESISTANCE DATA (MARGIN OF ERROR: ± 15%)

| | |
|---|---|
| Thermal Resistance (16-QFN) | theta-ja = 40°C/W, theta-jc = 26°C/W |
| Thermal Resistance (16-TSSOP) | theta-ja = 105°C/W, theta-jc = 20°C/W |

TSSOP-16 versions available, QFN-16 versions obsolete

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

# ELECTRICAL CHARACTERISTICS

## *DC ELECTRICAL CHARACTERISTICS*

**UNLESS OTHERWISE NOTED: TA = -40° TO +85°C, VCC IS 1.65V TO 3.6V**

| SYMBOL | PARAMETER | LIMITS 1.8V ± 10% MIN | LIMITS 1.8V ± 10% MAX | LIMITS 2.5V ± 10% MIN | LIMITS 2.5V ± 10% MAX | LIMITS 3.3V ± 10% MIN | LIMITS 3.3V ± 10% MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.3VCC | -0.3 | 0.3VCC | -0.3 | 0.3VCC | V | Note 1 |
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.2 | -0.3 | 0.5 | -0.3 | 0.8 | V | Note 2 |
| $V_{IH}$ | Input High Voltage | 1.3 | VCC | 1.8 | VCC | 2.3 | VCC | V | Note 1 |
| $V_{IH}$ | Input High Voltage | 1.4 | 5.5 | 1.8 | 5.5 | 2.0 | 5.5 | V | Note 2 |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V<br>V<br>V | $I_{OL}$ = 3 mA<br>$I_{OL}$ = 3 mA<br>$I_{OL}$ = 3 mA<br>Note 3 |
| $V_{OL}$ | Output Low Voltage | | 0.5 | | 0.5 | | 0.5 | V | $I_{OL}$ = 8 mA<br>Note 4 |
| $V_{OL}$ | Output Low Voltage | | 0.4 | | 0.4 | | 0.4 | V<br>V<br>V | $I_{OL}$ = 6 mA<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 1.5 mA<br>Note 5 |
| $V_{OH}$ | Output High Voltage | 1.2 | | 1.8 | | 2.6 | | V<br>V<br>V | $I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>$I_{OH}$ = -8 mA<br>Note 4 |
| $I_{IL}$ | Input Low Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $I_{IH}$ | Input High Leakage Current | | ±10 | | ±10 | | ±10 | uA | |
| $I_{CC}$ | Power Supply Current | | 50 | | 100 | | 200 | uA | Test 1 |
| $I_{CC}$ | Power Supply Current | | 150 | | 250 | | 500 | uA | Test 2 |
| $I_{CCS}$ | Standby Current | | 1 | | 2 | | 5 | uA | Test 3 |
| $C_{IN}$ | Input Pin Capacitance | | 5 | | 5 | | 5 | pF | |
| $R_{GPIO}$ | GPIO pull-up resistance | 60 | 140 | 60 | 140 | 60 | 140 | kΩ | 100kΩ ± 40% |

The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

***NOTES:***

1. *For I2C input signals (SDA, SCL);*
2. *For GPIOs, A0, A1 and A2 signals;*
3. *For I2C output signal SDA;*
4. *For GPIOs;*
5. *For IRQ# signal;*

Test 1: SCL frequency is 400 KHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 2: SCL frequency is 400 KHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

### *AC ELECTRICAL CHARACTERISTICS*

*Unless otherwise noted: TA=-40° to +85°C, Vcc=1.65V - 3.6V*

| SYMBOL | PARAMETER | STANDARD MODE I²C-BUS | | FAST MODE I²C-BUS | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ | Operating frequency | 0 | 100 | 0 | 400 | kHz |
| $T_{BUF}$ | Bus free time between STOP and START | 4.7 | | 1.3 | | µs |
| $T_{HD;STA}$ | START condition hold time | 4.0 | | 0.6 | | µs |
| $T_{SU;STA}$ | START condition setup time | 4.7 | | 0.6 | | µs |
| $T_{HD;DAT}$ | Data hold time | 0 | | 0 | | ns |
| $T_{VD;ACK}$ | Data valid acknowledge | | 0.6 | | 0.6 | µs |
| $T_{VD;DAT}$ | SCL LOW to data out valid | | 0.6 | | 0.6 | ns |
| $T_{SU;DAT}$ | Data setup time | 250 | | 150 | | ns |
| $T_{LOW}$ | Clock LOW period | 4.7 | | 1.3 | | µs |
| $T_{HIGH}$ | Clock HIGH period | 4.0 | | 0.6 | | µs |
| $T_F$ | Clock/data fall time | | 300 | | 300 | ns |
| $T_R$ | Clock/data rise time | | 1000 | | 300 | ns |
| $T_{SP}$ | Pulse width of spikes tolerance | 50 | | 50 | | ns |
| $T_{D1}$ | I²C-bus GPIO output valid | | 0.2 | | 0.2 | µs |
| $T_{D4}$ | I²C input pin interrupt valid | | 4 | | 4 | µs |
| $T_{D5}$ | I²C input pin interrupt clear | | 4 | | 4 | µs |
| $T_{D15}$ | SCL delay after reset | 3 | | 3 | | µs |

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

**FIGURE 6. I²C-BUS TIMING DIAGRAM**

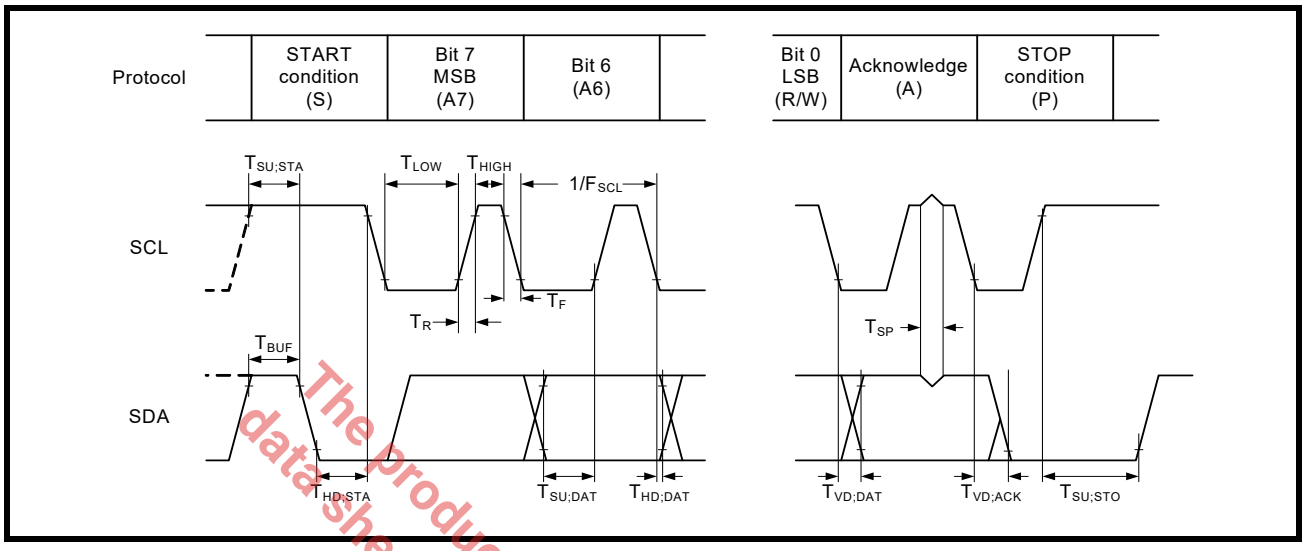



**FIGURE 7. WRITE TO OUTPUT**

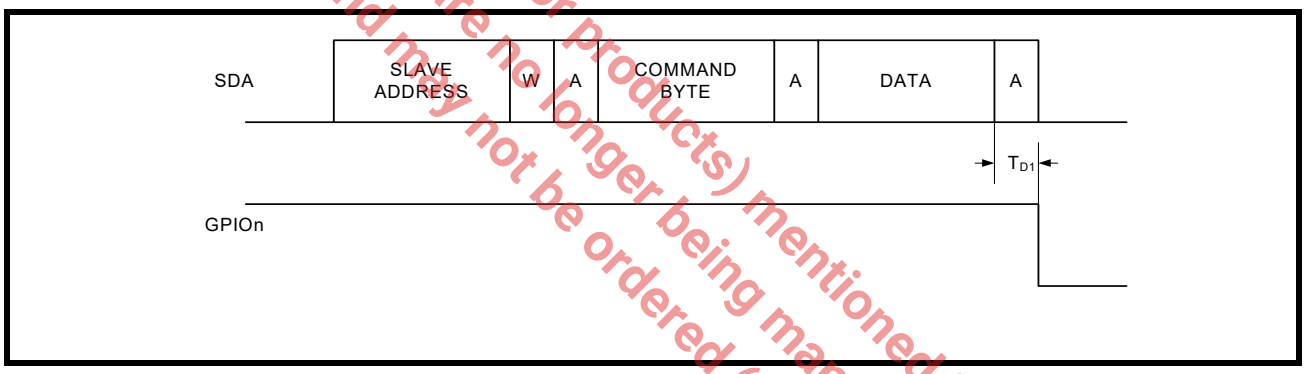
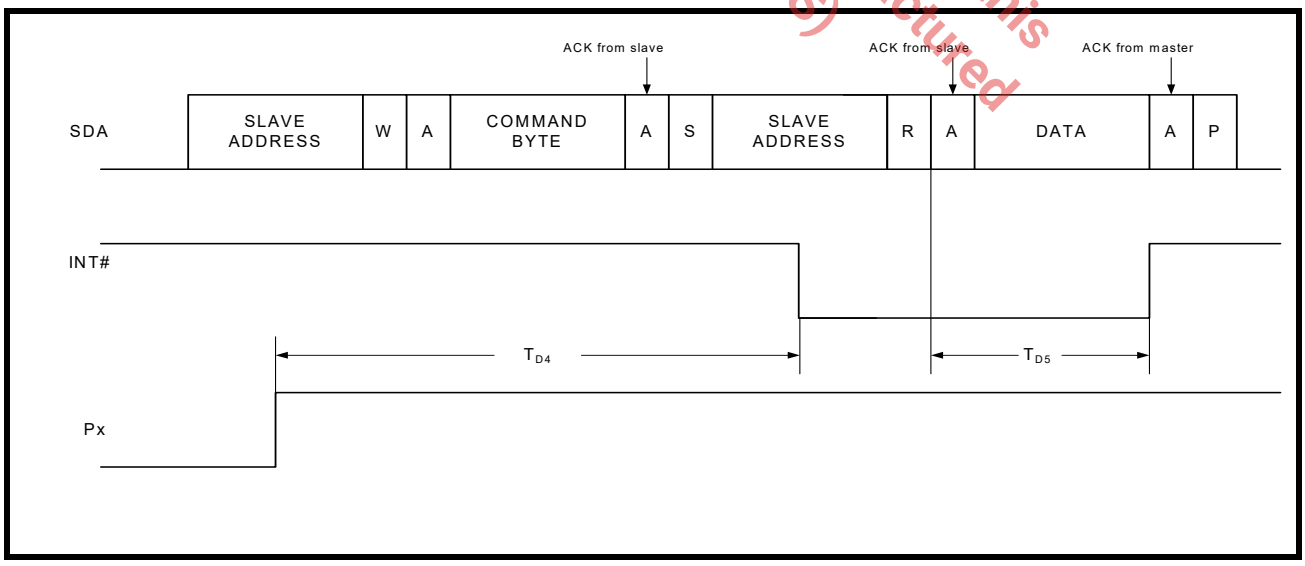


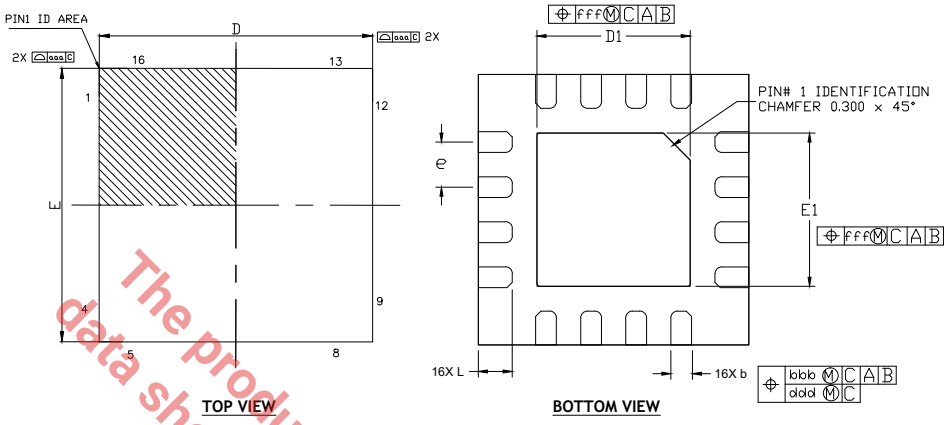

**FIGURE 8. GPIO PIN INTERRUPT**

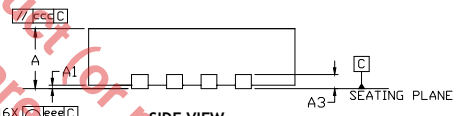



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## MECHANICAL DIMENSIONS (16 PIN QFN - 3 X 3 X 0.9 mm, 0.50 PITCH)

**QFN-16 VERSION OBSOLETE**




| DIMENSION TABLE | | | |
|---|---|---|---|
| SYMBOL | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20Ref | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 3.00 BSC | |
| E | | 3.00 BSC | |
| e | | 0.50 BSC | |
| D1 | 1.50 | 1.65 | 1.80 |
| E1 | 1.50 | 1.65 | 1.80 |
| L | 0.20 | 0.30 | 0.40 |
| K | 0.20 | – | – |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |
| N | | 16 | |

**TERMINAL DETAILS**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD- 00000138

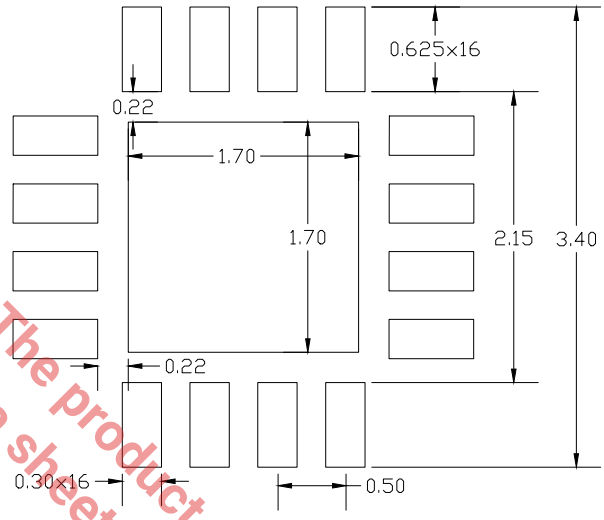
Revision: A

*Note: The control dimension is in millimeter.*

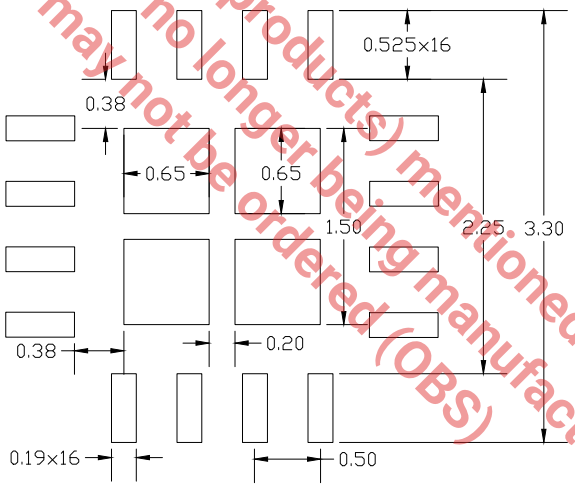
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## RECOMMENDED LAND PATTERN AND STENCIL (16 PIN QFN - 3 X 3 X 0.9 mm, 0.50 PITCH)

**QFN-16 VERSION OBSOLETE**




TYPICAL RECOMMENDED LAND PATTERN




TYPICAL RECOMMENDED STENCIL

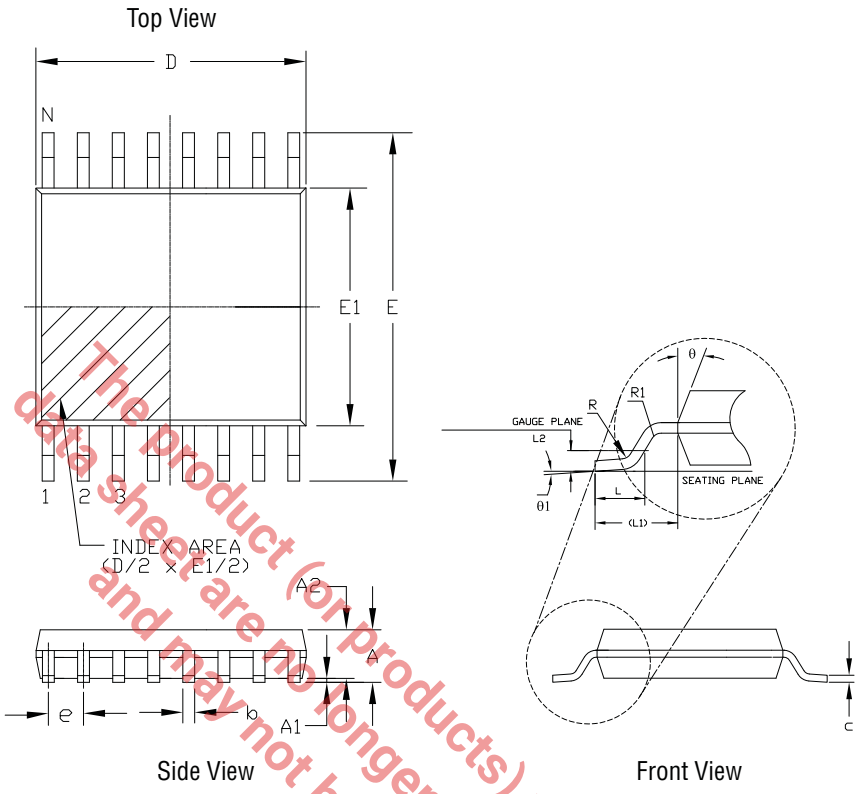
Drawing No.: POD- 00000138

Revision: A

*Note: The control dimension is in millimeter.*

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## MECHANICAL DIMENSIONS (16 PIN TSSOP - 4.4 mm)




The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

| 16 Pin TSSOP JEDEC MO-153 Variation AB | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| b | 0.19 | — | 0.30 | 0.007 | — | 0.012 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| E | 6.40 BSC | | | 0.252 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 0.169 | 0.173 | 0.177 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.09 | — | — | 0.035 | — | — |
| R1 | 0.09 | — | — | 0.035 | — | — |
| θ | 12° REF | | | 12° REF | | |
| θ1 | 0° | — | 8° | 0° | — | 8° |
| D | 4.90 | 5.00 | 5.10 | 0.193 | 0.197 | 0.200 |
| N | 16 | | | 16 | | |

Drawing No: POD-00000117
Revision: A

*Note: The control dimension is in millimeter.*

## *REVISION HISTORY*

| DATE | REVISION | DESCRIPTION |
|---|---|---|
| September 2011 | 1.0.0 | Final Datasheet. |
| August 2020 | 1.0.1 | Update to MaxLinear Logo. Update Ordering Information. |
| February 2, 2022 | 1.0.2 | **Updated:**<br>■ In the "TSSOP-16 versions available, QFN-16 versions obsolete" table, GPIOs parameter description.<br>■ "GPIO Configuration Register (GCR) - Read/Write" section.<br>■ "Input Internal Pull-up Enable/Disable Register (PUR) - Read/Write" section.<br>■ "Input Interrupt Enable Register (IER) - Read/Write" section.<br>■ "Mechanical Dimensions (16 pin QFN)" figure.<br>■ "Recommended and Pattern and Stencil (16 pin QFN)" figure.<br>■ "Mechanical Dimensions (16 pin TSSOP)" figure. |

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