15A Synchronous Step Down COT Regulator

General Description

The XR76115 is a synchronous step-down regulator combining the controller, drivers, bootstrap diode and MOSFETs in a single package for point-of-load supplies. The XR76115 has a load current rating of 15A. A wide 5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR76115 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.25% load and 0.12% line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads, thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR76115 is available in a RoHS-compliant, green / halogen-free, space-saving QFN 6x6mm package.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FEATURES

- 15A capable step down regulator
  - 4.5V to 5.5V low V_{IN} operation
  - 5V to 22V wide single input voltage
  - ≥0.6V adjustable output voltage
- Controller, drivers, bootstrap diode and MOSFETs integrated in one package
- Proprietary Constant On-Time control
  - No loop compensation required
  - Ceramic output capacitor stable operation
  - Programmable 200ns - 2µs on-time
  - Quasi constant 200kHz - 800kHz frequency
  - Selectable CCM or CCM / DCM operation
- Precision enable and Power-Good flag
- Programmable soft-start
- 6x6mm 37-pin QFN package

APPLICATIONS

- Distributed power architecture
- Point-of-Load converters
- Power supply modules
- FPGA, DSP, and processor supplies
- Base stations, switches / routers, and server

Typical Application

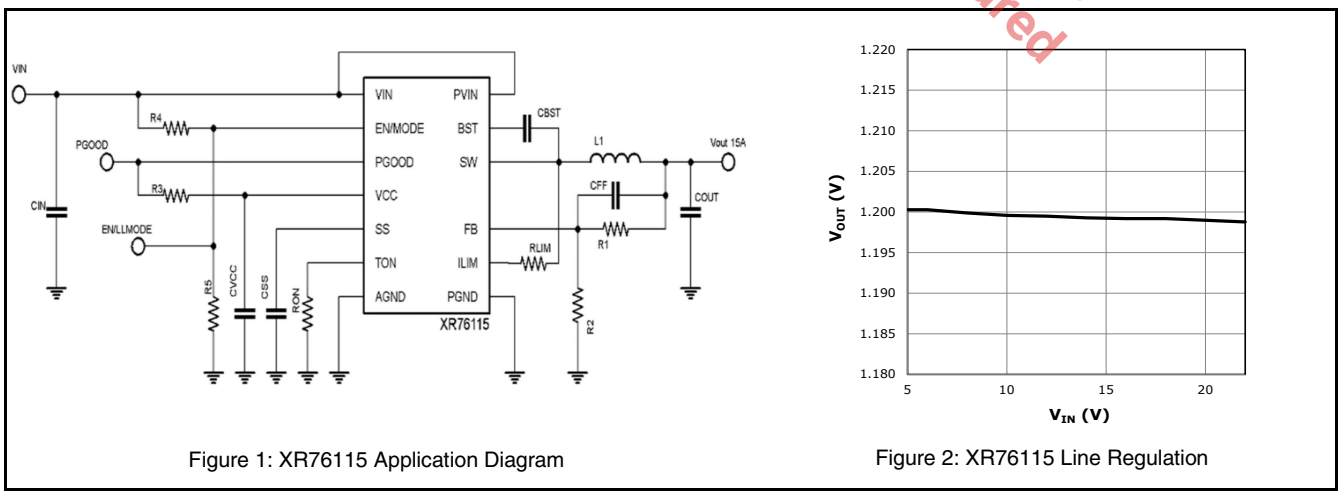


Figure 1: XR76115 Application Diagram

Figure 2: XR76115 Line Regulation

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} ..... -0.3V to 25V
V_{CC} ..... -0.3V to 6.0V
BST ..... -0.3V to 31V(1)
BST-SW ..... -0.3V to 6V
SW, I_{LIM} ..... -1V to 25V(1,2)
All other pins..... -0.3V to V_{CC}+0.3V
Storage temperature..... -65°C to 150°C
Junction temperature..... 150°C
Power dissipation ..... Internally Limited
Lead temperature (soldering, 10 sec)..... 300°C
ESD rating (HBM - Human Body Model)..... 2kV

Operating Ratings

PV_{IN} ..... 3V to 22V
V_{IN} ..... 4.5V to 22V
V_{CC} ..... 4.5V to 5.5V
SW, I_{LIM} ..... -1V to 22V(2)
PGOOD, V_{CC}, T_{ON}, SS, EN..... -0.3V to 5.5V
Switching Frequency ..... 200kHz - 800kHz(3)
Junction Temperature Range (T_J) ..... -40°C to 125°C
XR76115 Package Power Dissipation max at 25°C 5.2W
XR76115 JEDEC51 Package Thermal Resistance θ_{JA}..... 19°C/W

Note 1: No external voltage applied
Note 2: SW pin's DC range is -1V, transient is -5V for less than 50ns
Note 3: Recommended

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Ordering Information(1)

Part Number	Operating Temperature Range	Package	Packing Method	Lead-Free(2)
XR76115EL-F	-40°C≤T_J≤+125°C	6x6mm QFN	Bulk	Yes
XR76115ELTR-F	-40°C≤T_J≤+125°C	6x6mm QFN	Tape & Reel	Yes
XR76115EVB	XR76115 Evaluation Board			

NOTES:

1. Refer to www.maxlinear.com/XR76115 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

Electrical Characteristics

Specifications are for the operating junction temperature of T_J = 25°C only; limits applying over the full operating junction temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN}=12V.

Parameter	Min.	Typ.	Max.	Units		Conditions
Power Supply Characteristics						
V_{IN}, input voltage range	5	12	22	V	•	V_{CC} regulating
	4.5	5.0	5.5			V_{CC} tied to V_{IN}
I_{VIN}, V_{IN} supply current		0.7	1.3	mA	•	Not switching, V_{IN} = 12V, V_{FB} = 0.7V
I_{VCC}, V_{CC} quiescent current		0.7	1.3	mA	•	Not switching, V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V
I_{VIN}, V_{IN} supply current		11		mA		f = 300kHz, R_{ON} = 107k, V_{FB} = 0.58V
I_{OFF}, shutdown current		0.5		µA		Enable = 0V, V_{IN} = 12V, V_{IN} = PV_{IN}
Enable and Under-Voltage Lock-Out UVLO						
V_{IH_EN}, EN pin rising threshold	1.8	1.9	2.0	V	•	
V_{EN_HYS}, EN pin hysteresis		50		mV		
V_{IH_EN}, EN pin rising threshold for DCM / CCM operation	2.8	3.0	3.1	V	•	
V_{EN_HYS}, EN pin hysteresis		100		mV		
V_{CC} UVLO start threshold, rising edge	4.00	4.25	4.50	V	•	
V_{CC} UVLO hysteresis		200		mV		

Parameter	Min.	Typ.	Max.	Units		Conditions
Reference Voltage						
V_{REF}, reference voltage	0.597	0.600	0.603	V		V_{IN} = 5V - 22V → V_{CC} regulating
	0.596	0.600	0.604	V		V_{IN} = 4.5V - 5.5V → V_{CC} tied to V_{IN}
	0.594	0.600	0.606	V	•	V_{IN} = 5V - 22V → V_{CC} regulating, V_{IN} = 4.5V - 5.5V → V_{CC} tied to V_{IN}
DC load regulation		±0.25		%		CCM operation, closed loop, applies to any C_{OUT}
DC line regulation		±0.12		%		
Programmable Constant On-Time						
On-time 1	1.66	1.95	2.24	µs	•	R_{ON} = 140kΩ, V_{IN} = 22V
f corresponding to on-time 1	243	280	329	kHz		V_{IN} = 22V, V_{OUT} = 12V
Minimum programmable on-time		109		ns		R_{ON} = 6.98kΩ, V_{IN} = 22V
On-time 2	170	200	230	ns	•	R_{ON} = 6.98kΩ, V_{IN} = 12V
f corresponding to on-time 2	362	417	490	kHz		V_{OUT} = 1.0V
On-time 3	365	430	495	ns	•	R_{ON} = 16.2kΩ, V_{IN} = 12V
Minimum off-time		250	350	ns	•	
Diode Emulation Mode						
Zero crossing threshold		-2		mV		DC value measured during test
Soft-Start						
SS charge current	-14	-10	-6	µA	•	
SS discharge current	1	3		mA	•	Fault present
V_{CC} Linear Regulator						
V_{CC} output voltage	4.8	5.0	5.2	V	•	V_{IN} = 6V to 22V, I_{load} = 0 to 30mA
	4.51	4.7			•	V_{IN} = 5V, I_{load} = 0 to 20mA
Dropout voltage	100	300	490	mV	•	I_{VCC} = 30mA
Power Good Output						
Power Good threshold	-10	-7.5	-5	%		
Power Good hysteresis		2	4	%		
Power Good sink current	1	15		mA		
Protection: OCP, OTP, Short-Circuit						
Hiccup timeout		110		ms		
I_{LIM} pin source current	45	50	55	µA		
I_{LIM} current temperature coefficient		0.4		%/°C		
I_{LIM} comparator offset	-8	0	+8	mV	•	
Current limit blanking		100		ns		
Thermal shutdown threshold		150		°C		Rising temperature
Thermal hysteresis		15		°C		
Feedback pin short-circuit threshold	50	60	70	%	•	Percent of V_{REF}, short circuit is active After PGOOD is up
Output Power Stage						
High-side MOSFET R_{DSON}		7	10	mΩ		V_{GS} = 4.5V, I_{DS} = 2A
Low-side MOSFET R_{DSON}		4	4.6	mΩ		V_{GS} = 4.5V, I_{DS} = 2A
Maximum output current	15			A	•	

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Block Diagram

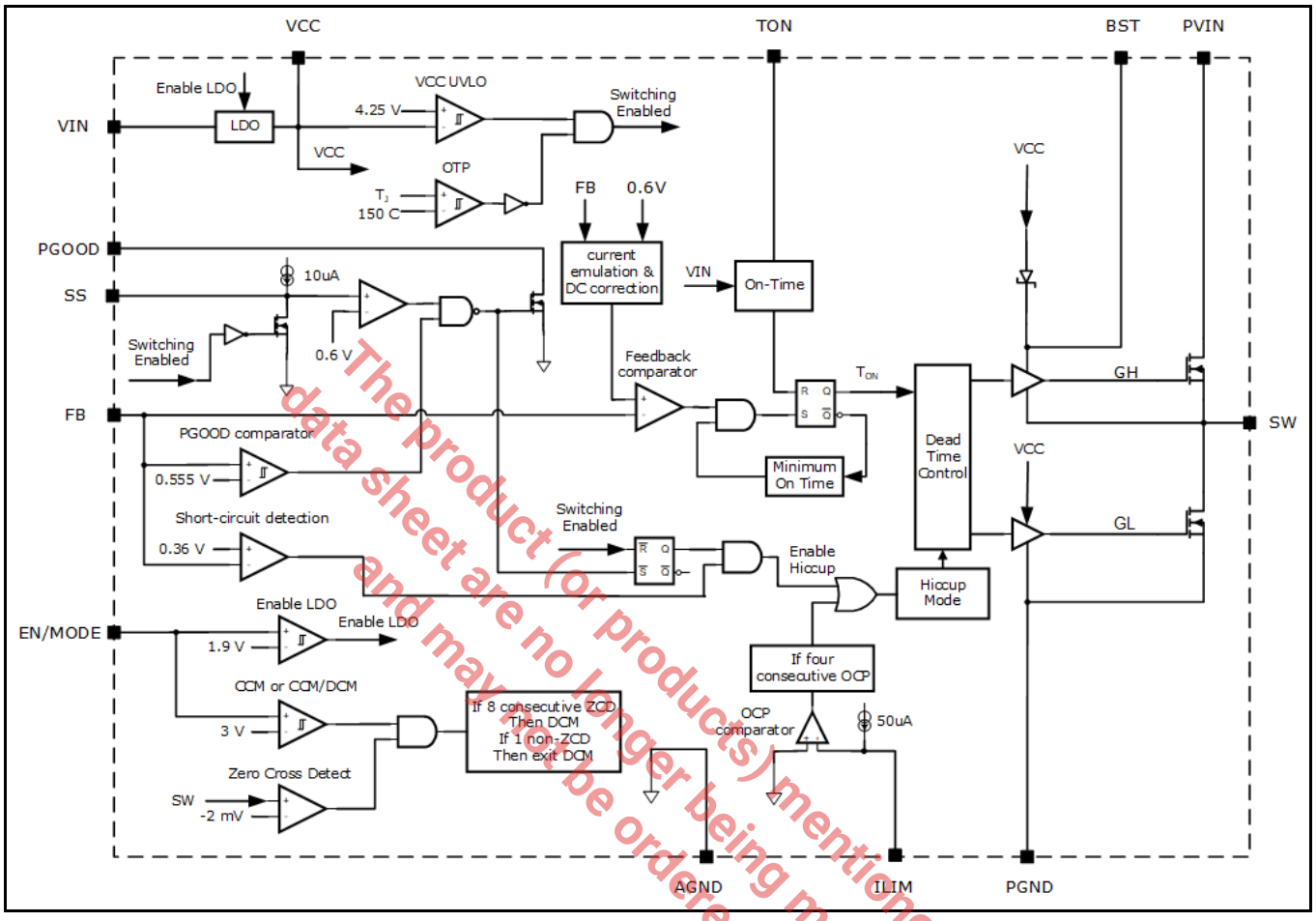


Figure 3: XR76115 Block Diagram

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Pin Assignment

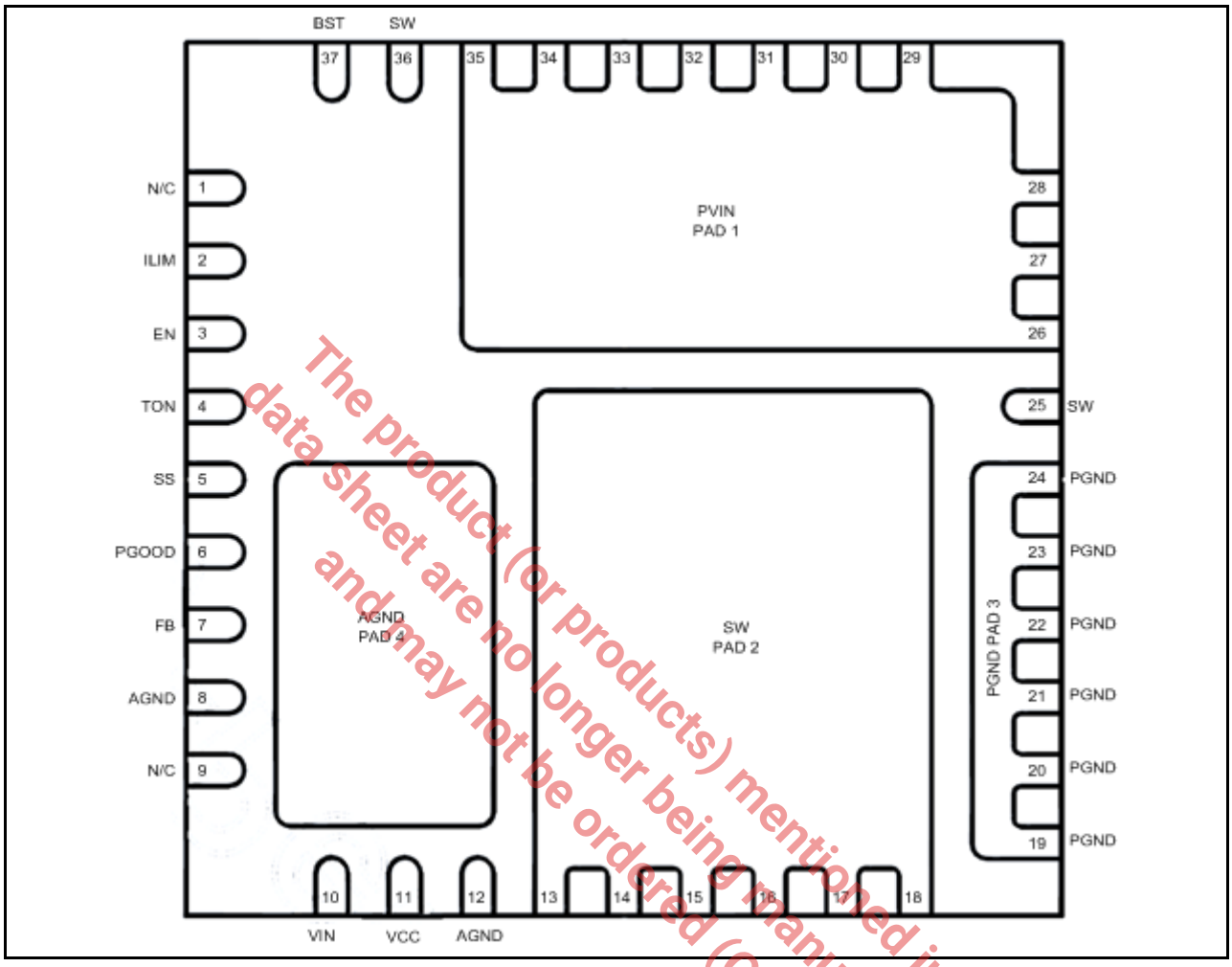


Figure 4: XR76115 Pin Assignment, Top View

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Pin Description

Name	Pin Number	Description
NC	1,9	Not connected.
ILIM	2	Over-current protection programming. Connect with a resistor to SW.
EN/MODE	3	Precision enable pin. Pulling this pin above 1.9V will turn the regulator on and it will operate in CCM. If the voltage is raised above 3.0V then the regulator will operate in DCM / CCM depending on load.
TON	4	Constant on-time programming pin. Connect with a resistor to AGND.
SS	5	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.
PGOOD	6	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
FB	7	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program V_{OUT}.
AGND	8, 12, AGND Pad	Signal ground for control circuitry. Connect AGND Pad with a short trace to pins 8 and 12.
VIN	10	Supply input for the regulator's LDO. Normally it is connected to PVIN.
VCC	11	The output of regulator's LDO. For operation using a 5V rail, VCC should be shorted to VIN.
SW	13-18, 25, 36, SW Pad	Switch node. The drain of the low-side N-channel MOSFET. The source of the high-side MOSFET is wire-bonded to the SW pad.
PGND	19-24, PGND Pad	Ground of the power stage. Should be connected to the system's power ground plane. The source of the low-side MOSFET is wire-bonded to PGND Pad.
PVIN	26-35, PVIN Pad	Input voltage for the power stage. The drain of the high-side N-channel MOSFET.
BST	37	High-side driver supply pin. Connect a 1µF bootstrap capacitor between BST and SW.

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Typical Performance Characteristics

All data taken at V_{IN} = 12V, V_{OUT} = 1.2V, f = 600kHz, T_A = 25°C, no air flow, Forced CCM, unless otherwise specified. The schematic and BOM are from the Applications Circuit section of this datasheet.

REGULATION

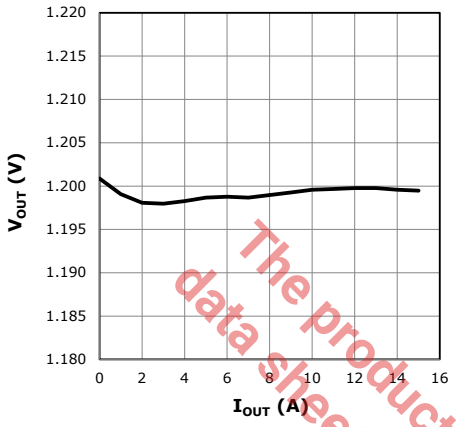


Figure 5: Load Regulation, V_{IN}=12V

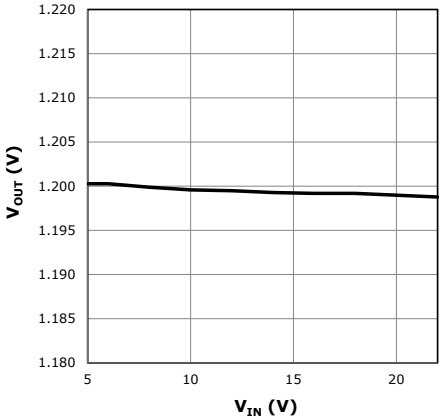


Figure 6: Line Regulation, I_{OUT}=15A

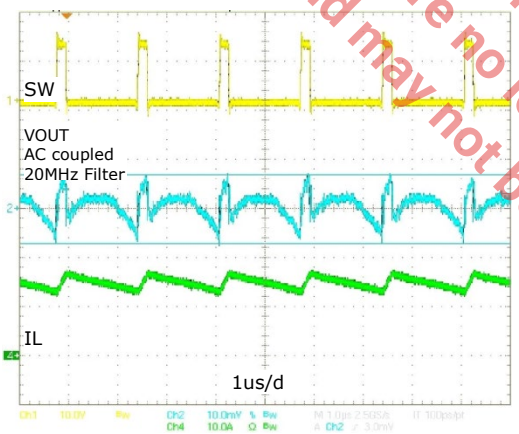


Figure 7: V_{OUT} Ripple is 14mV at 15A



Figure 8: V_{OUT} Ripple is 23mV at 0A, DCM

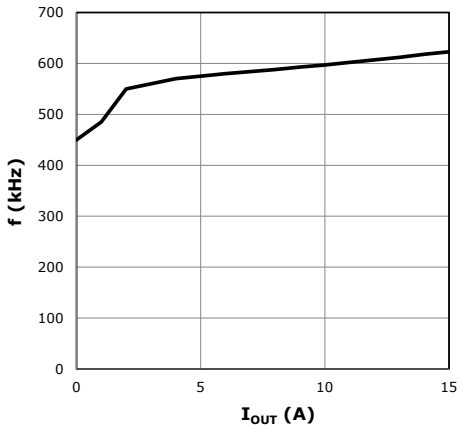


Figure 9: Frequency vs. I_{OUT}, Forced CCM

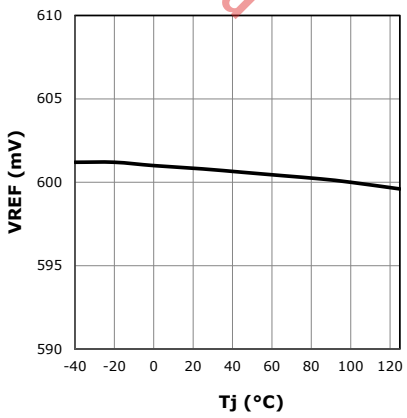


Figure 10: V_{REF} vs. Temperature

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Typical Performance Characteristics

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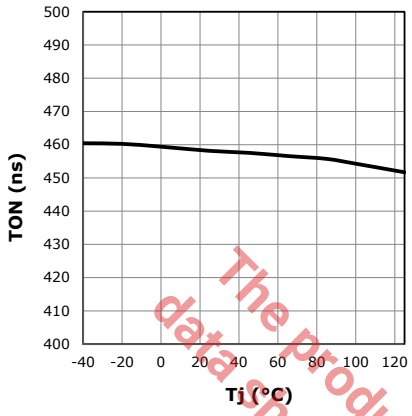


Figure 11: On-Time vs. Temperature

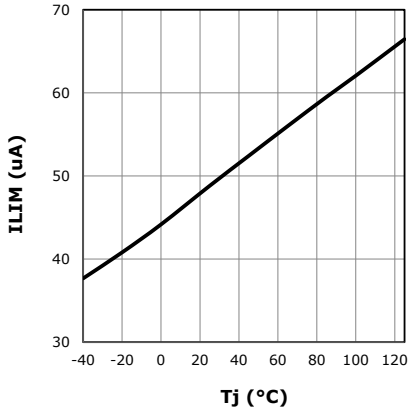


Figure 12: I_{LIM} vs. Temperature

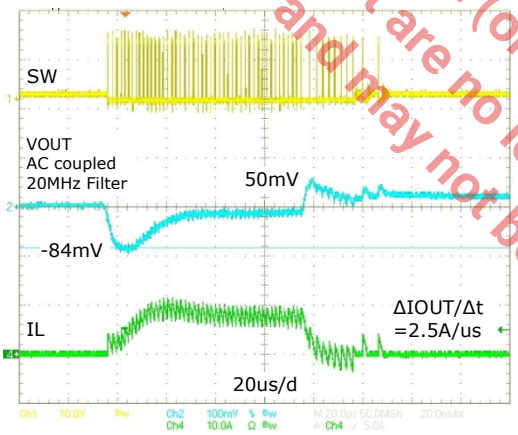


Figure 13: Load Step, DCM / CCM, 0A - 7.5A - 0A

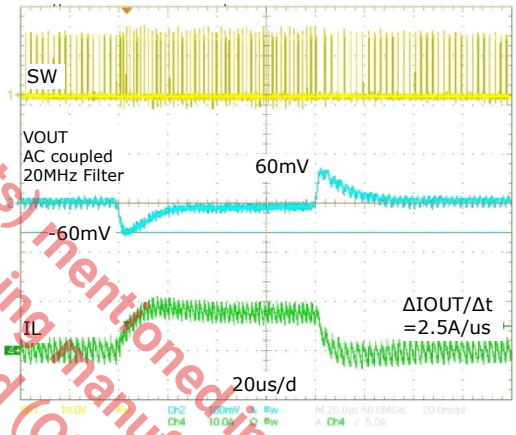


Figure 14: Load Step, Forced CCM, 0A - 7.5 - 0A

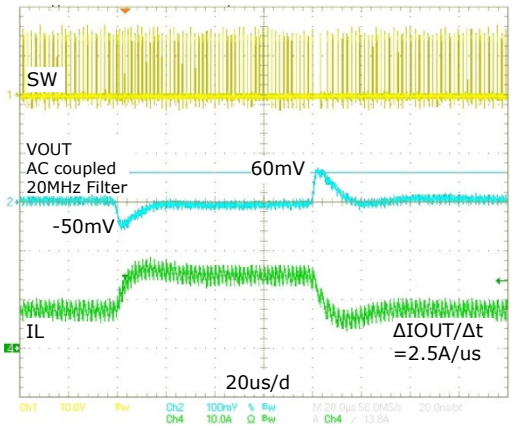


Figure 15: Load Step, Forced CCM, 7.5A - 15A - 7.5A

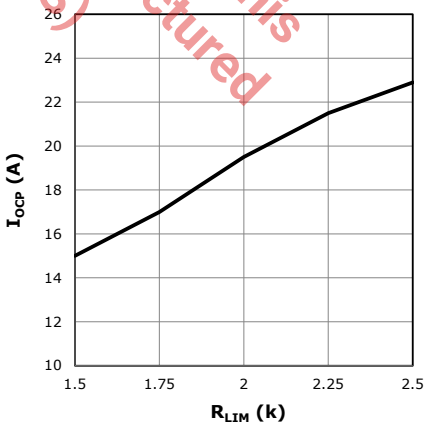


Figure 16: Typical I_{OCP} versus R_{LIM}

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Power-up

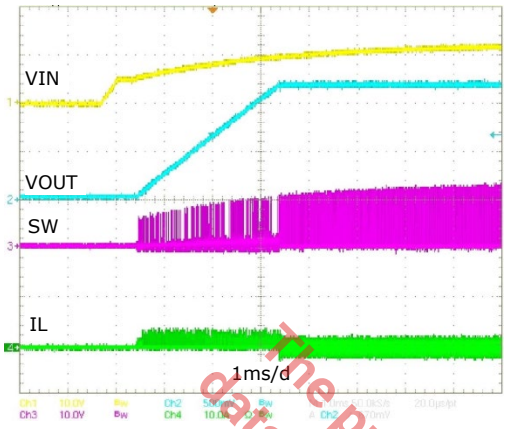


Figure 17: Power-up, Forced CCM, I_{OUT} = 0A

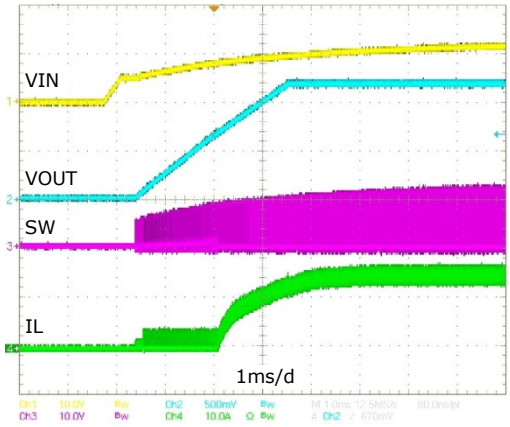


Figure 18: Power-up, Forced CCM, I_{OUT} = 15A

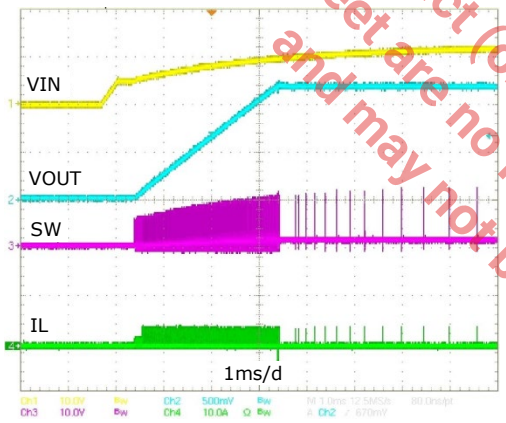


Figure 19: Power-up, DCM / CCM, I_{OUT} = 0A

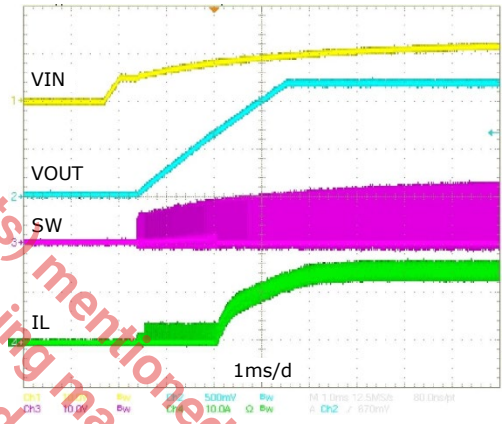


Figure 20: Power-up, DCM / CCM, I_{OUT} =15A

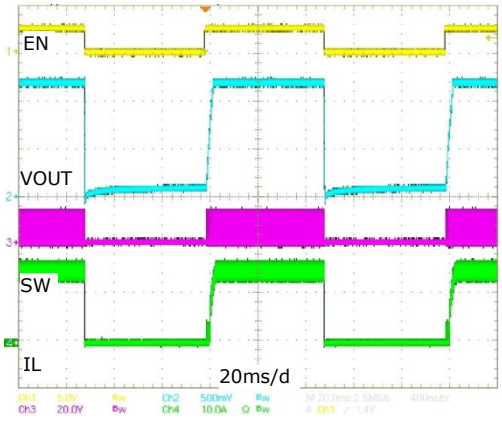


Figure 21: Enable Turn On / Turn Off, 1.2V_{OUT}, 15A

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Efficiency and Thermal Characteristics

$T_{AMBIENT}$ = 25°C, no air flow, inductor losses are included.

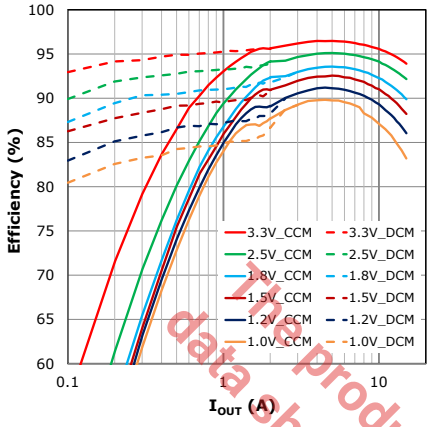


Figure 22: $5V_{IN}$, 600kHz, 0.47µH

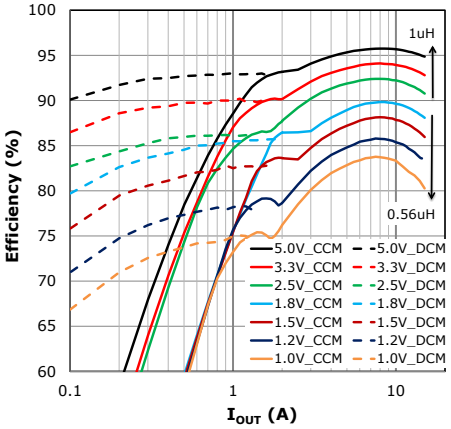


Figure 23: $12V_{IN}$, 600kHz

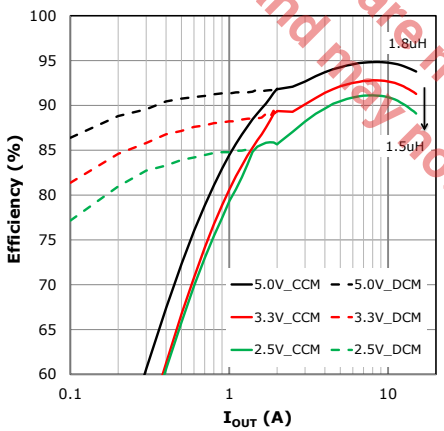


Figure 24: $22V_{IN}$, 400kHz

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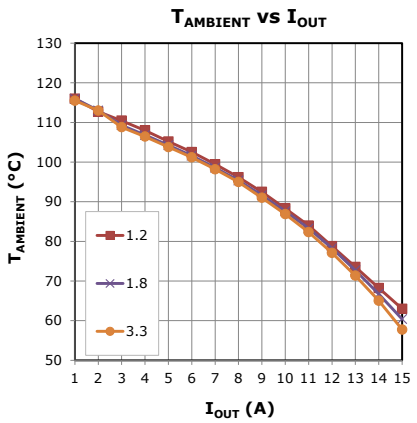


Figure 25: Package Thermal Derating, 12VIN

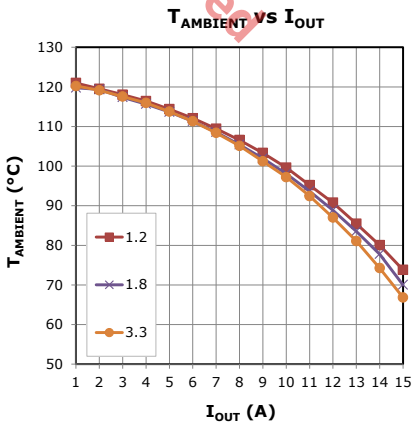


Figure 26: Package Thermal Derating, 5VIN

Detailed Operation

The XR76115 uses a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) control scheme. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with the high-side (switching) FET turning on for a pre-programmed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed the Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and allows for the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable / Mode

The EN/MODE pin accepts a tri-level signal that is used to control channel turn-on and turn-off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN is pulled below 1.9V, the regulator shuts down. A voltage between 1.9V and 3V selects the Forced CCM mode, which will run the converter in continuous conduction for all load currents. A voltage higher than 3V selects the DCM / CCM mode, which will run the converter in discontinuous conduction mode at light loads.

Selecting the Forced CCM Mode

In order to set the controller to operate in Forced CCM, a voltage between 1.9V and 3.0V must be applied to the EN/MODE pin. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE signal can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 27 can be used to generate the required voltage. Note that at V_{IN} of 5.5V to 22V, the nominal Zener voltage is respectively 4.0V to 5.0V. Therefore, for V_{IN} in the range of 5.5V to 22V, the circuit shown in Figure 27 will generate voltage at the EN/MODE pin required for Forced CCM.

Selecting the DCM / CCM Mode

In order to set the controller operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to the EN/MODE pin. In applications where an external control signal is not available, the EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4.0V. If V_{IN} varies over a wide range, the circuit shown in Figure 28 can be used to generate the required voltage.

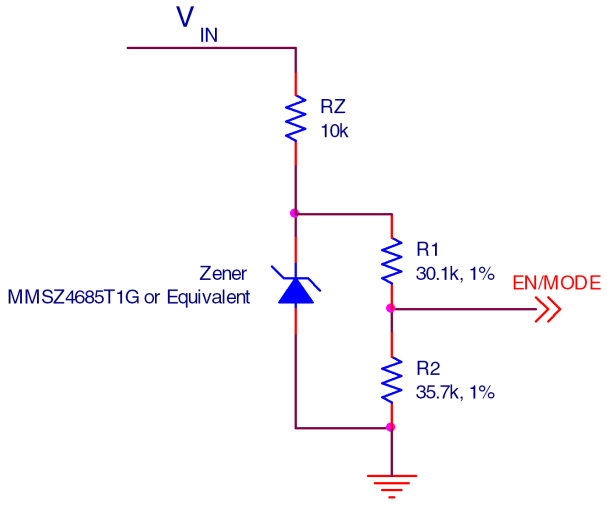


Figure 27: Selecting Forced CCM by deriving EN/MODE from V_{IN}

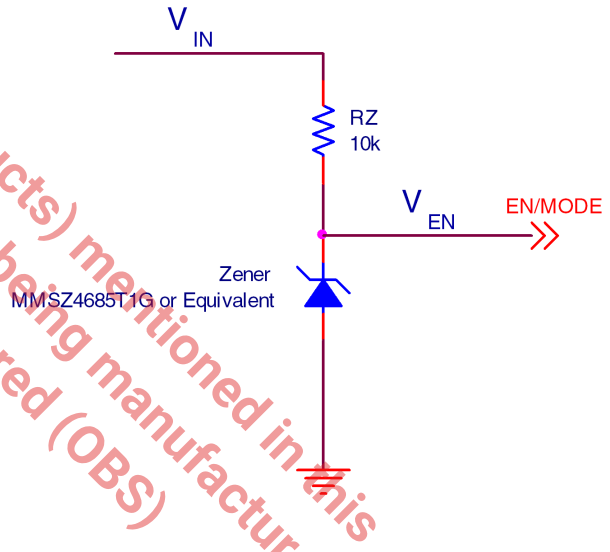


Figure 28: Selecting DCM/CCM by Deriving EN/MODE from V_{IN}

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Programming the On-Time

The on-time T_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON} - (2.5 \times 10^{-8})]}{3 \times 10^{-10}}$$

T_{ON} is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff.}$$

where:

f is the desired switching frequency at nominal I_{OUT}

Eff. is the converter efficiency corresponding to nominal I_{OUT}

Substituting for T_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{f \times Eff.}\right) - [(2.5 \times 10^{-8}) \times V_{IN}]}{(3 \times 10^{-10})}$$

Over-Current Protection (OCP)

If the load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then the regulator enters the hiccup mode of operation. In hiccup mode, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, the hiccup timeout will repeat. The regulator will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program over-current protection, use the following equation:

$$R_{ILIM} = \frac{(I_{OCP} \times R_{DSON}) + 8mV}{I_{LIM}}$$

where:

R_{LIM} is resistor value for programming I_{OCP}

I_{OCP} is the over-current value to be programmed

R_{DSON} = 4.6mΩ (maximum specification)

8mV is the OCP comparator offset

I_{LIM} is the internal current that generates the necessary OCP comparator threshold (use 45µA)

Note that I_{LIM} has a positive temperature coefficient of 0.4%/°C. This is meant to approximately match and compensate for positive temperature coefficient of the synchronous FET.

The above equation is for worst-case analysis and safeguards against premature OCP. The actual value of I_{OCP}, for a given R_{LIM}, will be higher than that predicted by the above equation. Typical I_{OCP} versus R_{LIM} is shown in Figure 16.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the regulator will enter hiccup mode. Hiccup mode will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature Protection (OTP)

OTP triggers at a nominal controller temperature of 150°C. The gates of the switching FET and the synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in Figure 1 to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

The recommended value for R2 is 2kΩ.

Programming the Soft-start

Place a capacitor C_{SS} between the SS and GND pins to program the soft-start. In order to program a soft-start time of T_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS} = T_{SS} \times \frac{10uA}{0.6V}$$

Feed-Forward Capacitor C_{FF}

A feed-forward capacitor C_{FF} may be necessary, depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used, then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2\ x\ \pi\ x\ R1\ x\ 7\ x\ f_{LC}}$$

where:

R1 is the resistor that C_{FF} is placed in parallel with

f_{LC} is the frequency of the output filter double pole

f_{LC} must be less than 15kHz when using ceramic C_{OUT}. If necessary, increase C_{OUT} and / or L in order to meet this constraint.

When using capacitors with higher ESR, such as the Panasonic TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of the output LC double pole f_{LC} should be less than 10kHz
2. The frequency of ESR zero $f_{ZERO,ESR}$ should be at least five times larger than f_{LC}

Note that if $f_{ZERO,ESR}$ is less than 5 x f_{LC}, then it is recommended to set the f_{LC} at less than 2kHz. C_{FF} is still not required.

Feed-Forward Resistor R_{FF}

Poor PCB layout and / or extremely fast switching FETs can cause switching noise at the output and may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor R_{FF} in series with C_{FF}. An R_{FF} value up to 2% of R1 is acceptable.

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Maximum Allowable Voltage Ripple at FB Pin

Note that the steady-state voltage ripple at the feedback pin ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the controller to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV, then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Thermal Design

Proper thermal design is critical in controlling device temperatures and in achieving robust designs. There are a number of factors that affect the thermal performance. One key factor is the temperature rise of the devices in the package, which is a function of the thermal resistances of the devices inside the package and the power being dissipated.

The thermal resistance of the XR76115 is specified in the "Operating Ratings" section of this datasheet. The JEDEC θ_{JA} thermal resistance provided is based on tests that comply with the JESD51-2A "Integrated Circuit Thermal Test Method Environmental Conditions – Natural Convection" standard. JESD51-xx are a group of standards whose intent is to provide comparative data based on a standard test condition which includes a defined board construction. Since the actual board design in the final application will be different from the board defined in the standard, the thermal resistances in the final design may be different from those shown.

The package thermal derating curves for the XR76115 are shown in Figures 25 and 26. These correspond to input voltage of 12V and 5V, respectively.

Applications Circuit

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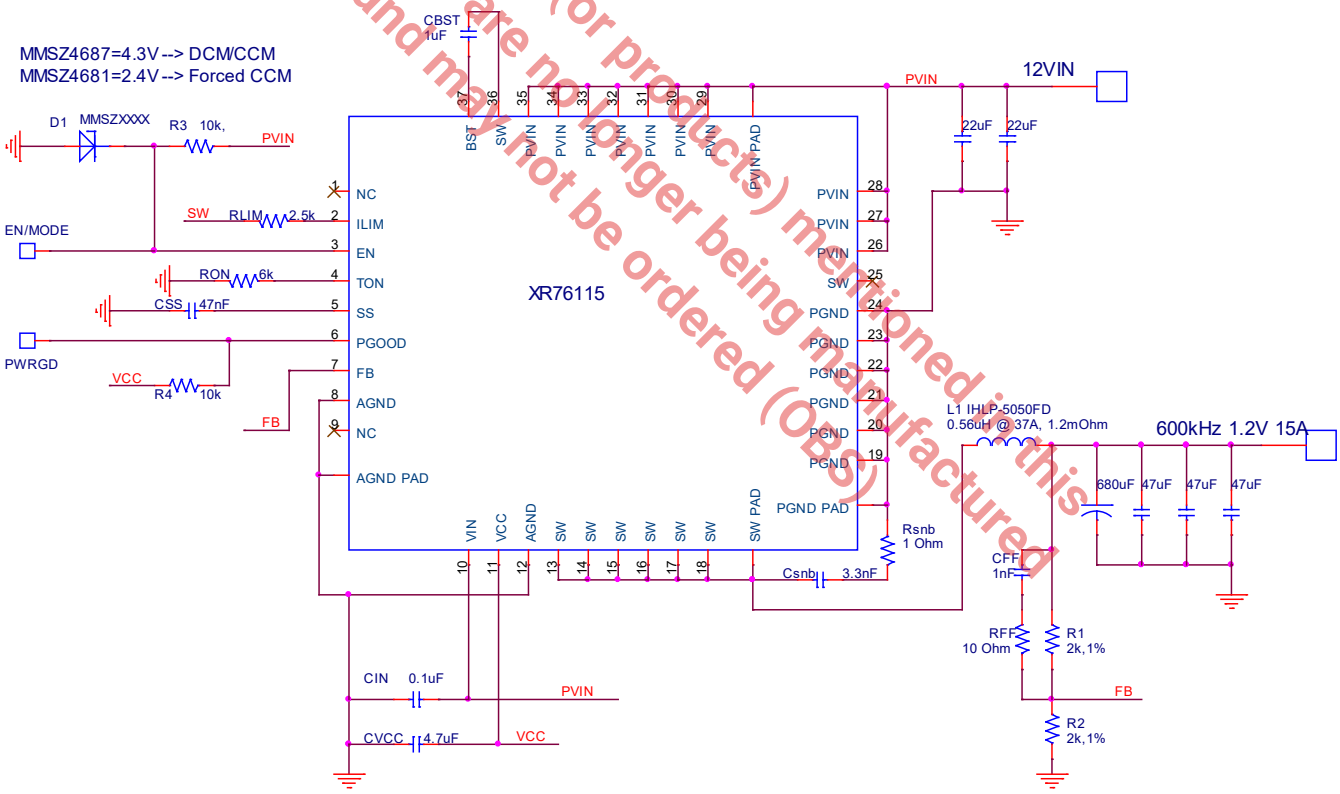
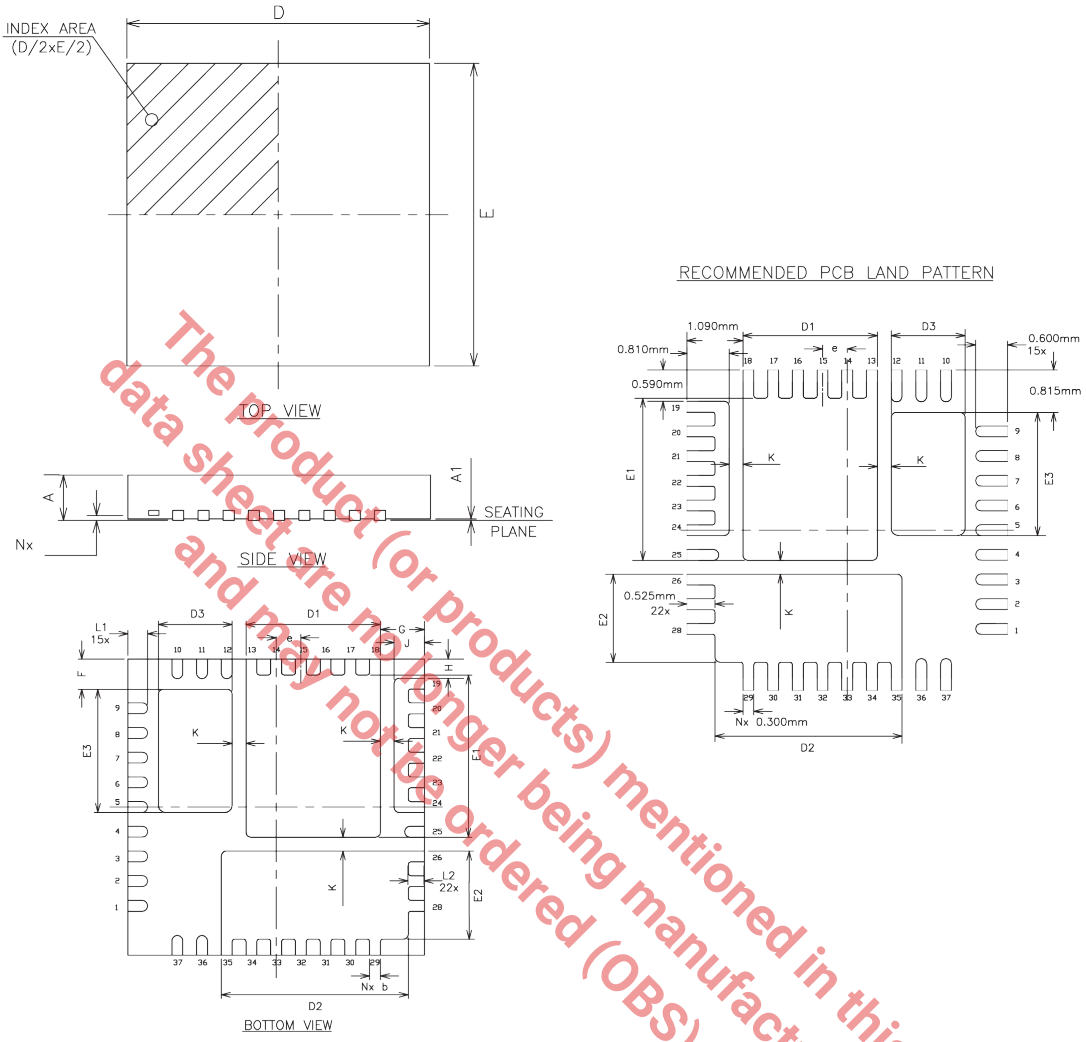


Figure 29: XR76115 Application Circuit Schematic

Mechanical Dimensions



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37LD 6x6mm QFN 0.50 PITCH						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.800	0.900	1.000	0.031	0.035	0.039
A1	0.000	0.020	0.050	0.000	0.001	0.002
b	0.180	0.250	0.300	0.007	0.010	0.012
D		6.000 BSC			0.240 BSC	
E		6.000 BSC			0.240 BSC	
e		0.500 BSC			0.020 BSC	
F		0.615 REF			0.024 REF	
G		0.890 REF			0.035 REF	
H		0.390 REF			0.015 REF	
J		0.610 REF			0.024 REF	
K		0.280 REF			0.011 REF	
D1	2.570	2.720	2.820	0.101	0.107	0.111
E1	3.135	3.285	3.385	0.123	0.129	0.133
D2	3.635	3.785	3.885	0.143	0.149	0.153
E2	1.635	1.785	1.885	0.064	0.070	0.074
D3	1.345	1.495	1.595	0.053	0.059	0.063
E3	2.345	2.495	2.595	0.092	0.098	0.102
L1	0.300	0.400	0.500	0.012	0.016	0.020
L2	0.225	0.325	0.425	0.009	0.013	0.017
N		37			37	

Drawing No: POD-00000019
Revision: A

Revision History

Revision	Date	Description
1A	March 2014	Initial release: ECN 1413-14 03-26-2014
1B	August 2015	Changed “On-Time 2” specification to: Min=170ns, Typ=200ns, Max= 230ns Changed “On-Time 3” specification to: Min=365ns, Typ=430ns, Max= 495ns Changed “f corresponding to On-Time 2” specification to: Min=362 kHz, Typ=417 kHz, Max= 490 kHz removed “f corresponding to On-Time 2” specifications for VOUT=3.3V, removed Diode Emulation Mode write up, modified Functional Block Diagram, modified Feed-Forward Capacitor write up, modified Programming the On-Time write up; added “Selecting the Forced CCM Mode”, “Selecting the DCM/CCM Mode”, “Feed-Forward Resistor”, “Maximum Allowable Voltage Ripple at FB Pin” sections
1C	June 2018	Updated to MaxLinear logo. Updated format and Ordering Information table.
1D	10/18/19	Correct block diagram by changing the input gate into the Hiccup Mode from an AND gate to an OR gate. Update ordering information.

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Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com

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