XR81411

Universal Quad Clock - High Frequency LVCMOS/LVDS/LVPECL Clock Synthesizer

General Description

The XR81411 is a Quad Clock synthesizer with 4 independent PLLs in a compact LGA-45 package. Each synthesizer generates ANY frequency in the range of 10 MHz to 800MHz by utilizing a highly flexible delta sigma modulator and a wide ranging VCO. The outputs are independently configurable for single ended LVCMOS or differential LVDS or LVPECL. The clock outputs have very low typical phase noise jitter of sub 0.6ps RMS, while consuming extremely low power. The XR81411 uses a single reference and provides 4 independent outputs that can be configured as needed to support a wide variety of applications.

Each of the XR81411's 4 independent PLLs include an integer/fractional divider, LVCMOS/LVDS/LVPECL output driver, 3.3V/2.5V supply, and generates one of four selectable output frequencies from a single reference. The XR81411 is optimized for use with a fundamental mode 10MHz to 60MHz crystal (or system clock) and generates a selection of output frequencies ranging from 10MHz to 800MHz in either integer or fractional mode. In fractional mode, frequency resolution of better than 2Hz steps can be achieved.

The application diagram below shows a typical LAN synthesizer configuration with any standard crystal oscillating in fundamental mode.

The typical phase noise plot below shows the jitter integrated over the 12KHz to 20MHz range that is widely used in these systems.

FEATURES

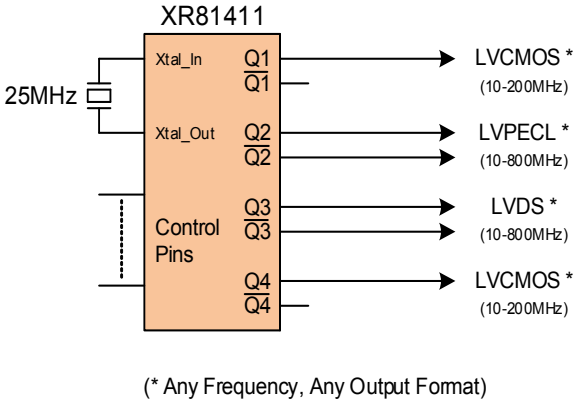
- Small footprint 5mm x 5mm LGA package
- Configurable Outputs - As differential LVPECL/ LVDS pair or as a single ended LVCMOS.
- Crystal oscillator interface which can also be overdriven using a single-ended reference clock
- Output frequency range: 10MHz - 800MHz
- Crystal/input frequency: 10MHz to 60MHz, parallel resonant crystal
- VCO range: 2GHz - 3GHz
- Phase jitter @
  - 125MHz (12KHz - 20MHz): <0.6ps RMS
  - 125MHz (1.875MHz -20MHz): <0.25ps RMS
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) package

APPLICATIONS

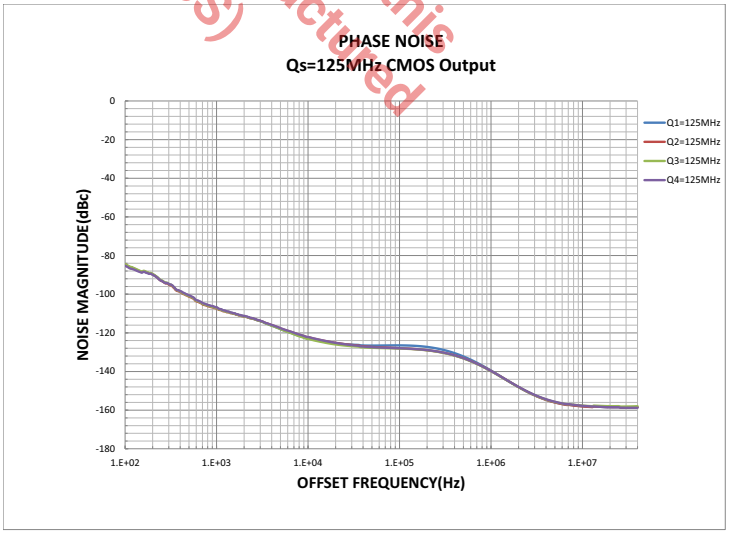
- 10GE, GE LAN/WAN
- 2.5G/10G SONET/SDH/OTN
- xDSL, PCIe
- Low-jitter Clock Generation
- Synchronized clock systems

Ordering Information – Last Page

Typical Application Diagram and Performance



(* Any Frequency, Any Output Format)



Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Maximum Rating condition for extended periods may affect device reliability and lifetime.

Power Supply Voltage (V_{DD}).....+4.2V

Input Voltage.....-0.5V to V_{DD} + 0.5V

Output Voltage.....-0.5V to V_{DD} + 0.5V

Reference Frequency/Input Crystal.....10MHz to 60MHz

Storage Temperature.....-55°C to +125°C

Lead Temperature (Soldering, 10 sec).....300°C

ESD Rating (HBM - Human Body Model).....2.0kV

Operating Conditions

Operating Temperature Range.....-40°C to +85°C

Electrical Characteristics

Specifications are at T_A = 25°C, V_{DD} = 3.3V±5% or 2.5V±5%, V_L = V_{DD}; Limits applying over the full -40°C to +85°C operating temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
3.3V Power Supply DC Characteristics							
V_{DD}	Power Supply Voltage		•	3.135	3.3	3.465	V
I_{DD}	Power Supply Current LVPECL LVDS LVCMOS	Includes output loading Measured at 800MHz, Figure 5, (note 1) Measured at 800MHz, Figure 8, (note 1) Measured at 200MHz, Figure 10, (note 1, 2)	 • • •		 385 165 140	 415 190 170	 mA mA mA
2.5V Power Supply DC Characteristics							
V_{DD}	Power Supply Voltage		•	2.375	2.5	2.625	V
I_{DD}	Power Supply Current LVPECL LVDS LVCMOS	Includes output loading Measured at 800MHz, Figure 6, (note 1) Measured at 800MHz, Figure 9, (note 1) Measured at 200MHz, Figure 10, (note 1, 2)	 • • •		 285 115 85	 305 135 110	 mA mA mA
LVCMOS/LVTTL DC Input Characteristics							
V_{IH}	Input High Voltage (OE, FSEL[1:0])	V_{DD} = 3.465V	•	2.42		V_{DD} + 0.3	V
		V_{DD} = 2.625V	•	1.83		V_{DD} + 0.3	V

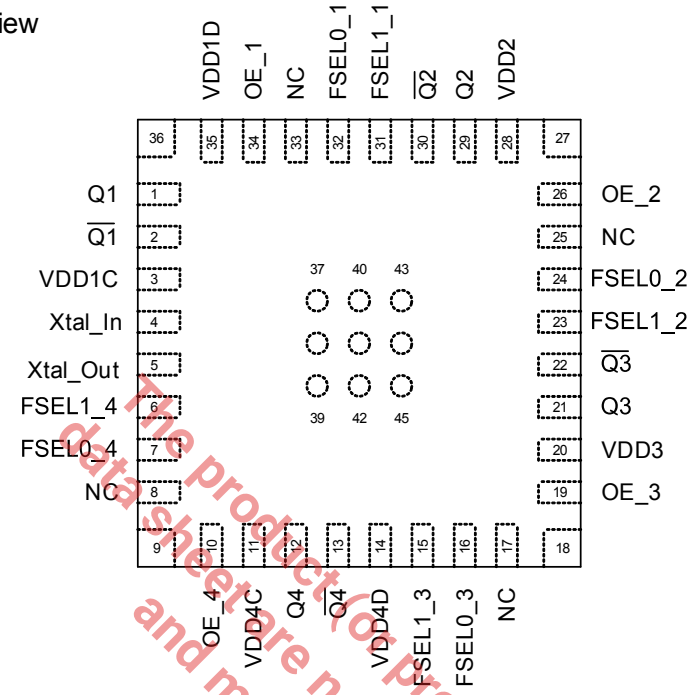
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage (OE, FSEL[1:0])	V_{DD} = 3.465V	•	-0.3		1.03	V
		V_{DD}= 2.625V	•	-0.3		0.785	V
I_{IH}	Input High Current (OE, FSEL[1:0])	V_{IN} = V_{DD} = 3.465V or 2.625V	•			15	µA
I_{IL}	Input Low Current (OE, FSEL[1:0])	V_{IN} = 0V, V_{DD} = 3.465V or 2.625V	•	-10			µA
LVCMOS DC Output Characteristics (V_{DD} = 3.3 +/- 5% or V_{DD} = 2.5 +/- 5%)							
V_{OH}	Output High Voltage	Output Unloaded	•	0.8 * V_{DD}			V
V_{OL}	Output Low Voltage	Output Unloaded	•			0.1 * V_{DD}	V
LVPECL DC Output Characteristics (V_{DD} = 3.3 +/- 5% or V_{DD} = 2.5 +/- 5%)							
V_{OH}	Output High Voltage		•	V_{DD} - 1.3		V_{DD} - 0.3	V
V_{OL}	Output Low Voltage		•	V_{DD} - 2.0		V_{DD} - 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		•	0.6		1.2	V
LVDS DC Output Characteristics (V_{DD} = 3.3 +/- 5% or V_{DD} =2.5 +/- 5%)							
V_{OD}	Differential Output Voltage	Output < 1GHz	•	200		600	mV
V_{OC}	Common Mode Voltage		•		1.25		V
Crystal Characteristics							
X_{Mode}	Mode of Oscillations			Fundamental			
X_f	Frequency			10		60	MHz
ESR	Equivalent Series Resistance					50	Ω
C_S	Shunt Capacitance					7	pF
AC Characteristics							
f_{OUT}	Output Frequency			10		800	MHz
$t1_{jit}(\phi)$	Jitter GbE	125MHz (w/25MHz ref) Integration Range 12kHz-20MHz			0.6	1.0	pS
$t2_{jit}(\phi)$	Jitter GbE	125MHz (w/25MHz ref) Integration Range 1.85MHz-20MHz			0.25	0.45	pS
$t3_{jit}(\phi)$	Jitter OC12	155.52MHz (w/19.44MHz ref) Integration Range 12kHz-5MHz			0.7		pS
t_R/t_F	Output Rise/Fall Time	20% to 80%, see Figure 12	•	100		500	pS
Odc	Output Duty Cycle	see Figure 13	•	45		55	%

* Note 1: All outputs configured identically.

* Note 2: Does not include the load current.

Pin Configuration

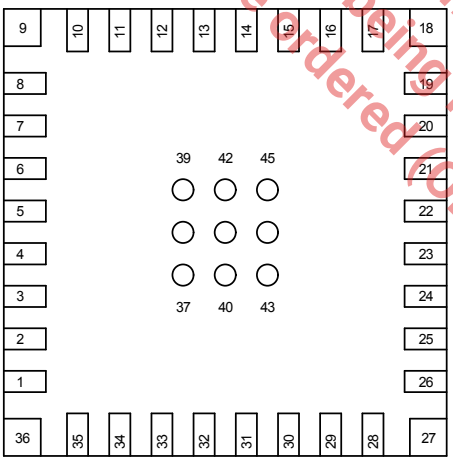
Top View



GND Pads

9, 18, 27, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45

Bottom View

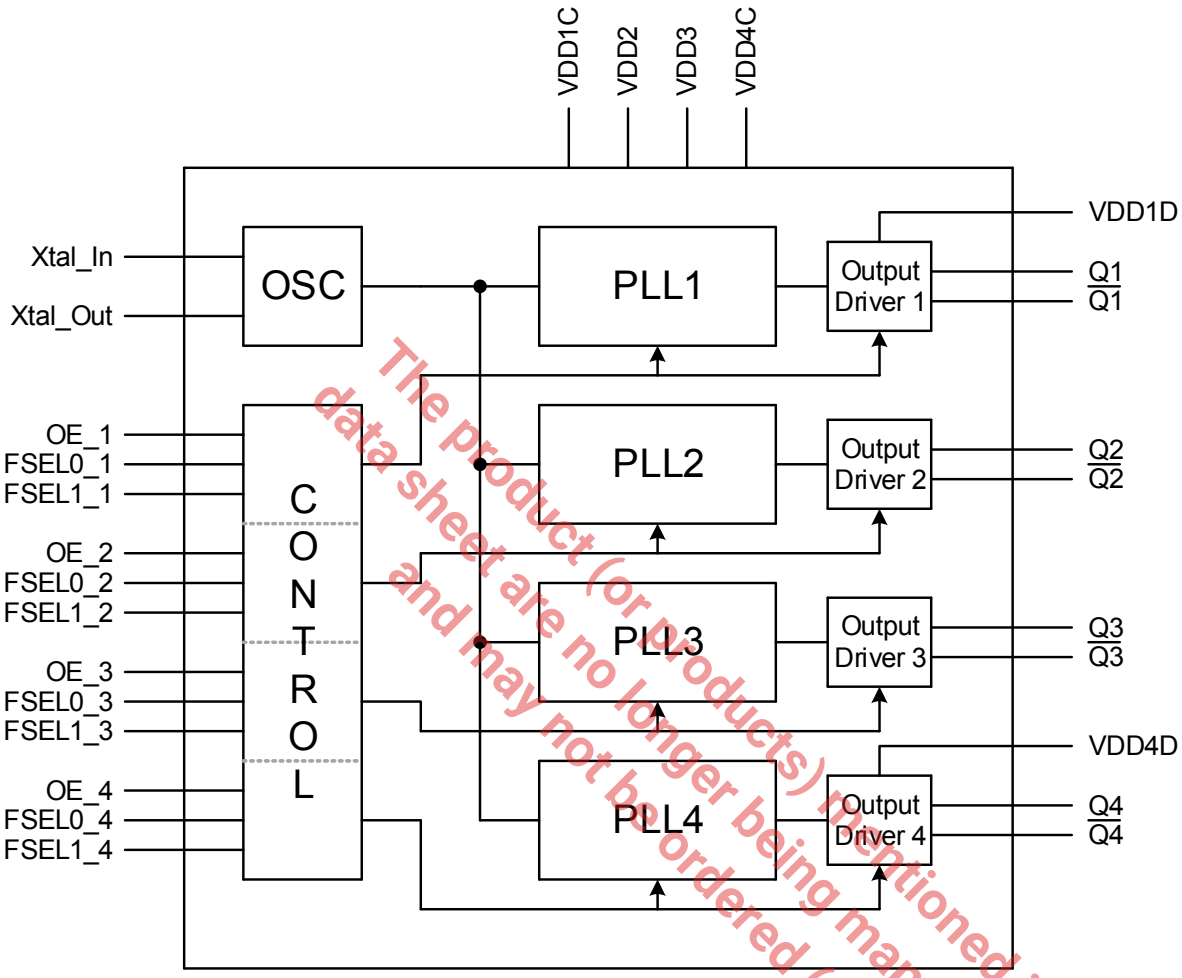


Pin Assignments

Pin No.	Pin Name	Type	Description
1	Q1	Output	Channel 1 Positive Clock Output
2	$\overline{Q1}$	Output	Channel 1Inverted Clock Output
3	VDD1C	Power	Channel 1 Core Supply Voltage
4	XTAL_IN	Input	Crystal oscillator input.
5	XTAL_OUT	Output	Crystal oscillator output (external reference input)
6	FSEL1_4	Input (900KΩ pull-dwn)	Channel 4 Output frequency select 1, MSB (LVCMOS/LVTTL input).
7	FSEL0_4	Input (900KΩ pull-dwn)	Channel 4 Output frequency select 0, LSB (LVCMOS/LVTTL input).
8	NC	No Connection	Do not connect.
9	GND	GND	Ground.
10	OE_4	Input (900KΩ pull-up)	Channel 4 Output enable - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
11	VDD4C	Power	Channel 4 Core Supply Voltage.)
12	Q4	Output	Channel 4 Positive Clock Output.
13	$\overline{Q4}$	Output	Channel 4 Inverted Clock Output.
14	VDD4D	Power	Channel 4 Driver Supply Voltage.)
15	FSEL1_3	Input (900KΩ pull-dwn)	Channel 3 Output frequency select 1, MSB (LVCMOS/LVTTL input).
16	FSEL0_3	Input (900KΩ pull-dwn)	Channel 3 Output frequency select 0, LSB (LVCMOS/LVTTL input).
17	NC	No Connection	Do not connect.
18	GND	GND	Ground.
19	OE_3	Input (900KΩ pull-up)	Channel 3 Output enable - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
20	VDD3	Power	Channel 3 Core and Driver Supply Voltage.
21	Q3	Output	Channel 3 Positive Clock Output.
22	$\overline{Q3}$	Output	Channel 3 Inverted Output.
23	FSEL1_2	Input (900KΩ pull-dwn)	Channel 2 Output frequency select 1, MSB (LVCMOS/LVTTL input).
24	FSEL0_2	Input (900KΩ pull-dwn)	Channel 2 Output frequency select 0, LSB (LVCMOS/LVTTL input).
25	NC	No Connection	Do not connect.
26	OE_2	Input (900KΩ pull-up)	Channel 2 Output enable - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
27	GND	GND	Ground.

Pin No.	Pin Name	Type	Description
28	VDD2	Power	Channel 2 Core and Driver Supply Voltage.
29	Q2	Output	Channel 2 Positive Clock Output.
30	$\overline{Q2}$	Output	Channel 2 Inverted Clock Output.
31	FSEL1_1	Input (900KΩ pull-dwn)	Channel 1 Output frequency select 1, MSB (LVCMOS/LVTTL input).
32	FSEL0_1	Input (900KΩ pull-dwn)	Channel 1 Output frequency select 0, LSB (LVCMOS/LVTTL input).
33	NC	No Connection	Do not connect.
34	OE_1	Input (900KΩ pull-up)	Channel 1 Output enable - LVCMOS/LVTTL active high input. Outputs are enabled when OE = high. Outputs are disabled when OE = low.
35	VDD1D	Power	Channel 1 Driver Supply Voltage.

Functional Block Diagram



Typical Performance Characteristics

Figures 1, 2, 3 and 4 show typical phase noise performance plots for 125 MHz clock outputs on each of the four outputs. The data was taken using the industry standard Agilent E5052B instrument. The integration range is the widely referenced 12KHz to 20MHz range most often used in LAN applications.

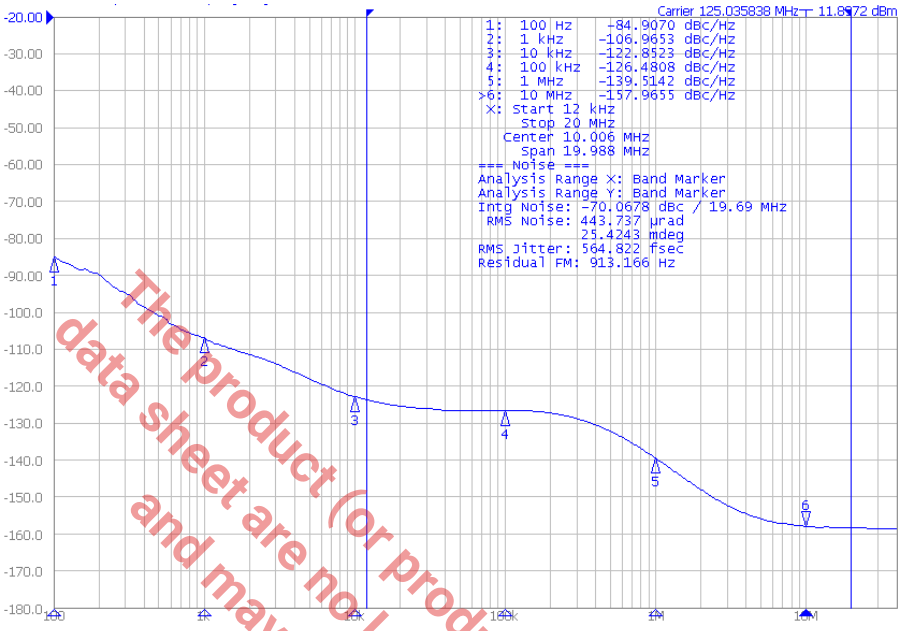


Figure 1: Q1 - 125MHz Operation, Phase Noise at 3.3V

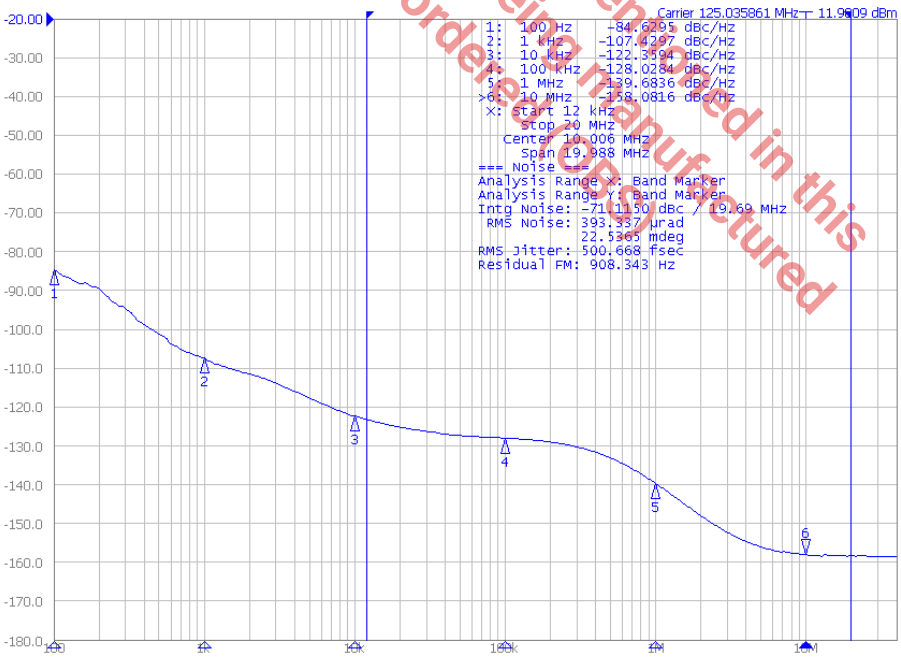


Figure 2: Q2 - 125MHz Operation, Phase Noise at 3.3V)

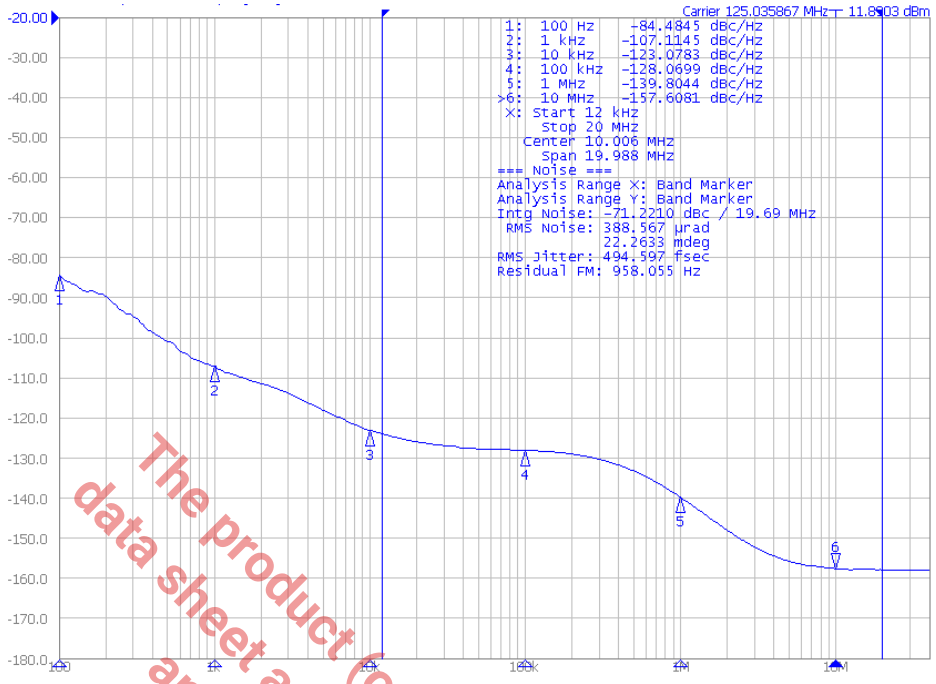


Figure 3: Q3 - 125MHz Operation, Phase Noise at 3.3V

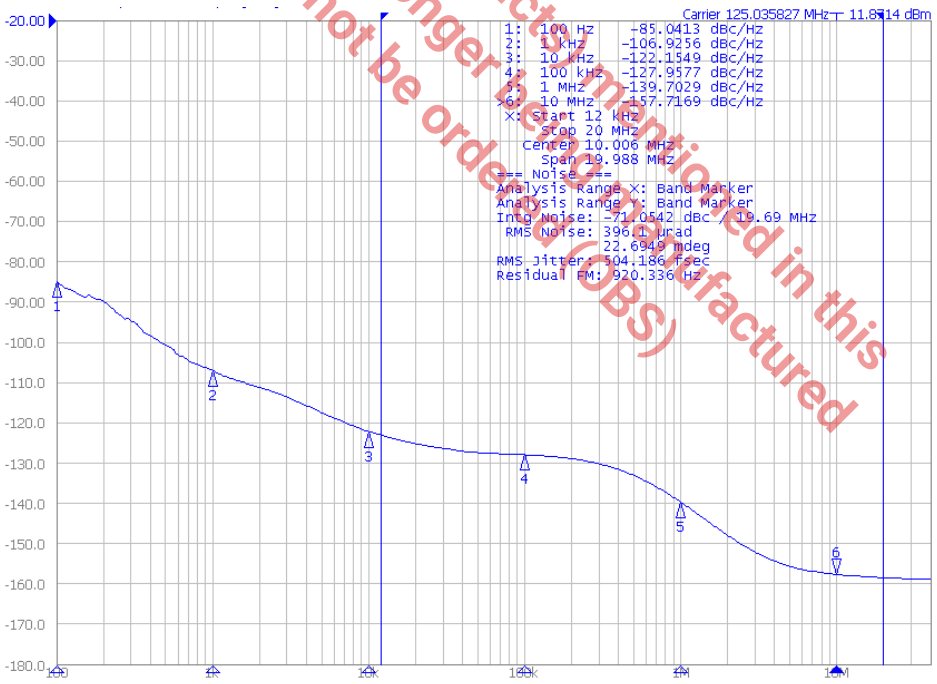


Figure 4: Q4 - 125MHz Operation, Phase Noise at 3.3V

Application Information

Termination for LVPECL Outputs

The termination schemes shown in Figure 5 and Figure 6 are typical for LVPECL outputs. Matched impedance layout techniques should be used for the LVPECL output pairs to minimize any distortion that could impact your maximum operating frequency. Figure 7 is an alternate termination scheme that uses a Y-termination approach.

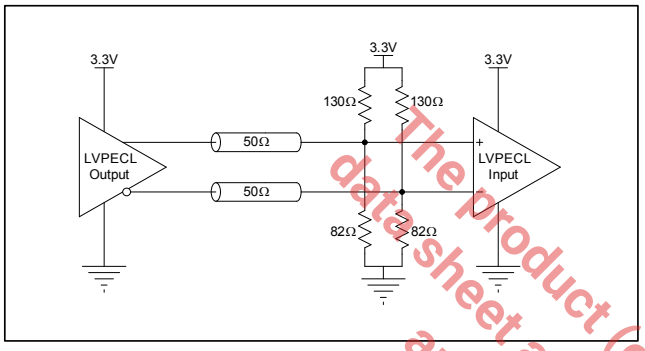


Figure 5: XR81411 3.3V LVPECL Output Termination

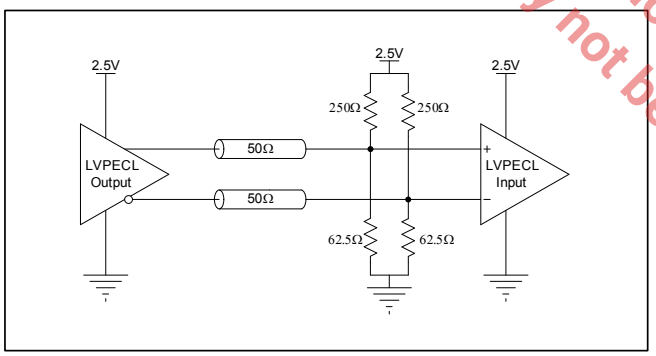


Figure 6: XR81411 2.5V LVPECL Output Termination

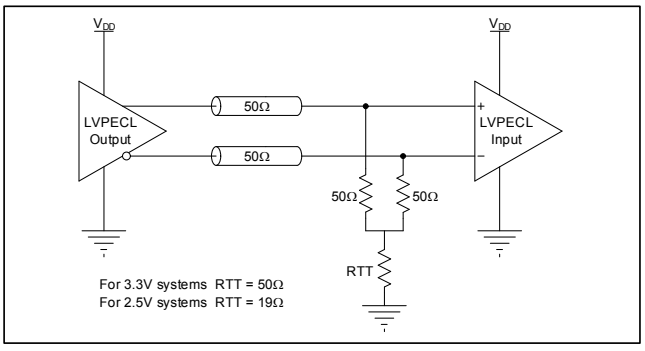


Figure 7: XR81411 Alternate LVPECL Output Termination Using Y-termination

Termination for LVDS Outputs

The termination schemes shown in Figure 8 and Figure 9 are typical for LVDS outputs. LVDS swing is a small, typically 350mV, on 1.2V of common mode. The LVDS output pair needs a 100Ω resistor across the differential pair as close to the destination as possible.

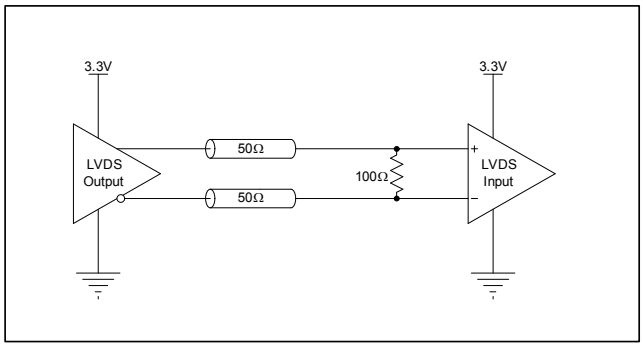


Figure 8: XR81411 3.3V LVDS Output Termination

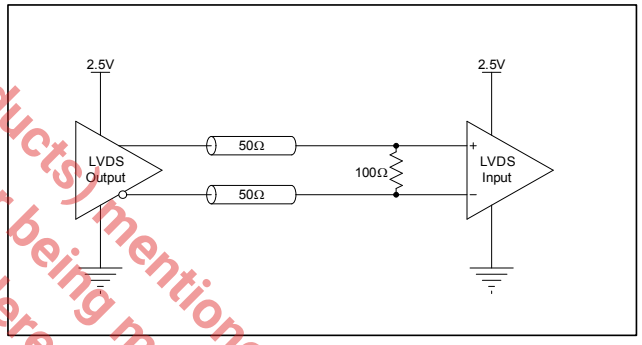


Figure 9: XR81411 2.5V LVDS Output Termination

Termination for LVCMOS Outputs

The termination scheme shown in Figure 10 is typical for LVCMOS outputs. A split supply approach can be used utilizing the scope's internal 50Ω impedance, as shown in Figure 11.

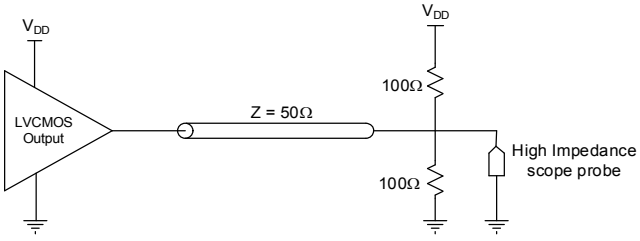


Figure 10: XR81411 LVCMOS Output Termination

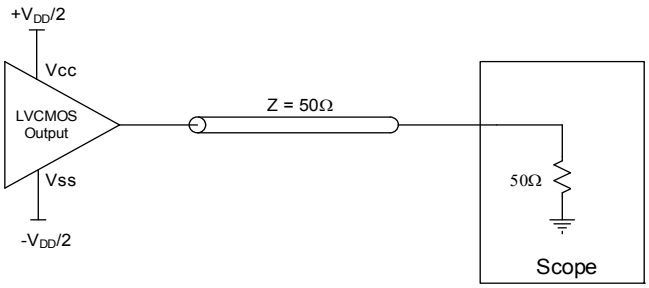


Figure 11: XR81411 Split Supply LVCMOS Output Termination

Output Signal Timing Definitions

The following diagrams clarify the common definitions of the AC timing measurements.

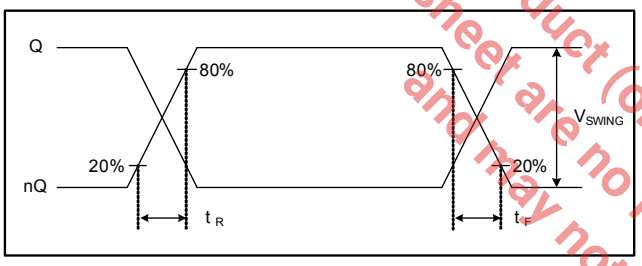


Figure 12: Output Rise/Fall Time and Swing

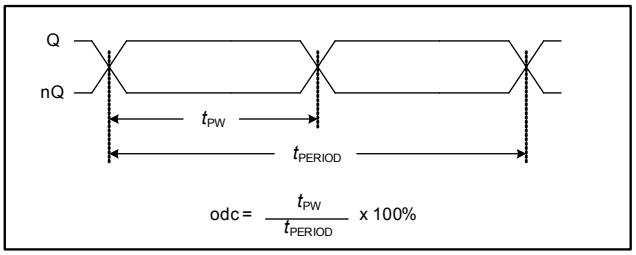


Figure 13: Output Period and Duty Cycle

Configurable Attributes

The XR81411 is highly adaptable and can be configured for many different applications. The device performance of the input stage, PLL stages and the output stages can be adjusted (programmed by the factory) to meet any number of application requirements.

Input Stage

The XR81411's input is designed to be used with a parallel resonant crystal in the range of 10MHz to 60MHz. It can also be overdriven by an external single-ended source. The XR81411 uses a Pierce oscillator circuit that has a variable gain control and selectable capacitor load options on each of the XTAL pins.

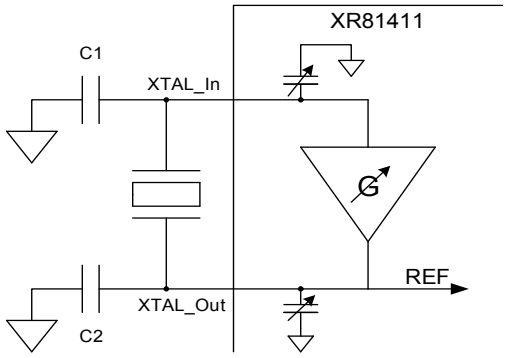


Figure 14: XR81411 Input Stage

The XR81411 input stage also has the ability to use a startup state that can configure the gain and capacitor loading conditions different from normal operation to improve crystal startup time.

PLL Stages

Each of the independent PLLs within the XR81411 can be configured operate at any of four distinct settings. The PLL takes the REF output from the Input stage and can produce any frequency from 10MHz to 800MHz. The PLL can be configured for integer or fractional operation. The internal calibration circuitry of the XR81411 will optimize the configuration of the VCO, LPF and divider (DSM, N and Output) settings for the input and output frequencies chosen.

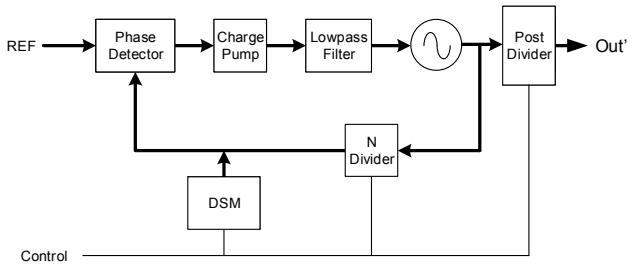


Figure 15: XR81411 PLL

Each of the four Universal Clocks can support up to 4 individual output frequency configurations. Once configured, the two frequency select pins, FSLEL[1:0], will determine the output frequency from the device. This allows the XR81411 to support a variety of applications. If the FSEL pins are left floating, the XR81411 will default (with internal pull-down resistors on the FSEL inputs) to the Frequency #1 output.

Table 1: Output Frequency Selection

FSEL[1:0]	Output Frequency (MHz)
00	Frequency #1
01	Frequency #2
10	Frequency #3
11	Frequency #4
ZZ	Frequency #1

Output Stages

Each of the XR81411's output interfaces can select between LVCMOS, LVPECL or LVDS. If selected for LVCMOS operation, the driver can operate up to 200MHz. If selected for LVPECL or LVDS operation the driver can operate up to 800MHz.

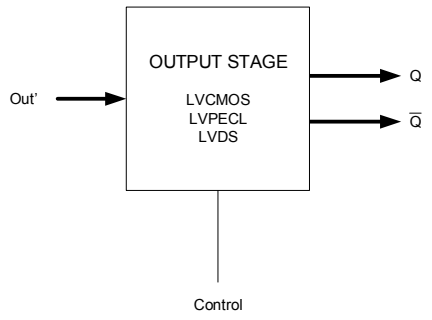


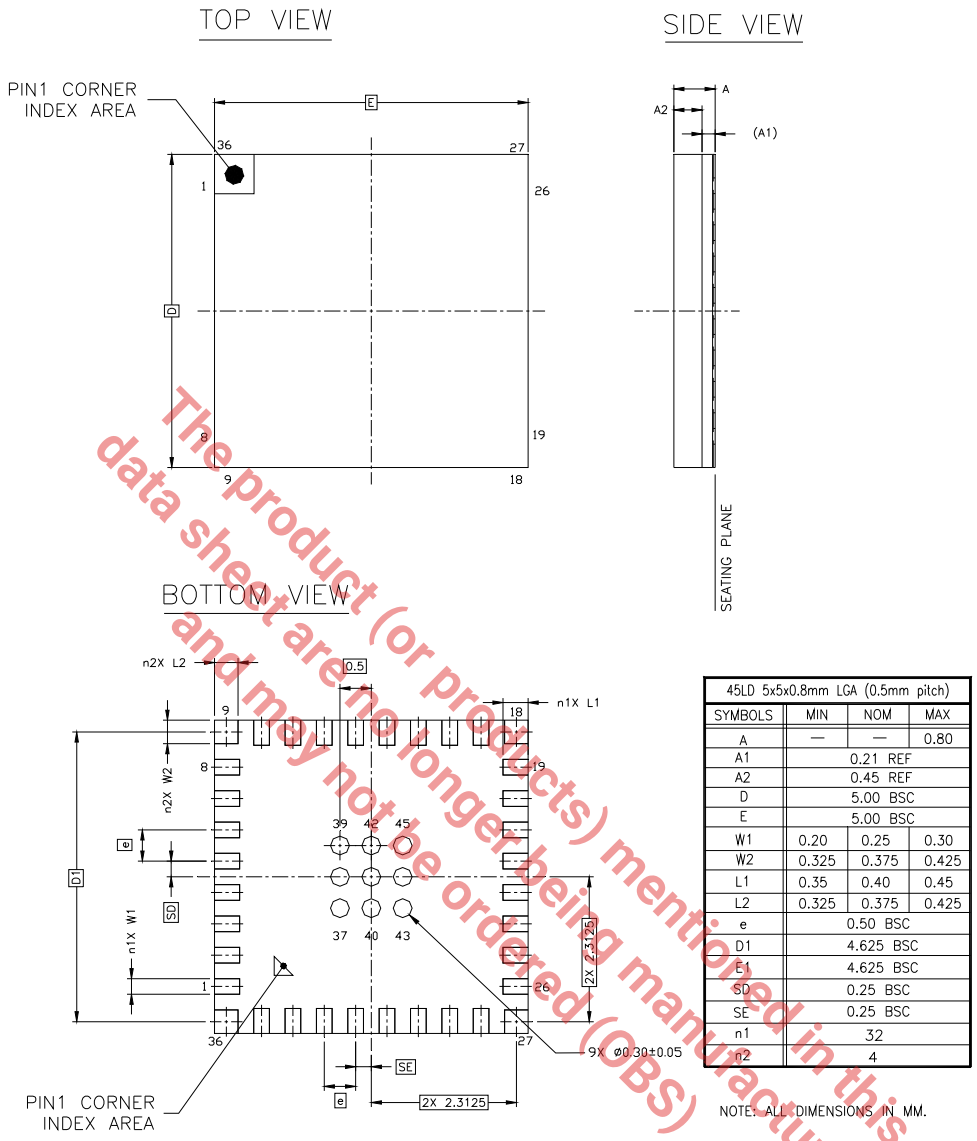
Figure 16: XR81411 Output Stage

Configuration of Universal Clock

For each of the stages - Input, PLL and Output - the final configuration needs to be programmed by the factory. Please contact the factory so that samples can be programmed for your specific application requirements and sent to you for your validation before ordering. To see a list of configuration options available for the XR81411 please send your request to *commtechsupport@exar.com*.

Mechanical Dimensions

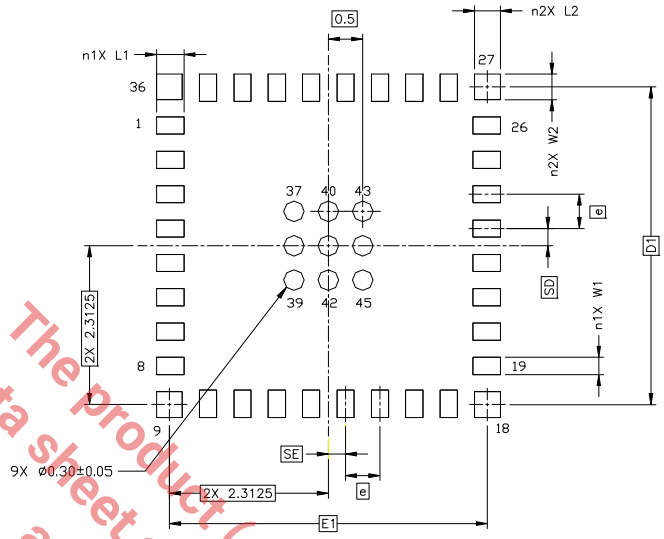
45-Pin LGA



45LD 5x5x0.8mm LGA (0.5mm pitch)			
SYMBOLS	MIN	NOM	MAX
A	—	—	0.80
A1		0.21 REF	
A2		0.45 REF	
D		5.00 BSC	
E		5.00 BSC	
W1	0.20	0.25	0.30
W2	0.325	0.375	0.425
L1	0.35	0.40	0.45
L2	0.325	0.375	0.425
e		0.50 BSC	
D1		4.625 BSC	
E1		4.625 BSC	
SD		0.25 BSC	
SE		0.25 BSC	
n1		32	
n2		4	

NOTE: ALL DIMENSIONS IN MM.

RECOMMENDED PCB LAND PATTERN



Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging	Marking
XR81411-F*	45-pin LGA	Yes	-40°C to +85°C	Tray	XR81411
XR81411TR-F*	45-pin LGA	Yes	-40°C to +85°C	Tape and Reel	XR81411
XR81411EVB	Eval Board	N/A	N/A	N/A	N/A

Note: * All devices must be factory programmed to the customer's configuration for use. Contact factory for programming options at commtechsupport@exar.com.

Revision History

Revision	Date	Description
1A	November 2014	Initial release.

For Further Assistance:

Email: commtechsupport@exar.com

Exar Technical Documentation: http://www.exar.com/techdoc/

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A New Direction in Mixed-Signal