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XR17V35x PCIe UARTs

Design Guide

Revision History

Document No.	Release Date	Change Description
200DGR00	4/24/20	Initial release.

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Introduction

The XR17V35x Design Guide provides a helpful checklist of schematic design and PCB layout tips to aid in applying a XR17V35x PCIe UART to your product design. The XR17V35x Family provides a single lane PCIe 2.0 Gen 1 compliant bridge to 2, 4 or 8 independent enhanced 16550 compatible UARTs and also includes 16 multi-purpose I/Os (MPIOs), a 16-bit general purpose counter / timer and a global interrupt status register.

The design guide contains design information for XR17V354 and XR17V358 which may have a single (master) device or have a dual (master / slave) configuration using the Expansion Interface signals documented. The XR17V352 can only be designed as a single device and does not have an Expansion Interface.

Please refer to the respective XR17V35x datasheet for more information, including application block diagram and pin-out diagram.

Reference Documentation

XR17V352 Data Sheet

XR17V354 Data Sheet

XR17V358 Data Sheet

Visit www.maxlinear.com to obtain copies of these documents.

Pin Groups

The tables below are arranged by the following pin groups:

- PCIe Interface
- Buck Regulator Output
- PCIe UART Expansion Interface Signals (XR17V354 / XR17V358)
- Other PCIe UART "Special Handling" Device Pins
- Analog Voltage Inputs
- Test Inputs
- Voltage Rails

Design and Layout Recommendations

Table 1: PCIe Interface

Schematic Design Recommendations
TX +/- and RX +/- must be AC coupled using 100nF 0603 or smaller (0402) recommended) ceramic capacitors at the transmitting source.
Layout Recommendations
TX +/- and RX +/- are critical nets at 2.5GHz and must follow specific PCB layout rules: Ensure 100Ω differential impedance.
TX +/- and **RX +/-** are critical nets at 2.5GHz and must follow specific PCB layout rules: **1.** Limit to maximum of 2 vias per signal. **2.** Trace length on add-in board should be a maximum of 3.5 inches. **3.** Differential pair should be routed symmetrically, length matched within 20 mils. **4.** No stubs, test points (if used) should be in series. **5.** Traces should not cross split reference planes.
CLK +/- should be routed as symmetrical differential pairs with minimal trace length.

Table 2: Buck Regulator Output

Schematic Design Recommendations
LX pins (pins A13 and A14 on XR17V354 and XR17V358 and pins A9 and A10 on XR17V352), should be connected together and through 4.7uH inductor to FB pin.
FB pin should be additionally decoupled with 47µF ceramic capacitor.
PWRGD can be connected to an LED or test point for indicating that the 1.2V buck output voltage is stable. If PWRGD is used to monitor whether the BUCK is in or out of regulation, a glitch filter must be used to ensure that the PWRGD is low >100µs before the determining that the BUCK is out of regulation. This will ensure that noisy environments that can cause glitches on the PWRGD output at the switching frequency are not interpreted as a bad BUCK output.

Table 3: XR17V354 / XR17V358 PCIe UART Expansion Interface Signals

Schematic Design and Layout Recommendations			
Pins	Master Only (No Slave)	Slave Present	
		Master	Slave
CLK, D[7:0], SEL, INT	Leave open / unconnected	Must be routed between master and slave with <25pF of trace capacitance[1]	
MODE	Pull high	Pull high	Tie to ground
PRES	Leave unconnected or tie to ground	Pull high	Leave unconnected or tie to ground

1. Estimated trace capacitance using FR4 dielectric is 3.3pF / inch.

Table 4: Other PCIe UART "Special Handling" Device Pins

Schematic Design Recommendations
Device Reset
Internally logically “AND”ed together.
Connect **PERST#** to PCIe edge connector reset input.
Connect **RESET#** to PERST# or connect to pull-up.
CLKREQ#
CLKREQ# support is optional in PCIe specification and is not supported in the XR17V35x device. Leave this pin unconnected.
MPIO Pins
If unused, it is recommended that **MPIO** pins are pulled to defined logic states, either high or low.
JTAG Signals
TRST#, TCK, TMS, TDI and **TDO** may be left unconnected if unused.
EEPROM Signals
If unused, **EECK, EECS, EEDI** and **EEDO** may be left unconnected.
EECS must be pulled high with 4.7kΩ resistor if an external EEPROM is connected for its contents to be read by the XR17V35x device.
Other
ENIR# should be pulled high unless IR mode is used.
EN485# should be pulled high unless automatic RS-485 mode is used on all UART ports.
TMRCK should be pulled high unless an external timer / counter clock input is required.
Connect **REXT** to ground through 191Ω 1% resistor via a short trace.
Unused UART Inputs
RI#, CD#, CTS# and **DSR#** are all inputs. If unused, they are recommended to be pulled to defined logic state, either high or low.
Layout Recommendations
CLK, D[7:0], SEL, INT must be routed between master and slave with < 25pF of trace capacitance[1].

Table 5: Analog Voltage Inputs

Schematic Design Recommendations
Isolate **VCC33A** from digital **VCC33** with ferrite bead to this pin.
Isolate **VCC12A** from digital 1.2V source (either XR17V35x buck output or external 1.2V source) with ferrite bead to this pin.
Isolate **VCC12** from digital 1.2V source (either XR17V35x buck output or external 1.2V source) with ferrite bead to this pin. If using external 1.2V source, add 250Ω pull-down resistor to this pin per ECN.

Table 6: Test Inputs

Schematic Design Recommendations
On XR17V354 and XR17V358: **TEST0, TEST1** and **TEST2** should be tied to ground for device normal operation.
On XR17V352: **TEST0, TEST1, TEST2, TEST3** and **TEST5** should be tied to ground for normal device operation. TEST4# should be pulled high for normal device operation.

Table 7: Voltage Rails

Schematic Design Recommendations
All decoupling capacitors should be implemented without traces to power or ground reference planes if possible.
Bulk Decoupling
For all designs, a minimum of 10µF of bulk decoupling is recommended for add-in PCIe designs. Additional bulk capacitance should be added as deemed appropriate. In general bulk capacitance should be located near DC voltage rail entry to the PCB, and (if multiple capacitors are used), can then also be distributed on the PCB.
High Frequency Decoupling
For all designs a 100nF high frequency decoupling capacitor is recommend on each power pin located as close as possible to the device power pin.

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