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MAXLINEAR

XR2280x
USB Ethernet Bridges
Design Guide

Revision History

Document No.	Release Date	Change Description
201DGR00	4/20/20	Initial release.

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Introduction

The XR2280x Design Guide a helpful checklist of schematic design and PCB layout tips to aid in applying a XR2280x USB Ethernet Bridge to your PCB design. The XR2280x Family provides a high-speed USB 2.0 compound device with an embedded hub and 3, 4, 5 or 7 downstream functions: 100 / 100 Ethernet MAC and PHY; 0, 1, 2 or 4 UARTs; multi-master capable I2C Controller and an Enhanced Dedicated GPIO Entity (EDGE) controller. On-chip One-Time Programmable (OTP) memory is also included.

Please refer to the respective XR2280x Data Sheet for more information, including application block diagram and pin-out diagram.

Reference Documentation

XR22800 Data Sheet

XR22801 Data Sheet

XR22802 Data Sheet

XR22804 Data Sheet

Visit www.maxlinear.com to obtain copies of these documents.

Pin Groups

The tables below are arranged by the following pin groups:

- USB
- Ethernet
- USB Ethernet Bridge "Special Handling" Device Pins
- Voltage Rails
- General PCB Layout

Design and Layout Recommendations

Table 1: USB

Schematic Design Recommendations
Ensure there are no external components on **USBD+ / USBD-** unless tested in compliance with the USB 2.0 spec. For example, no series resistance, inductance or capacitance. No shunt capacitance. Exceptions are ESD protection diodes, EMI filters that have demonstrated compliance with USB 2.0 high speed signaling.
Layout Recommendations
USBD+ / USBD- are high speed USB signaling at 480MHz. Ensure 90Ω differential impedance.
USBD+ / USBD- should not be routed over a split reference plane.
USBD+ / USBD- should be length matched, ideally to within ± 20 mils.
USBD+ / USBD- should have no greater than 2 vias.
USBD+ / USBD- should have no stubs on these traces greater than 200 mils, for example to test points.

Table 2: Ethernet

Schematic Design Recommendations
Ensure 100Ω differential impedance.
Ethernet **RX** and **TX** differential pairs should be AC coupled with 100nF in “back to back” XR2280x configurations, i.e. in configurations where 2 XR2280x Ethernet devices are connected RX to TX and TX to RX on the same PCB.
Ethernet **RX** and **TX** differential pairs should be transformer coupled in all other configurations. Transformer coupling provides the essential elements for robust Ethernet transmission by: **1.** Isolation: Isolating the Ethernet device from noise, voltage / current on the twisted pair wiring connections of Ethernet link partners. **2.** Common mode rejection: Transformer converts a single ended transmitter and receiver signals to differential for transmission on the twisted pair wiring providing common mode rejection. **3.** Setting the common mode voltage for the receiving device.
Layout Recommendations
Ethernet **RX** and **TX** differential pairs should be length matched, ideally to within ±20 mils.
Ethernet **RX** and **TX** differential pairs should have no stubs on these traces, for example to test points greater than 200 mils.

Table 3: USB Ethernet Bridges "Special Handling" Device Pins

Schematic Design Recommendations
Connect **VBUS_SENSE** using pin description in the datasheet, with voltage divider from USB host VBUS power input. Required for proper operation in self-powered USB designs.
Decouple **3V3_OUT** with a minimum of 4.7uF and connect to CAP1 and CAP2 pins.
For USB suspend mode power compliance, use **LOW_PWR#** output to power down other devices powered by USB VBUS.
Layout Recommendations
Connect **XTAL** pins with short traces isolated from other high frequency nets.
Connect **REXT** with short trace.
Connect **CNTR_PAD** with multiple thermal vias to power plane for electrical and thermal performance. For sensitive thermal applications refer to MaxLinear XR2280x ESD and thermal recommendations FAQ.

Table 4: Voltage Rails

Schematic Design Recommendations
An in-rush current limiting circuit is recommended (refer to XR2280x Evaluation board schematics) to meet USB compliance.
All decoupling capacitors should be implemented without traces to power or ground rails if possible.
Bulk decoupling
USB requires between 1 and 10uF of bulk capacitance on the VBUS power rail from the USB host. We recommend 4.7uF. In general if no in-rush current limiting circuit is used, a tantalum capacitor is recommend except for embedded applications or applications where no external USB cable will be used. For all other voltage rails (including any external V_{CC} supply voltages to the XR224xx device in self-powered mode) a minimum of 10uF of bulk decoupling should be used.
High frequency decoupling
For all designs, a 100nF high frequency decoupling capacitor is recommended on each power pin, located as close as possible to the device power pin.

Table 5: General PCB Layout

Layout Recommendations
A minimum of 4 layer PCB is critical with 5V power and ground reference planes (2 and 3) and microstrip signal layers (layers 1 and 4).

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
760.692.0711 p.
760.444.8598 f.

www.maxlinear.com