88LX2741

Data Sheet
Wave-2 G.hn AFE

General Description

This data sheet describes MaxLinear's 88LX2741 Wave-2 G.hn AFE.

The 88LX2741 is a programmable, high-performance Wave-2 G.hn AFE with industrial temperature range. The device features a dual transmission channel (one for powerline and another for coaxial or phone line) and two reception channels to enable SISO operation using one device and MIMO using two devices (for powerline and phone line).

Applications

- Multi-medium-to-Ethernet adapter.
- Embedded Smart Grid module.
- Multi-medium-embedded G.hn modem.
- G.hn access multiplexer for outdoor use.

Features

- Designed for powerline, baseband coaxial and phone line wiring.
- Programmable transmission and reception gains.
- Integrated filters.
- Integrated line drivers.
- Power down and standby mode.
- Very low noise and distortion over the entire transmission and reception paths.
- 28 pin QFN 4×4mm package.
- Support for multiple AFEs operating in parallel with only one digital baseband (DBB) processor 88LX5153A.

Supported Standards

- Code of Conduct on Energy Consumption of Broadband Equipment Version 5.0, European Commission.
- ITU-T G.9960: Unified high-speed wireline-based home networking transceivers – System architecture and physical layer specification *(*referenced as ITU-T G.9960*).*
- ITU-T G.9961: Unified high-speed wire-line based home networking transceivers – Data link layer specification *(*referenced as ITU-T G.9961*).*
- ITU-G.9962: Unified high-speed wire-line based home networking transceivers – Management specification *(*referenced as ITU-T G.9962*).*
- ITU-T G.9963: Unified high-speed wireline-based home networking transceivers – Multiple input/multiple output specification *(*referenced as ITU-T G.9963*).*
- ITU-T G.9964: Unified high-speed wire-line based home networking transceivers - Power spectral density specification *(*referenced as ITU-T G.9964).

Revision History

Document No.	Release Date	Change Description
073-2741DSR02	July 14, 2020	**Updated:** ■ Confidentiality protection removed.
073-2741DSR01	April 7, 2020	**Updated:** ■ "Required Operating Conditions" table. ■ "Biasing" table. ■ New template applied. ■ General document review.
073-2741DSR00	September 19, 2018	Initial release.

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Introduction

The 88LX2741 is a programmable, high-performance Wave-2 G.hn AFE with industrial temperature range. The device features a dual transmission channel (one for powerline and another for coaxial or phone line) and two reception channels to enable SISO operation using one device and MIMO using two devices (for powerline and phone line). In addition to the transmission and reception paths, the 88LX2741 contains a biasing circuit and a register block controlled from the digital interface.

Transmission path comprises a programmable transimpedance amplifier, a filter, and two line drivers to condition and amplify the OFDM signal from the DAC up to a level suitable for the wireline. Each reception path comprises an attenuator, a LNA, a filter, and a PGA to accommodate the signal from the wireline to a level suitable for the ADC range.

The operating mode of the 88LX2741 is highly configurable to balance performance and power consumption based on the requirements of bandwidth, power density, and physical medium.

The biasing block uses a bandgap reference generator adjusted with an external resistor to generate the biasing current and voltage for all the blocks of the circuit.

The digital interface is used to configure the register set from the baseband transceiver.

The 88LX2741 is supplied from 5V and 3.3V.

IC Block Diagram

The following figure shows the functional block diagram of the 88LX2741.

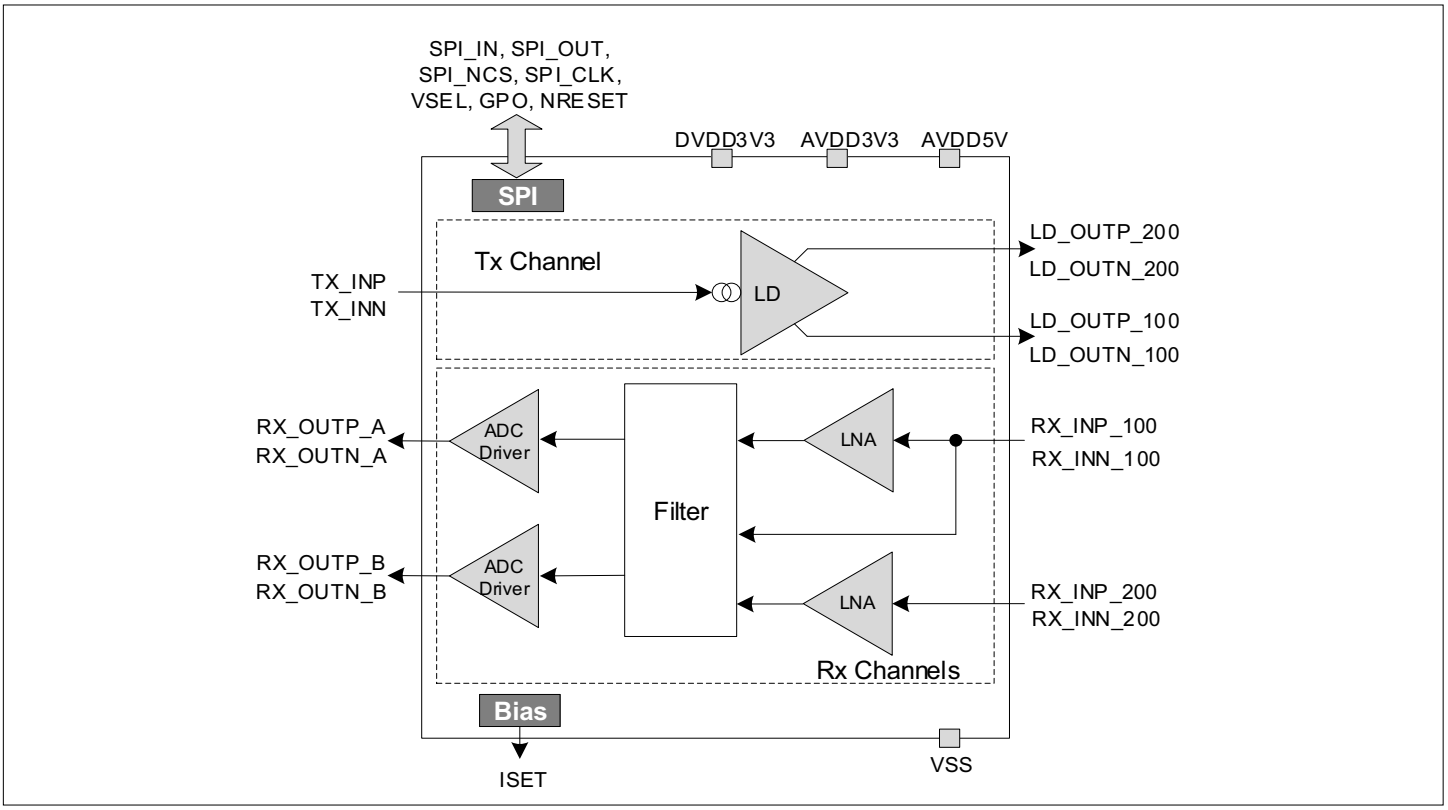

Figure 1: 88LX2741 Block Diagram

Typical Application

The Wave-2 G.hn chipset (88LX5153A and 88LX2741) enables the possibility to support both powerline and coaxial/phone line interfaces in a single device implementation. It can be used in stand-alone or embedded applications. The typical applications are listed in the following subsections

Multi-Medium-to-Ethernet Adapter

The multi-medium-to-Ethernet adapter is a stand-alone design containing the Wave-2 G.hn chipset, the power supply, and the Ethernet interface in a single wall-plug box.

Depending on which path is active, it can support SISO/MIMO powerline, SISO/MIMO phone line, or SISO coaxial connectivity.

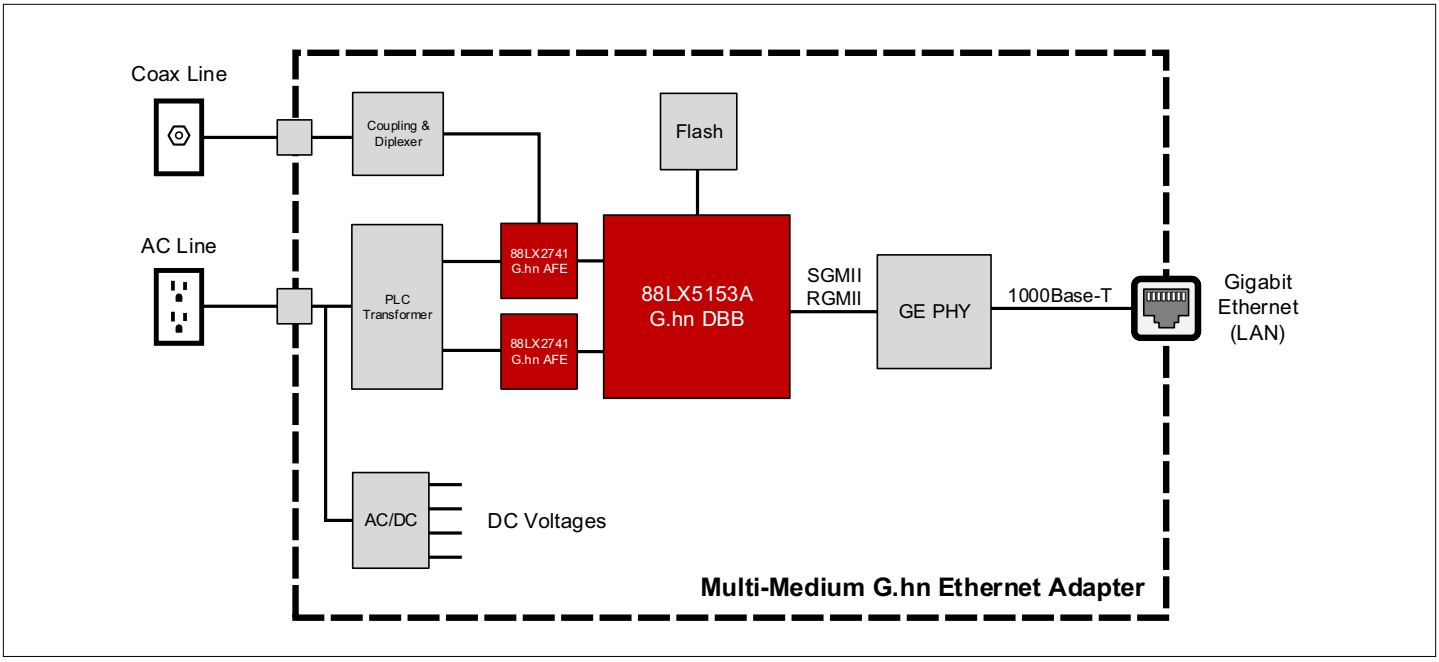

Figure 2: Multi-Medium G.hn Gigabit Ethenet Adapter Block Diagram

Embedded Smart Grid Module

This module is intended to be embedded in electricity meters, demand management equipment, and lighting control devices. The module includes the minimal chipset to use power line communication in Smart Grids. The single-phase module uses one 88LX5153A and one 88LX2741 to implement SISO communication. The three-phase module uses one 88LX5153A and two 88LX2741 to implement MISO and SIMO communication to and from the end nodes.
The module communicates to the host CPU or metering device using MII, RGMII, or UART.

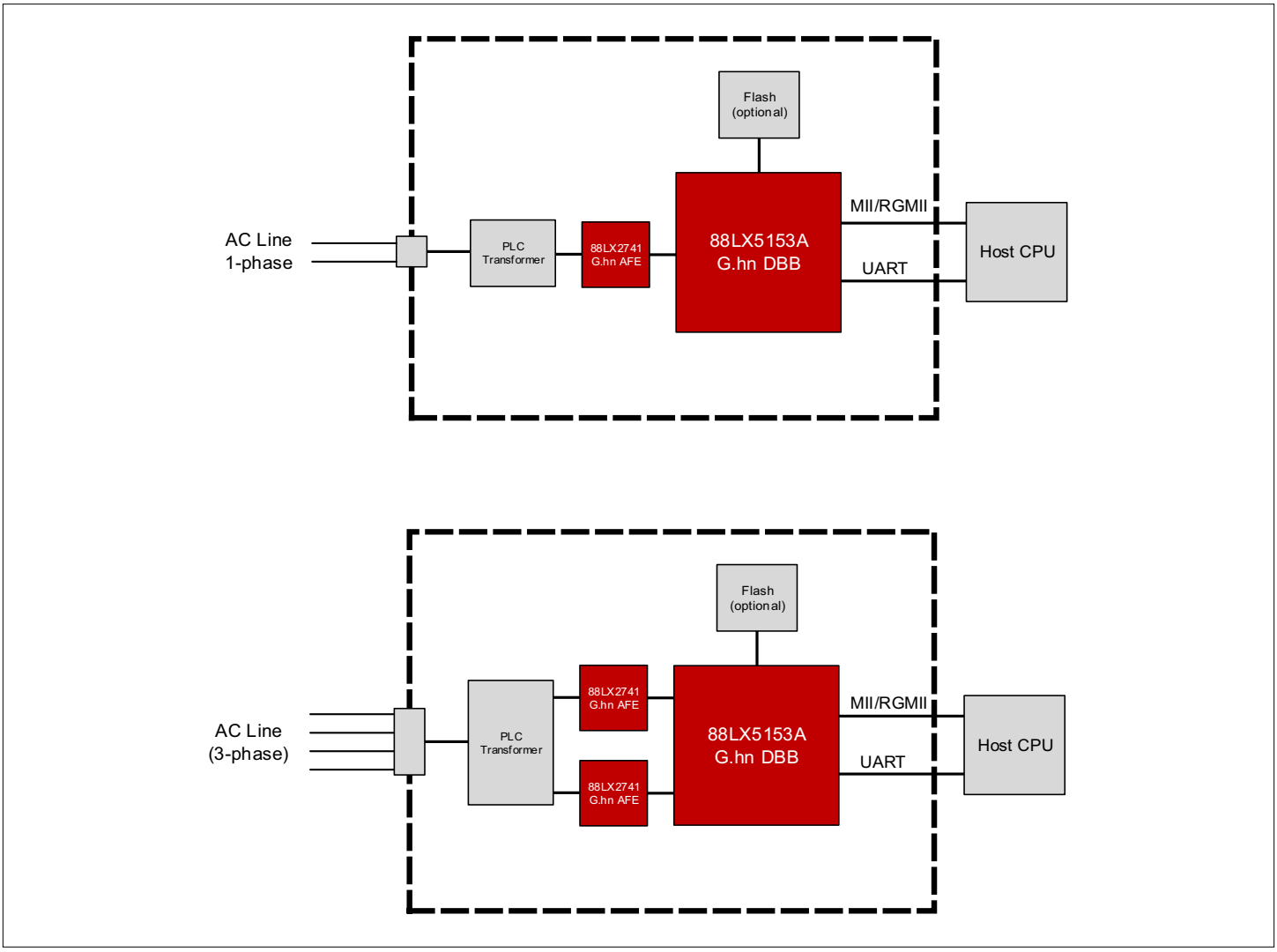

Figure 3: Embedded Smart Grid Module

Industrial G.hn Aggregation Multiplexer

The GAM application is a multi-port platform that includes one G.hn chipset per channel, high-end switching, and a CPU to support MDU access scenarios over existing phone lines.
Each port uses one 88LX2741 for a SISO implementation or two 88LX2741 for a MIMO implementation.

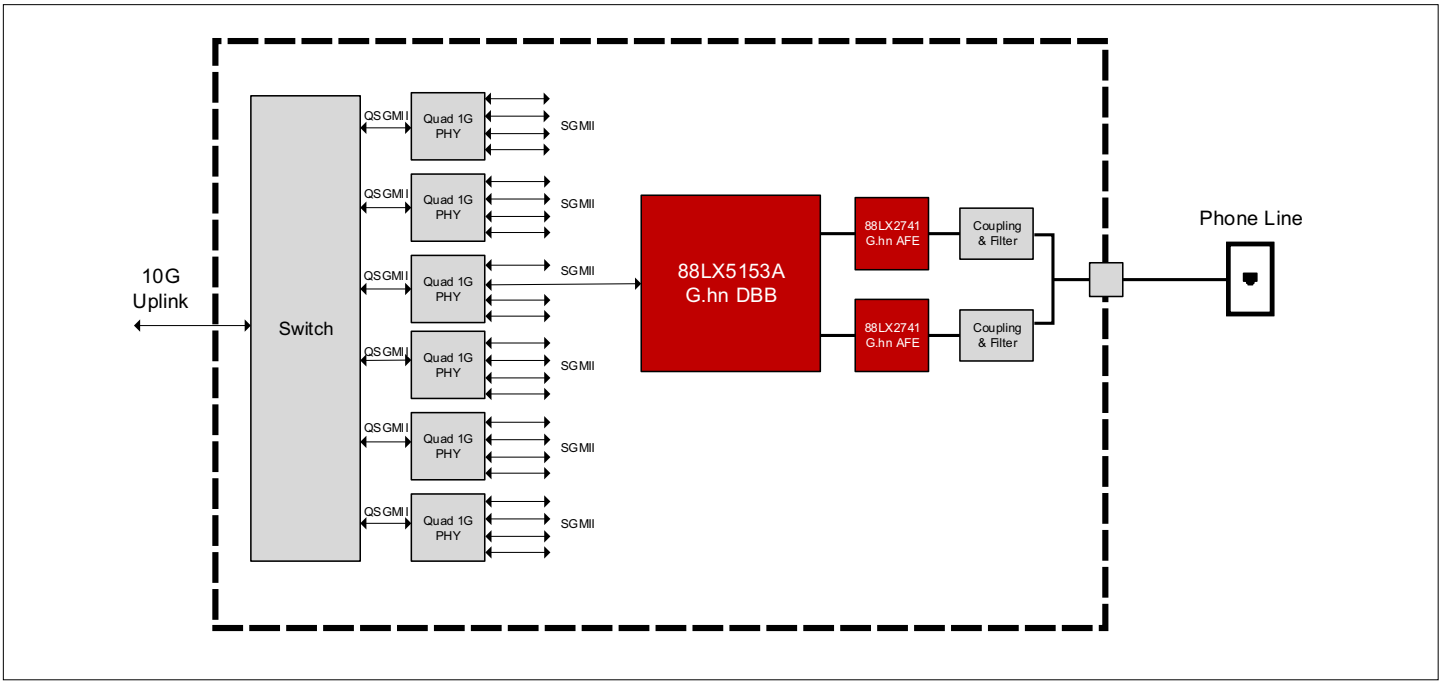

Figure 4: Industrial G.hn Aggregation Multiplexer

Multi-Medium Embedded G.hn Modem

The G.hn chipset can be embedded in other designs to provide a powerful networking capability on wired media other than Ethernet.

The following figure shows the block diagram of an embedded multi-medium G.hn modem. As for Ethernet adapters and WiFi extenders all media modes are supported.

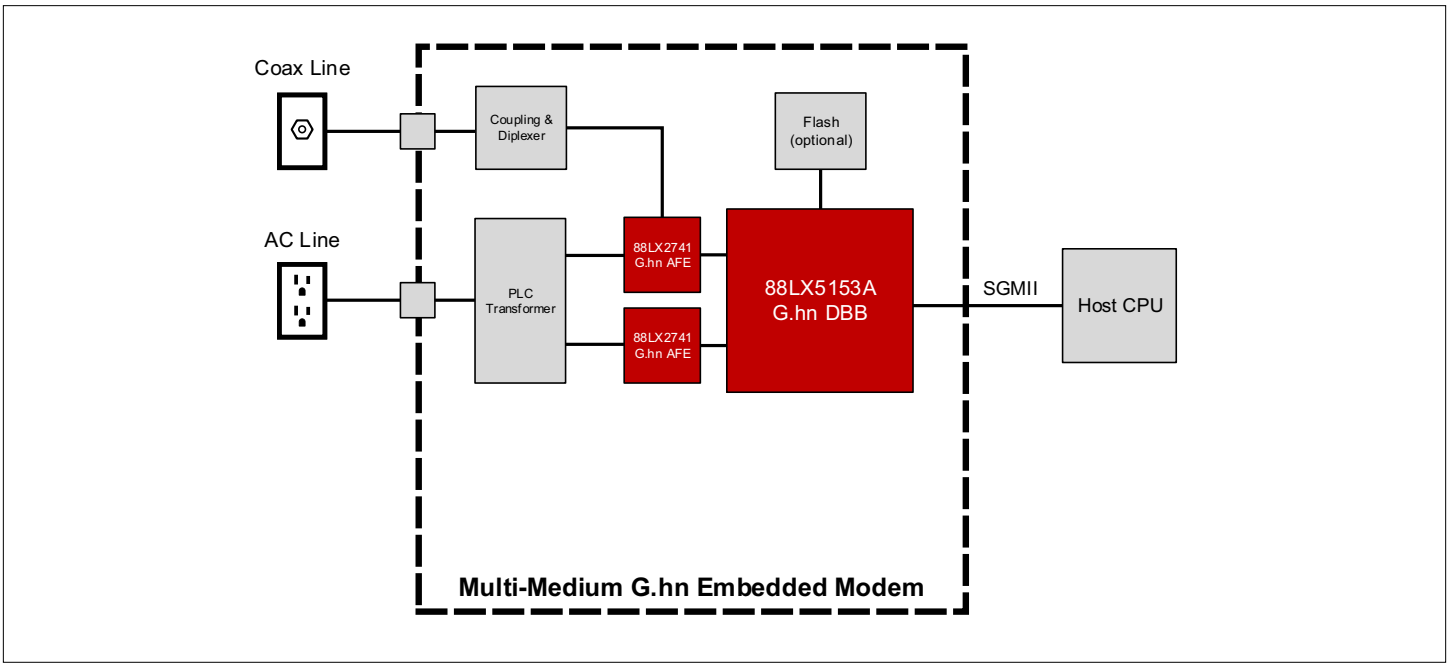

Figure 5: Multi Medium Embedded Block Diagram

Pin Information

Pin Configuration

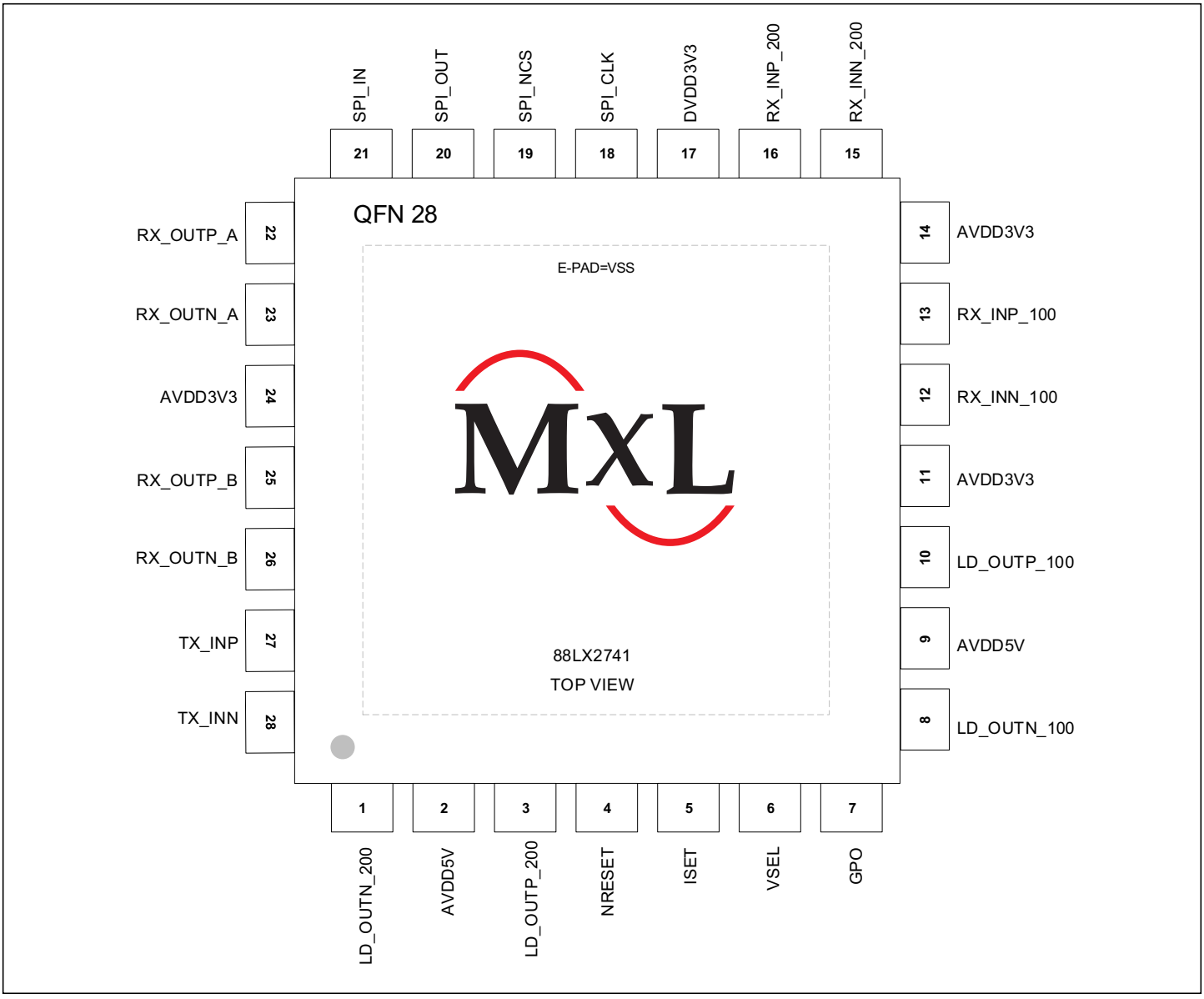

Figure 6: 88LX2741 Package Pinout

Pin Description

The following table lists pins and signal names. Power pins are also listed in this table.

Table 1: 88LX2741 Pin Description

Pin #	Pin Name	Type	Description
11, 14, 24	AVDD3V3	PWR	Analog 3.3V supply.
2, 9	AVDD5V	PWR	Analog 5V supply.
17	DVDD3V3	PWR	Digital 3.3V supply.
7	GPO	DO	General Purpose Output.
5	ISET	AO	Biasing resistor (6kΩ 1% accuracy connected to ground).
8	LD_OUTN_100	AO	Tx 100 negative output.
1	LD_OUTN_200	AO	Tx 200 negative output.
10	LD_OUTP_100	AO	Tx 100 positive output.
3	LD_OUTP_200	AO	Tx 200 positive output.
4	NRESET	DI	SPI Reset (active low).
12	RX_INN_100	AI	Rx 100 negative input.
15	RX_INN_200	AI	Rx 200 negative input.
13	RX_INP_100	AI	Rx 100 positive input.
16	RX_INP_200	AI	Rx 200 positive input.
23	RX_OUTN_A	AO	Rx A negative output.
26	RX_OUTN_B	AO	Rx B negative output.
22	RX_OUTP_A	AO	Rx A positive output.
25	RX_OUTP_B	AO	Rx B positive output.
18	SPI_CLK	DI	SPI Clock.
21	SPI_IN	DI	SPI Data input.
19	SPI_NCS	DI	SPI Chip Select (active low).
20	SPI_OUT	DI/DO	SPI Data output.
28	TX_INN	AI	Tx negative input.
27	TX_INP	AI	Tx positive input.
6	VSEL	AI	IC selector in multi AFE use cases.
Exposed Pad	VSS	GND	Ground.

Signal Description

Table 2: Signal Types

Pin Name	Description
AI	Analog Input.
AO	Analog Output.
DI	Digital Input.
DO	Digital Output.
DI/DO	Digital input/Digital Output.
GND	Ground.
PWR	Power Supply.

Electrical Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard.

Table 3: Absolute Maximum Ratings

Parameter	Maximum	Units
AVDD5V to VSS	From –0.3 to 6.0	V
AVDD3V3, DVDD3V3 to VSS	From –0.3 to 4.0	V
LD_OUTP_200, LD_OUTN_200, LD_OUTN_100, LD_OUTP_100, RX_INN_100, RX_INP_100, RX_INN_200, RX_INP_200, VSEL to VSS	From –0.3 to AVDD5V + 0.3	V
NRESET, ISET, GPO, SPI_CLK, SPI_NCS, SPI_OUT, SPI_IN, RX_OUTP_A, RX_OUTN_A, RX_OUTP_B, RX_OUTN_B to VSS	From –0.3 to AVDD3V3 + 0.3	V
TX_INP, TX_INN to VSS	From –0.3 to 1.95	V
ESD susceptibility at all pins, HBM	2	kV
Maximum Junction Temperature	150	°C
Storage Temperature Range	From –65 to 150	°C

Required Operating Conditions

Table 4: Required Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
V_{AVDD5V}	Analog Supply Voltage AVDD5V	4.75	5	5.5	V
$V_{AVDD3V3}$	Analog Supply Voltage AVDD3V3	3.135	3.3	3.465	V
$V_{DVDD3V3}$	Digital Supply Voltage DVDD3V3	3.135	3.3	3.465	V
T_A	Ambient Operating Temperature (Industrial Grade)	–40	-	85	°C
T_{JMAX}	Maximum Operational Junction Temperature	-	-	125	°C

Electrical Characteristics

Note: Power consumption figures depend on the configuration programmed in the firmware. The values listed in this section correspond to the optimal AFE configuration at the time of qualifying the silicon.

The following figures, unless otherwise stated, are measured at T_A = –40..85°C, AVDD3V3 = 3.3V±5%, DVDD3V3 = 3.3V±5%, AVDD5V = 4.75..5.5V. Typical values are at T_A = 25°C, AVDD3V3 = 3.3V, DVDD3V3 = 3.3V, AVDD5V = 5V, unless otherwise noted. Biasing setup configured as nominal value.

Specifications over the operating temperature range are assured by design, characterization and correlation with statistical process controls.

Table 5: Power Node Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
General, all the IC						
I_{AVDD5V}	Total Quiescent Current at AVDD5V	V(NRESET)=0	-	0.7	-	mA
		V(NRESET)=AVDD3V3	-	3.8	-	
$I_{AVDD3V3}$	Total Quiescent Current at AVDD3V3	V(NRESET)=0	-	0.3	-	mA
		V(NRESET)=AVDD3V3	-	0.7	-	
$I_{DVDD3V3}$	Total Quiescent Current at DVDD3V3	V(NRESET)=0	-	0.1		mA
		V(NRESET)=AVDD3V3	-	0.2	-	

Table 6: Transmission Mode

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
I_{AVDD5V}	Total Current at AVDD5V	Powerline mode. Output signal: 16.5dBm over 100Ω load through 1:3 transformer.	-	130	-	mA
		Coaxial/phone line mode. Output signal: 8dBm over 100Ω load through 1:2 transformer.	-	121	-	
$I_{AVDD3V3}$	Total Current at AVDD3V3	Powerline mode. Output signal: 16.5dBm over 100Ω load through 1:3 transformer.	-	50	-	mA
		Coaxial/phone line mode. Output signal: 8dBm over 100Ω load through 1:2 transformer.	-	35	-	
R_F	Programmable Differential Transimpedance	Powerline mode	-	1783 1416 1125 893 710 563	-	Ω
		Coaxial/phone line mode	-	1125 893 710 563 448	-	
ΔR_F	Gain Step	R_F = 448–1783	-	2	-	dB

Table 6: Transmission Mode (Continued)

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
f_c	–3dB Bandwidth	Powerline mode R_F = 563–1783 Small Signal Bandwidth Load = Powerline	100	-	-	MHz
		Coaxial/phone line mode R_F = 448 –1125 Small Signal Bandwidth Load = 75/100Ω	200	-	-	
I_{INdiff}	Recommended Differential Input Current Range	-	-	5	-	mApp

Table 7: Receptions Mode

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
I_{AVDD5V}	Total Current at AVDD5V	Powerline mode	-	5	-	mA
		Coaxial/phone line mode	4	-	8	
$I_{AVDD3V3}$	Total Current at AVDD3V3	Powerline mode	-	227	-	mA
		Coaxial/phone line mode	-	210	-	
ΔG	Gain Step	Powerline mode G= From –26dB to + 30dB	-	2		dB
		Coaxial/phone line mode G= From –20dB to + 36dB	-	2	-	
f_c	–3dB Bandwidth	Powerline mode G= From –26dB to + 30dB Small Signal Bandwidth Load=ADC	100	-	-	MHz
		Coaxial/phone line mode G= From –20dB to +36dB Small Signal Bandwidth Load=ADC	200	-	-	
V_{INdiff}	Recommended Differential Input Current Range	-	0	-	2× AVDD5V	Vpp
$V_{OUTdiff}$	Recommended Differential Output Voltage Range	-	-	1.5	-	Vpp
R_{indiff}	Differential Input Resistance	Powerline mode G= From –26dB to +30dB	-	1200	-	Ω
		Coaxial/phone line mode G= From –20dB to +36dB	-	100 75	-	

Table 8: Biasing

Symbol	Symbol	Conditions	Minimum	Typical	Maximum	Units
V_{ISET}	Voltage at ISET	External 6kΩ (1% accuracy) resistor connected to VSS	-	1.2	-	V
$Von_{AVDD3V3}$	Turn-On Threshold at AVDD3V3	Increasing AVDD3V3	-	-	2.85	V
$Voff_{AVDD3V3}$	Turn-Off Threshold at AVDD3V3	Decreasing AVDD3V3	2.5	-	-	V
$Vhys_{AVDD3V3}$	Hysteresis at AVDD3V3	-	-	130	-	mV
Von_{AVDD5V}	Turn-On Threshold at AVDD5V	Increasing AVDD5V	-		4.45	V
$Voff_{AVDD5V}$	Turn-Off Threshold at AVDD5V	Decreasing AVDD5V	3.9	-	-	V
$Vhys_{AVDD5V}$	Hysteresis at AVDD5V	-	-	350	-	mV
V_{INVSEL}	Recommended Input Voltage Range at VSEL pin. (See "Strapping Values" on page 15)	2b'11	-	AVDD5V	-	V
		2b'10	-	AVDD3V3	-	
		2b'01	-	1.5	-	
		2b'00	-	0	-	

Table 9: Digital Inputs and Outputs

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High Threshold at SPI_CLK, SPI_IN, SPI_NCS, NRESET	-	0.7×DVDD3V3	-	-	V
V_{IL}	Low Threshold at SPI_CLK, SPI_IN, SPI_NCS, NRESET	-	-	-	0.3× DVDD3V3	V
R_{PU}	Pull-Up Resistor at NRESET, SPI_NCS	-	-	70	-	KΩ
V_{OH}	Output High Level at SPI_OUT, GPO	I()=4mA	DVDD3V3-0.4	-	-	V
V_{OL}	Output Low Level at SPI_OUT, GPO	I()=4mA	-	-	0.4	V
$I_{LEAKAGE}$	Input Leakage Current at SPI_CLK, SPI_IN, SPI_NCS, SPI_OUT, NRESET, GPO	0 < V < DVDD3V3	-	-	10	µA

Digital Interface

The 88LX2741 includes a 4-wire serial interface similar to SPI. The operation of this interface and the mapping of the registers is specifically designed to work with 88LX5153A, therefore the information provided in this section is only informative and not intended to explain the use of this device in stand-alone mode.

- Maximum clock frequency for write operations = 100MHz.
- Maximum clock frequency for read operations = 25MHz.
- Bit ordering within frames = MSB first.

The 88LX2741 supports two operating modes on the SPI interface:

- Single input mode = In this mode only the SPI_IN pin is used to send information to the AFE chip. The SPI_OUT pin remains in high impedance during write operations and outputs data during read operations. This mode is equivalent to the standard SPI mode 3 (CPOL=1, CPHA=1).

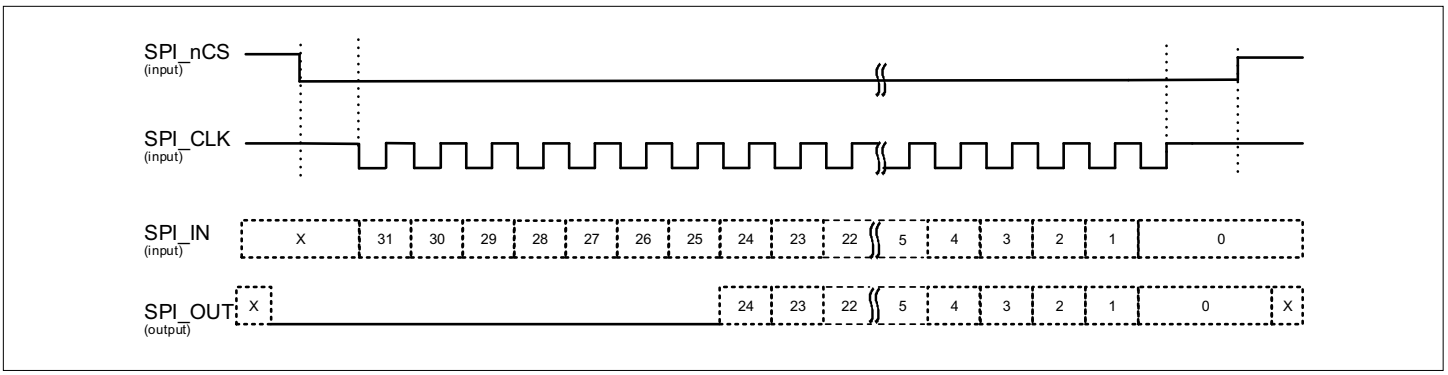

Figure 7: Single Input Mode

- Parallel input mode = In this mode the SPI_OUT pin becomes an input and works in parallel with SPI_IN, doubling the data rate and reducing the duration of the frame by half. The change to parallel input mode is configured in one of the registers during a previous single input transaction.

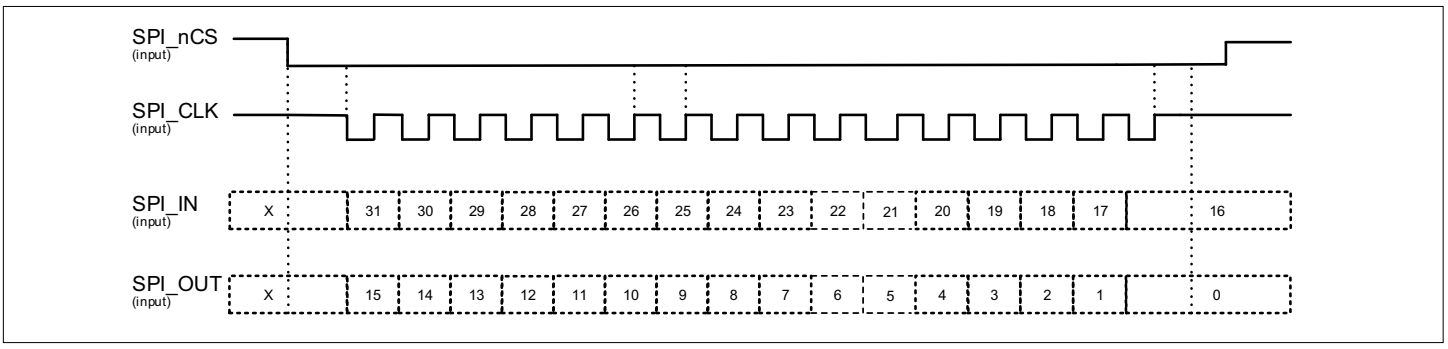

Figure 8: Parallel Input Mode

SPI_OUT remains in high impedance when SPI_NCS is not asserted. The biasing of the line is assured by the internal pull-up resistors of the AFE and the DBB devices.

When more than one AFE is used in a product, the SPI lines should be routed in a T shape with the branches reaching each device that has the same length.

Strapping Values

The 88LX2741 AFE may operate in multi-AFE systems comprising one 88LX5153A DBB processor and one or more AFE IC's all of them sharing a common SPI interface. To control each AFE IC separately a strapping value must be set externally to identify each AFE IC. This strapping value provides an internal identifier (2bits) for each AFE IC. This identifier must be used to compose the 6 bit address field of the SPI transaction.

Strapping is performed using VSEL pin which can be set to four different voltage values to define the device identifiers as listed in the following table.

Table 10: Strapping Values

VSEL pin (V)	VSEL field
0	2b'00
1.5	2b'01
3.3	2b'10
5	2b'11

Mechanical Drawings

28-Pin QFN Package

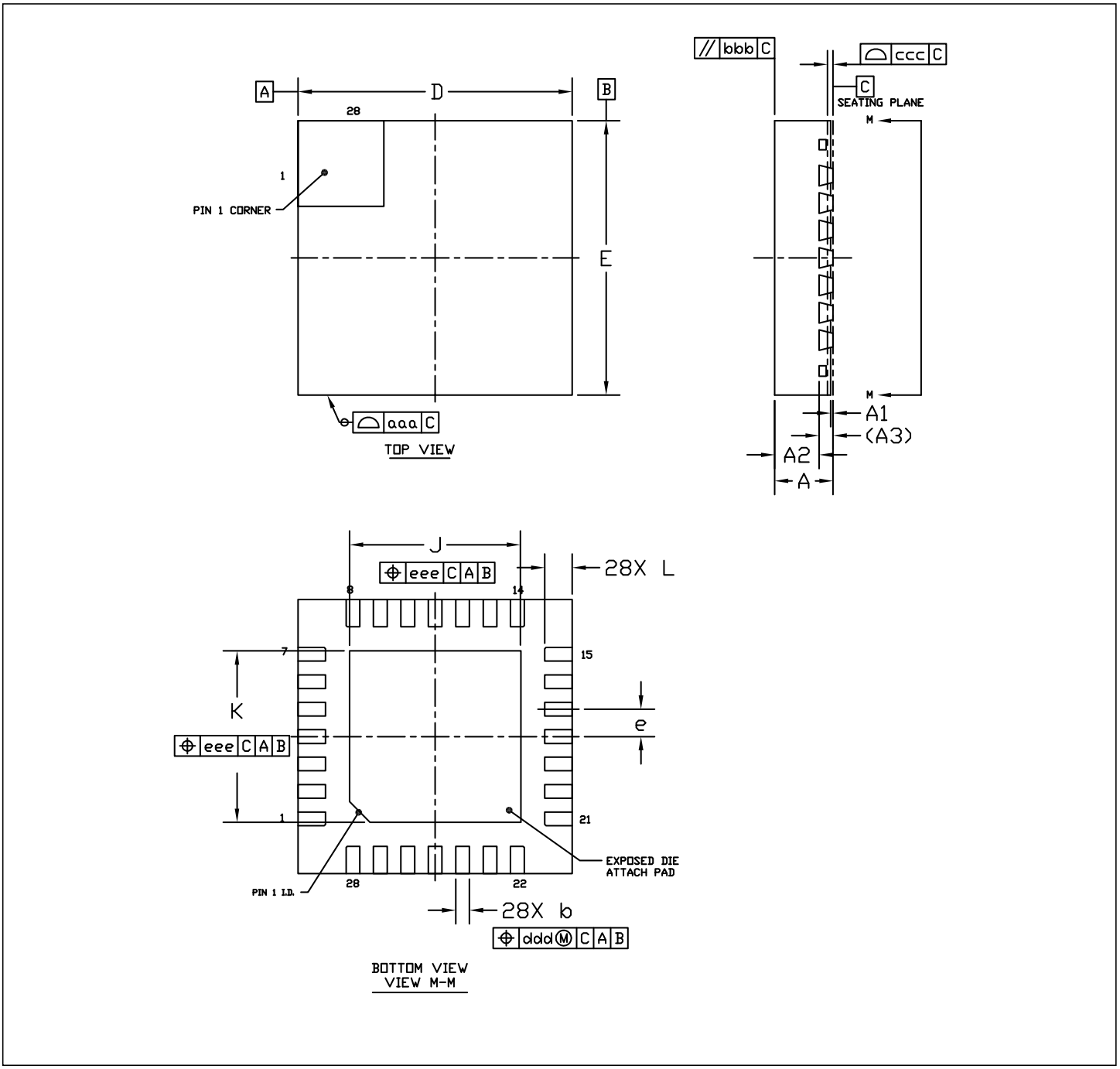

Figure 9: 28 QFN 4x4 Package Top and Lateral Views

Package Outline Parameters

Symbol	Parameter	Nominal	Maximum
A	0.80	0.85	0.90
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203 REF	-
b	0.15	0.20	0.25
D	-	4.0 BSC	-
E	-	4.0 BSC	-
e	-	0.40 BSC	-
J	2.4	2.5	2.6
K	2.4	2.5	2.6
L	0.35	0.40	0.45
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.08	-
ddd	-	0.10	-
eee	-	0.10	-

Note: All dimensions are in millimeters.

Table 11: Package Thermal Information

Symbol	Parameter	Minimum	Typical	Maximum	Unit
θ_{JC}	Thermal Resistance from Junction to the Top of the package	-	20.16	-	°C/W
θ_{JB}	Thermal Resistance from Junction to the Bottom of the package	-	19.45	-	°C/W

Ordering Information

Part Order Numbering

The following figure shows the part order numbering scheme for the 88LX2741. For more information, contact MaxLinear Customer Technical Support.

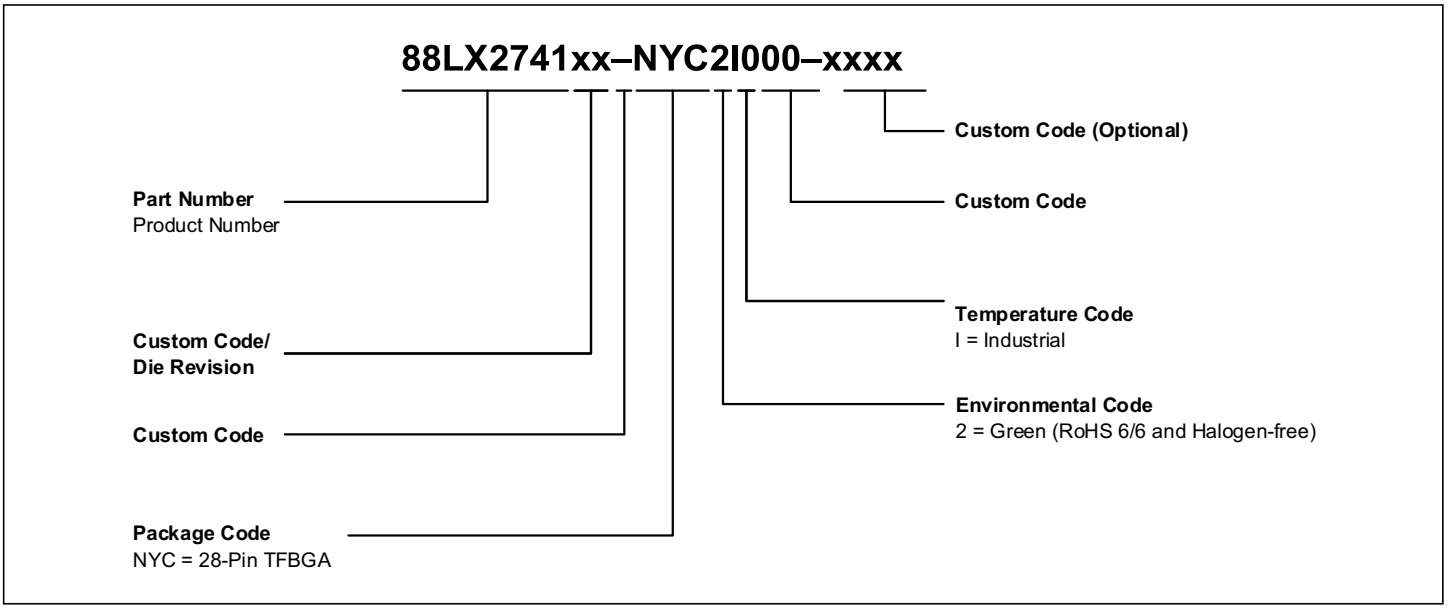

Figure 10: 88LX2741 Sample Part Number

Table 12: 88LX2741 Part Order Options

Package Type	Part Order Number	Description
28-Pin QFN	88LX2741A0-NYC2I000	G.hn Wave-2 Industrial AFE—single channel—coax/ialphone line/powerline

Package Marking

The following figure shows a sample package marking and pin 1 location for the 88LX2741.

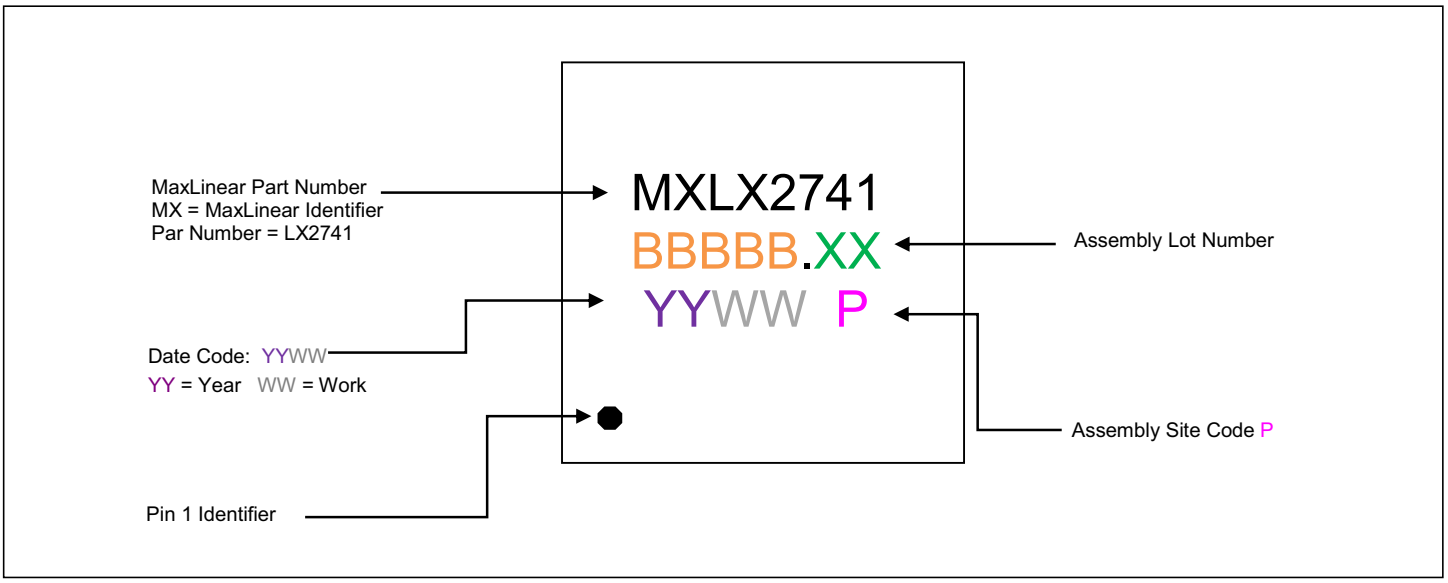

Figure 11: 88LX2741 Package Marking and Pin 1 Location

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