MxL93543

Product Brief
400G PAM4 DSP SoC

General Description

The MxL93543 is a highly integrated PAM4 DSP SoC that enables 400Gbps optical interconnects using 100Gbps over a single optical wavelength 100G/λ.

The device has a high-speed electrical interface with eight transmit (Tx) and receive (Rx) input/output (I/O) that connect electrically through a module connector to the host ASIC. The device also has a high-speed optical side interface that has four Tx and Rx that connect through the optical components to the optical fibers.

The electrical interface supports 56Gbps PAM4 signaling over an electrical channel with 13dB channel loss, including the host connector.

The optics interface supports 112Gbps PAM4 signaling to enable 500m DR4, 2km FR4 use cases.

The device supports DSP functions including Tx digital pre-distortion (DPD), transmit pre-emphasis (TX FIR), receive feed forward equalization (FFE) and decision feedback equalization (DFE) required for 56 Gbaud optics.

The MxL93543, in a 12mm × 12mm package, has a differential driver output for optic transmitter device. It offers exceptional signal integrity for 56 Gbaud signals in a compact footprint suitable for next generation optical module form-factors such as QSFP-DD and OSFP.

Applications

- QSFP-DD optical modules
- SFP optical modules

Features

- 400G capacity that enables 400G DR4 and FR4 requirements
- 400G to 100G break-out mode
- Tx equalization includes pre-emphasis, digital pre-distortion, and reflection cancellation
- Rx equalization includes CTLE, multi-tap FFE and DFE, and reflection cancellation
- Integrated crystal oscillator eliminates the need for a costly reference clock source
- Digital I/O compatibility with the host processor. This removes the need for level shifters and saves valuable module board space
- Small package size to enable the QSFP-DD space requirements
- BER monitoring
- SNR reporting for each receiver on both electrical and optical interfaces
- Diagnostic loop-backs and test pattern generation and checking
- SPI and I^2C slave interface to communicate to module MCU
- SPI master for flash memory interface
- SPI and I^2C master interface for TIA direct control (the I^2C master enables control of the MxL9154 TIA for optimal performance)
- Embedded CPU for real-time control
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected

Supported Standards

- OIF-CEI-56G-VSR
- IEEE Std P802.3bs

Block Diagram

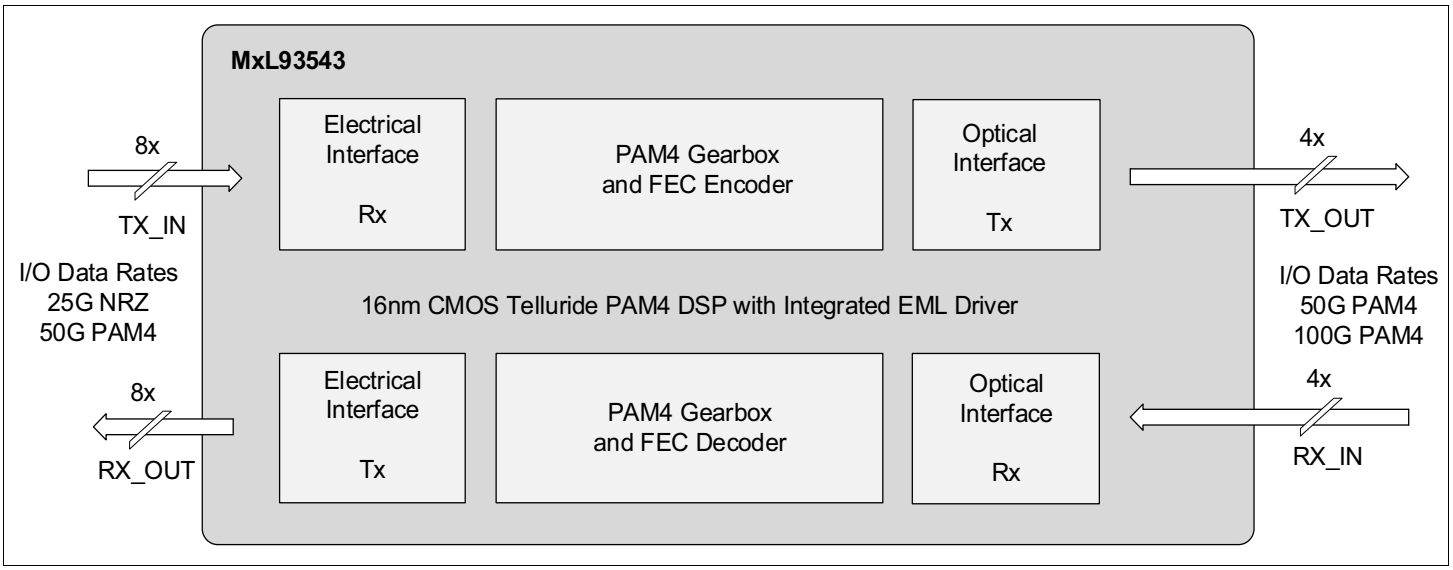

Figure 1: MxL93543 Functional Block Diagram

Ordering Information

Marketing Part Number	Ordering Part Number	Package	Shipping
MxL93543	MxL93543-AP-T	400G DSP without EA-EML driver, DC-coupled differential driver.	-

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