



General Description

The MxL9364x (MxL93642 and MxL93643) are highly integrated PAM4 DSP SoCs that enable 400Gbps optical interconnects using 100Gbps over a single optical wavelength ($100G/\lambda$).

The devices have a high-speed electrical interface with four transmit (Tx) and receive (Rx) input/output (I/O) that connect electrically through a module connector to the host ASIC.

The devices also have a high-speed optical side interface that has four Tx and Rx I/O that connect through the optical components to optical fibers.

The electrical interface supports 106.25Gbps PAM4 signaling per lane over C2M host channels.

The optical interface supports 106.25Gbps PAM4 signaling per wavelength for DR, FR, and LR applications.

The devices support DSP functions including line side Tx digital pre-distortion (DPD), transmit pre-emphasis (Tx FIR), and receive feed-forward equalization (Rx FFE).

The MxL9364x, in a 12mm × 13mm package, includes integrated TOSA drivers with differential and single-ended options for both silicon photonics (SiPh) and electro-absorption modulated laser (EML) implementations. It offers exceptional signal integrity for signals in a compact footprint suitable for next generation optical module form-factors.

Applications

- QSFP112 optical modules
- QSFP112 AEC/ACC and AOC

Features

- 400G retimer capability that enables 400G DR4, FR4, LR4, VR4/SR4
- 400G to 100G break-out mode
- Full 4 × 4 crossbar functionality
- Tx equalization that includes pre-emphasis, digital pre-distortion, and reflection cancellation
- Rx equalization that includes CTLE, multi-tap FFE, and reflection cancellation
- Supports host channels with Nyquist loss in excess of 20dB
- Integrated crystal oscillator that eliminates the need for a costly reference clock source
- Small package size to enable the QSFP112 space requirements
- Mission mode BER monitoring
- SNR/Histogram reporting for each receiver on both electrical and optical interfaces
- Diagnostic loop-back and test pattern generation and error checking
- SPI and I²C slave interface to communicate to module MCU
- SPI master for flash memory interface
- I²C master interface for TIA direct control
- Embedded CPU for real-time control
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected

Supported Standards

- IEEE Std 802.3bs
- IEEE Std 802.3cd
- IEEE Std 802.3ck
- IEEE Std 802.3cm
- IEEE Std 802.3cu
- IEEE Std 802.3db

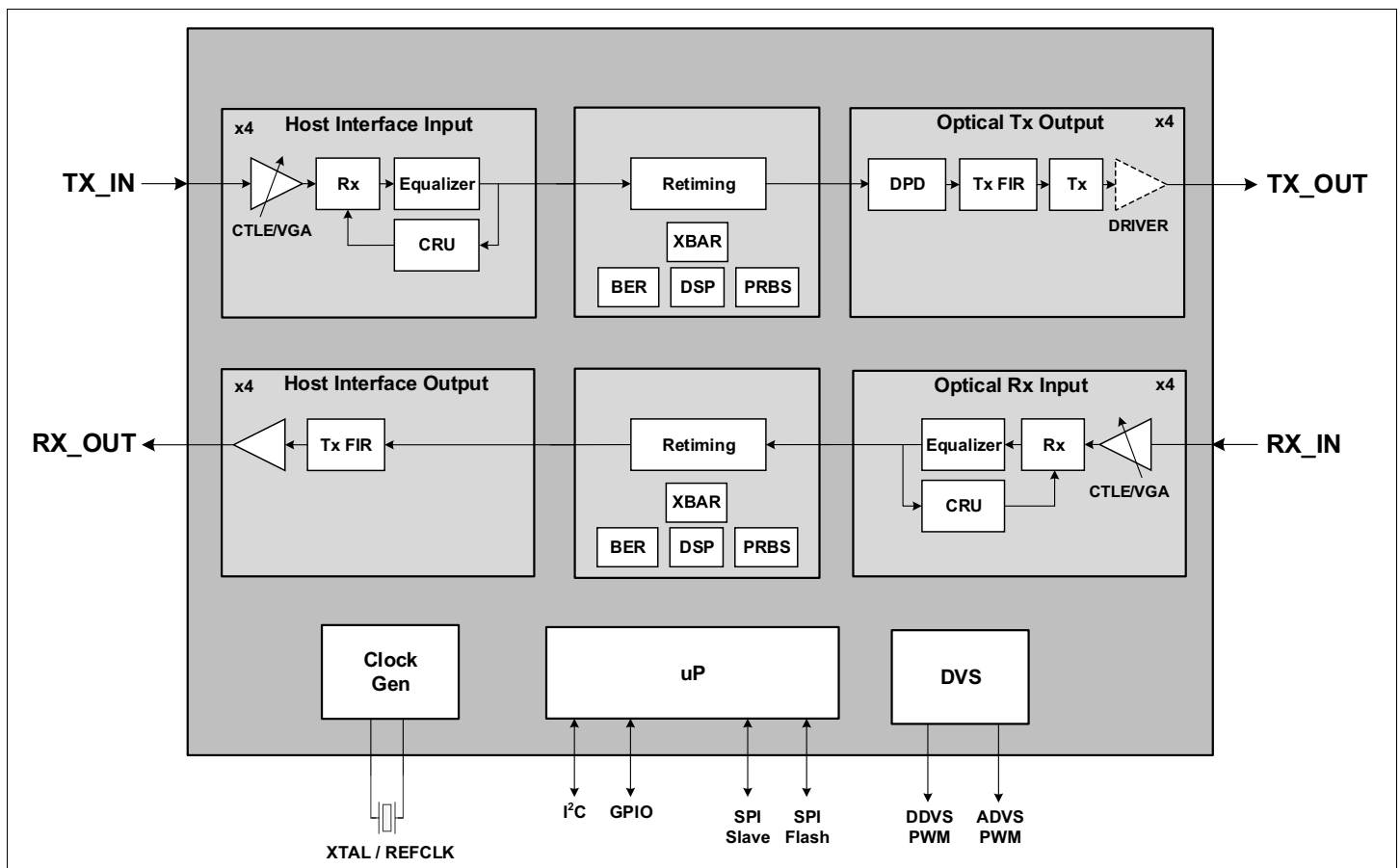
Introduction

The MxL9364x device is a highly integrated PAM4 DSP SoC that operates at a capacity of 400G and enables 100G for each optical wavelength. The SoC includes Tx DPD, Tx pre-emphasis (Tx FIR), Rx equalization (FFE) functionality, and a full 4 × 4 crossbar with broadcast capability. Additional mission mode BER monitoring capabilities are also available.

The main mode of operation is the retiming mode: the bit streams are forwarded between electrical and optical serializer/deserializer (SerDes) interfaces on a one-to-one basis. The bit streams are PAM-4 encoded.

IC Block Diagram

Figure 1 shows the functional block diagram of the MxL93642 device. The MxL93643 device is similar, however the output driver is not included in the optical Tx output block.



Ordering Information

Table 1: Ordering Information

Marketing Part Number	Ordering Part Number	Description	Package	Shipping
MxL93642	MXL93642-PV-T	400G retimer DSP with integrated driver	FC-FBGA	Tray
MxL93643	MXL93643-PV-T	400G retimer DSP without integrated driver	FC-FBGA	Tray



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