MxL93644A

400G PAM4 DSP SoC
Product Brief

General Description

The MxL93644A is a highly integrated PAM4 DSP SoC that enables 400Gbps optical interconnects using 100Gbps over a single optical wavelength (100G/λ).

The device has a high-speed electrical interface with eight transmit (Tx) and receive (Rx) input/output (I/O) that connect electrically through a module connector to the host ASIC.
The device also has a high-speed optical side interface that has four Tx and Rx I/O that connect through the optical components to optical fibers.

The electrical interface supports 53.125Gbps PAM4 signaling per lane over C2M host channels.

The optical interface supports 106.25Gbps PAM4 signaling per wavelength for SR applications.

The device supports DSP functions including line side Tx digital pre-distortion (DPD), transmit pre-emphasis (Tx FIR), and receive feed-forward equalization (Rx FFE).

The MxL93644A, in a 12mm × 13mm package, includes integrated drivers with DC bias and modulation for vertical-cavity surface-emitting laser (VCSEL) based implementations. It offers exceptional signal integrity for signals in a compact footprint suitable for next generation optical module form-factors.

Applications

- QSFP-DD optical modules
- OSFP optical modules
- QSFP-DD AEC/ACC and AOC
- OSFP AEC/ACC and AOC

Features

- 400G gearbox capability that enables 400G VR4/SR4
- 400G to 100G break-out mode
- Tx equalization that includes pre-emphasis, digital pre-distortion, and reflection cancellation
- Rx equalization that includes CTLE, multi-tap FFE, and reflection cancellation
- Supports host channels with Nyquist loss in excess of 20dB
- Integrated crystal oscillator that eliminates the need for a costly reference clock source
- Small package size to enable the QSFP-DD space requirements
- Mission mode BER monitoring
- SNR/Histogram reporting for each receiver on both electrical and optical interfaces
- Diagnostic loop-back and test pattern generation and error checking
- SPI and I^2C slave interface to communicate to module MCU
- SPI master for flash memory interface
- I^2C master interface for TIA direct control
- Embedded CPU for real-time control
- Squelch function when loss of signal (LOS) or loss of lock (LOL) is detected

Supported Standards

- IEEE Std 802.3ck
- IEEE Std 802.3cm
- IEEE Std 802.3db

Introduction

The MxL93644A device is a highly integrated PAM4 DSP SoC that operates at a capacity of 400G and enables 100G for each optical wavelength. The SoC includes Tx DPD, Tx pre-emphasis (Tx FIR), and Rx equalization (FFE) functionality. Additional mission mode BER monitoring capabilities are also available.

The main mode of operation is the gearbox mode: the bit streams from a pair of electrical SerDes interfaces are multiplexed into a single stream at the bit level and transmitted to one optical SerDes interface. The bit stream from one optical SerDes interface is de-multiplexed into two separate streams at the bit level and transmitted to a pair of electrical SerDes interfaces. The bit streams from the electrical and optical SerDes interface are PAM-4 encoded.

IC Block Diagram

Figure 1 shows the functional block diagram of the MxL93644A device. The MxL93644A includes integrated drivers, with the addition of programmable DC bias support for VCSEL-based optics.

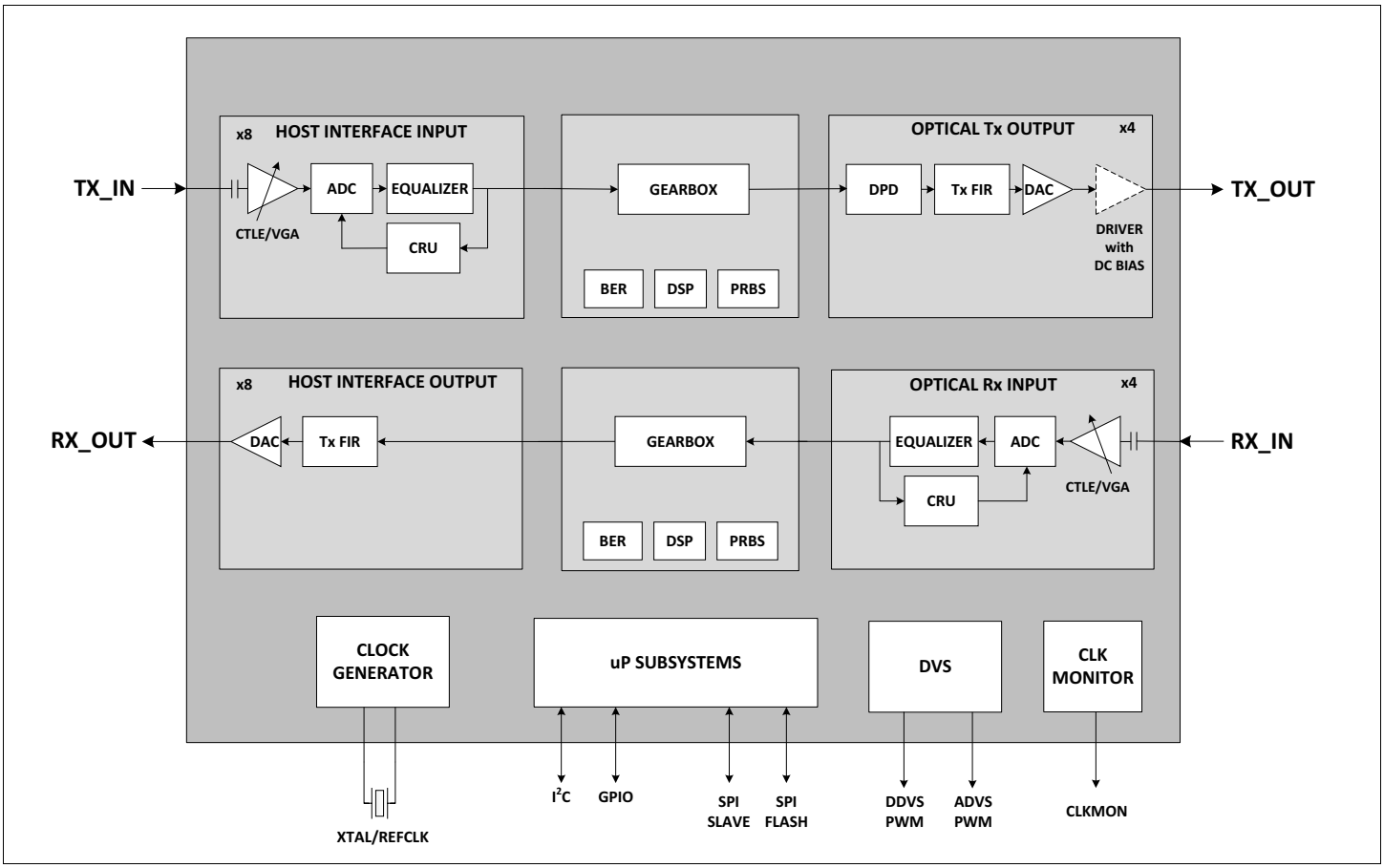

Figure 1: MxL93644A Simplified Block Diagram

Ordering Information

Table 1: Ordering Information

Marketing Part Number	Ordering Part Number	Description	Package	Shipping
MxL93644A	MXL93644A-PV-T	400G gearbox DSP with integrated VCSEL driver.	FC-FBGA	Tray

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598

www.maxlinear.com