MxL76505

15V, 5A Synchronous Step-Down Regulator
Data Sheet

General Description

The MxL76505 is a synchronous step-down switching voltage regulator capable of delivering up to 5A of load current. The device has a working input voltage range of 4.5V to 15V. Output voltage can be adjusted between 0.6V and 6V.

The MxL76505 can be configured to work in either diode emulation mode (DEM) that improves the efficiency at light loads by lowering the switching frequency or forced continuous conduction mode (FCCM) that maintains the same switching frequency regardless of load. Dynamic switching between DEM and FCCM is supported.

The MxL76505 comes in two switching frequency versions, 500kHz and 1MHz. The 500kHz version has less switching loss and supports a higher input-to-output voltage conversion ratio. The 1MHz version supports a smaller output LC filter and is also faster in responding to load transients.

The MxL76505 employs a fixed frequency constant on-time (COT) control architecture. Feedback loop compensation is internal and has been designed to work with an all-ceramic output capacitor bank. Load transient response, both in CCM and DCM, is ultra fast with a properly selected output LC filter. Soft-start is programmable via an external capacitor.

Protection features include over-current protection (OCP), over-voltage protection (OVP), and under-voltage protection (UVP), thermal shutdown and input under-voltage lockout (UVLO).

The MxL76505 is available in a 2mm × 2mm thermally enhanced 10-pin QFN package.

Features

- Up to 5A of load current
- Input voltage range from 4.5V to 15V
- Output voltage range from 0.6V to 6V
- Fast load transient response
- Excellent line transient rejection
- 500kHz or 1MHz switching frequency
- High light-load efficiency in DEM
- Dynamic switching between DEM and FCCM
- Programmable soft-start
- Output over-current protection
- Output under-voltage protection
- Thermal shutdown
- Input under-voltage lockout
- Hiccup or latch operation upon fault
- Thermally enhanced 2mm × 2mm QFN package

Applications

- Set-top boxes
- Point-of-load regulators
- FPGA power

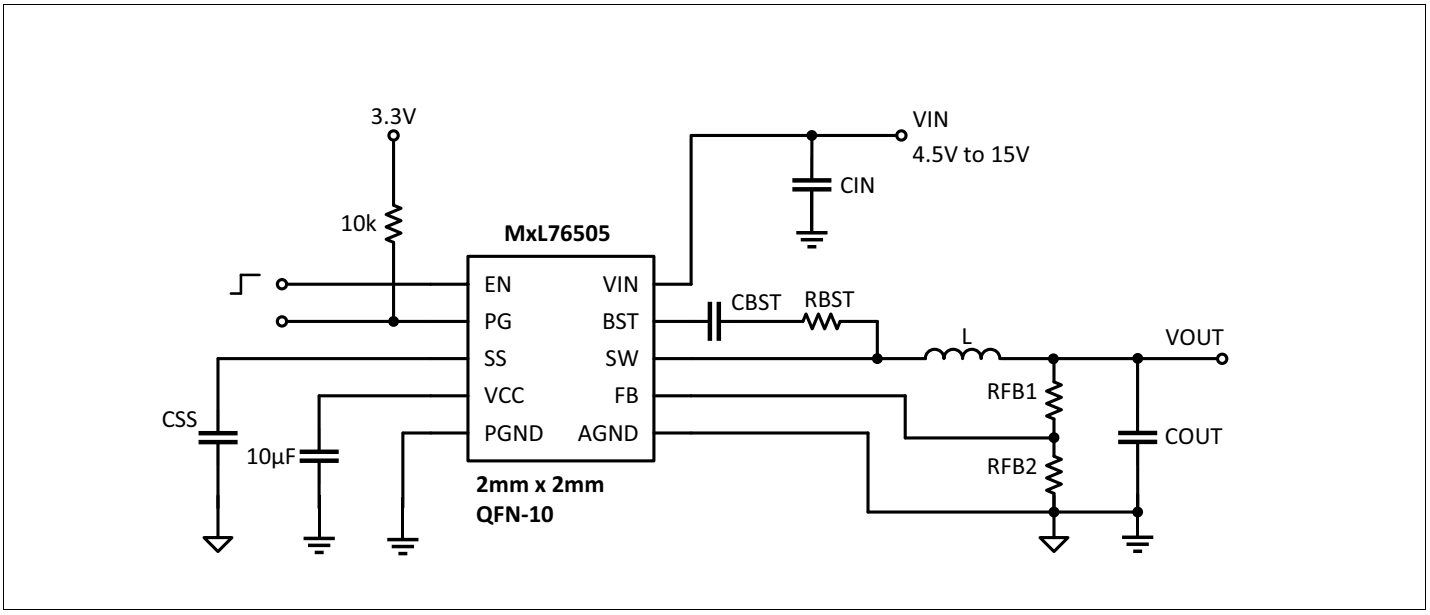

Figure 1: Typical Application

Revision History

Document No.	Release Date	Change Description
254DSR05	March 30, 2026	Initial final release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard. The thermal resistance profile is based on the *JEDEC EIA/JESD51-(2A, 8, 29)* standards.

Table 1: MxL76505 Absolute Maximum Ratings

Parameter	Conditions	Minimum	Maximum	Unit
Supply Voltage VIN	-	-	17	V
SW Pin Voltage	DC	–0.3	VIN + 0.3	V
SW Pin Voltage	AC (10ns)	–2V	VIN + 5	V
BST Pin Voltage	-	-	VSW + 6	V
VCC Pin Voltage	-	-	6	V
EN Pin Voltage	-	-	6	V
PG Pin Voltage	-	-	6	V
SS Pin Voltage	-	-	6	V
FB Pin Voltage	-	-	3.6	V
Junction Temperature	-	-	150	°C
Storage Temperature	-	–65	150	°C

Operating Conditions

Table 2: MxL76505 Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage VIN	4.5	15	V
Continuous Output Current	0	5	A
Junction Temperature	–40	125	°C

Table 3: ESD Ratings

ESD Model	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC-001	±2000	V
Charged Device Model (CDM), per JESD22-C101	±500	V

Thermal Specifications

Table 4: MxL76505 Thermal Specifications

Symbol	Parameter	Conditions	Typical	Unit
$\theta_{JC(top)}$	Junction-to-Case Top Thermal Resistance	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	102	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	28	°C/W
θ_{JA}	Junction-to-Ambient Thermal Resistance	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection.	56	°C/W
Ψ_{JB}	Junction-to-Board Thermal Characteristic	JEDEC 2s2p 4.5” × 3” PCB with thermal vias. Natural convection. Measured at 1mm from package edge on PCB.	32	°C/W

Electrical Characteristics

The • denotes specifications that apply over junction temperature range under "Operating Conditions" on page 1. Otherwise, T_J = 25°C. The typical specifications are T_J = 25°C only. VIN = 12V unless otherwise noted.

Table 5: MxL76505 Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply Current							
I_IN_NS	Input Supply Current, Non-Switching	EN = 3.3V, FB = 1V	•	-	320	520	µA
I_IN_SD	Input Supply Current, Shutdown	EN = 0V	•	-	8	20	µA
Switching Frequency							
FSW_500	Switching Frequency, 500kHz Version	VOUT = 1.2V, FCCM, no load.		-	500	-	kHz
FSW_1M	Switching Frequency, 1MHz Version	VOUT = 1.2V, FCCM, no load.		-	1000	-	kHz
Enable and Mode of Operation							
V_EN_FCCM	EN Pin Rise Threshold for FCCM Operation	-	•	1.15	1.3	1.4	V
V_EN_DEM	EN Pin Threshold for DEM Operation	EN rising.	•	1.9	2	2.2	V
V_EN_HYS	EN Pin Hysteresis	-		-	100	-	mV
T_EN_DLY	Enable Delay	From rising edge of EN to start of switching.	•	-	0.5	1	ms
Start-up and Shutdown							
I_SS	SS Pin Sourcing Current during Soft-Start	-		-	6.8	-	µA
R_SS	SS Pin Discharging Resistance during Shutdown	-	•	-	-	30	Ω
Error Amplifier							
I_FB	FB Pin Input Current	-	•	–100	-	100	nA
V_FB_REG	FB Pin DC Voltage	FCCM. Regulator is in steady state and VOUT is regulated.	•	591	600	609	mV
Protection							
T_TSD_THR	Thermal Shutdown Threshold	-		-	150	-	°C
T_TSD_HYS	Thermal Shutdown Hysteresis	-		-	20	-	°C
V_UVP	FB Trigger Voltage for Output UVP	FB voltage falling toward 0V.		-	0.39	-	V
ILIM	Current Limit Threshold	Inductor valley current.	•	5.1	6.7	8	A
I_SS_HIC	SS Pin Charging Current during Hiccup	-		-	140		nA
VTH_HIC	SS Pin Voltage Threshold for End of Hiccup Delay	-		-	0.7	-	V
I_NOC	Negative Current Limit Threshold	Inductor valley current.		-	–3.9	-	A
UVLO	Input Under-Voltage Lockout Threshold, Rising	VIN rising.	•	-	-	4.4	V
UVLO_HYS	Input UVLO Hysteresis	VIN falling.		-	600	-	mV

Table 5: MxL76505 Electrical Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power Good							
V_PG_THL	Power Good UV Rising threshold as a percentage of V_{FB_REG}	FB rising.		87	92	97	%
V_PG_HYS	Power Good Hysteresis as a Percentage of V_{FB_REG}	FB falling.		-	8	-	%
VPG_THU	Power Good OV Rising threshold as a percentage of V_{FB_REG}	FB rising.		110	117	124	%
V_PG	PG Pin Voltage when Power Good is Asserted.	Isink = 1mA.		-	0.13	0.4	V
Power FETs							
RON_HS	ON Resistance of the High-Side FET	VCC = 5V, VBST-VSW = 5V		-	48	-	mΩ
RON_LS	ON Resistance of the Low-Side FET	VCC = 5V		-	24	-	mΩ
Others							
T_ON_MIN	Minimum ON Time	-	•	-	90	-	ns
T_OFF_MIN	Minimum OFF Time	-	•	-	400	-	ns
I_ZCD	SW Node Zero Crossing Detector Threshold	Low-side FET source-to-drain current.		-	100	-	mA
V_VCC	VCC Pin Voltage	VIN > 5.5V		-	5	-	V

Pin Configuration

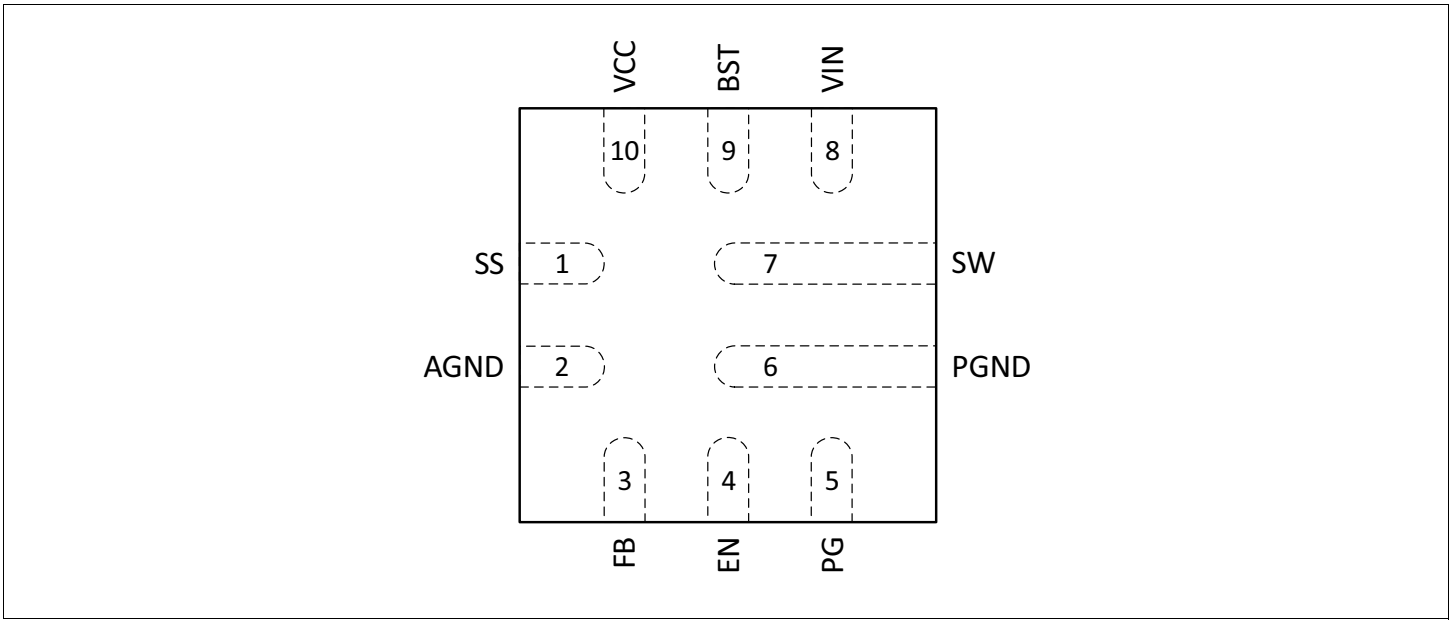


Figure 2: MxL76505 Pin Configuration (Top View)

Pin Description

Table 6: MxL76505 Pin Functions

Pin Name	Pin Number	Description
SS	1	Soft-start programming. Connect a capacitor between this pin and PGND to control the VOUT slew rate.
AGND	2	Ground connection for quiet internal analog circuitry. Connect this pin to local PCB ground.
FB	3	VOUT feedback connection. If target VOUT is higher than 0.6V, connect this pin to the center of the feedback voltage divider.
EN	4	Soft-start enable and DEM/FCCM select. Bring this pin above 1.35V to operate in FCCM or above 2.2V to operate in DEM. Dynamic switching between FCCM and DEM is allowed.
PG	5	Open-drain power good indicator. An internal MOSFET between this pin and PGND turns off once FB voltage is above 552mV (typical). The internal MOSFET is open-drain when EN is low or there is no input power.
PGND	6	Power ground. Connect to system power ground plane where input and output capacitors connect to.
SW	7	Switch node. This pin connects to the source of the internal high-side NFET and drain of the internal low-side NFET. Connect a 0.1µF capacitor between this pin and the BST pin to provide power for the high-side FET drive.
VIN	8	Input supply. Place a 1µF 0402 ceramic capacitor between this pin and PGND pin as close to the IC as possible to reduce switching ringing.
BST	9	Bootstrap pin. Connect a 0.1µF ceramic capacitor between this pin and the SW pin to provide power for the high-side FET gate drive.
VCC	10	Output of the internal linear regulator. Decouple VCC LDO with an 0603 10µF X7R type ceramic capacitor between this pin and PGND.

Typical Performance Characteristics

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1V, f_{SW} = 1MHz, unless otherwise noted.

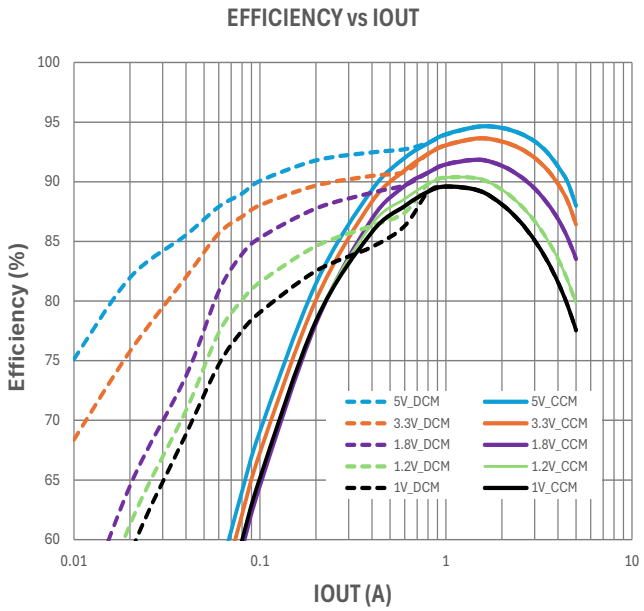


Figure 3: MxL76505A Efficiency 12V_{IN} 500kHz

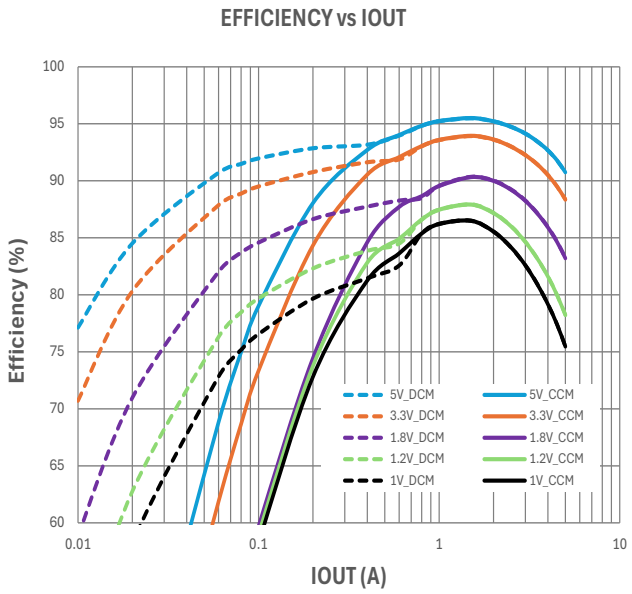


Figure 4: MxL76505B Efficiency 12V_{IN} 1MHz

Table 7: Inductor information (500kHz)

f_{SW} = 500kHz		
VOUT	**Inductor (µH)**	**DCR (mΩ)**
5	3.3	9
3.3	3.3	9
1.8	2.2	5.58
1.2	2.2	5.58
1	2.2	5.58

Table 8: Inductor information (1MHz)

f_{SW} = 1MHz		
VOUT	**Inductor (µH)**	**DCR (mΩ)**
5	2.2	5.58
3.3	1.5	9.9
1.8	1	5.2
1.2	1	5.2
1	1	5.2

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless other wise noted.

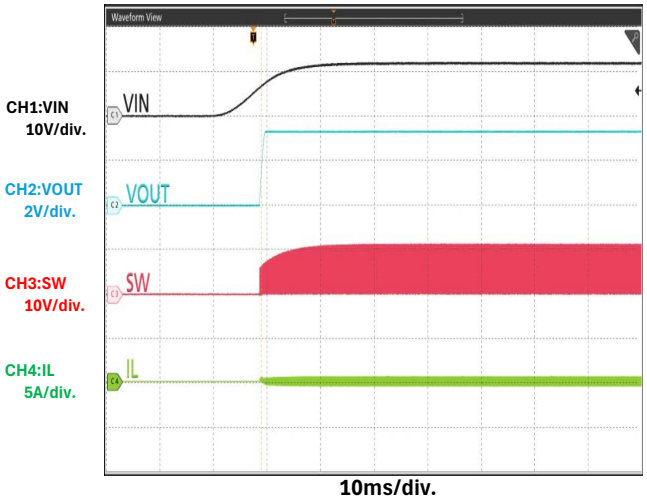


Figure 5: Start Up through V_{IN}, Load = 0A

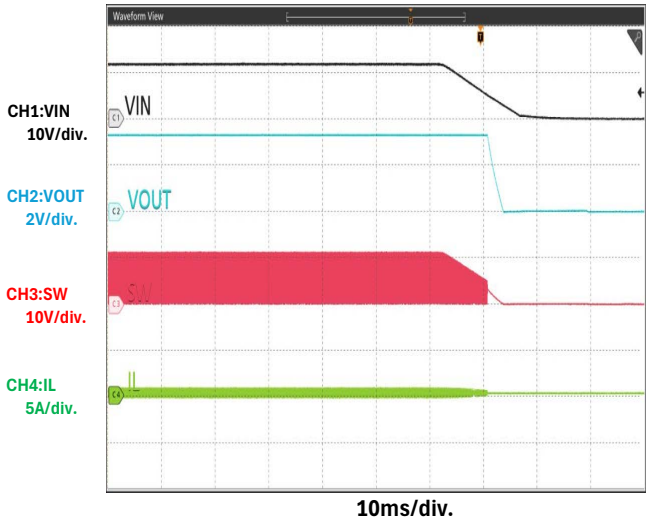


Figure 6: Power Down through V_{IN}, Load = 0A

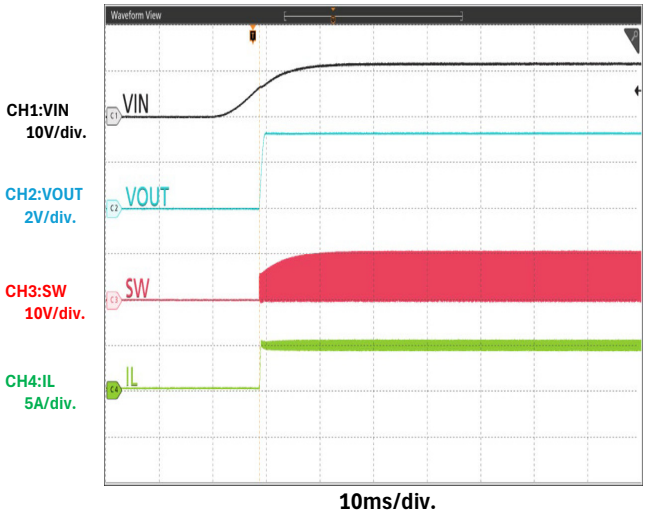


Figure 7: Start Up through V_{IN}, Load = 5A

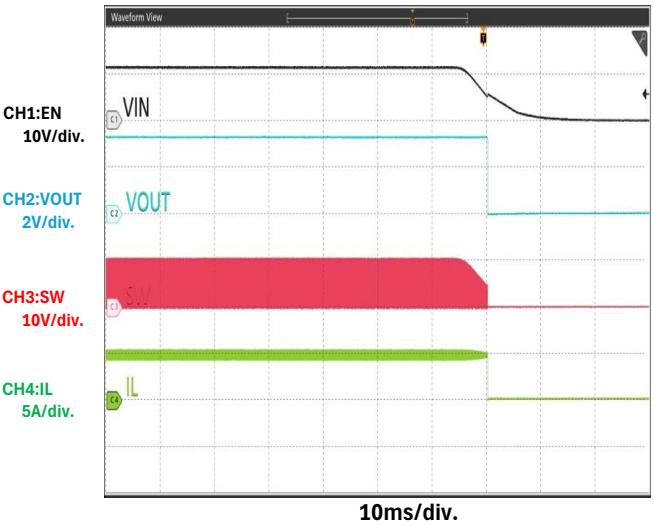


Figure 8: Power Down through V_{IN}, Load = 5A

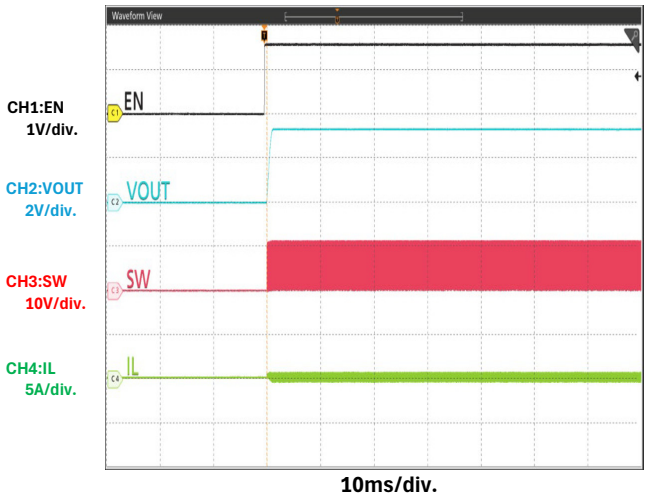


Figure 9: Start Up through EN, Load = 0A

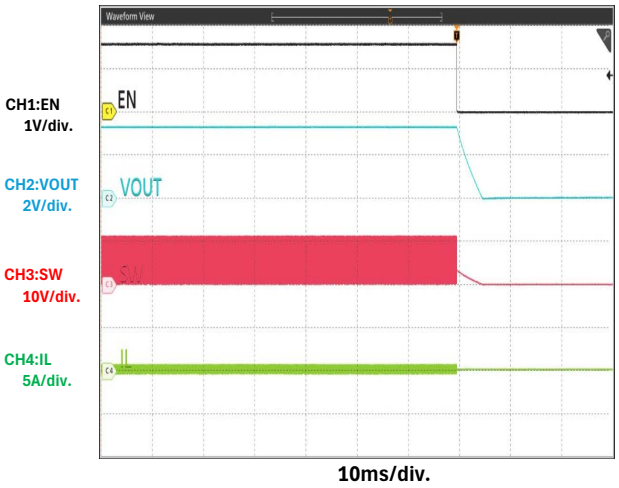


Figure 10: Power Down through EN, Load = 0A

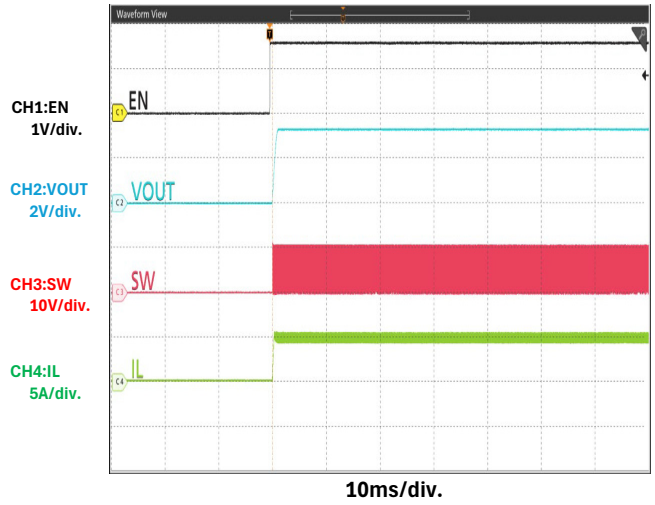


Figure 11: Start Up through EN, Load = 5A

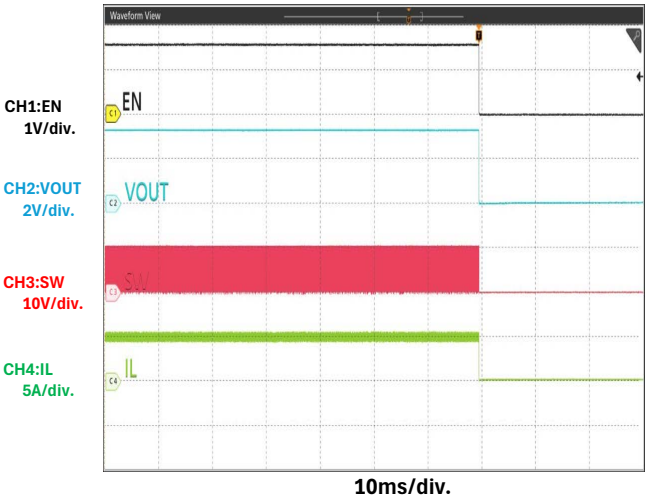


Figure 12: Power Down through EN, Load = 5A

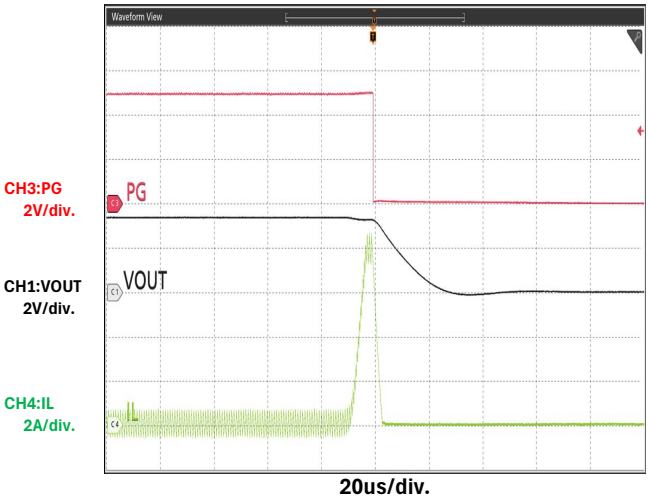


Figure 13: Over-Current Protection Entry

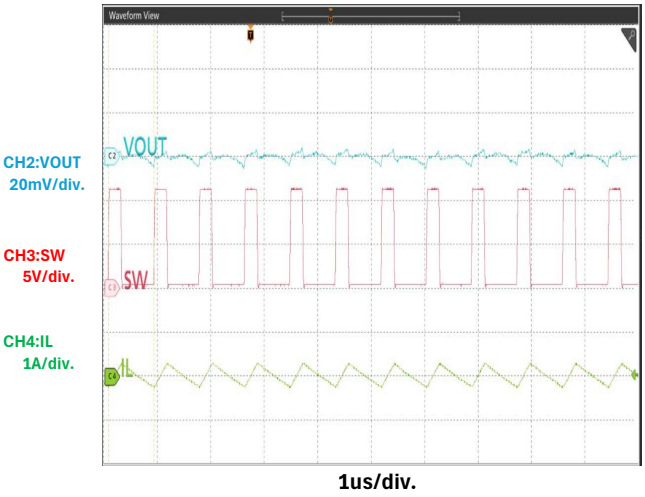


Figure 14: Output Ripple, Load = 0A

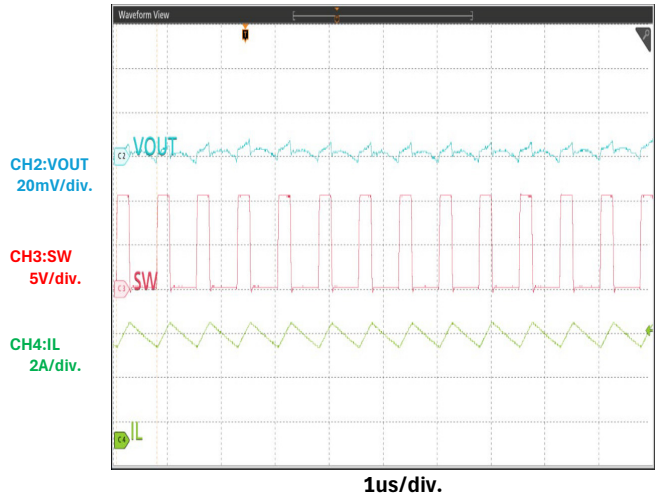


Figure 15: Output Ripple, Load = 5A

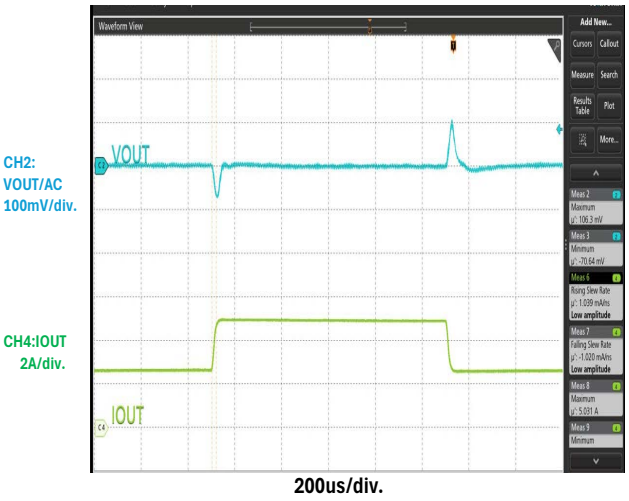


Figure 16: Load Transient Response, I_{OUT} = 2.5A - 5A - 2.5A, Slew Rate = 1A/µs

Block Diagram

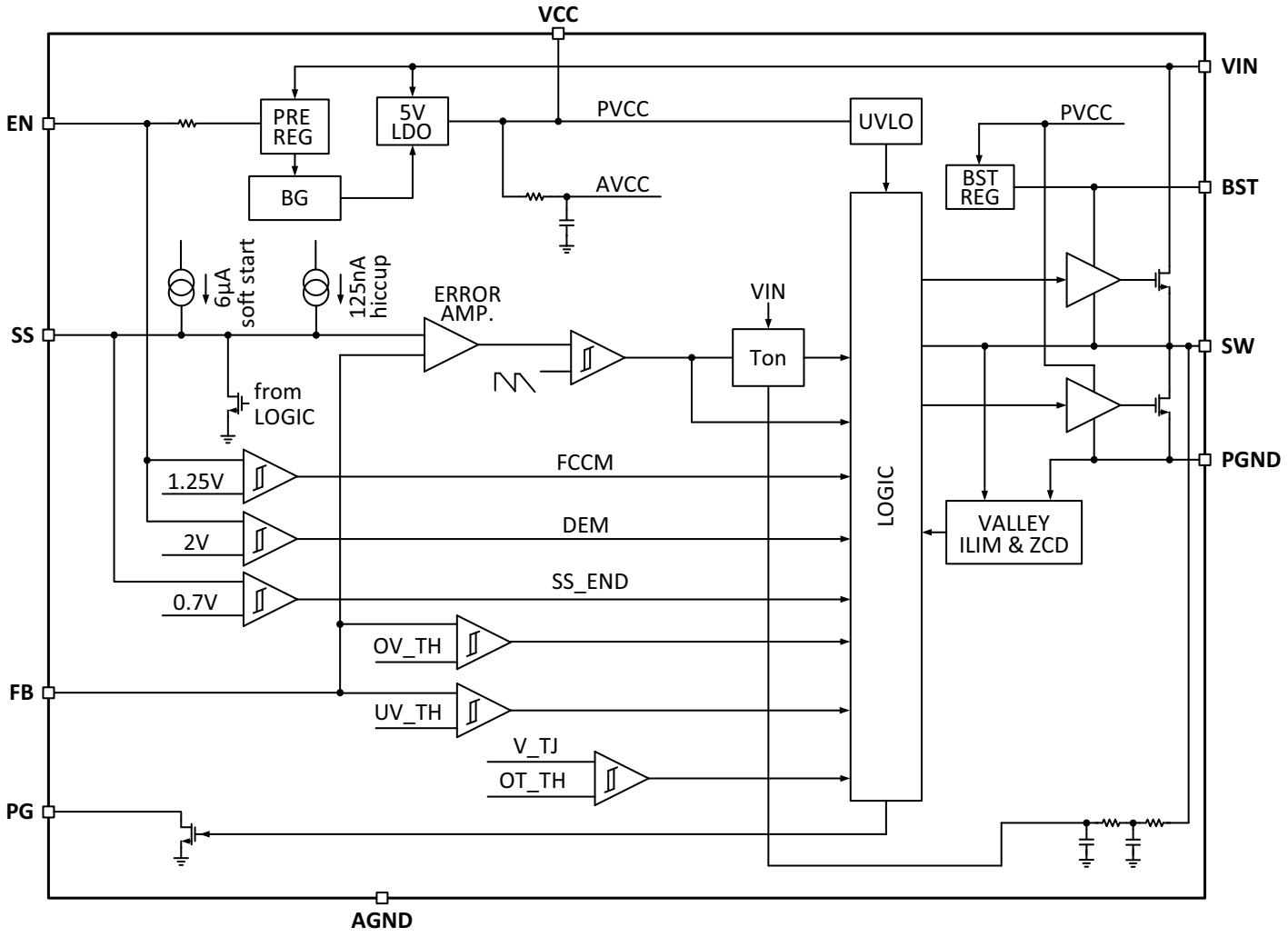


Figure 17: MxL76505 Block Diagram

Function Description

The Control Loop

The MxL76505 is a fully integrated, monolithic, synchronous step-down switched-mode converter capable of 5Amp continuous current. The MxL76505's feedback control is based on an adaptive voltage-mode constant on-time (COT) mechanism. Loop stability is achieved through adaptive on-time control with an internally compensated error amplifier feeding a comparator. The error amplifier output is compared to a compensating ramp which ensures stability when using ceramic output capacitors. No external compensation is typically necessary. Response to a large unloading transient is aided by voltage clamps in and around the error amplifier circuit.

Output voltage is set by an external feedback resistor divider whose center point is regulated to 0.6V in steady state.

FCCM and DEM Control

The MxL76505 can be programmed to operate in either forced continuous conduction mode (FCCM) or diode emulation mode (DEM). In FCCM, the high-side and low-side MOSFETs operate in a fully synchronous manner, resulting in CCM and constant frequency operation regardless of load current. In DEM, a zero-crossing detector circuit is activated which turns off the low-side preventing negative current flow thus emulating the functionality of a diode. In discontinuous conduction mode (DCM), as load decreases, on-time remains constant while off-time increases, resulting in lowered switching frequency and improved light-load efficiency.

To operate in FCCM, set the EN pin voltage between 1.35V and 1.9V. To operate in DEM, set the EN pin voltage above 2.2V. After soft-start the mode of operation is set by the EN pin voltage level. The FCCM/DEM mode of operation can be changed dynamically.

Enabling Device

The device can be enabled by using one of the following two different methods.

Method 1

Drive the EN pin with an external logic signal as shown in Figure 18. Ensure that the logic signal does not get set high until the VIN pin crosses 5V.

To disable the device, the logic signal must be reduced to 1.15V or below.

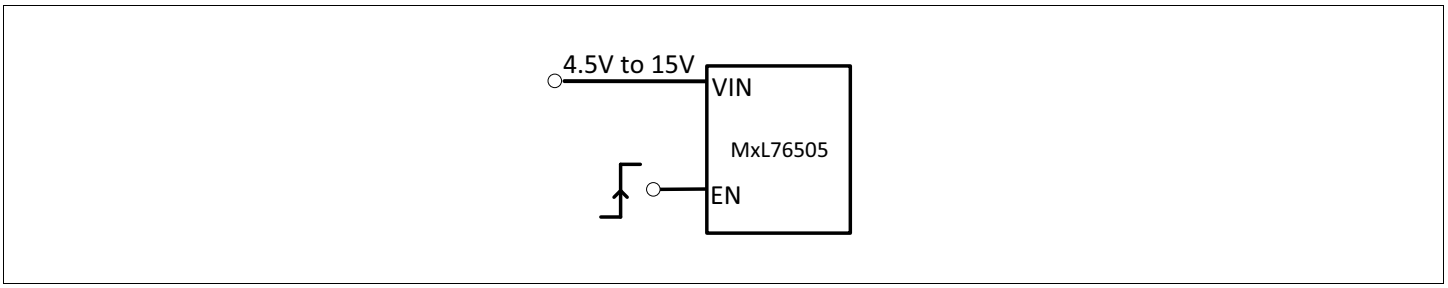


Figure 18: EN Pin Driven by a Logic Signal

Method 2

Self-start method. This method uses a resistor divider to divide down the VIN pin and drive the EN pin with the divided voltage. The choice of the resistor divider ratio depends on the VIN.

To ensure proper start-up, Maxlinear recommends you to use resistor values that guarantee that the VIN pin reaches 5V before the EN pin crosses the ON threshold. The following equation shows the relationship between R1, R2, and VIN_{TH} which is the VIN value when the EN pin voltage crosses 1.32V.

$$1 + \frac{R1}{R2} = \frac{VIN_{TH}}{1.32V}$$

Note: Select R1 and R2 by letting VIN_{TH} = 5V.

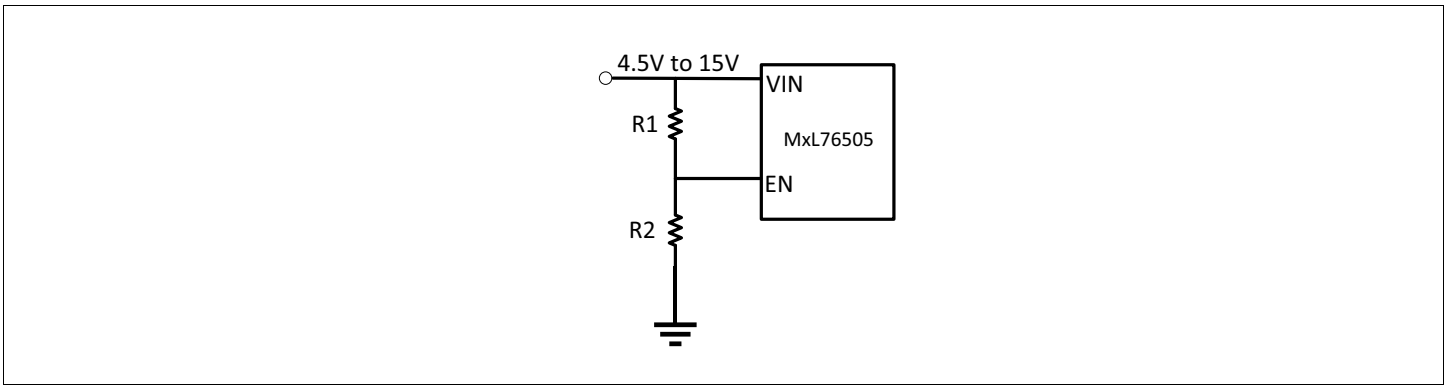


Figure 19: Self-Start for VIN Range from 4.5V to 15V

Soft-Start

When the EN pin is asserted and after ~500µs delay, a 6µA current is supplied by the SS pin to charge the soft-start capacitor C_{SS}. The output ramps to its final value once the SS pin reaches 0.6V. To program a soft-start time of t_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS}(nF) = \frac{t_{SS}(ms) \cdot 6(\mu A)}{0.6V}$$

However, the MxL76505 exits start-up mode only once the SS pin is greater than~0.7V. At that point PGOOD is released and switching operates in either DEM or FCCM, depending on the EN pin voltage.

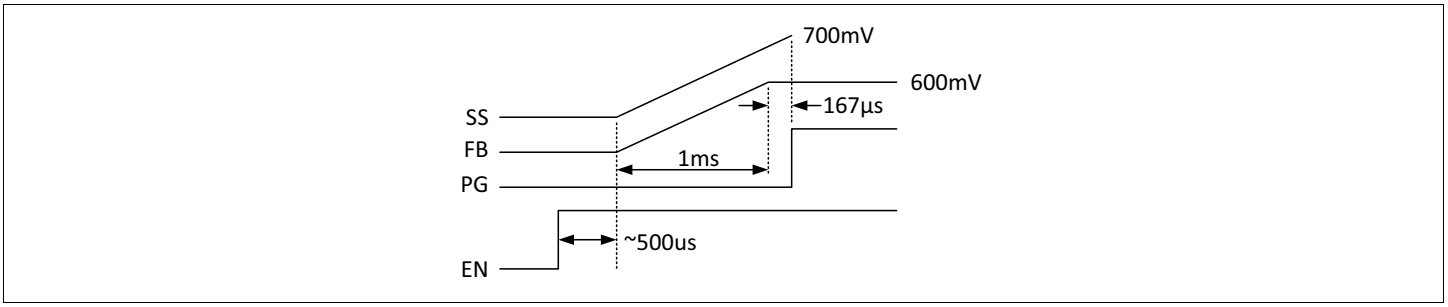


Figure 20: Start-up Sequence and Timing

For example in Figure 1: if 1ms is the desired start-up time, then C_{SS} = 10nF. The power good (PG) pin goes high in ~167µs (1ms divided by 6) after the output reaches regulation.

During start-up, the under-voltage protection (UVP) is disabled but the over-current protection (OCP), over-temperature protection (OTP), and over-voltage protection (OVP) are all enabled.

In the case of a pre-biased start-up where the output voltage is greater than 0V to begin with, both high-side and low-side FETs remains off until the SS pin reaches the pre-biased FB voltage. This behavior prevents output capacitor from being discharged and provides a monotonic voltage ramp during start-up.

Shutdown

To shut down the MxL76505, bring the EN pin below 1.15V. Both FETs turns off and output voltage decays based upon loading at the output. The external SS capacitor C_{SS} is discharged by a 30Ω internal resistance.

Over-Current Protection (OCP)

The MxL76505 monitors the current in the low-side MOSFET. During each switching cycle when the feedback loop attempts to turn on the high-side FET, if the sensed low-side FET current is higher than 6.7A, an OCP counter increments by 1 and the high-side FET is not allowed to turn on until the current drops below 6.7A. Otherwise, the OCP counter resets to 0. If the OCP counter counts to four, the MxL76505 turns off both FETs. For the latch version, the MxL76505 does not re-start until the EN voltage has been cycled; for the hiccup version, the MxL76505 autonomously re-starts after the hiccup delay expires. For more details, see “Recovering from a Fault” on page 14.

Negative Over-Current (NOC)

The MxL76505 has a negative inductor current limit to protect the device from being damaged in such a case as output voltage being pulled up by another voltage rail. If the instantaneous inductor current becomes more negative than –3.9A, the negative over-current (NOC) circuit will turn off the low-side FET and turn on the high-side FET for one ON time. Afterwards, the feedback loop takes back the control. A NOC event only causes early termination of the off-time of the present cycle. During the next cycle the low-side FET is allowed to turn on again.

NOC always operates when the device is in FCCM operation.When the device is operating in DEM, during a load release that moves the operating point from CCM to DCM the –3.9A NOC is active for the first four switching cycles before reverting to DEM. Allowing a few cycles of negative current improves unloading transient response.

Over-Temperature Protection (OTP)

During operation, if the die temperature exceeds 150°C, the MxL76505 turns off both FETs and shut down. Once the die temperature drops by 20°C, the device re-starts after the hiccup time out or, for the latch version, after the input, or the EN pin is cycled. For more details, see “Recovering from a Fault” on page 14.

Note: If VIN is cycled after OTP and the die temperature drops below 150°C, the MxL76505 attempts to re-start.

Over-Voltage Protection (OVP)

Over-voltage protection (OVP) protects the device when a higher external voltage is inadvertently connected to the output of the regulator. Initially NOC protects the device as it attempts to regulate by sinking current from the output. As the output voltage rises above ~117% of the set point, PGOOD is pulled low and the MOSFETs tri-state. When the output drops by the hysteresis (~8%), PGOOD goes high and normal operation resumes. For a device set for FCCM, switching resumes and the output is actively pulled down limited by NOC. For devices set for DEM, switching does not resume until the voltage has fallen within the normal regulation range.

An over-voltage protection (OVP) event is not considered a fault and does not cause the part to shut down.

Power Good (PG) Flag

The power good (PG) pin is an open drain signal which indicates whether VOUT is within ~92% to ~117% of the target output voltage. When outside the regulation window or a fault has occurred, the PG pin pulls low.

During start-up, PG is initially low. After the SS pin exceeds 700mV and the output is within the PG window, the PG pin goes high impedance, asserting power good.

When VIN is lower than the UVLO threshold, the PG pin is in high-impedance state. This does not indicate a power good state.

Under-Voltage Protection (UVP)

If the FB pin is quickly pulled down to <0.39V during normal operation, under-voltage protection (UVP) is triggered in which case the MxL76505 turns off both FETs and shut off. For the latch version, the MxL76505 does not re-start until the EN voltage is cycled; for the hiccup version, the MxL76505 autonomously re-starts after the hiccup delay expires. For more details, see “Recovering from a Fault” on page 14.

An UVP event can be caused by shorting VOUT to ground or by disconnecting the upper feedback resistor during normal operation. UVP is disabled during start-up although most events resulting in UVP causes an OCP event during start-up.

Recovering from a Fault

Upon triggering OCP, UVP or OTP, the MxL76505 turns off both FETs and shut down. The external SS capacitor is discharged by a 30Ω internal resistance.

For the latch version of the MxL76505, cycle the EN pin or input voltage to initiate a soft-start and recover from the fault protection mode.For the hiccup version, the MxL76505 autonomously re-starts after a delay. During the hiccup delay time, a 125nA current charges the soft-start capacitor until the SS pin voltage reaches 0.7V. After that, the soft-start capacitor is again discharged by the 30Ω internal resistor. Once SS pin voltage drops below 0.1V, a new soft-start event begins. The hiccup delay can be calculated as follows:

$$t_{hiccup\_delay} = C_{SS} \cdot \frac{0.7V}{125nA}$$

Where C_{SS} is the capacitance at the SS pin. As an example, if C_{SS} = 10nF, the hiccup delay is 56ms. Note that as C_{SS} is changed to meet sequencing requirements the hiccup delay also changes.

Application Information

The MxL76505 is a fully integrated, monolithic synchronous buck switching regulator that works with an input ranging from 4.5V to 15V and regulates an output from 0.6V to 6V. The maximum continuous load current rating is 5A within thermal limits of the device. The MxL76505 offers two nominal switching frequency options, 500kHz and 1MHz, and two fault handling options, latch, and hiccup.

The following figure shows a design example utilizing the 500kHz MxL76505A.

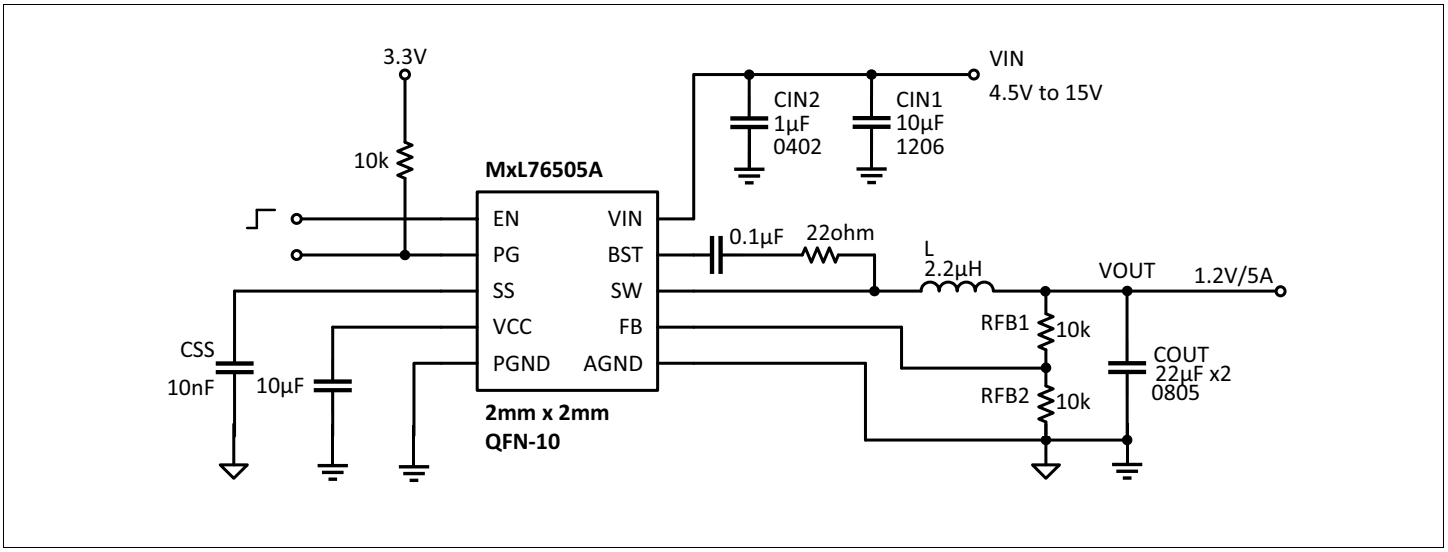


Figure 21: Design Example Using the 500kHz MxL76505A

The following figure shows another design example utilizing the 1MHz MxL76505B.

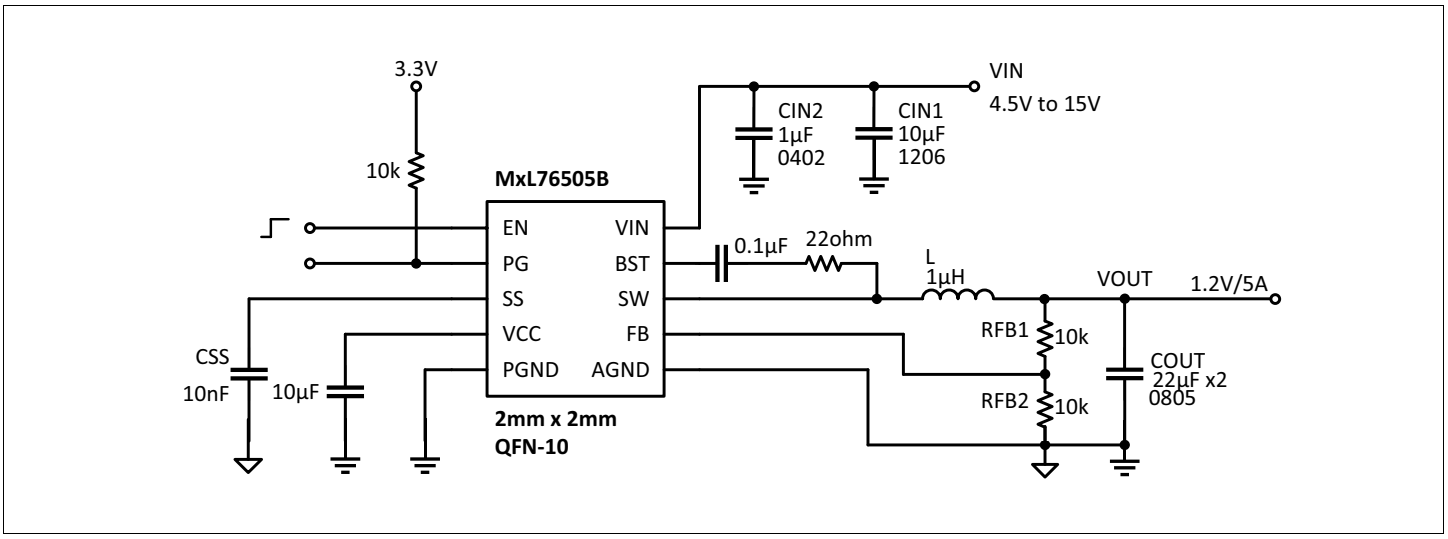


Figure 22: Design Example Using the 1MHz MxL76505B

Setting the Output Voltage

To set the nominal value of the output voltage, use 10kΩ for RFB2 (see Figure 2 on page 4), then use the following equation to find out the value for RFB1:

$$\mathrm{RFB1} = \mathrm{RFB2} \cdot \left(\frac{\mathrm{VOUT}}{0.6\mathrm{V}} - 1\right)$$

To avoid interfering with the internal loop compensation network, use an RFB2 value lower than or equal to 10kΩ.

Since the minimum on-time of the high-side FET is ~90ns, the minimum CCM duty cycle for the 1MHz option is around 90ns/1µs or 9%, at no load. This means that for a 12V application, the maximum regulated VOUT is 1.08V. If the lower duty cycle conversion is desired, MaxLinear recommends the use of 500KH.

The minimum off-time of the high-side FET is 400ns, therefore the maximum duty cycle for the 1MHz option is around (1µs – 400ns)/1µs or 60%.If the input voltage drops further, the device is in dropout and the output also drops.

Bootstrap Capacitor

MaxLinear recommends the use of a 0.1µF ceramic capacitor for the bootstrap capacitor which is connected between the SW pin and the BST pin. MaxLinear recommends the use of a 22Ω resistor in series with this capacitor to reduce ringing on the switch node and control high frequency conducted EMI.

VCC Capacitor

MaxLinear recommends the use of a 10µF ceramic capacitor of 0603 size or smaller for the capacitor between VCC pin and PGND.

Input Capacitors

The devices require input decoupling capacitors on the power supply input, VIN. The input capacitors (C_{IN}) provides the AC component of the input current, reducing both conducted noise emitted back to the input voltage rail as well as ripple voltage seen by the VIN pin. MaxLinear recommends that you use high-quality X5R or X7R input decoupling capacitors. The MxL76505 uses a 10µF to 22µF 1206 or 0805 for primary bypassing and a 0.1µF to 1µF 0402 for high frequency bypassing. Pay attention to inductive loops which are described in the “Layout Guidelines” on page 20.

The minimum input capacitance required is as follows:

$$C_{IN(min)} = \frac{I_{OUT} \cdot V_{OUT}}{VIN_{ripple} \cdot VIN \cdot f_{SW}}$$

Ensure that the input capacitor RMS current rating matches the application requirements. That current can be calculated as follows:

$$I_{in\_ac\_rms} = IOUT\sqrt{D \cdot (1 - D)}$$

Where D is CCM duty cycle approximately equal to VOUT/VIN, and $I_{in\_ac\_rms}$ is the RMS value of the AC current that flows through the capacitors. Manufacturers of capacitors can provide curves of temperature rise versus AC RMS current.

Output LC Filter and Feedback Loop Stability

The MxL76505 includes an internal feedback loop compensation network that is optimized for ceramic output capacitors. Therefore, LC filter component selection impacts stability, transient performance, and efficiency. Since the feedback loop compensation network is internal and fixed, double-pole frequency of the output LC filter needs to be bounded to achieve a stable loop. The following table is a fast and easy guide that lists the inductor and output capacitor selection for the LC filter.

Table 9: Output Inductance and Capacitance for 500KHz and VIN = 12V

VOUT	Inductor (µH)	Output Capacitance (µH)
0.6	1	88
0.8	1	88
1	2.2	44
1.2	2.2	44
1.8	2.2	44
2.5	2.2	44
3.3	3.3	22
5	3.3	22

Table 10: Output Inductance and Capacitance for 500KHz and VIN = 5V

VOUT	Inductor (µH)	Output Capacitance (µH)
0.6	1	88
0.8	1	88
1	2.2	44
1.2	2.2	44
1.8	2.2	44
2.5	3.3	22
3.3	3.3	22

Table 11: Output Inductance and Capacitance for 1MHz and VIN = 12V

VOUT	Inductor (µH)	Output Capacitance (µH)
1	1	88
1.2	1	88
1.8	1	88
2.5	1.5	66
3.3	1.5	66
5	2.2	44

Table 12: Output Inductance and Capacitance for 1MHz and VIN = 5V

VOUT	Inductor (µH)	Output Capacitance (µH)
0.6	1	88
0.8	1	88
1	1	88
1.2	1.5	88
1.8	1.5	66
2.5	1.5	66
3.3	2.2	44

Note: The nominal output capacitance is calculated for the greater of 1% output ripple or 10mV with the nominal inductor.

These guidelines also ensure the device is stable when in DCM operation.

Specifying the Inductor

There are three main factors in specifying a suitable inductor: inductance, saturation current, and power loss. Using Table 11 and selecting 1.8V output, the recommended inductance value is 1µH. Inductor manufacturers typically provide inductance versus current curves and/or a saturation current as shown in Figure 22 on page 15.The saturation current is typically a value where the initial inductance has fallen by 30%, although vendors can have various standards.

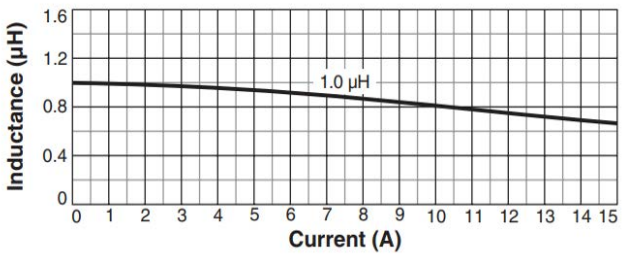


Figure 23: Coilcraft XAL5030-102ME Inductance vs Current

The peak current in the inductor during normal operation is as follows:

$$\mathrm{Ipk} = \frac{\Delta \mathrm{i}}{2} + \mathrm{IOUT}$$

Δi is calculated as follows:

$$\Delta \mathrm{i} = \frac{\mathrm{VOUT} \cdot (1 - \frac{\mathrm{VOUT}}{\mathrm{VIN}})}{\mathrm{f_{sw}} \cdot \mathrm{L}}$$

Calculating Δi and I_{pk} for the 1.8V output:

$$\Delta \mathrm{i} = \frac{1.8 \cdot (1 - \frac{1.8}{12})}{1\mathrm{MHz} \cdot 1\mu\mathrm{H}} = 1.5\mathrm{A}$$

$$\mathrm{Ipk} = \frac{1.5\mathrm{A}}{2} + 5\mathrm{A} = 5.7\mathrm{A}$$

The selected inductor should have 1μH at 5.7A, the inductor in Figure 22 on page 15 is 1μH.

The last step is to determine power loss. In many cases, one simply calculates the RMS current in the inductor and uses the DC resistance (DCR) to calculate losses.For a first estimate this works as expected. The inductor data sheet also provides thermal ratings based on the RMS current. The RMS current is calculated as follows:

$$I_{RMS} = \sqrt{IOUT^2 + \frac{\Delta i^2}{12}}$$

In the case of the XAL5030-102ME, the device states a 20°C rise at 8.7Arms which is more than sufficient. The DCR is specified as 8.5mΩ which gives a power loss of 212mW, or ~2.3% of the output power.A value between 2% and 4% loss results in small and cost-effective inductors.

A last check for inductor losses would be to determine the core losses. These are typically not published in the inductor data sheet but are available through online tools. In general, if the peak current is far below the saturation point the core losses are minimal.

Layout Guidelines

The second layer should be used as an internal PGND plane. Minimize the distance between the top layer and the second layer, if possible. For more information, see Figure 22 on page 15 and Figure 23 on page 18. The MxL76505 is mounted on the top layer.

1. The high frequency 0.1µF 0402 bypassing cap uses the 2nd layer PGND plane to minimize the effective loop length. This reduces inductance to a minimum making the cap more effective at bypassing HF content of the AC input current. The return current on the second layer does not follow a direct path back but tends to follow the same path as the current on the top layer due to coupling.
2. Place four or more PGND vias in the area between the PGND and PG pins.
3. Assign as much copper as allowed to VIN and PGND pins to help keep the MxL76505 cool. In this case, VIN has via connections to the large 12V power plane on an inner layer.
4. Place the VCC capacitor as close as possible to the VCC pin. Add PGND vias right next to the C_{VCC} PGND pin.
5. C_{BST} is on the bottom layer connecting to R_{BST} on the top layer which is close to the BST pin.
6. If remote ground sensing is desired, connect the AGND pin to the PGND net at the remote sensing location. Otherwise, short the AGND net to the PGND net at the AGND pin.
7. Place feedback voltage divider, RFB1 and RFB2, close to the FB pin.
8. VOUT feedback trace should avoid passing under the inductor or overlap with any SW traces.

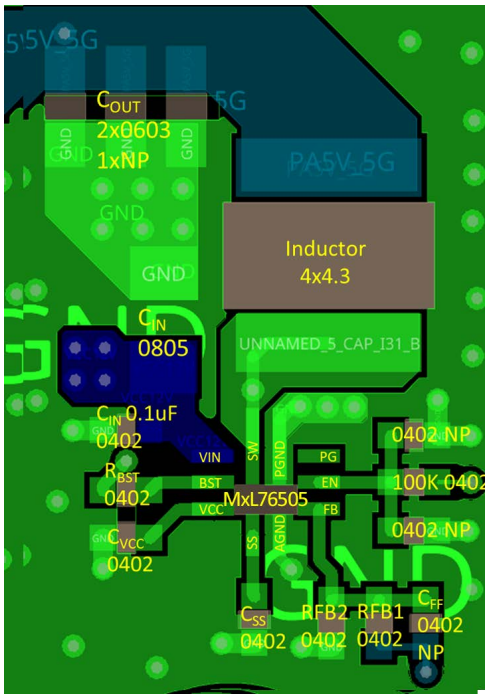


Figure 24: Recommended PCB Layout—Top Layer

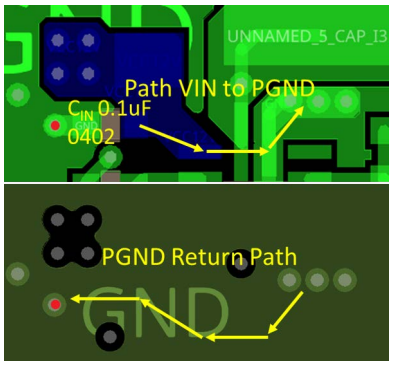
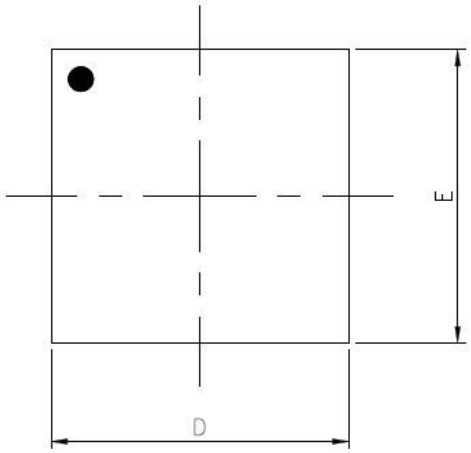


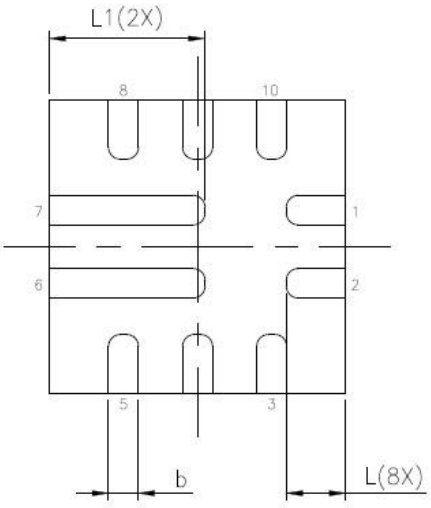
Figure 25: Recommended PCB Layout—2nd Layer HF PGND Return

Packaging

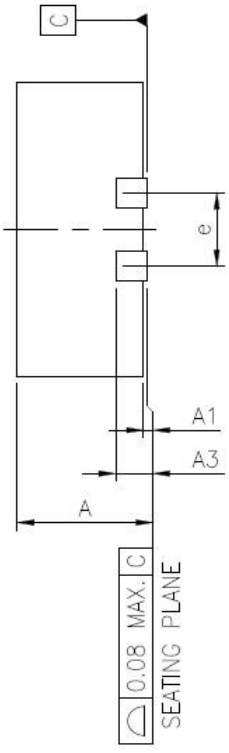
Mechanical Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

JEDEC OUTLINE	N/A		
PKG CODE	VQFN		
SYMBOLS	**MIN**	**NOM**	**MAX**
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	0.50 BSC		
L	0.35	0.40	0.45
L1	1.00	1.05	1.10

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

NOTE:
1. All dimensions are in millimeters
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

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Figure 26: MxL76505 Packaging Dimensions

Ordering Information

Table 13: Ordering Information

Ordering Part Number	Frequency	Fault Handling	Package	TJ Range	Packing Method	SPQ	Lead Free
MXL76505A-AQF-R	500KHz	Hiccup	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL76505B-AQF-R	1MHz	Hiccup	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL76505C-AQF-R	500KHz	Latch	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL76505D-AQF-R	1MHz	Latch	2 × 2mm QFN-10	–40°C to 125°C	Tape and Reel	5000	Yes
MXL76505A-EVK-1	MxL76505A Evaluation Kit						
MXL76505B-EVK-1	MxL76505B Evaluation Kit						
MXL76505C-EVK-1	MxL76505C Evaluation Kit						

Note: For more information about the EVK, refer to *MxL76505 EVK User Manual* (035UM).

MaxLinear, Inc.
5966 La Place Court, Suite 100
Carlsbad, CA 92008
Tel.: +1 (760) 692-0711
Fax: +1 (760) 444-8598

www.maxlinear.com