MxL82212

8-bit I²C/SMBUS GPIO Expander with Reset
Preliminary Data Sheet

General Description

The MxL82212 is a 8-bit GPIO expander with an I²C/SMBus interface. The MxL82212 has the internal pull-up resistors enabled upon power-up in case it is necessary for the inputs to be in a known state.

In addition, the GPIOs on the MxL82212 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote device, but it may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt can be programmed for different behaviors. The interrupts can be programmed to generate an interrupt on the rising edge, falling edge, or on both edges. The interrupt can be cleared if the input changes back to its original state or by reading the current state of the inputs.

The MxL82212 is 16-pin QFN. It is pin and software compatible with the PCA9538 (note that the software registers are compatible to the PCA9538, but the I²C slave address is different).

Applications

- Personal digital assistants (PDA)
- Cellular phones/Data devices
- Battery-Operated devices
- Global Positioning System (GPS)
- Bluetooth

Features

- 1.62V to 5.5V operating voltage
- 8 General Purpose I/Os (GPIOs)
- Maximum stand-by current of 1μA at +1.8V
- I²C/SMBus bus interface
- I²C clock frequency up to 1000kHz
- Noise filter on SDA and SCL inputs
- Up to 16 I²C Slave addresses
- Individually programmable inputs
- Internal pull-up resistors
- Polarity inversion
- Individual interrupt enable
- Rising edge and/or falling edge interrupt
- Input filter
- Individually programmable outputs
- Output level control
- Output three-state control
- Open-drain active low interrupt output
- Active-low reset input
- Pin and software compatible with PCA9538
- 3kV HBM ESD protection per JESD22-A114F
- 200mA latch-up performance per JESD78B

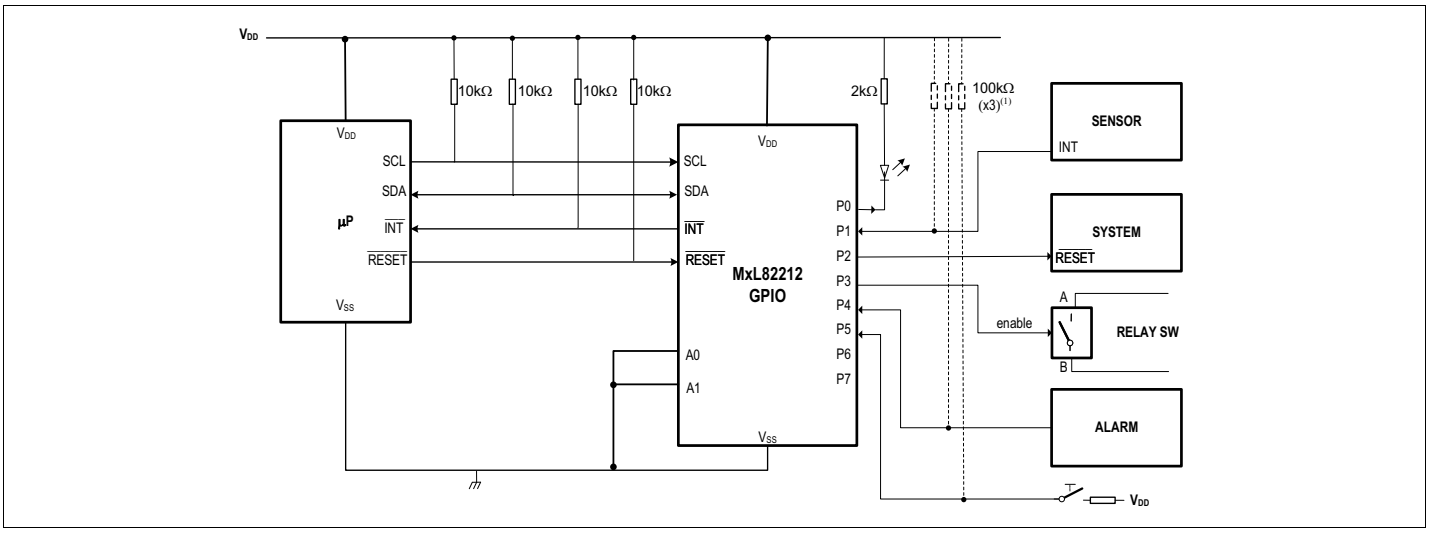

Figure 1: Typical Application Schematic

Revision History

Document No.	Release Date	Change Description
299DSR01	April 24, 2026	**Updated:** ■ Typo in the " General Description" section.
299DSR00	April 15, 2026	Initial preliminary release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard. The thermal resistance profile is based on the *JEDEC EIA/JESD51-(2A, 8, 29)* standards.

Table 1: Absolute Maximum Ratings

Parameter	Conditions	Minimum	Maximum	Unit
Power Supply Voltage	-	-	6V	V
Supply Current	-	-	-	-
Ground Current	-	-	-	-
External Current limit of each GPIO	-	-	-	-
Total Current limit for GPIO[7:0]	-	-	-	-
Total Supply Current sourced by all GPIOs	-	-	-	-
Operating Temperature	-	-	-	-
Storage Temperature	-	–40	+85	°C
Power Dissipation	-	-	-	-

Thermal Specifications

Table 2: Thermal Specifications (Margin of Error: ±15%)

Symbol	Thermal Metric	Typical	Unit
θ_{JC}	Junction-to-Case Thermal Resistance	26	°C/W
θ_{JA}	Junction-to-Ambient Thermal Resistance	40	°C/W

Electrical Characteristics

DC Electrical Characteristics

Unless otherwise noted, T_A = –40° to +85°C, V_{CC} is from 1.62V to 5.5V.

Table 3: DC Electrical Characteristics

Symbol	Parameter	Limits 1.8V ± 10% Min	Limits 1.8V ± 10% Max	Limits 2.5V ± 10% Min	Limits 2.5V ± 10% Max	Limits 3.3V ± 10% Min	Limits 3.3V ± 10% Max	Limits 5V ± 10% Min	Limits 5V ± 10% Max	Units	Conditions
V_{IL}	Input Low Voltage	–0.3	0.3VCC	–0.3	0.3VCC	–0.3	0.3VCC	-	-	V	-
V_{IL}	Input Low Voltage	–0.3	0.2	–0.3	0.5	–0.3	0.8	-	-	V	Note 1
V_{IH}	Input High Voltage	1.3	VCC	1.8	VCC	2.3	VCC	-	-	V	Note 2
V_{IH}	Input High Voltage	1.4	5.5	1.8	5.5	2.0	5.5	-	-	V	Note 1
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	-	-	V V V	Note 2
V_{OL}	Output Low Voltage	-	0.5	-	0.5		0.5	-	-	V	I_{OL} = 3mA I_{OL} = 3mA I_{OL} = 3mA Note 3
V_{OL}	Output Low Voltage	-	0.4	-	0.4	-	0.4	-	-	V V V	I_{OL} = 8mA Note 4
V_{OH}	Output High Voltage	1.2	-	1.8	-	2.6	-	-	-	V V V	I_{OL} = 6mA I_{OL} = 4mA I_{OL} = 1.5mA Note 5
I_{IL}	Input Low Leakage Current	-	±10	-	±10	-	±10	-	-	µA	I_{OH} = –8mA I_{OH} = –8mA I_{OH} = –8mA Note 4
I_{IH}	Input High Leakage Current	-	±10	-	±10	-	±10	-	-	µA	-
I_{CC}	Power Supply Current	-	50	-	100	-	200	-	-	µA	-
I_{CC}	Power Supply Current	-	150	-	250	-	500	-	-	µA	Test 1
I_{CCS}	Standby Current	-	1	-	2	-	5	-	-	µA	Test 2
C_{IN}	Input Pin Capacitance	-	5	-	5	-	5	-	-	pF	Test 3
R_{GPIO}	GPIO pull-up Resistance	60	140	60	140	60	140	-	-	kΩ	-
$R_{RESET\#}$	Reset# Pull-Up Resistance	35	85	35	85	35	85	-	-	kΩ	100kΩ ± 40%

1. For I^2C input signals (SDA, SCL).
2. For GPIOs, A0, A1, and A2 signals.
3. For I^2C output signal SDA.

4. For GPIOs.

5. For IRQ# signal.

6. Test 1: SCL frequency is 400KHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

7. Test 2: SCL frequency is 400Hz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

8. Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

AC Electrical Characteristics

Unless otherwise noted, T_A = –40^o to +85^{o}C, V_{CC} is from 1.62V to 5.5V.

Table 4: AC Electrical Characteristics

Symbol	Parameter	Standard Mode I^{2}C-Bus		Fast Mode I^{2}C-Bus		Fast Mode I^{2}C-Bus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Operating Frequency	0	100	0	400	-	1000	kHz
T_{BUF}	Bus Free Time between STOP and START	4.7	-	1.3	-	-	-	µs
$T_{HD;STA}$	START Condition Hold Time	4.0	-	0.6	-	-	-	µs
$T_{SU;STA}$	START Condition Setup Time	4.7	-	0.6	-	-	-	µs
$T_{HD;DAT}$	Data Hold Time	0	-	0	-	-	-	ns
$T_{VD;ACK}$	Data Valid Acknowledge	-	0.6	-	0.6	-	-	µs
$T_{VD;DAT}$	SCL LOW to Data Out Valid	-	0.6	-	0.6	-	-	ns
$T_{SU;DAT}$	Data Setup time	250	-	150	-	-	-	ns
T_{LOW}	Clock LOW Period	4.7	-	1.3	-	-	-	µs
T_{HIGH}	Clock HIGH Period	4.0	-	0.6	-	-	-	µs
T_F	Clock/Data Fall Time	-	300	-	300	-	-	ns
T_R	Clock/Data Rise Time	-	1000	-	300	-	-	ns
T_{SP}	Pulse width of Spikes Tolerance	50	-	50	-	-	-	ns
T_{D1}	I^{2}C-bus GPIO Output Valid	-	0.2	-	0.2	-	-	µs
T_{D4}	I^{2}C Input Pin Interrupt Valid	-	4	-	4	-	-	µs
T_{D5}	I^{2}C Input Pin Interrupt Clear	-	4	-	4	-	-	µs
T_{D15}	SCL Delay after Reset	3	-	3	-	-	-	µs

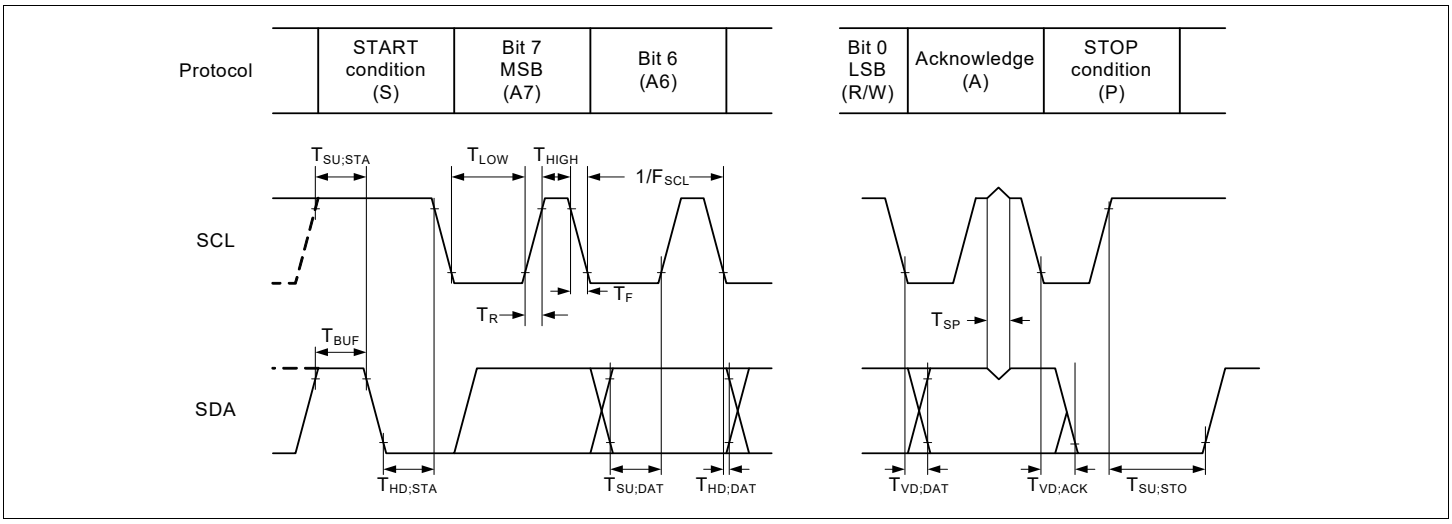


Figure 1: I²C-Bus Timing Diagram

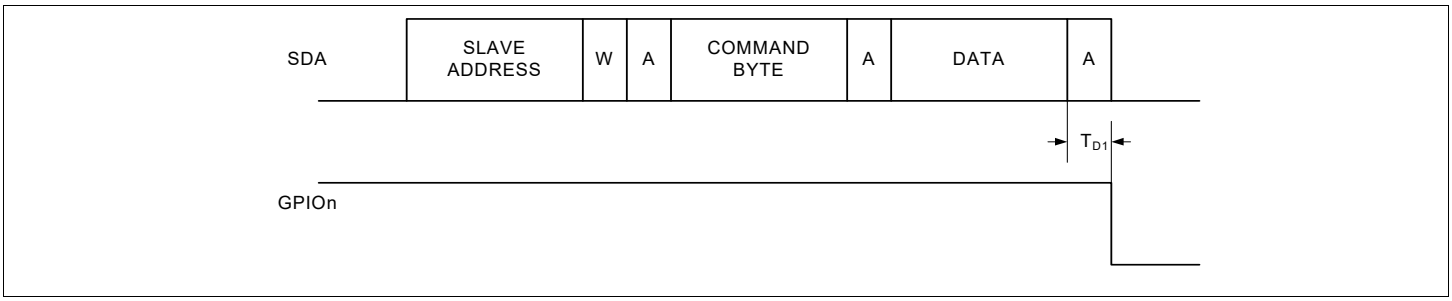


Figure 2: Write To Output

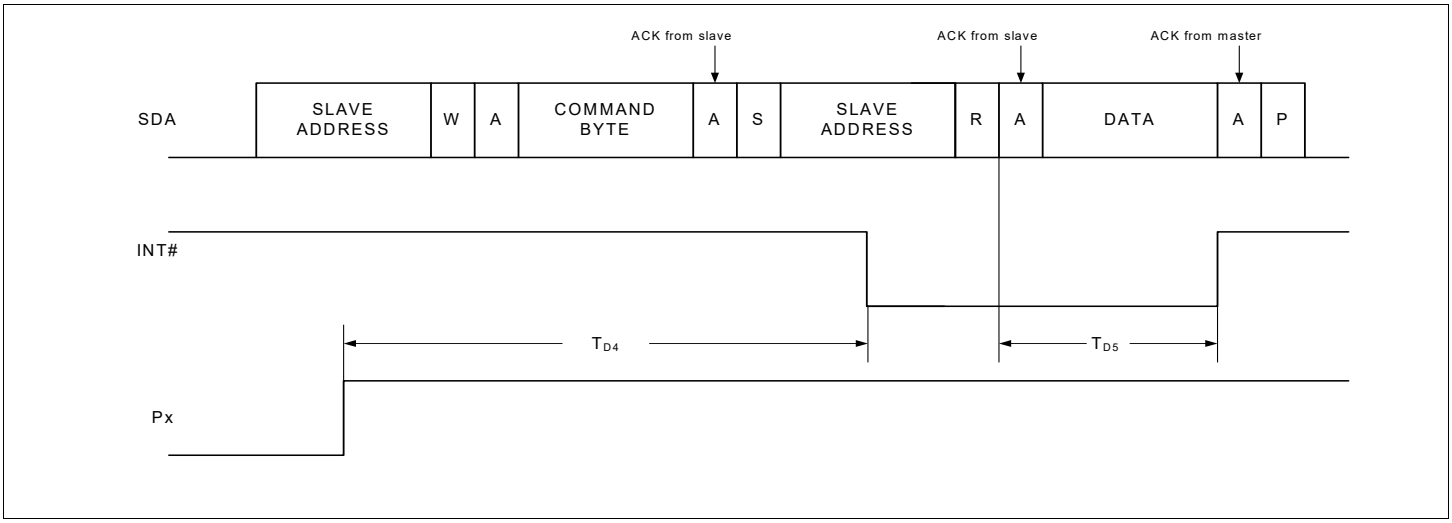


Figure 3: GPIO Pin Interrupt

Pin Configuration

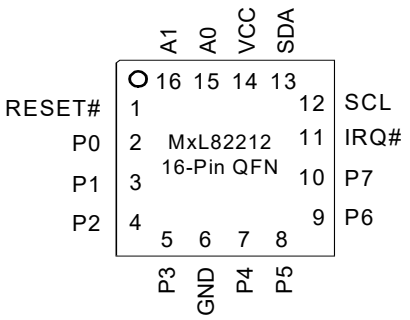


Figure 2: Pin Configuration (Top View)

Pin Description

Table 5: Pin Description

Name	QFN-16 Pin#	Type	Description
I²C Interface			
SDA	13	I/O	I²C-bus data input/output (open-drain).
SCL	12	I	I²C-bus serial input clock.
IRQ#	11	OD	Interrupt output (open-drain, active LOW).
A0 A1	15 16	I I	These pins select the I²C slave address. See Table 6 on page 8.
RESET#	1	I	Reset (active LOW) - A longer than 40ns LOW pulse on this pin resets the internal registers and all GPIOs is configured as inputs.
GPIOs			
P0 P1 P2 P3 P4 P5 P6 P7	2 3 4 5 7 8 9 10	I/O I/O I/O I/O I/O I/O I/O I/O	General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset. After power-up or reset, the internal pull-up resistors are enabled.
Ancillary Signals			
VCC	14	Pwr	1.62V to 5.5V VCC supply voltage.
GND	6	Pwr	Power supply common, ground.
GND	Center Pad	Pwr	The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential.

Note: Pin type: I = Input, O = Output, I/O = Input/Output, OD = Output Open Drain.

Block Diagram

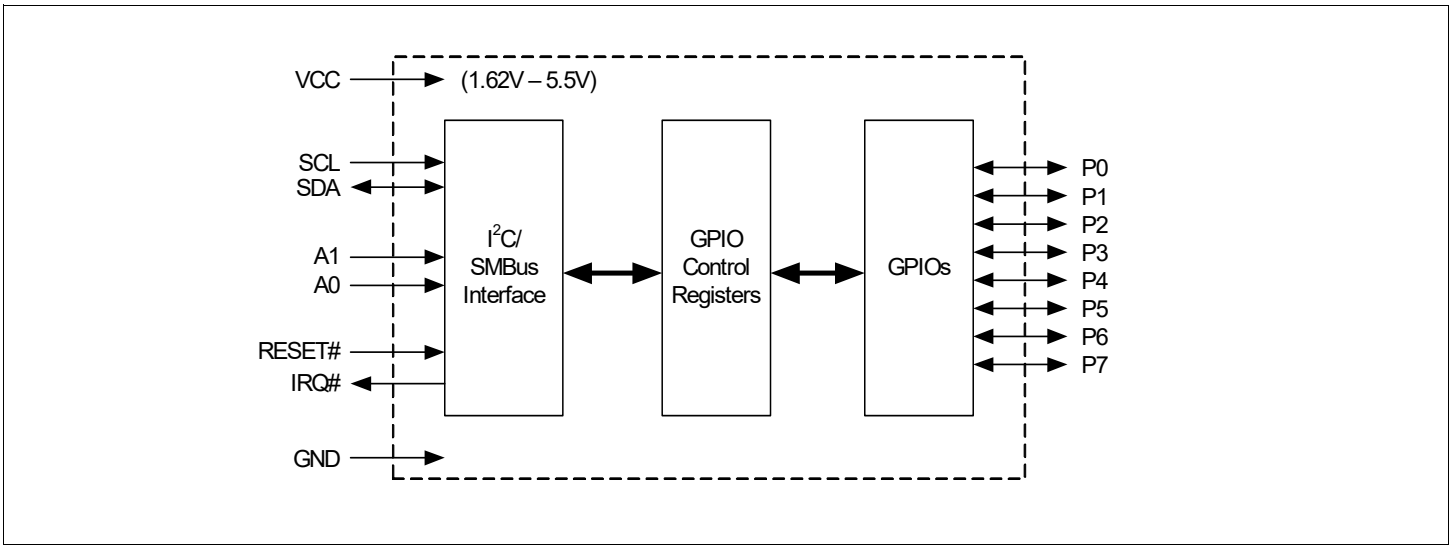


Figure 3: Functional Block Diagram

Functional Description

I²C-bus Interface

The I²C-bus interface is compliant with the standard-mode and fast-mode I2C-bus specifications. The I²C-bus interface consists of two lines: serial data (SDA) and serial clock (SCL). In the standard-mode, the serial clock and serial data can go up to 100kbps, in the fast-mode, the serial clock and serial data can go up to 400kbps, and the fast-mode plus can go up to 1MHz bps.

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The MxL82212 responds to each write with an acknowledge (SDA driven LOW by MxL82212 for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figure 4, Figure 5, and Figure 6. For complete details, see the I²C-bus specifications.

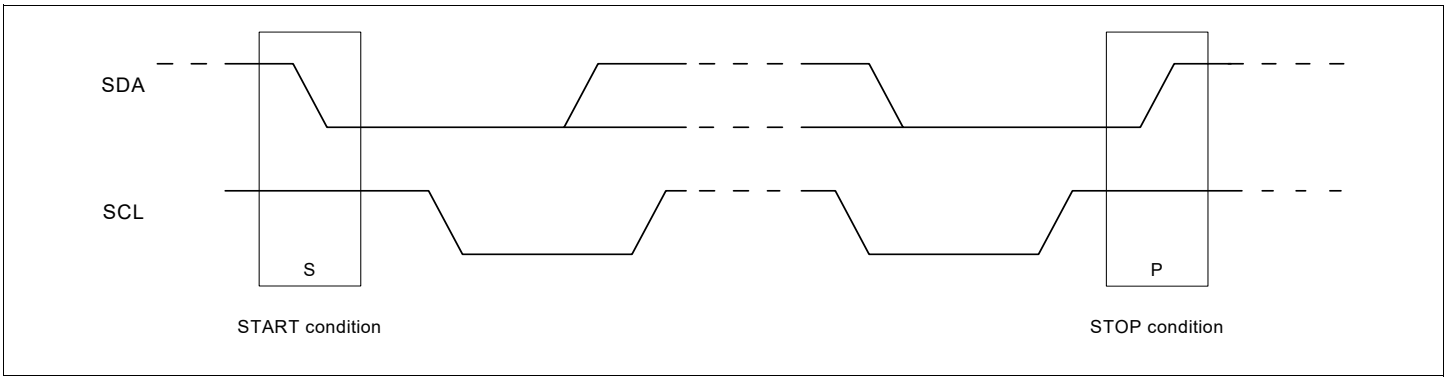


Figure 4: I²C Start and Stop Conditions

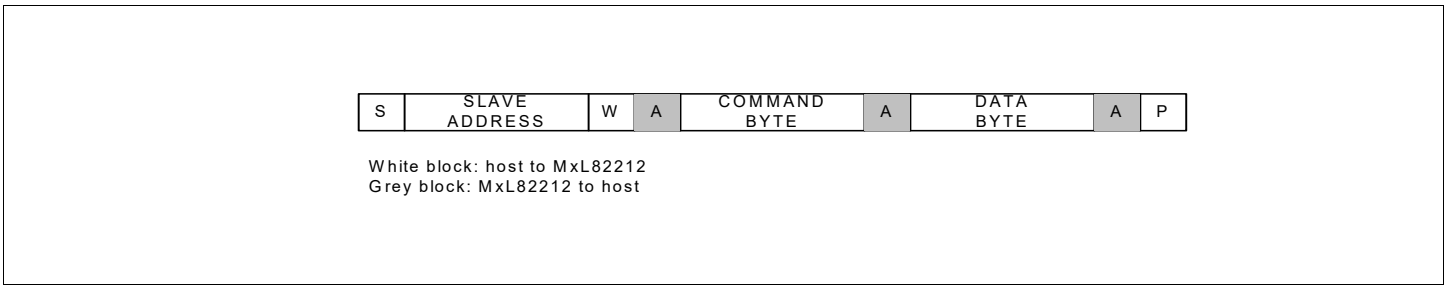


Figure 5: Master Writes To Slave

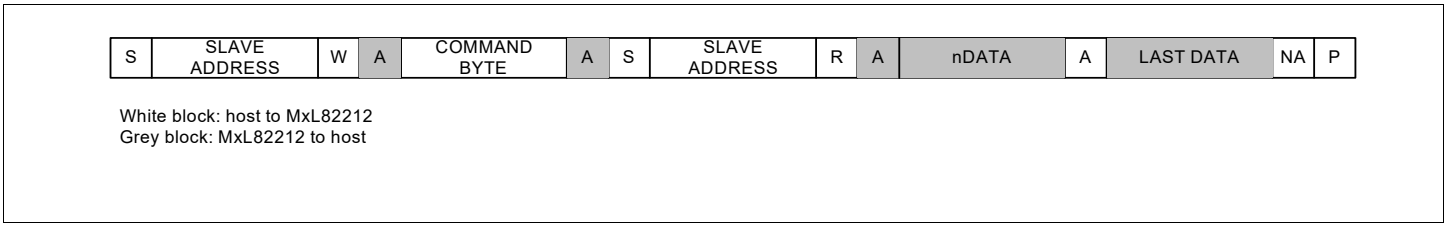


Figure 6: Master Reads From Slave

I²C-bus Addressing

There can be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the MxL82212 has up to 16 I²C slave addresses using the A1-A0 address lines. The following table lists the different addresses that can be selected.

Table 6: I²C Address Map

A1	A0	I²C Address
SCL	GND	0x20 (0010 000X)
SCL	VCC	0x22 (0010 001X)
SDA	GND	0x24 (0010 010X)
SDA	VCC	0x26 (0010 011X)
SCL	SCL	0x30 (0011 000X)
SCL	SDA	0x32 (0011 001X)
SDA	SCL	0x34 (0011 010X)
SDA	SDA	0x36 (0011 011X)
GND	GND	0x40 (0100 000X)
GND	VCC	0x42 (0100 001X)
VCC	GND	0x44 (0100 010X)
VCC	VCC	0x46 (0100 011X)
GND	SCL	0x50 (0101 000X)
GND	SDA	0x52 (0101 001X)
VCC	SCL	0x54 (0101 010X)
VCC	SDA	0x56 (0101 011X)

²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is ’0’, then it is a write transaction. If bit-0 is ’1’, then it is a read transaction.

I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that is accessed. The following table lists the command bytes for each register.

Table 7: I²C Command Byte (Register Address)

Command Byte	Register Name Description	Read/Write	Default Values
0x00	GSR - GPIO State	Read-Only	0xXX
0x01	OCR - Output Control	Read/Write	0xFF
0x02	PIR - Input Polarity Inversion	Read/Write	0x00
0x03	GCR - GPIO Configuration	Read/Write	0xFF
0x04	PUR - Input Internal Pull-up Resistor Enable/Disable	Read/Write	0xFF
0x05	IER - Input Interrupt Enable	Read/Write	0x00
0x06	TSCR - Output Three-State Control	Read/Write	0x00
0x07	ISR - Input Interrupt Status	Read	0x00
0x08	REIR - Input Rising Edge Interrupt Enable	Read/Write	0x00
0x09	FEIR - Input Falling Edge Interrupt Enable	Read/Write	0x00
0x0A	IFR - Input Filter Enable/Disable	Read/Write	0xFF

Interrupts

The following table lists the interrupt behavior of the different register settings for the MxL82212.

Table 8: Interrupt Generation and Clearing

GCR Bit	IER Bit	REIR Bit	FEIR Bit	IFR Bit	Interrupt Generated By:	Interrupt Cleared By:
1	0	X	X	X	No interrupts enabled (default).	N/A
1	1	0	0	0	A rising or falling edge on the input.	Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR)
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
1	1	1	0	0	A rising edge on the input.	Reading the GSR register
				1	A rising edge on the input and remains high for more than 1075ns.	
1	1	0	1	0	A falling edge on the input.	Reading the GSR register
				1	A falling edge on the input and remains low for more than 1075ns.	
1	1	1	1	0	A rising or falling edge on the input.	Reading the GSR register
				1	A rising or falling edge on the input and remains in the new state for more than 1075ns.	
0	x	x	x	x	No interrupts in output mode.	N/A

Register Description

GPIO State Register (GSR) - Read-Only

The status of P7 - P0 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register clears an input interrupt (for complete details, see Table 8 on page 9). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (that is. this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Control Register (OCR) - Read/Write

When P7 - P0 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Polarity Inversion Register (PIR) - Read/Write

When P7 - P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to ’1’, the value of this bit in the GSR Register is the inverted value of the input pin. If the corresponding bit in this register is set to ’0’, the value of this bit in the GSR Register is the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

GPIO Configuration Register (GCR) - Read/Write

This register configures the GPIOs as inputs or outputs. After power-up or after reset, the GPIOs are inputs. Setting these bits to ’0’ enables the GPIOs as outputs. Setting these bits to ’1’ enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Internal Pull-up Enable/Disable Register (PUR) - Read/Write

After power-up or after reset, the internal pull-up resistors are enabled for the MxL82212.Writing a ’0’ to these bits disable the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Enable Register (IER) - Read/Write

This register enables/disables the interrupts for an input. After power-up or after reset, the interrupts are disabled. Writing a ’1’ to these bits enable the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 8 on page 9. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Output Three-State Control Register (TSCR) - Read/Write

This register can enable/disable the three-state mode of an output. Writing a ’1’ to these bits enable the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Interrupt Status Register (ISR) - Read-Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 8 on page 9. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Rising Edge Interrupt Enable Register (REIR) - Read/Write

Writing a ’1’ to these bits enable the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 8 on page 9. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Falling Edge Interrupt Enable Register (FEIR) - Read/Write

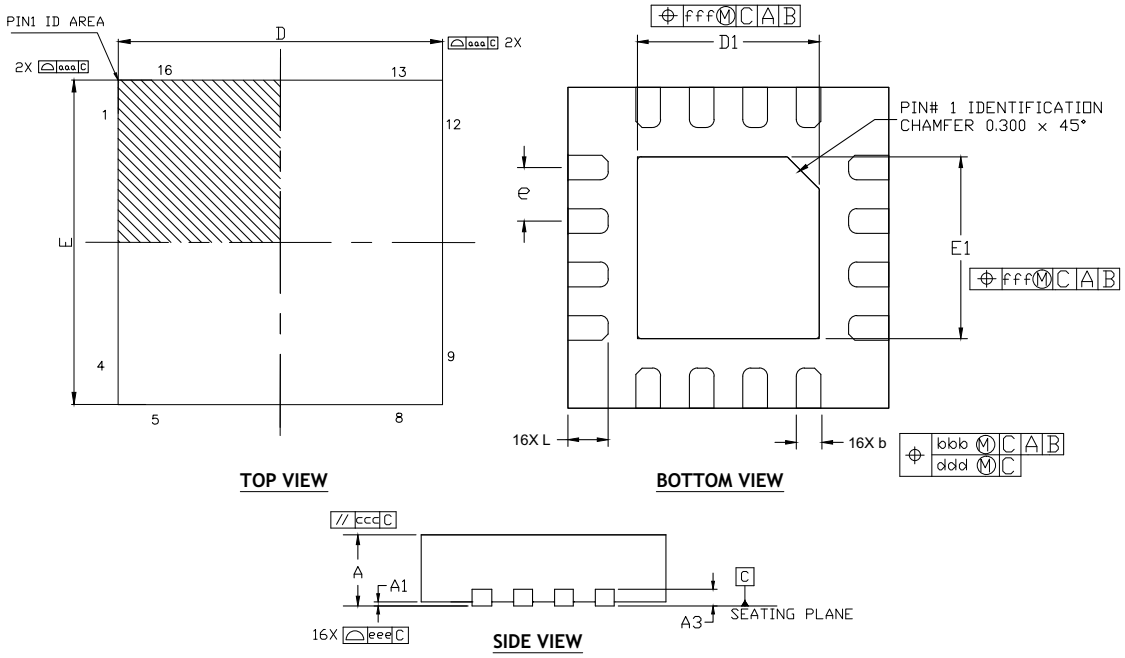
Writing a ’1’ to these bits enable the corresponding input to generate an interrupt on the falling edge. Writing a ’1’ to these bits make that input generate an interrupt on the rising edge only. For complete details of the interrupt behavior for various register settings, see Table 8 on page 9. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Input Filter Enable Register (IFR) - Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 225ns are filtered and do not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a ’0’ to these bits disable the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, see Table 8 on page 9. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

Mechanical Dimensions

16-Pin QFN



DIMENSION TABLE			
SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20Ref	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
D1	1.50	1.65	1.80
E1	1.50	1.65	1.80
L	0.20	0.30	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		16	

TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

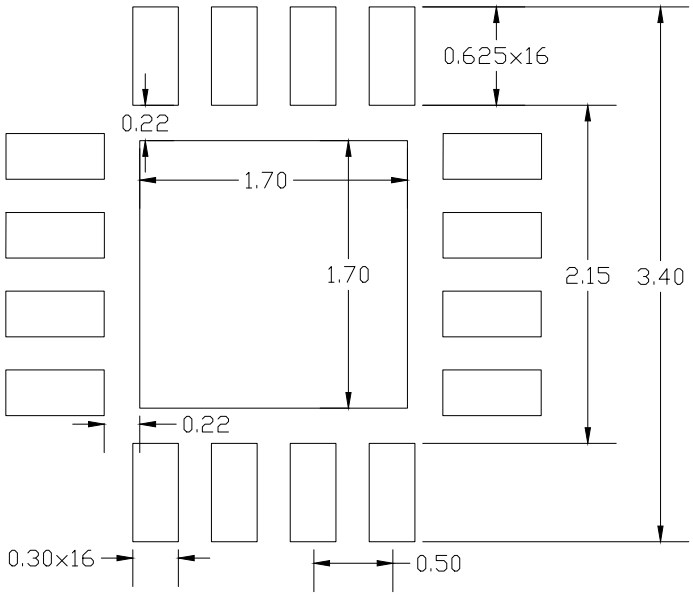
Drawing No.: POD-00000138

Revision: A

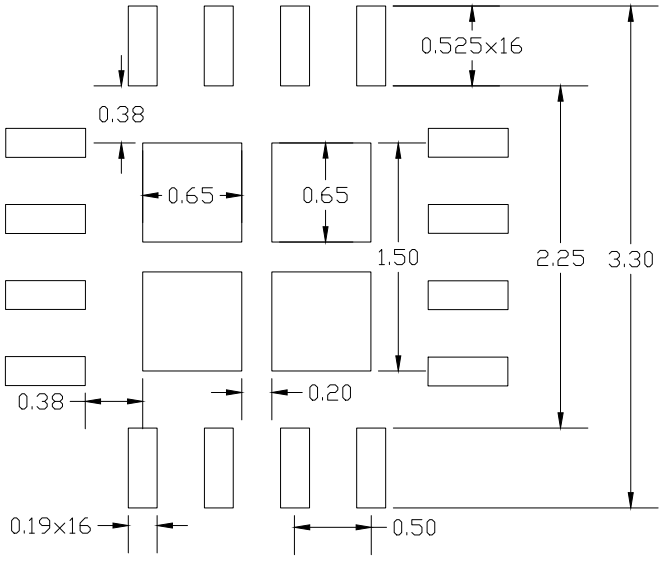
Figure 7: Mechanical Dimensions

Recommended Land Pattern and Stencil

16-Pin QFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000138

Revision: A

Figure 8: Recommended Land Pattern and Stencil

Ordering Information

Table 9: Ordering Information

Ordering Part Number	Package	Number of GPIOs	Operating Temperature Range	Packing Method
MXL82212I-AQB-R	QFN-16	8	–40°C to 85°C	Tape and Reel

MaxLinear, Inc.
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