# MxL82206

8-bit I²C/SMBUS GPIO Expander with Integrated Level Shifters
Data Sheet

## General Description

The MxL82206 is an 8-bit GPIO expander with an I²C/SMBus interface. After power-up, the MxL82206 has internal 100kΩ pull-up resistors on each I/O pin that can be individually enabled.

In addition, the GPIOs on the MxL82206 can individually be controlled and configured. As outputs, the GPIOs can be outputs that are high, low or in three-state mode. The three-state mode feature is useful for applications where the power is removed from the remote devices, but they may still be connected to the GPIO expander.

As inputs, the internal pull-up resistors can be enabled or disabled and the input polarity can be inverted. The interrupt behavior is configurable. It can be set to trigger on a rising edge, falling edge, or both edges. The interrupt condition is cleared either when the input returns to its original state or when the current input state is read.

The MxL82206 is an enhanced version of the TCA6408. The MxL82206 is pin and software compatible with the TCA6408.

The MxL82206 is available in a 3mm × 3mm 16-pin QFN as well as 5mm × 4.4mm 16-pin TSSOP packages.

## Applications

- Telecom, networking, and server platforms (BMC)
- GPIO expansion for embedded systems
- Industrial automation and robotics
- IoT and smart sensor devices
- System monitoring and control
- Power sequencing and control
- Human interface control (LEDs, keypads, switches)
- Test and measurement equipment
- Systems using GPIO-limited processors

## Features

- 1.62V to 5.5V operating voltage
- Integrated level shifters
- 8 General purpose I/Os (GPIOs)
- Maximum standby current of 1μA at +1.8V
- I²C/SMBus bus interface
  - I²C clock frequency up to 1MHz
  - Noise filter on SDA and SCL inputs
  - Up to 4 I²C Slave addresses
- Individually programmable inputs
  - Internal pull-up resistors
  - Polarity inversion
  - Individual interrupt enable
  - Rising edge and/or falling edge interrupt
  - Input filter
- Individually programmable outputs
  - Output level control
  - Output three-state control
- Open-drain active low interrupt output
- Active-low reset input
- Pin and software compatible with TCA6408
- 3kV HBM ESD protection per *JESD22-A114F*
- ±100mA latch-up performance per *JESD78B*

# Revision History

| Document No. | Release Date | Change Description |
|---|---|---|
| 303DSR01 | July 28, 2026 | Initial final release. |

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# Specifications

## Absolute Maximum Ratings

**Important:** The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard.

**Table 1: Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Power Supply Voltage | - | 6 | V |
| Supply Current | - | 160 | mA |
| Ground Current | - | 200 | mA |
| External Current limit of each GPIO | - | 25 | mA |
| Total Current limit for GPIO[7:0] | - | 100 | mA |
| Total Supply Current sourced by all GPIOs | - | 160 | mA |
| Operating Temperature | –40 | +85 | °C |
| Storage Temperature | –65 | +150 | °C |
| Power Dissipation | - | 200 | mW |

## Thermal Information

**Table 2: Thermal Information**

| Symbol | Thermal Metric | Typical | | Unit |
|---|---|---|---|---|
| | | QFN-16 | TSSOP-16 | |
| $\theta_{JC(top)}$ | Junction-to-Case Top Thermal Resistance | 97 | 56 | °C/W |
| $\theta_{JC(bottom)}$ | Junction-to-Case Bottom Thermal Resistance | 38 | 91 | |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | 47 | 91 | |
| $\theta_{JA}$ | Junction-to-Ambient Thermal Resistance | 69 | 111 | |
| $\Psi_{JT}$ | Junction-to-Case Top Thermal Characterization | 15 | 4 | |
| $\Psi_{JB}$ | Junction-to-Board Thermal Characterization | 44 | 83 | |

# Electrical Characteristics

## DC Electrical Characteristics

Unless otherwise noted, $T_A$ = –40° to +85°C, $V_{CC}$ is from 1.62V to 5.5V.

**Table 3: DC Electrical Characteristics**

| Symbol | Parameter | Limits 1.8V ± 10% Min | Limits 1.8V ± 10% Max | Limits 2.5V ± 10% Min | Limits 2.5V ± 10% Max | Limits 3.3V ± 10% Min | Limits 3.3V ± 10% Max | Limits 5V ± 10% Min | Limits 5V ± 10% Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | –0.3 | 0.3*VCC | –0.3 | 0.3*VCC | –0.3 | 0.3*VCC | –0.3 | 0.3*VCC | V | Note 1 |
| $V_{IL}$ | Input Low Voltage | –0.3 | 0.2 | –0.3 | 0.5 | –0.3 | 0.8 | –0.3 | 1.1 | V | Note 2 |
| $V_{IH}$ | Input High Voltage | 0.7*VCC | VCC | 0.7*VCC | VCC | 0.7*VCC | VCC | 0.7*VCC | VCC | V | Note 1 |
| $V_{IH}$ | Input High Voltage | 1.4 | 5.5 | 1.8 | 5.5 | 2.0 | 5.5 | 2.3 | 5.5 | V | Note 2 |
| $V_{OL}$ | Output Low Voltage | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | $I_{OL}$ = 3mA Note 3 |
| $V_{OL}$ | Output Low Voltage | 0 | 0.5 | 0 | 0.5 | 0 | 0.5 | 0 | 0.2 | V | $I_{OL}$ = 8mA Note 4 |
| $V_{OL}$ | Output Low Voltage | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | $I_{OL}$ = 1.5mA $I_{OL}$ = 4mA $I_{OL}$ = 6mA Note 5 |
| $V_{OH}$ | Output High Voltage | 1.2 | - | 1.8 | - | 2.6 | - | 4.1 | - | V | $I_{OH}$ = –8mA Note 4 |
| $I_{IL}$ | Input Low Leakage Current | - | ±10 | - | ±10 | - | ±10 | - | ±10 | µA | - |
| $I_{IH}$ | Input High Leakage Current | - | ±10 | - | ±10 | - | ±10 | - | ±10 | µA | - |
| $I_{CC}$ | Power Supply Current | - | 50 | - | 100 | - | 200 | - | 400 | µA | Note 6 |
| $I_{CC}$ | Power Supply Current | - | 150 | - | 250 | - | 500 | - | 1000 | µA | Note 7 |
| $I_{CCS}$ | Standby Current | - | 1 | - | 2 | - | 5 | - | 7 | µA | Note 8 |
| $C_{IN}$ | Input Pin Capacitance | - | 5 | - | 5 | - | 5 | - | 5 | pF | - |
| $R_{GPIO}$ | GPIO pull-up Resistance | 60 | 140 | 60 | 140 | 60 | 140 | 60 | 140 | kΩ | 100kΩ ±40% |
| $R_{RESET\#}$ | Pull-up Resistance | 35 | 85 | 35 | 85 | 35 | 85 | 35 | 85 | kΩ | 60kΩ ±40% |

1. For $I^2C$ input signals (SDA, SCL).

2. For GPIOs and A0 signals.

3. For $I^2C$ output signal SDA.

4. For GPIOs.

5. For IRQ# signal

6. Test 1: SCL frequency is 1MHz with internal pull-ups disabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

7. Test 2: SCL frequency is 1MHz with internal pull-ups enabled. All GPIOs are configured as inputs. All inputs are steady at VCC or GND. Outputs are floating or in the tri-state mode.

8. Test 3: All inputs are steady at VCC or GND to minimize standby current. If internal pull-up is enabled, input voltage level should be the same as VCC. All GPIOs are configured as inputs. SCL and SDA are at VCC. Outputs are left floating or in tri-state mode.

# AC Electrical Characteristics

Unless otherwise noted, $T_A$ = –40° to +85°C, $V_{CC}$ is from 1.62V to 5.5V.

**Table 4: AC Electrical Characteristics**

| Symbol | Parameter | Standard Mode $I^2C$-Bus | | Fast Mode $I^2C$-Bus | | Fast Mode Plus $I^2C$-Bus | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{SCL}$ | Operating Frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $T_{BUF}$ | Bus Free Time between STOP and START | 4.7 | - | 1.3 | - | 0.5 | - | µs |
| $T_{HD;STA}$ | START Condition Hold Time | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $T_{SU;STA}$ | START Condition Setup Time | 4.7 | - | 0.6 | - | 0.26 | - | µs |
| $T_{HD;DAT}$ | Data Hold Time | 0 | - | 0 | - | 0 | - | ns |
| $T_{VD;ACK}$ | Data Valid Acknowledge | - | 0.6 | - | 0.6 | - | 0.45 | µs |
| $T_{VD;DAT}$ | SCL LOW to Data Out Valid | - | 0.6 | - | 0.6 | - | 0.45 | µs |
| $T_{SU;DAT}$ | Data Setup time | 250 | - | 100 | - | 50 | - | ns |
| $T_{LOW}$ | Clock LOW Period | 4.7 | - | 1.3 | - | 0.5 | - | µs |
| $T_{HIGH}$ | Clock HIGH Period | 4.0 | - | 0.6 | - | 0.26 | - | µs |
| $T_F$ | Clock/Data Fall Time | - | 300 | - | 300 | - | 120 | ns |
| $T_R$ | Clock/Data Rise Time | - | 1000 | - | 300 | - | 120 | ns |
| $T_{SP}$ | Pulse width of Spikes Tolerance | - | 50 | - | 50 | - | 50 | ns |
| $T_{D1}$ | $I^2C$-bus GPIO Output Valid | - | 0.2 | - | 0.2 | - | 0.4 | µs |
| $T_{D4}$ | $I^2C$ Input Pin Interrupt Valid | - | 4 | - | 4 | - | 4 | µs |
| $T_{D5}$ | $I^2C$ Input Pin Interrupt Clear | - | 4 | - | 4 | - | 4 | µs |
| $T_{D15}$ | SCL Delay after Reset | 3 | - | 3 | - | 3 | - | µs |

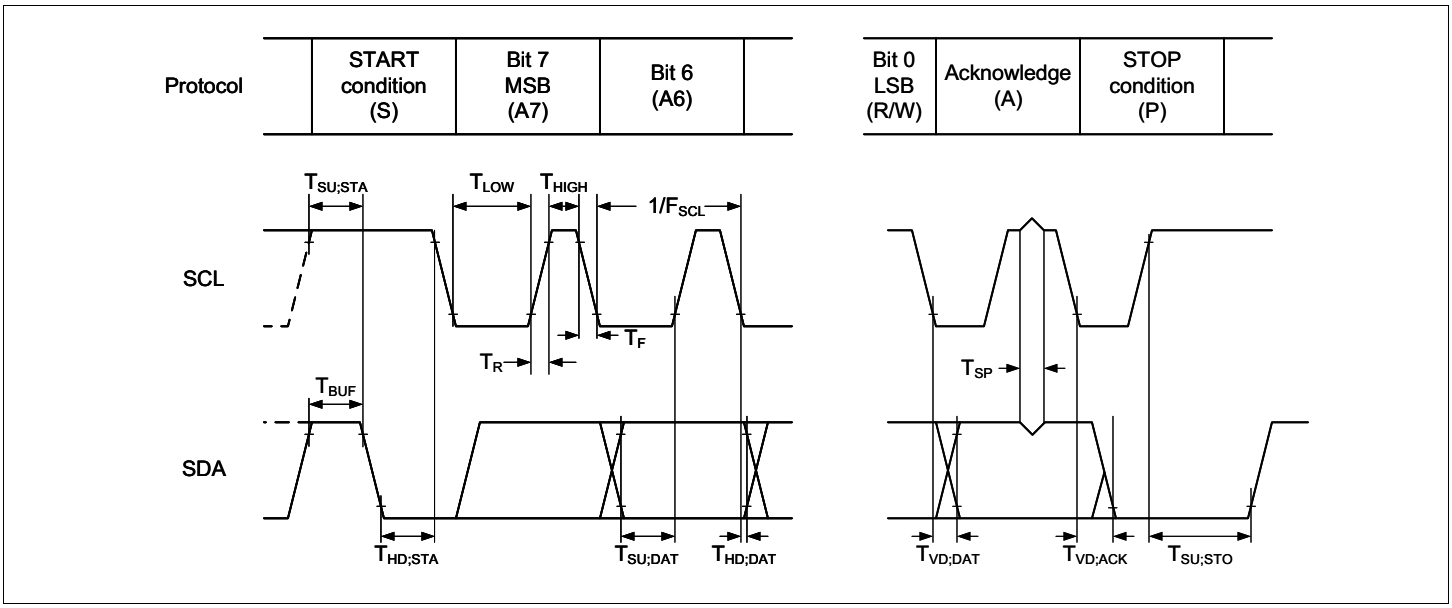



**Figure 1: I²C-Bus Timing Diagram**

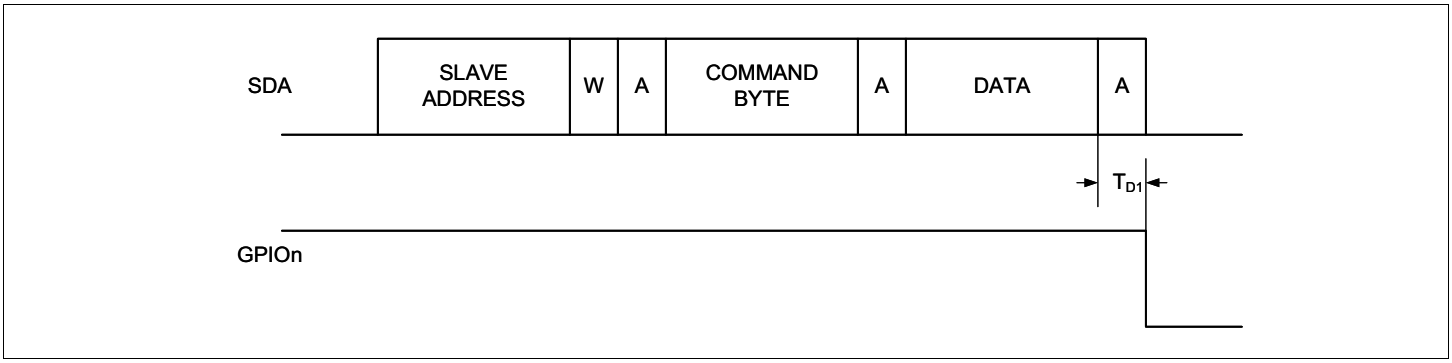



**Figure 2: Write To Output**

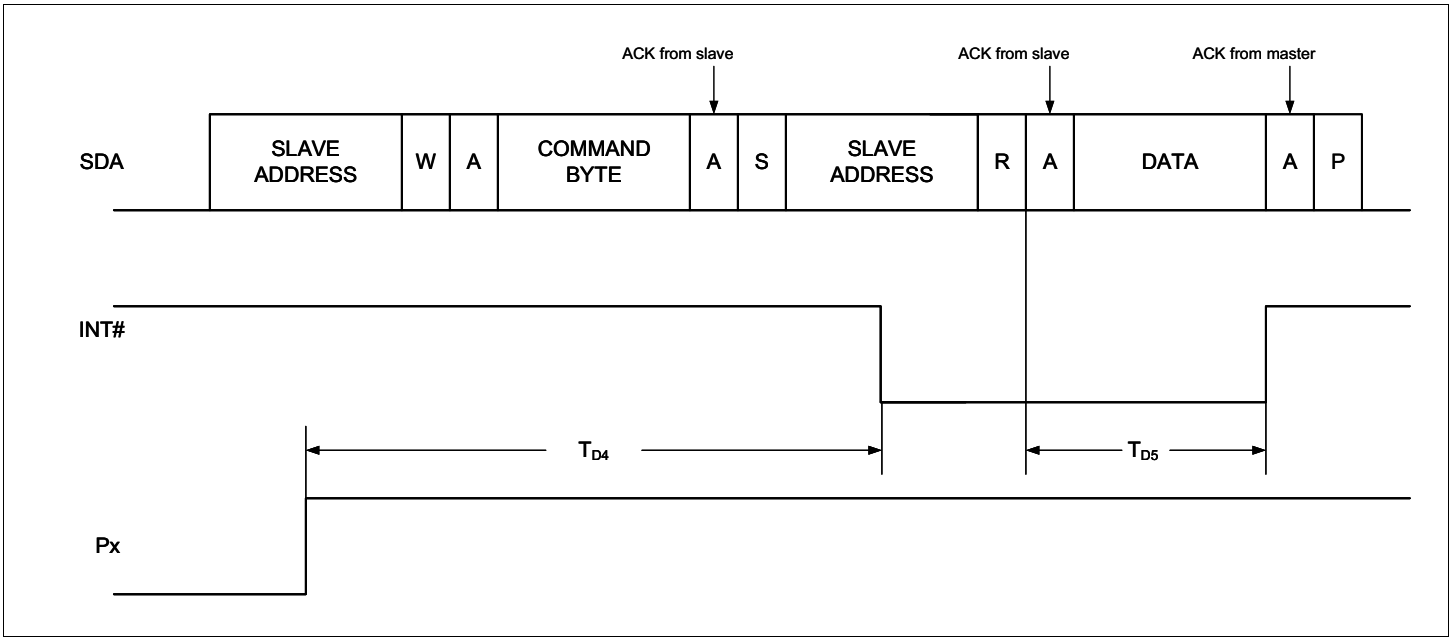



**Figure 3: GPIO Pin Interrupt**

# Pin Configuration

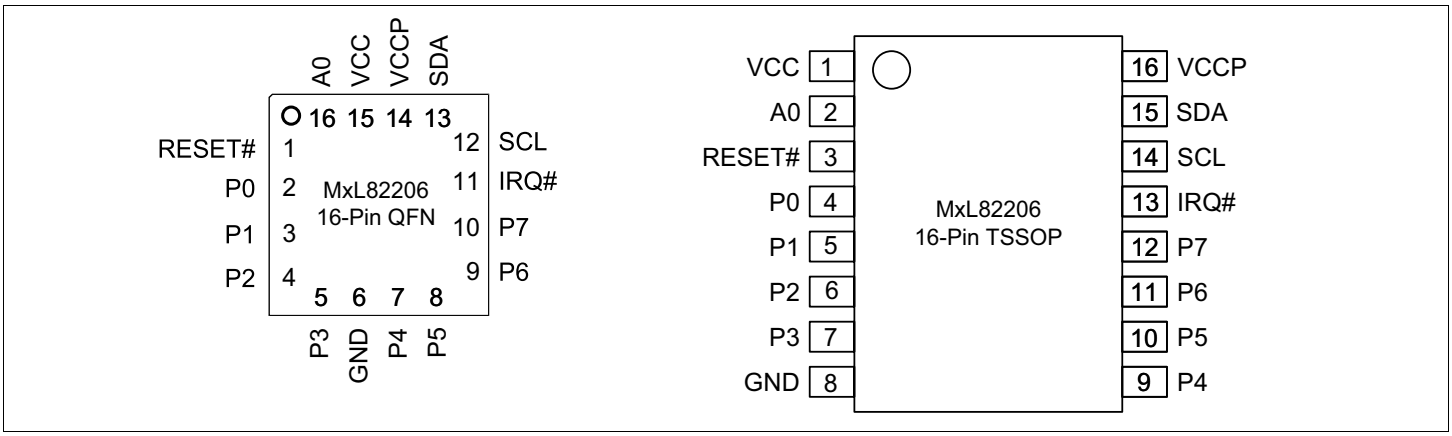



**Figure 4: Pin Configuration (Top View)**

## Pin Description

**Table 5: Pin Description**

| Name | QFN-16 Pin# | TSSOP-16 Pin# | Type | Description |
|---|---|---|---|---|
| **I²C Interface** | | | | |
| SDA | 13 | 15 | I/O | I²C-bus data input/output (open-drain). |
| SCL | 12 | 14 | I | I²C-bus serial input clock. |
| IRQ# | 11 | 13 | OD | Interrupt output (open-drain, active LOW). |
| A0 | 16 | 2 | I | These pins select the I²C slave address. See Table 6 on page 10. |
| RESET# | 1 | 3 | I | Reset (active LOW) - A longer than 40ns LOW pulse on this pin resets the internal registers and all GPIOs are configured as inputs. |
| **GPIOs** | | | | |
| P0 | 2 | 4 | I/O | General purpose I/Os P0-P7. All GPIOs are configured as inputs upon power-up or after a reset. |
| P1 | 3 | 5 | I/O | |
| P2 | 4 | 6 | I/O | |
| P3 | 5 | 7 | I/O | |
| P4 | 7 | 9 | I/O | |
| P5 | 8 | 10 | I/O | |
| P6 | 9 | 11 | I/O | |
| P7 | 10 | 12 | I/O | |
| **Ancillary Signals** | | | | |
| VCCP | 14 | 16 | Pwr | 1.62V to 5.5V VCC supply voltage. |
| VCC | 15 | 1 | Pwr | 1.62V to 5.5V VCC supply voltage for I²C-bus interface |
| GND | 6 | 8 | Pwr | Power supply common, ground. |

**Table 5: Pin Description (Continued)**

| Name | QFN-16 Pin# | TSSOP-16 Pin# | Type | Description |
|---|---|---|---|---|
| GND | Center Pad | - | Pwr | The exposed pad at the bottom surface of the package is designed for thermal performance. Use of a center pad on the PCB is strongly recommended for thermal conductivity as well as to provide mechanical stability of the package on the PCB. The center pad is recommended to be solder masked defined with opening size less than or equal to the exposed thermal pad on the package bottom to prevent solder bridging to the outer leads of the device. Thermal vias must be connected to GND plane as the thermal pad of package is at GND potential. |

**Note:** Pin type: I = Input, O = Output, I/O = Input/Output, OD = Output Open Drain.

# Block Diagram

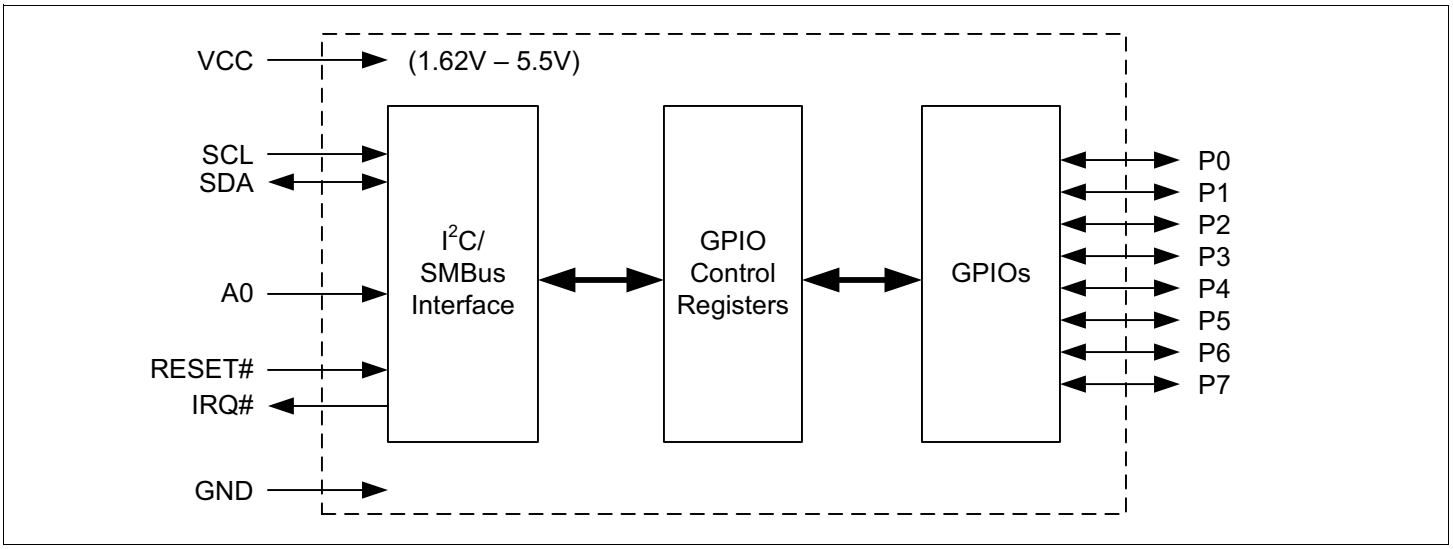



**Figure 5: Functional Block Diagram**

# Functional Description

## I²C-Bus Interface

The I2C-bus interface complies with the standard-, fast-, and fast mode plus specifications. It uses two lines: serial data (SDA) and serial clock (SCL). In standard mode, both signals operate up to 100kHz, while fast mode supports speeds up to 400kHz and fast mode plus extends operation up to 1MHz (1000kHz).

The first byte sent by an I²C-bus master contains a start bit (SDA transition from HIGH to LOW when SCL is HIGH), 7-bit slave address and whether it is a read or write transaction. The next byte is the sub-address that contains the address of the register to access. The MxL82206 responds to each write with an acknowledge (SDA driven LOW by MxL82206 for one clock cycle when SCL is HIGH). The last byte sent by an I²C-bus master contains a stop bit (SDA transition from LOW to HIGH when SCL is HIGH). See Figure 6, Figure 7, and Figure 8. For complete details, see the I²C-bus specifications.

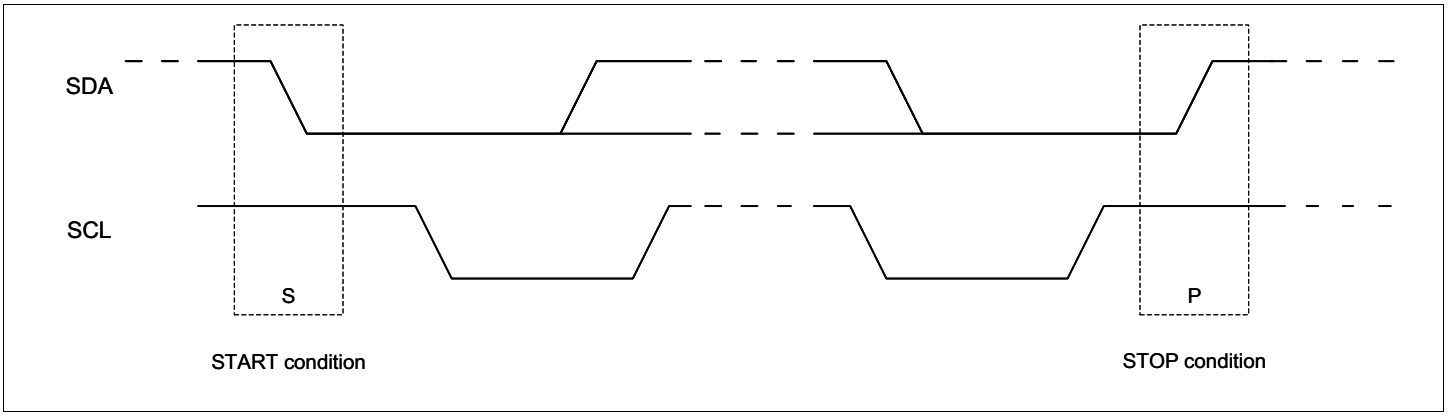



**Figure 6: I²C Start and Stop Conditions**

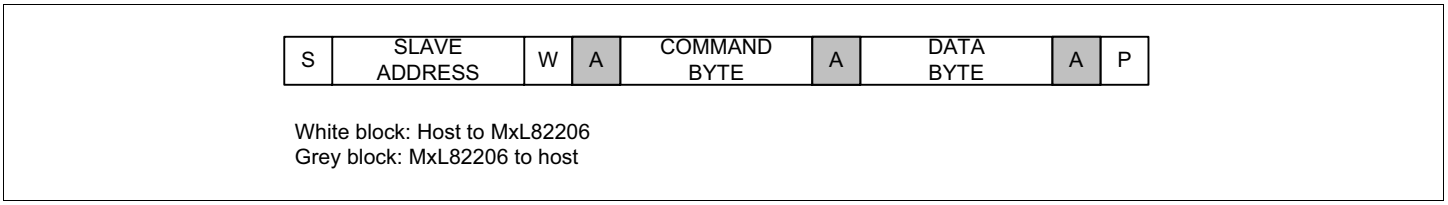



**Figure 7: Master Writes To Slave**

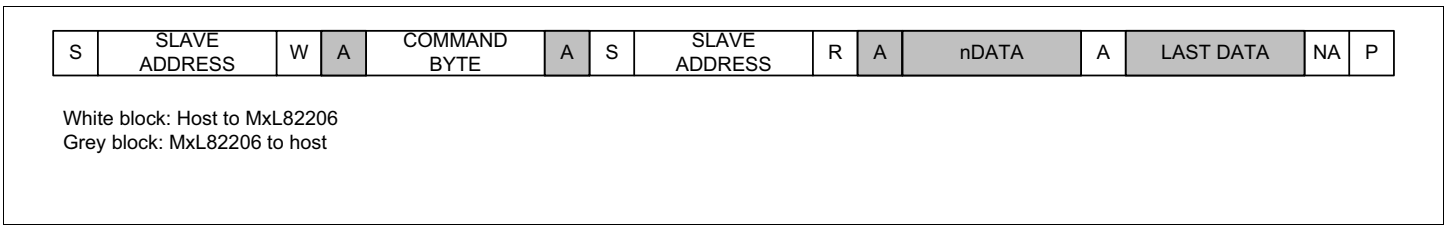



**Figure 8: Master Reads From Slave**

# I²C-Bus Addressing

There can be many devices on the I²C-bus. To distinguish itself from the other devices on the I²C-bus, the MxL82206 has up to 4 I²C slave addresses using the A0 address line. The following table lists the different addresses that can be selected.

**Table 6: I²C Address Map**

| A1 | I²C Address |
|---|---|
| GND | 0x40 (0100 000X) |
| VCC | 0x42 (0100 001X) |
| SCL | 0x50 (0101 000X) |
| SDA | 0x52 (0101 001X) |

# I²C Read and Write

A read or write transaction is determined by bit-0 of the slave address. If bit-0 is ’0’, then it is a write transaction. If bit-0 is ’1’, then it is a read transaction.

# I²C Command Byte

An I²C command byte is sent by the I²C master following the slave address. The command byte indicates the address offset of the register that is accessed. The following table lists the command bytes for each register.

**Table 7: I²C Command Byte (Register Address)**

| Command Byte | Register Name Description | Read/Write | Default Values |
|---|---|---|---|
| 0x00 | GSR–GPIO State | Read-Only | 0xXX |
| 0x01 | OCR–Output Control | Read/Write | 0xFF |
| 0x02 | PIR–Input Polarity Inversion | Read/Write | 0x00 |
| 0x03 | GCR–GPIO Configuration | Read/Write | 0xFF |
| 0x04 | PUR–Input Internal Pull-up Resistor Enable/Disable | Read/Write | 0x00 |
| 0x05 | IER–Input Interrupt Enable | Read/Write | 0x00 |
| 0x06 | TSCR–Output Three-State Control | Read/Write | 0x00 |
| 0x07 | ISR–Input Interrupt Status | Read | 0x00 |
| 0x08 | REIR–Input Rising Edge Interrupt Enable | Read/Write | 0x00 |
| 0x09 | FEIR–Input Falling Edge Interrupt Enable | Read/Write | 0x00 |
| 0x0A | IFR–Input Filter Enable/Disable | Read/Write | 0xFF |

# Interrupts

The following table lists the interrupt behavior of the different register settings for the MxL82206 device.

**Table 8: Interrupt Generation and Clearing**

| GCR Bit | IER Bit | REIR Bit | FEIR Bit | IFR Bit | Interrupt Generated By: | Interrupt Cleared By: |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | X | No interrupts enabled (default). | N/A |
| 1 | 1 | 0 | 0 | 0 | A rising or falling edge on the input. | Reading the GSR register or if the input changes back to its previous state (state of input during last read to GSR) |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns. | |
| 1 | 1 | 1 | 0 | 0 | A rising edge on the input. | Reading the GSR register |
| | | | | 1 | A rising edge on the input and remains high for more than 1075ns. | |
| 1 | 1 | 0 | 1 | 0 | A falling edge on the input. | Reading the GSR register |
| | | | | 1 | A falling edge on the input and remains low for more than 1075ns. | |
| 1 | 1 | 1 | 1 | 0 | A rising or falling edge on the input. | Reading the GSR register |
| | | | | 1 | A rising or falling edge on the input and remains in the new state for more than 1075ns. | |
| 0 | x | x | x | x | No interrupts in output mode. | N/A |

# Register Description

## GPIO State Register (GSR)—Read-Only

The status of P7–P0 can be read via this register. A read shows the current state of these pins (or the inverted state of these pins if enabled via the PIR Register). Reading this register clears an input interrupt (for complete details, see Table 8 on page 11). Reading this register also returns the last value written to the OCR register for any pins that are configured as outputs (note that this is not the same as the state of the actual output pin since the output pin can be in three-state mode). A write to this register has no effect. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Output Control Register (OCR)—Read/Write

When P7–P0 are defined as outputs, they can be controlled by writing to this register. Reading this register returns the last value written to it, however, this value may not be the actual state of the output pin since these pins can be in three-state mode. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Polarity Inversion Register (PIR)—Read/Write

When P7–P0 are defined as inputs, this register inverts the polarity of the input value read from the Input Port Register. If the corresponding bit in this register is set to *1*, the value of this bit in the GSR Register is the inverted value of the input pin. If the corresponding bit in this register is set to *0*, the value of this bit in the GSR Register is the actual value of the input pin. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## GPIO Configuration Register (GCR)—Read/Write

This register configures the GPIOs as inputs or outputs. After power-up or after reset, the GPIOs are inputs. Setting these bits to *0* enables the GPIOs as outputs. Setting these bits to *1* enable the GPIOs as inputs. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Internal Pull-up Enable/Disable Register (PUR)—Read/Write

This register enables/disables the internal pull-up resistors for an input. After power-up and reset, the internal pull-up resistors are disabled for the MxL82206. Writing a *1* to these bits enables the internal pull-up resistors. Writing a *0* to these bits disables the internal pull-up resistors. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Interrupt Enable Register (IER)—Read/Write

This register enables/disables the interrupts for an input. After power-up or after reset, the interrupts are disabled. Writing a *1* to these bits enables the interrupt for the corresponding input pins. For complete details of the interrupt behavior for various register settings, see Table 8 on page 11. No interrupts are generated for outputs when GCR bit is 0. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Output Three-State Control Register (TSCR)—Read/Write

This register can enable/disable the three-state mode of an output. Writing a *1* to these bits enables the three-state mode for the corresponding output pins. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Interrupt Status Register (ISR)—Read–Only

This register reports the input pins that have generated an interrupt. For complete details of the interrupt behavior for various register settings, see Table 8 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Rising Edge Interrupt Enable Register (REIR)—Read/Write

Writing a *1* to these bits enables the corresponding input to generate an interrupt on the rising edge. For complete details of the interrupt behavior for various register settings, see Table 8 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Falling Edge Interrupt Enable Register (FEIR)—Read/Write

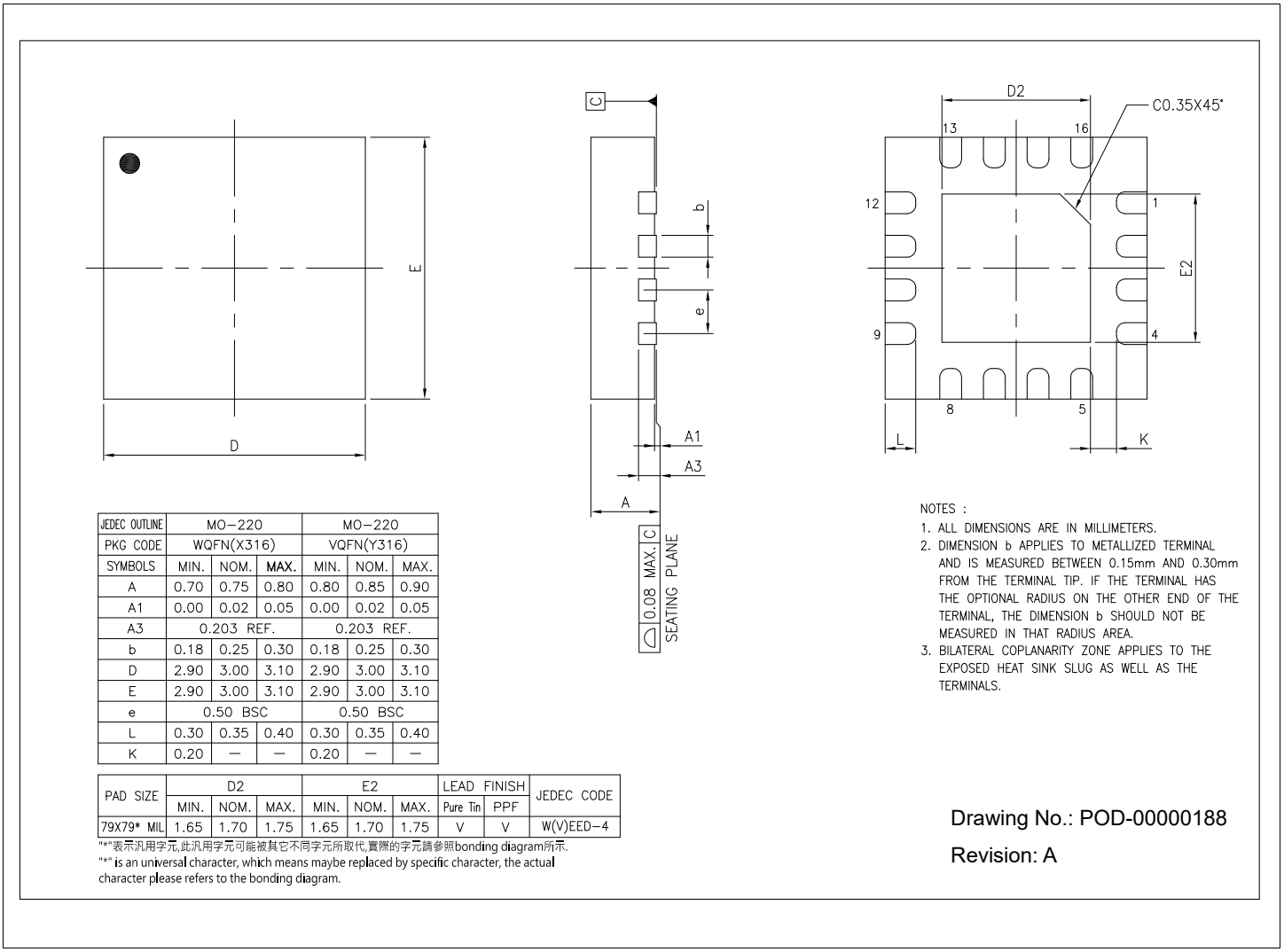
Writing a *1* to these bits disables the level-sensitive interrupt logic and enables the falling edge interrupt logic if the corresponding GPIO pin is configured as an input For complete details of the interrupt behavior for various register settings, see Table 8 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

## Input Filter Enable Register (IFR)—Read/Write

By default, the input filters are enabled (IFR = 0xFF). When the input filters are enabled, any pulse that is greater than 1075ns generates an interrupt (if enabled). Pulses that are less than 190ns are filtered and do not generate an interrupt. Pulses in between this range may or may not generate an interrupt. Writing a *0* to these bits disables the input filter for the corresponding inputs. With the input filters disabled, any change on the inputs generates an interrupt (if enabled). For complete details of the interrupt behavior for various register settings, see Table 8 on page 11. The MSB of this register corresponds with P7 and the LSB of this register corresponds with P0.

# Mechanical Dimensions

## 16-Pin QFN




| JEDEC OUTLINE | MO-220 | | | MO-220 | | |
|---|---|---|---|---|---|---|
| PKG CODE | WQFN(X316) | | | VQFN(Y316) | | |
| SYMBOLS | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | | 0.203 REF. | | |
| b | 0.18 | 0.25 | 0.30 | 0.18 | 0.25 | 0.30 |
| D | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC | | | 0.50 BSC | | |
| L | 0.30 | 0.35 | 0.40 | 0.30 | 0.35 | 0.40 |
| K | 0.20 | — | — | 0.20 | — | — |

| PAD SIZE | D2 | | | E2 | | | LEAD FINISH | | JEDEC CODE |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | Pure Tin | PPF | |
| 79X79* MIL | 1.65 | 1.70 | 1.75 | 1.65 | 1.70 | 1.75 | V | V | W(V)EED-4 |

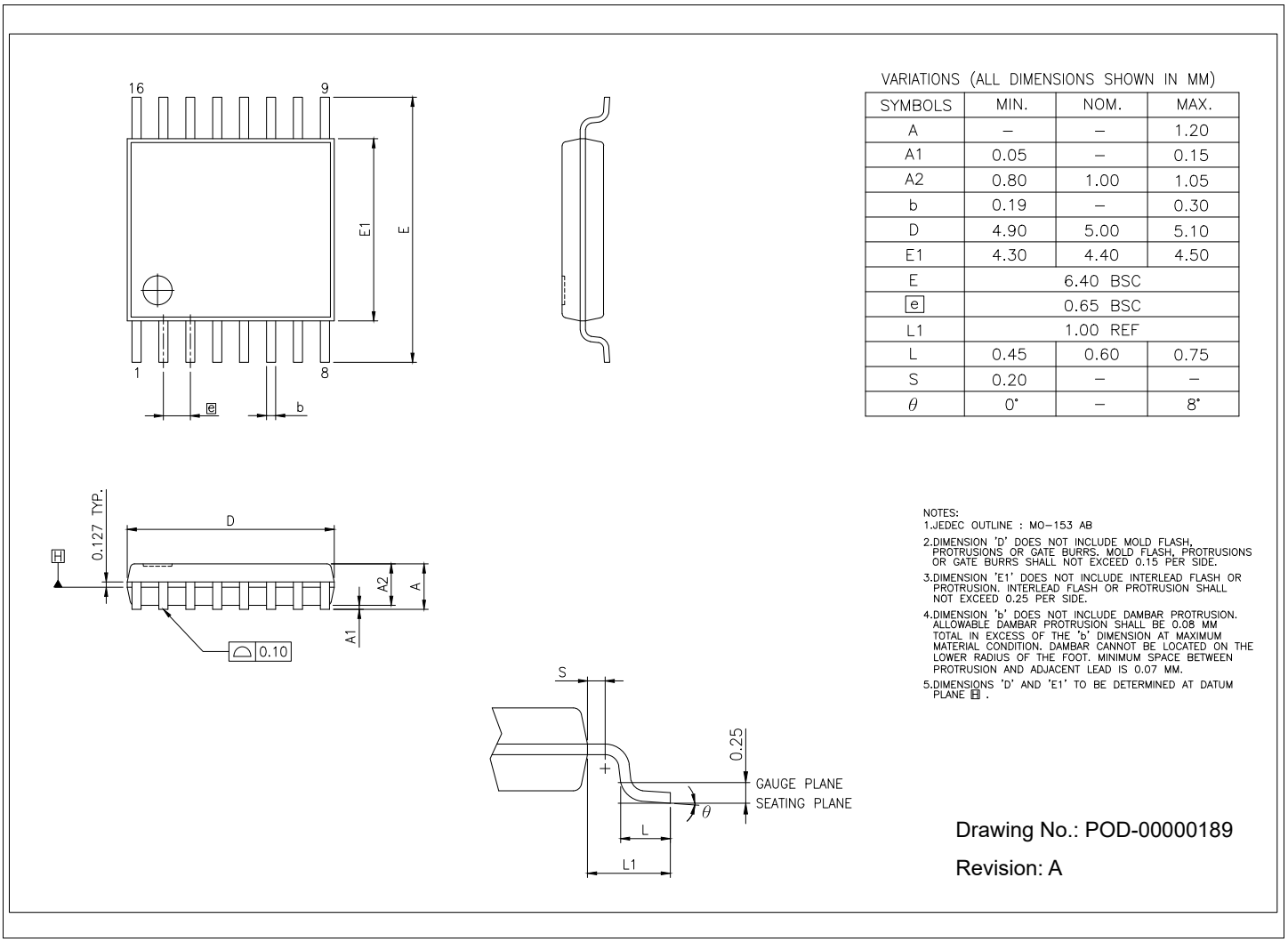
"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Drawing No.: POD-00000188
Revision: A

**Figure 9: QFN-16 Mechanical Dimensions**

# 16-Pin TSSOP




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| b | 0.19 | – | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |

NOTES:
1. JEDEC OUTLINE : MO-153 AB
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS "D" AND "E1" TO BE DETERMINED AT DATUM PLANE H .

Drawing No.: POD-00000189

Revision: A

**Figure 10: TSSOP-16 Mechanical Dimensions**

# Ordering Information

**Table 9: Ordering Information**

| Ordering Part Number | Package | Number of GPIOs | Operating Temperature Range | Packing Method | Lead-Free |
|---|---|---|---|---|---|
| MXL82206I-AGA-R | TSSOP-16 | 8 | –40°C to 85°C | Tape and Reel | Yes |
| MXL82206I-AQB-R | QFN-16 | 8 | –40°C to 85°C | Tape and Reel | Yes |
| MXL82206I-AQB-EVK-1 | MxL82206 Evaluation Kit | | | | |

**Note:**

- For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL82206.
- For more information about the EVK, refer to the *MxL82206 and MxL82207 User Manual* (045UM00).

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