MxL81434

Hi-Speed USB Bridge with 4 UARTs
Data Sheet

General Description

The MxL81434 is a hi-speed USB 2.0 compound device with an embedded hub and six downstream USB functions: four UARTs, a multi-master-capable I^2C controller, and an enhanced dedicated GPIO entity (EDGE) controller.

The upstream USB interface has an integrated USB 2.0 PHY and device controller that is compliant with both hi-speed (480Mbps) and full-speed (12Mbps) USB 2.0. The Vendor ID, Product ID, power mode, remote wake-up support, and maximum power consumption are amongst the values that can be programmed using the on-chip one-time programmable (OTP) memory.

The enhanced UARTs have a maximum data rate of 15Mbps. Using a fractional baud rate generator, any baud rate between 300bps and 15Mbps can be accurately generated. In addition, the UARTs have a large 1024-byte Tx FIFO and Rx FIFO to optimize the overall data throughput for various applications. The automatic RS-485 control feature simplifies both the hardware and software for half-duplex RS-485 applications. If required, the multidrop (9-bit) mode feature further simplifies typical multidrop applications by enabling/disabling the UART receiver depending on the address byte received.

The multi-master-capable I^2C controller and EDGE controller (up to 32 GPIOs) can be accessed via the USB HID interface. The EDGE pins or I^2C interface can be used for controlling and monitoring other peripherals. Up to two EDGE pins can be configured as PWM generators.

Features

- Hi-Speed (480Mbps) and Full-Speed (12Mbps) USB 2.0-compliant interface
- Enhanced UART
- I^2C multi-master
- Enhanced Dedicated GPIO Entity (EDGE)
- Single 5.0V power supply input
- Regulated 3.3V output power
- Single 25MHz crystal
- ±15kV HBM ESD protection on USB data pins
- ±8kV HBM ESD protection on all other pins
- USB CDC-ACM and HID-compliant
- Custom software drivers
- Available in 8.0mm × 8.0mm QFN-56 package

Applications

- UARTs
- POS terminals
- Test instrumentation
- Factory automation and process controls
- Industrial applications

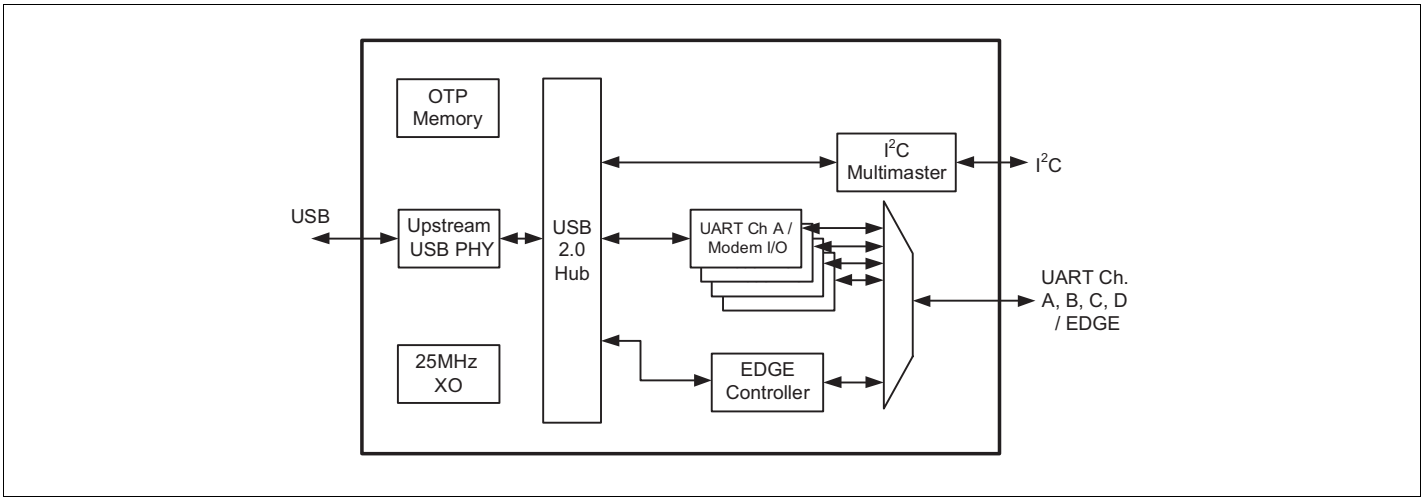


Figure 1: Block Diagram

Extended Features

- USB 2.0-compliant interface
  - Integrated USB 2.0 PHY
  - Supports 480Mbps USB Hi-Speed and 12Mbps USB Full-Speed data rate
  - Supports USB suspend, resume, and remote wake-up operations
  - Compatible with USB CDC-ACM
- Enhanced UART features
  - Data rates up to 15Mbps
  - Fractional baud rate generator
  - 1024-byte Tx and Rx FIFOs
  - 7, 8, or 9 data bits, 1 or 2 stop bits
  - Automatic hardware flow control
  - Automatic software flow control
  - Multidrop (9-bit) mode
  - Auto RS-485 half-duplex control
- I^2C multi-master
  - Up to 400kbps transfers
  - Multi-master capable
- Enhanced Dedicated GPIO Entity (EDGE)
  - Parallel GPIO access
  - Two PWM generators
- Custom software drivers
  - Windows
  - Linux
  - macOS

Revision History

Document No.	Release Date	Change Description
318DSR01	October 26, 2026	Initial final release.

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Specifications

Absolute Maximum Ratings

Important: The stresses above what is listed under the following table may cause permanent damage to the device. This is a stress rating only—functional operation of the device above what is listed under the following table or any other conditions beyond what MaxLinear recommends is not implied. Exposure to conditions above the recommended extended periods of time may affect device reliability. Solder reflow profile is specified in the *IPC/JEDEC J-STD-020C* standard. The thermal resistance profile is based on the *JEDEC EIA/JESD51-(2A, 8, 29)* standards.

Table 1: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{CC} Supply Voltage	-	5.75	V
Input Voltage (All Pins except SCL, SDA, USBD+, and USBD-)	–0.3	4.0	V
Input Voltage (USBD+ and USBD-)	–0.3	5.75	V
Input Voltage (SCL and SDA)	–0.3	6.0	V
Junction Temperature	-	125	°C

ESD Ratings

Table 2: ESD Ratings

Parameter	Limit	Units
HBM—Human Body Model (USBD+, USBD–)	±15	kV
HBM—Human Body Model (All other pins)	±8	kV

Thermal Specifications

Table 3: Thermal Specifications[1]

Symbol	Thermal Metric	Typical	Unit
		QFN-56	
$\theta_{JC(top)}$	Junction-to-Case Thermal Top Resistance	24	
θ_{JA}	Junction-to-Ambient Resistance	33	**°C/W**
θ_{JB}	Junction-to-Board Resistance	21	
Ψ_{JT}	Junction-to-Case Thermal Top Characterization	0.9	
Ψ_{JB}	Junction-to-Board Thermal Characterization	21	

1. Thermal parameters are determined using a 2s2p *JEDEC* PCB with thermal vias.

Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Operating Temperature Range	–40	-	85	°C
V_{CC} Supply Voltage	4.4	-	5.25	V

Electrical Characteristics

Unless otherwise noted, T_A = –40°C to 85°C, V_{CC} = 4.4V to 5.25V.

Table 5: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Consumption						
I_{CC}	Operating Current	No load on GPIO pins or 3V3_OUT	-	46	-	mA
I_{SUSP}	Suspend Mode Current	No load on GPIO pins or 3V3_OUT	-	1	-	mA
UART, VBUS_SENSE, LOW_PWR#, and EDGE Pins						
V_{IL}	Input Low Voltage	-	–0.3	-	0.8	V
V_{IH}	Input High Voltage	-	2.0	-	3.6	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	-	-	0.3	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.2	-	-	V
I_{IL}	Input Low Leakage Current	-	-	-	±10	µA
I_{IH}	Input High Leakage Current	-	-	-	±10	µA
C_{IN}	Input Pin Capacitance	-	-	-	5	pF
USB I/O Pins						
V_{OL}	Output Low Voltage	Full-Speed USB. External 15kΩ to GND on USBD+ and USBD- pins	0	-	0.3	V
V_{OH}	Output High Voltage	Full-Speed USB. External 15kΩ to GND on USBD+ and USBD- pins	2.8	-	3.6	V
V_{OL}	Output Low Voltage	Hi-Speed USB. External 45Ω to GND on USBD+ and USBD- pins	–300	-	300	mV
V_{OH}	Output High Voltage	Hi-Speed USB. External 45Ω to GND on USBD+ and USBD- pins	360	-	440	mV
V_{DrvZ}	Driver Output Impedance	-	-	45	-	Ω
I_{OSC}	Output Short Circuit Current	1.5V on USBD+ and USBD- pins	-	-	52	mA
3.3V Regulated Power Output						
V_{OUT}	Output Voltage	Maximum load current = 50mA	3.0	3.3	3.6	V

Pin Configuration

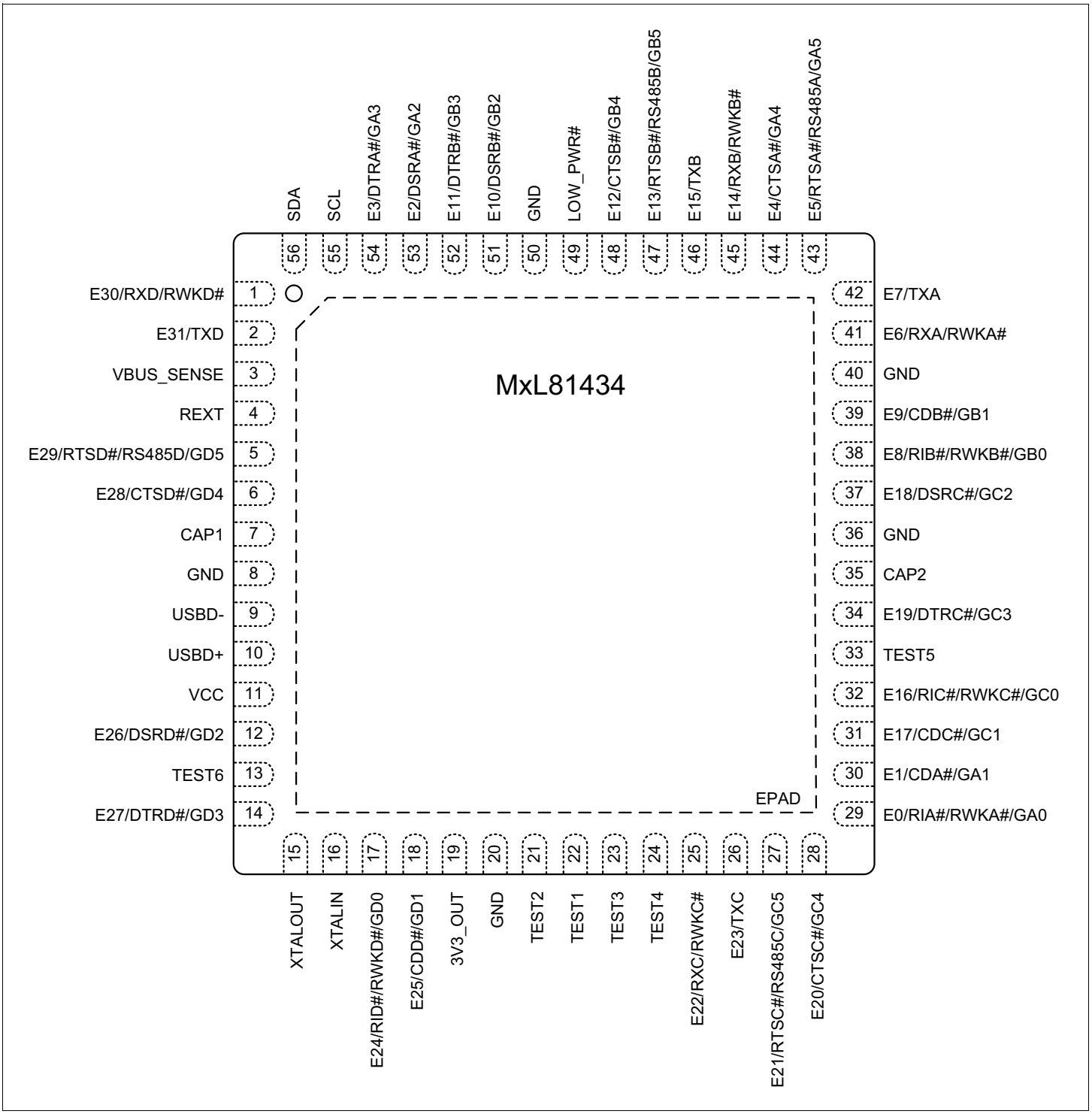


Figure 2: Pin Configuration (Top View)

Pin Description

Table 6: Pin Description

Pin No.	Pin Name	Type	Description
1	E30/RXD/RWKD#	I/O	Enhanced general-purpose I/O, or UART channel D Rx data, or remote wake-up. Defaults to UART Rx data.
2	E31/TXD	I/O	Enhanced general-purpose I/O, or UART channel D Tx data. Defaults to UART Tx data.
3	VBUS_SENSE	I	VBUS Sense input. In self-powered mode, the VBUS from the USB connector needs to be connected to this pin through a voltage divider circuit (VBUS = 5V, VBUS_SENSE = 3.3V input) using large resistance values to minimize power. It should also be decoupled by a 0.1µF capacitor. This feature may be enabled via the OTP whenever the hub function is configured for self-powered mode. The VBUS_SENSE input is used to disable the pull-up resistor on the USBD+ signal when VBUS is not present. In bus-powered mode, this pin is ignored.
4	REXT	I	Connect externally using short trace to 226Ω 1% resistor to ground.
5	E29/RTSD#/RS485D/ GD5	I/O	Enhanced general-purpose I/O, or UART channel D Request to Send, or channel D auto-RS-485 half-duplex enable, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See “Automatic RTS/CTS Hardware Flow Control” on page 13 or “Automatic RS-485 Half-Duplex Control” on page 15.
6	E28/CTSD#/GD4	I/O	Enhanced general-purpose I/O, or UART channel D Clear to Send, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See “Automatic RTS/CTS Hardware Flow Control” on page 13.
7	CAP1	I	Connect externally to CAP2 and 3V3_OUT using short trace.
8	GND	PWR	Power supply common, ground.
9	USBD–	I/O	USB port differential data negative.
10	USBD+	I/O	USB port differential data positive.
11	VCC	PWR	5.0V power supply input.
12	E26/DSRD#/GD2	I/O	Enhanced general-purpose I/O, or UART channel D Data Set Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
13	TEST6	O	Test pin (internal purpose)—NC.
14	E27/DTRD#/GD3	I/O	Enhanced general-purpose I/O, or UART channel D Data Terminal Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
15	XTALOUT	O	Crystal or buffered clock output.
16	XTALIN	I	25MHz ±50ppm crystal or external clock input.
17	E24/RID#/RWKD#/ GD0	I/O	Enhanced general-purpose I/O, or UART channel D Ring Indicator, or remote wake-up, or general-purpose I/O. Defaults to UART GPIO input. See “Remote Wake-up” on page 9.
18	E25/CDD#/GD1	I/O	Enhanced general-purpose I/O, or UART channel D Carrier Detect, or general-purpose I/O. Defaults to UART GPIO input.
19	3V3_OUT	PWR	3.3V output power. Connect externally to CAP1 and CAP2 using short trace and decouple with minimum of 4.7µF capacitor.
20	GND	PWR	Power supply common, ground.
21	TEST2	O	Test pin (internal purpose)—NC.
22	TEST1	O	Test pin (internal purpose)—NC.
23	TEST3	I	Test pin (internal purpose)—NC.
24	TEST4	I	Test pin (internal purpose)—NC.
25	E22/RXC/RWKC#	I/O	Enhanced general-purpose I/O, or UART channel C Rx data, or remote wake-up. Defaults to UART Rx data.

Table 6: Pin Description (Continued)

Pin No.	Pin Name	Type	Description
26	E23/TXC	I/O	Enhanced general-purpose I/O, or UART channel C Tx data. Defaults to UART Tx data.
27	E21/RTSC#/RS485C/ GC5	I/O	Enhanced general-purpose I/O, or UART channel C Request to Send, or channel C auto-RS-485 half-duplex enable, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See "Automatic RTS/CTS Hardware Flow Control" on page 13 or "Automatic RS-485 Half-Duplex Control" on page 15.
28	E20/CTSC#/GC4	I/O	Enhanced general-purpose I/O, or UART channel C Clear to Send, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See "Automatic RTS/CTS Hardware Flow Control" on page 13.
29	E0/RIA#/RWKA#/GA0	I/O	Enhanced general-purpose I/O, or UART channel A Ring Indicator, or remote wake-up, or general-purpose I/O. Defaults to UART GPIO input. See "Remote Wake-up" on page 9.
30	E1/CDA#/GA1	I/O	Enhanced general-purpose I/O, or UART channel A Carrier Detect, or general-purpose I/O. Defaults to UART GPIO input.
31	E17/CDC#/GC1	I/O	Enhanced general-purpose I/O, or UART channel C Carrier Detect, or general-purpose I/O. Defaults to UART GPIO input.
32	E16/RIC#/RWKC#/ GC0	I/O	Enhanced general-purpose I/O, or UART channel C Ring Indicator, or remote wake-up, or general-purpose I/O. Defaults to UART GPIO input. See "Remote Wake-up" on page 9.
33	TEST5	O	Test pin (internal purpose)—NC.
34	E19/DTRC#/GC3	I/O	Enhanced general-purpose I/O, or UART channel C Data Terminal Ready, or general-purpose I/O. Defaults to UART GPIO input. See "Automatic DTR/DSR Hardware Flow Control" on page 14.
35	CAP2	I	Connect externally to CAP1 and 3V3_OUT using short trace.
36	GND	PWR	Power supply common, ground.
37	E18/DSRC#/GC2	I/O	Enhanced general-purpose I/O, or UART channel C Data Set Ready, or general-purpose I/O. Defaults to UART GPIO input. See "Automatic DTR/DSR Hardware Flow Control" on page 14.
38	E8/RIB#/RWKB#/GB0	I/O	Enhanced general-purpose I/O, or UART channel B Ring Indicator, or remote wake-up, or general-purpose I/O. Defaults to UART GPIO input. See "Remote Wake-up" on page 9.
39	E9/CDB#/GB1	I/O	Enhanced general-purpose I/O, or UART channel B Carrier Detect, or general-purpose I/O. Defaults to UART GPIO input.
40	GND	PWR	Power supply common, ground.
41	E6/RXA/RWKA#	I/O	Enhanced general-purpose I/O, or UART channel A Rx data, or remote wake-up. Defaults to UART Rx data.
42	E7/TXA	I/O	Enhanced general-purpose I/O, or UART channel A Tx data. Defaults to UART Tx data.
43	E5/RTSA#/RS485A/ GA5	I/O	Enhanced general-purpose I/O, or UART channel A Request to Send, or channel A auto-RS-485 half-duplex enable, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See "Automatic RTS/CTS Hardware Flow Control" on page 13 or "Automatic RS-485 Half-Duplex Control" on page 15.
44	E4/CTSA#/GA4	I/O	Enhanced general-purpose I/O, or UART channel A Clear to Send, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See "Automatic RTS/CTS Hardware Flow Control" on page 13.
45	E14/RXB/RWKB#	I/O	Enhanced general-purpose I/O, or UART channel B Rx data, or remote wake-up. Defaults to UART Rx data.
46	E15/TXB	I/O	Enhanced general-purpose I/O, or UART channel B Tx data. Defaults to UART Tx data.
47	E13/RTSB#/RS485B/ GB5	I/O	Enhanced general-purpose I/O, or UART channel B Request to Send, or channel B auto-RS485 half-duplex enable, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See "Automatic RTS/CTS Hardware Flow Control" on page 13 or "Automatic RS-485 Half-Duplex Control" on page 15.

Table 6: Pin Description (Continued)

Pin No.	Pin Name	Type	Description
48	E12/CTSB#/GB4	I/O	Enhanced general-purpose I/O, or UART channel B Clear to Send, or general-purpose I/O. Defaults to UART GPIO input except when MxL81434 is used with CDC-ACM driver. See “Automatic RTS/CTS Hardware Flow Control” on page 13.
49	LOW_PWR#	O	The LOW_PWR# pin is asserted whenever it is not safe to draw the amount of current requested from VBUS in the Device Maximum Power field of the Configuration Descriptor. The LOW_PWR# pin is asserted when the MxL81434 is in suspend mode or when it is not yet configured. The LOW_PWR# pin is de-asserted whenever it is safe to draw the amount of current requested in the Device Maximum Power field. Note that the MxL81434 device is a high-power device. The default polarity of the LOW_PWR# output pin is active low and is programmable via the OTP.
50	GND	PWR	Power supply common, ground
51	E10/DSRB#/GB2	I/O	Enhanced general-purpose I/O, or UART channel B Data Set Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
52	E11/DTRB#/GB3	I/O	Enhanced general-purpose I/O, or UART channel B Data Terminal Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
53	E2/DSRA#/GA2	I/O	Enhanced general-purpose I/O, or UART channel A Data Set Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
54	E3/DTRA#/GA3	I/O	Enhanced general-purpose I/O, or UART channel A Data Terminal Ready, or general-purpose I/O. Defaults to UART GPIO input. See “Automatic DTR/DSR Hardware Flow Control” on page 14.
55	SCL	I/O OD	I^2C master controller serial clock (open-drain). External pull-up resistor required on this pin.
56	SDA	I/O OD	I^2C master controller data (open-drain). External pull-up resistor required on this pin.
	EPAD	PWR	Must be connected to ground.

Note: Type: I = Input, O = Output, I/O = Input/Output, OD = Open-Drain.

Block Diagram

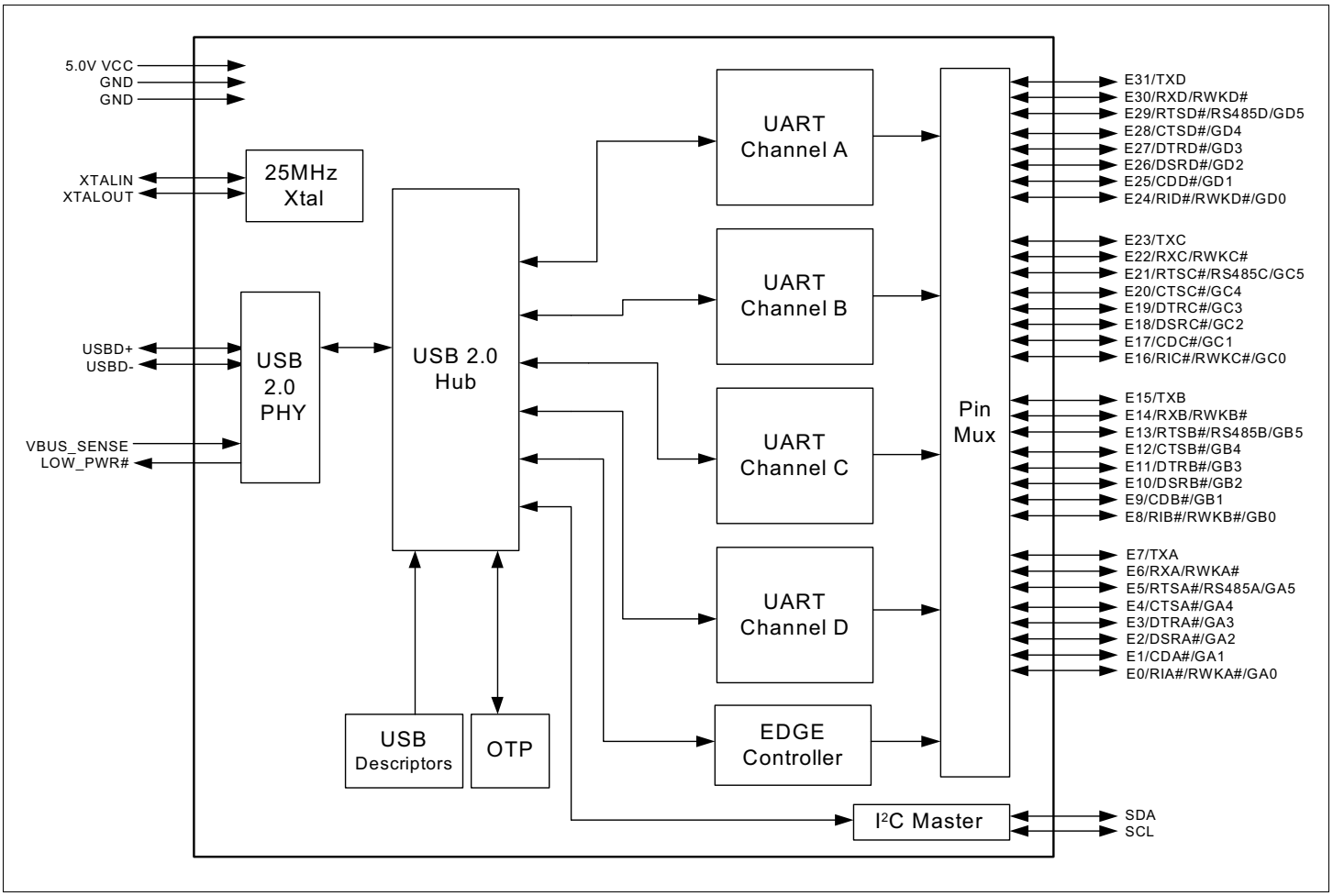


Figure 3: Functional Block Diagram

Functional Description

USB Interface

The MxL81434 is a USB compound device with an embedded hub and six downstream functions. The downstream functions of the MxL81434 are four UART functions, an I^2C function, and an enhanced dedicated GPIO entity (EDGE) function. The upstream USB interface of the MxL81434 is compliant with both USB 2.0 full-speed and hi-speed specifications.

The MxL81434 has a single Vendor ID and vendor string. Each function in the MxL81434 has an individual product string and serial string. The serial strings for multiple functions within the same device differ only by a single character which is assigned a value between 0 and 7. All string and ID values can be overridden via OTP.

The MxL81434 can be placed into a low power or suspended state by the USB host. By default, the MxL81434 hub is configured for bus-powered mode with a maximum power of 250mA. All other functions in the MxL81434 are configured for self-powered mode.

Each function of the MxL81434 supports one configuration and utilizes the following USB endpoints:

- USB hub
  - Control endpoint
  - Interrupt-in endpoint
- I^2C function
  - Control endpoint
  - Interrupt-in and interrupt-out endpoints
- EDGE controller function
  - Control endpoint
  - Interrupt-in and interrupt-out endpoints
- UART function
  - Control endpoint
  - Interrupt-in endpoint
  - Bulk-in and bulk-out endpoints

USB Vendor ID

MaxLinear's USB Vendor ID is 0x04E2 and is the default Vendor ID that is used for the MxL81434. You can obtain your own Vendor ID from USB.org. The MxL81434 OTP can then be modified to report this Vendor ID in the USB descriptors.

USB Product ID

Each function in the MxL81434 has an individual USB Product ID. Table 7 lists the default Product IDs for each of the functions. These values can be modified by programming the OTP. If you use your own Vendor ID, you can also select your own Product IDs. Additionally, upon request MaxLinear provides a selection of different Product IDs for use with MaxLinear's Vendor ID for the cases that do not wish to become members of USB.org. However, MaxLinear recommends to use your own Product ID.

Table 7: Default MxL81434 Product IDs

MxL81434 Function	Default Product ID
Hub	0x0804
UART Channel A	0x1400
UART Channel B	0x1401
UART Channel C	0x1402
UART Channel D	0x1403
I^2C	0x1100
EDGE	0x1200

USB Suspend

All USB peripheral devices must support the USB suspend mode. Per USB standard, the MxL81434 device begins to enter the suspend state if it does not detect any activity on its USB data lines, including Start-of-Frame (SOF) packets, for 3ms. The peripheral device must then reduce power consumption from VBUS power within the next 7ms to the allowed limit of 2.5mA for the suspended state. Because the MxL81434 is a compound device with seven functions, the suspend state power limit is 17.5mA for the device. In this context, the *device* is all circuitry, including the MxL81434, that draws power from the host VBUS.

Remote Wake-up

When the MxL81434 is suspended, the E0/RIA#/RWKA#/GA0, E8/RIB#/RWKB#/GB0, E16/RIC#/RWKC#/GC0, or the E24/RID#/RWKD#/GD0 pins can be used to request that the host exit the suspend state if configured as an input. A high-to-low transition on any of these pins may be used to signal a remote wake-up request to the host via MaxLinear's custom driver. However, because the four pins are internally logically ANDed, a logic *0* on any of the four inputs prevents the resume signaling. Note that the CDC-ACM driver does not support the remote wake-up feature. The E0/RIA#/RWKA#/GA0, E8/RIB#/RWKB#/GB0, E16/RIC#/RWKC#/GC0, or the E24/RID#/RWKD#/GD0 pins can be used to signal remote wake-up by default. Additionally, the E6/RXA/RWKA#, E14/RXB/RWKB#, E22/RXC/RWKC#, or E30/RXD/RWKD# pins, if configured as inputs, may also be used for remote wake-up if enabled using the `REMOTE_WAKEUP` register.

USB Strings

USB specifies three character string descriptors that are provided to the USB host during enumeration in string descriptors:

- Manufacturer string
- Product string
- Serial string

In a compound device such as the MxL81434, each function provides these strings to the USB host.

The default manufacturer string for the MxL81434 device is "Exar Corp.". Table 8 lists the default product strings for the hub, UART functions, I^2C function, and EDGE function. The serial number string is a unique alphanumeric ASCII string programmed into the device at the factory.

Table 8: Default MxL81434 Product Strings

MxL81434 Function	Default Product String
Hub	Exar's XR22804 Hub
UARTs	Exar USB UART
I^2C	Exar USB I^2C
EDGE	Exar USB Edge

The OTP may be used to override these strings. However, to ensure unique serial numbers for each device, MaxLinear recommends using the factory pre-programmed serial number string and not overwriting it via OTP.

USB Device Drivers

Each of the functions in the MxL81434 requires a USB device driver for operation. Both the I^2C and EDGE functions conform to the HID device class and as such, utilize the embedded HID driver that is native to each operating system. The embedded hub also uses the native hub driver.

The UART function can be used with either a class-specific CDC-ACM driver or a custom driver. When the CDC-ACM driver is used, the driver has no ability to read or write the MxL81434 device registers. Because of this, the MxL81434 device is initialized to the settings listed in Table 9. With a custom driver, all GPIOs default in hardware to inputs but these settings can be modified by a custom driver.

Table 9: MxL81434 Register Defaults with CDC-ACM Driver

Register	Value	Notes
FLOW_CONTROL	0x001	Hardware flow control.
GPIO_MODE	0x001	RTS/CTS flow control.
GPIO_DIRECTION	0x008	E3/DTRA#/GA3, E11/DTRB#/GB3, E19/DTRC#/GC3, and E27/DTRD#/GD3 are configured as outputs. All other GPIOs as inputs.
GPIO_INT_MASK	0x030	E[n]/RI#/RWK#/G[n], E[n]/CD#/G[n], and E[n]/DSR#/G[n] for all UART channels are interrupt sensitive, that is, can cause a USB interrupt to be generated.

These default settings can be overridden by programming the OTP.

If a custom driver is used, the CUSTOM_DRIVER Active bit should be immediately set to *1* by the USB UART driver. Once the CUSTOM_DRIVER Active bit is set, the custom driver can use standard CDC-ACM commands without configuring the device to the default register settings used with the CDC-ACM driver. Any changes to the register settings for the GPIOs and flow control specifically need to be configured by the driver/application software. Although there is no ability to read/write registers when using the CDC-ACM driver, basic UART functions, including setting baud rate, character format, and sending line break, are supported by the CDC driver. See the four CDC_ACM_IF USB control commands listed in Table 10 on page 17.

UART

The UART can be configured via USB control transfers from the USB host. The UART transmitter and receiver are described separately in the following sections.

At power-up, the MxL81434 defaults to 9600bps, 8 data bits, no parity bit, 1 stop bit, and no flow control. If a native CDC-ACM driver accesses the MxL81434, defaults change. See "USB Device Drivers" and Table 9 on page 10.

UART Transmitter

The transmitter consists of a 1024-byte Tx FIFO and a Transmit Shift Register (TSR). Once a bulk-out packet is received and the CRC is validated, the data bytes in that packet are written into the Tx FIFO of the specified UART channel. Data from the Tx FIFO is transferred to the TSR when the TSR is idle or has completed sending the previous data byte. The transmitter sends the start bit followed by the data bits (starting with the LSB), inserts the proper parity-bit if enabled, and adds the stop-bit(s). The transmitter can be configured for 7 or 8 data bits with or without parity or 9 data bits without parity. If 9 bit data is selected without wide mode, the ninth bit is always *0*.

UART Transmitter—Wide Mode

When both 9 bit data and wide mode are enabled, two bytes of data must be written. The first byte that is loaded into the Tx FIFO is the first eight bits (data bits 7-0) of the 9-bit data. Bit-0 of the second byte that is loaded into the Tx FIFO is bit-8 of the 9-bit data. The data that is transmitted on the Tx pin is as follows: start bit, 9-bit data, stop bit. Use the TX_WIDE_MODE register to enable transmit wide mode.

UART Receiver

The receiver consists of a 1024-byte Rx FIFO and a Receive Shift Register (RSR). Data that is received in the RSR via the Rx pin is transferred into the Rx FIFO. Data from the Rx FIFO is sent to the USB host in response to a bulk-in request. Depending on the mode, error/status information for that data character may or may not be stored in the Rx FIFO with the data.

UART Receiver—Normal Mode with 7- or 8-bit Data

Data that is received is stored in the Rx FIFO. Any parity, framing, or overrun error or break status information related to the data is discarded. Figure 4 on page 11 shows receive data format.

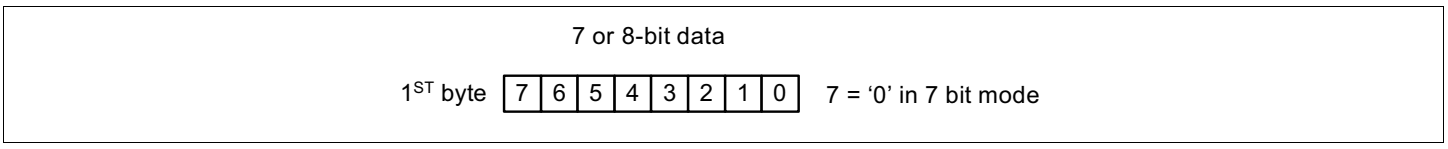


Figure 4: UART Normal Receive Data Format with 7- or 8-bit Data

UART Receiver—Normal Mode with 9-bit Data

The first eight bits of data received are stored in the Rx FIFO. The ninth bit as well as any parity, framing, or overrun error or break status information related to the data is discarded.

UART Receiver—Wide Mode with 7- or 8-bit Data

Two bytes of data are loaded into the Rx FIFO for each byte of data received. The first byte is the received data. The second byte consists of the error bits and break status. Figure 5 shows wide mode receive data format. Use the `RX_WIDE_MODE` register to enable receive wide mode.

UART Receiver—Wide Mode with 9-bit Data

Two bytes of data are loaded into the Rx FIFO for each byte of data received. The first byte is the first eight bits of the received data. The ninth bit received is stored in bit 0 of the second byte. The parity bit is not received/checked. The remainder of the second byte consists of the framing and overrun error bits and break status.

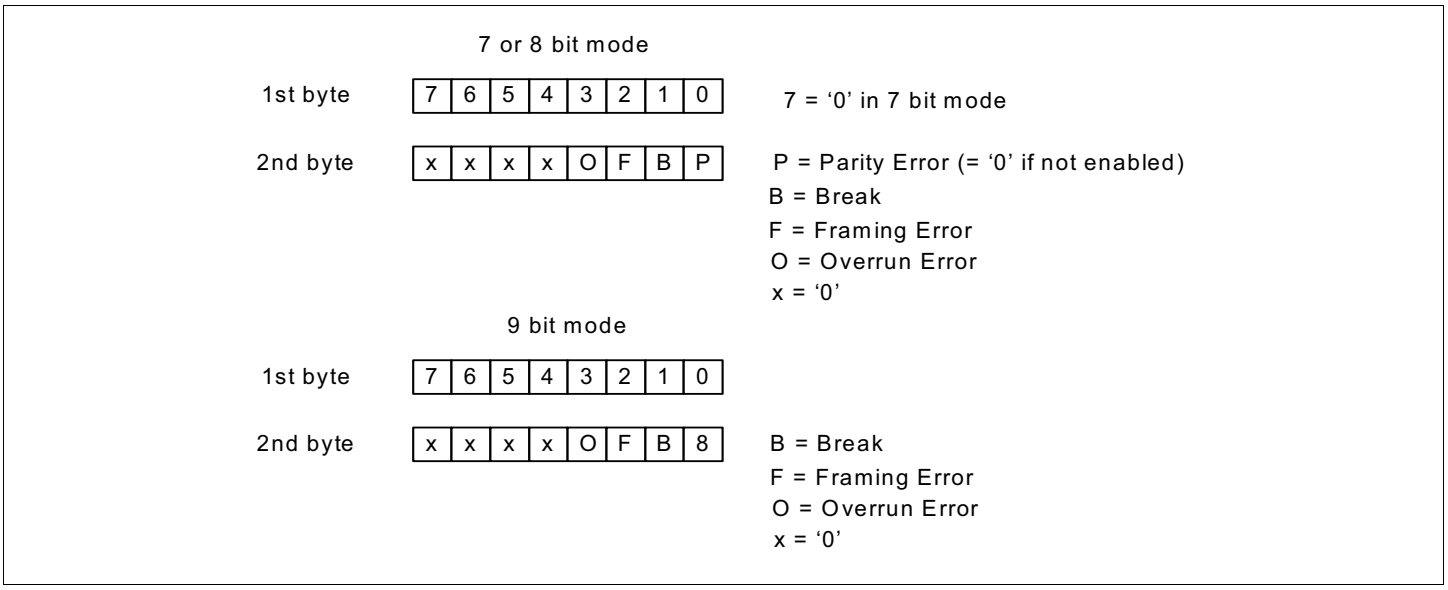


Figure 5: UART Receive Wide Mode Data Format with 7-, 8-, or 9-bit Data

Error flags are also available from the `ERROR_STATUS` register and the interrupt packet, however these flags are historical flags indicating that an error has occurred since the previous request.

Rx FIFO Low Latency

In normal operation, all bulk-in transfers are of `maxPacketSize` bytes (512 bytes in hi-speed mode and 64 bytes in full-speed mode) to improve throughput and to minimize host processing. When there are 512/64 bytes of data in the Rx FIFO, the MxL81434 acknowledges a bulk-in request from the host and transfers the data packet. If there are fewer than 512 bytes in the Rx FIFO, the MxL81434 may NAK the bulk-in request indicating that data is not ready to transfer at that time. However, if there are fewer than 512 bytes in the Rx FIFO and no data is received for more than three character times, the MxL81434 acknowledges the bulk-in request and transfers any data in the Rx FIFO to the USB host.

In some cases, particularly at low baud rates, this increases latency unacceptably. The MxL81434 has a low-latency register bit that causes the MxL81434 to immediately transfer any received data in the Rx FIFO to the USB host, that is, it does not wait for three character times. The custom driver may automatically set the `RX_CONTROL` register to force the MxL81434 to be in the low latency mode, or you may manually set this bit. With the CDC-ACM driver, the low latency mode is automatically set whenever the baud rate is set to a value of less than 46921bps using the `CDC_ACM_IF_SET_LINE_CODING` command.

GPIO

There can be up to eight GPIO pins in each MxL81434 UART channel including the UART Rx and Tx pins. These GPIO pins can be configured as UART GPIOs, or for other UART functions, for example RTS# function, or be assigned to the EDGE. See “Enhanced Dedicated GPIO Entity (EDGE)” on page 16.

Automatic RTS/CTS Hardware Flow Control

E[n]/RTS#/RS485/G[n] and E[n]/CTS#/G[n] of each UART channel may be enabled as the RTS# and CTS# signals for Auto RTS/CTS flow control when `GPIO_MODE[2:0]` = ’001’ and `FLOW_CONTROL[2:0]` = ’001’. Automatic RTS flow control is used to prevent data overrun errors in local Rx FIFO by de-asserting the RTS signal to the remote UART. When there is room in the Rx FIFO, the RTS pin is re-asserted. Automatic CTS flow control is used to prevent data overrun to the remote Rx FIFO. The CTS# input is monitored to suspend/restart the local transmitter. See the following figure:

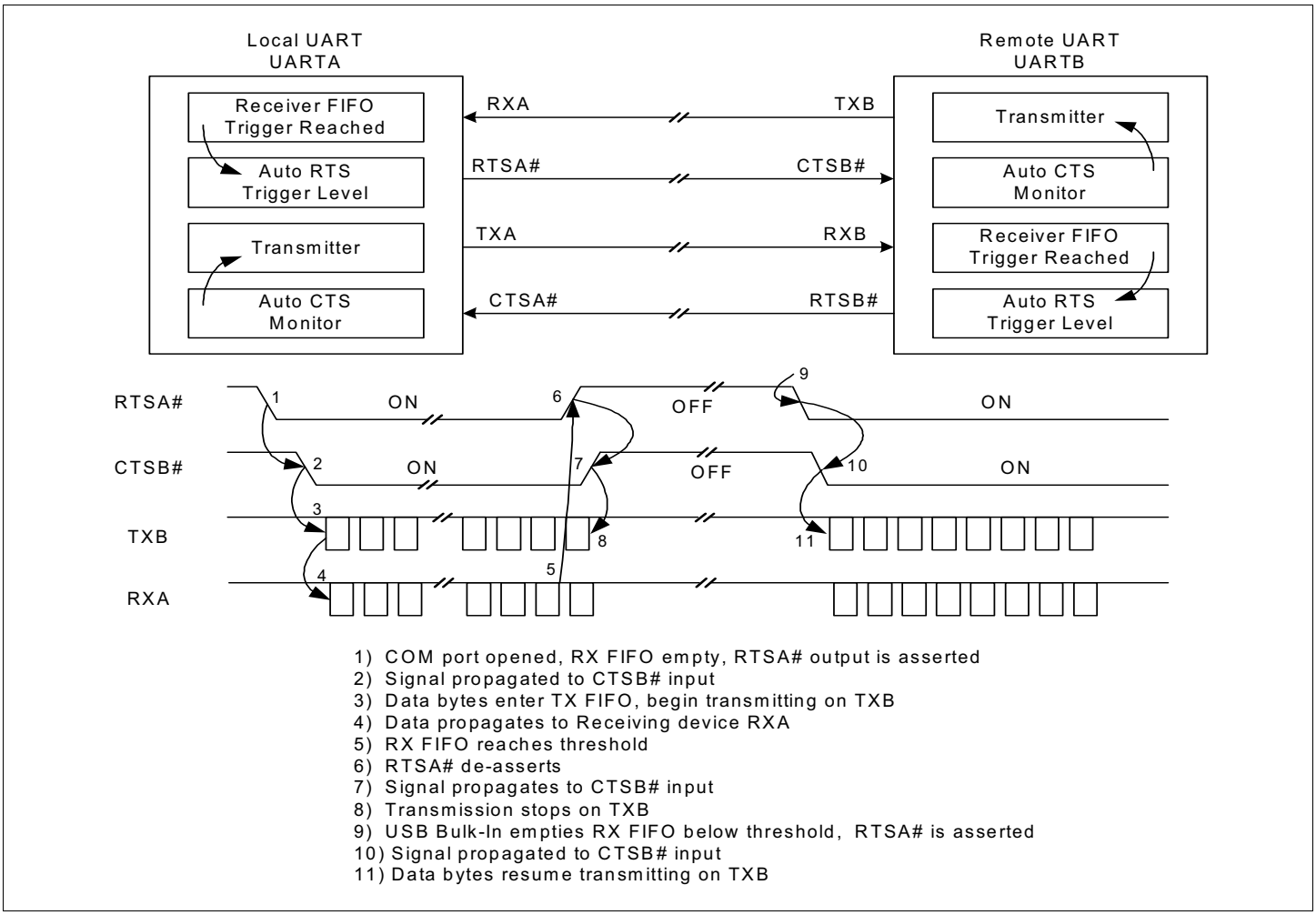


Figure 6: Auto RTS/CTS Hardware Flow Control

Automatic DTR/DSR Hardware Flow Control

Auto DTR/DSR hardware flow control behaves the same as the Auto RTS/CTS hardware flow control described above except that it uses the DTR# and DSR# signals. For Auto hardware flow control, `FLOW_CONTROL[2:0]` = ’001’. E[n]/DTR#/G[n] and E[n]/DSR#/G[n] of each UART channel become DTR# and DSR#, respectively, when `GPIO_MODE[2:0]` = ’010’.

Automatic XON/XOFF Software Flow Control

When software flow control is enabled, the MxL81434 compares the receive data characters with the programmed Xon or Xoff characters. If the received character matches the programmed Xoff character, the MxL81434 halts transmission as soon as the current character has completed transmission. Data transmission is resumed when a received character matches the Xon character. Software flow control is enabled when `FLOW_CONTROL[2:0]` = ’010’.

Automatic RS-485 Half-Duplex Control

The Auto RS-485 Half-Duplex Control feature changes the behavior of the E[n]/RTS#/RS485/G[n] pin of a UART channel when enabled by the GPIO_MODE register bits 2–0. See “GPIO_MODE (0x04C)—Read/Write” on page 22.
The FLOW_CONTROL register must also be set appropriately for use in multidrop applications. See “FLOW_CONTROL (0x046)—Read/Write” on page 20. If enabled, the transmitter automatically asserts the E[n]/RTS#/RS485/G[n] output prior to sending the data. By default, it de-asserts E[n]/RTS#/RS485/G[n] following the last stop bit of the last character that is transmitted, but the RS485_DELAY register may be used to delay the de-assertion. The polarity of the E[n]/RTS#/RS485/G[n] signal can also be modified using the GPIO_MODE register bit 3.

Multidrop Mode with Address Matching

The MxL81434 device has two address matching modes which are also set by the flow control register using modes 3 and 4. These modes are intended for a multidrop network application. In these modes, the XON_CHAR register holds a unicast address and the XOFF_CHAR holds a multicast address. A unicast address is used by a transmitting master to broadcast an address to all attached slave devices that is intended for only one slave device. A multicast address is used to broadcast an address intended for more than one recipient device. Each attached slave device should have a unique unicast address value stored in the XON_CHAR register, while multiple slaves may have the same multicast address stored in the XOFF_CHAR register. An address match occurs when an address byte (ninth bit or parity bit is *1*) is received that matches the value stored in either the XON_CHAR or XOFF_CHAR register.

Multidrop Mode Receiver

If an address match occurs in either flow control mode 3 or 4, the UART receiver is automatically enabled and all subsequent data bytes are loaded into the Rx FIFO. The UART receiver is automatically disabled when an address byte is received that does not match the values in the XON_CHAR or XOFF_CHAR register.

Multidrop Mode Transmitter

In flow control mode 3, the UART transmitter is always enabled, irrespective of the Rx address match.
In flow control mode 4, the UART transmitter is only enabled if there is an Rx address match.

Programmable Turn-Around Delay

By default, the E[n]/RTS#/RS485/G[n] pin is de-asserted immediately after the stop bit of the last byte is shifted. However, this can not be ideal for systems where the signal needs to propagate over long cables. Therefore, the de-assertion of E[n]/RTS#/RS485/G[n] pin can be delayed from 1 to 15 bit times via the RS485_DELAY register to allow for the data to reach distant UARTs.

Half-Duplex Mode

Half-duplex mode is enabled when FLOW_CONTROL[3] = 1. In this mode, the UART ignores any data on the Rx input when the UART is transmitting data.

IR Mode

The MxL81434 supports IR mode with transmit pulses of 3/16th or 4/16th of a bit period and centered in the bit period. Receive data may be inverted to conform to some manufacturer's non-standard devices. IR mode is disabled by default but may be enabled by the IR_MODE register.

Enhanced Dedicated GPIO Entity (EDGE)

The MxL81434 has 32 I/O pins that may be assigned to the EDGE. By default, these pins are all assigned to the corresponding UART channel functions, either to the UART data and/or flow control pins or to the UART GPIO. Note that UART GPIO and EDGE have separate register controls. Pins assigned to the UART function cannot be controlled by the EDGE registers and vice versa. To assign pins to the EDGE, use the `EDGE_FUNC_SEL` register. See "EDGE_FUNC_SEL_0 (0x3C0)—Read/Write" on page 34.

The EDGE controller allows for GPIO signals to be individually set or cleared or to be grouped, such that all pins in the group can be simultaneously accessed for reads or writes. Note that on write accesses, output pins change in 4-bit subgroups on core clock (60MHz) boundaries. For example, if an 8-bit data group is defined and the data value is written from 0x00 to 0xFF, 4 bits would change from *0* to *1* followed by the next 4 bits one clock cycle (~17ns) later.

EDGE I/Os can be configured as inputs or outputs. Outputs can be configured as push-pull or open-drain and can be tri-stated. Inputs can be configured to generate interrupts to the USB host on either negative or positive edge transitions.

Another feature of the EDGE controller is that up to two GPIO pins within the EDGE can be assigned to pulse-width modulated (PWM) outputs. Each of the PWM outputs can be used to generate an output clock or pulse of varying duty cycle. Both low and high cycles can be configured in steps of 267ns up to 1.092ms. The output can be controlled to generate a single o*ne-shot* pulse or to free run. See "EDGE_PWM0_CTRL (0x3D8)—Read/Write" on page 40 and "EDGE_PWM1_CTRL (0x3DB)—Read/Write" on page 41 for control of PWM outputs.

I^2C

The MxL81434 implements an I^2C multi-master using the control endpoint of the Full-Speed USB function to transfer data to and from the I^2C interface. The I^2C master supports both standard (100kbps) and fast (400kbps) modes and supports multiple master configurations to allow other devices to access slave devices on the I^2C. The I^2C function is an HID function and uses the native HID driver. It supports both 7- and 10-bit addressing modes.

Regulated 3.3V Power Output

The MxL81434 internal voltage regulator provides 3.3VDC output power which can be utilized by other circuitry. See "Electrical Characteristics" on page 2 for maximum power capability. For bus-powered devices, significant utilization of the 3V3 output power may require increasing the maximum power request above the 250mA default value from the USB host by programming the OTP.

OTP

The OTP is an on-chip non-volatile memory, that is one-time programmable via the USB interface. Bit locations within the memory may be programmed at various times allowing for customization of the MxL81434. Some bits are pre-programmed at the factory and caution must be taken not to program any locations except user-defined addresses. Contact the factory for information and assistance in programming the MxL81434 OTP.

USB Control Commands

Table 10 lists all of the USB control commands that are supported by the MxL81434. Commands include standard USB commands, USB class-specific CDC-ACM commands, and USB vendor-specific MaxLinear commands.

Table 10: Supported USB Control Commands

Name	Request Type	Request	Value		Index		Length		Description
			LSB	MSB	LSB	MSB	LSB	MSB	
USB Standard Requests									
DEV GET_STATUS	0x80	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Device: remote wake-up + self-powered
IF GET_STATUS	0x81	0x0	0x0	0x0	0x0	0x0	0x2	0x0	Interface: zero
EP GET_STATUS	0x82	0x0	0x0	0x0	0x0, 0x4, 0x84	0x0	0x2	0x0	Endpoint: halted
DEV CLEAR_FEATURE	0x00	0x1	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP CLEAR_FEATURE	0x02	0x1	0x0	0x0	0x0, 0x4, 0x84	0x0	0x0	0x0	Endpoint halt
DEV SET_FEATURE	0x00	0x3	0x1	0x0	0x0	0x0	0x0	0x0	Device remote wake-up
EP SET_FEATURE	0x02	0x3	0x0	0x0	0x0, 0x4, 0x84	0x0	0x0	0x0	Endpoint halt
SET_ADDRESS	0x00	0x5	addr	0x0	0x0	0x0	0x0	0x0	addr = 1 to 127
GET_DESCRIPTOR	0x80	0x6	0x0	0x1	0x0	0x0	len LSB	len MSB	Device descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x2	0x0	0x0	len LSB	len MSB	Configuration descriptor
GET_DESCRIPTOR	0x80	0x6	0x0	0x3	LangID	LangID	len LSB	len MSB	String descriptor
GET_CONFIGURATION	0x80	0x8	0x0	0x0	0x0	0x0	0x1	0x0	-
SET_CONFIGURATION	0x00	0x9	n	0x0	0x0	0x0	0x0	0x0	n = 0, 1
USB Class-Specific Requests									
CDC_ACM_IF SET_LINE_CODING	0x21	0x20	0x0	0x0	0x0	0x0	0x7	0x0	Set the UART baud rate, parity, stop bits, etc.
CDC_ACM_IF GET_LINE_CODING	0xA1	0x21	0x0	0x0	0x0	0x0	0x7	0x0	Get the UART baud rate, parity, stop bits, etc.
CDC_ACM_IF SET_CONTROL_ LINE_STATE	0x21	0x22	D7-2: 0 D1: RTS D0: DTR	0x0	0x0	0x0	0x0	0x0	Set/Clear RTS and DTR in CDC-ACM mode.
CDC_ACM_IF SEND_BREAK	0x21	0x23	val LSB	val MSB	0x0	0x0	0x0	0x0	Send a break for the specified duration.
USB Vendor-Specific Requests									
XR_GET_CHIP_ID	0xC0	0xFF	0x0	0x0	0x0	0x0	0x6	0x0	Get MaxLinear's/Exar's VID (2 bytes), PID (2 bytes) and bcdDevice (2 bytes)
XR_SET_REG See Table 11 on page 18	0x40	0x05	write-data LSB	write-data MSB	write addr LSB	write addr MSB	0x0	0x0	Vendor-specific register access
XR_GET_REG See Table 11 on page 18	0xC0	0x05	0x0	0x0	read addr LSB	read addr MSB	0x2	0x0	Vendor-specific register access

UART Registers

UART registers are accessible via the USB interface using the XR_SET_REG and XR_GET_REG USB commands. Note that all addresses not listed in Table 11 are reserved or undefined. Upper byte (bits 15:8) not listed in this table are also reserved and should remain 0x00. Writing to any register other than those defined in this table may result in undefined behavior of the device. The addresses for each of the UARTs in the MxL81434 are the same. Because each UART is assigned a unique USB address during enumeration by the USB host, a GUI connected to a specific COM port is directed via the driver to the appropriate UART channel.

UART Register Map

Table 11: MxL81434 UART Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x040	UART_ENABLE	0	0	0	0	0	0	Rx	Tx
0x045	FORMAT	STOP	PARITY			DATA_BITS			
0x046	FLOW_CONTROL	0	0	0	0	Half_ Duplex	MODE		
0x047	XON_CHAR	CHAR							
0x048	XOFF_CHAR	CHAR							
0x049	ERROR_STATUS	BREAK_ ACTIVE	OVERRUN	PARITY	FRAME	BREAK	0	0	0
0x04A	TX_BREAK (MSB)	VALUE (MSB)							
	TX_BREAK (LSB)	VALUE (LSB)							
0x04B	RS485_DELAY	0	0	0	0	VALUE			
0x04C	GPIO_MODE	0	0	0	0	RS485_ POL	MODE		
0x04D	GPIO_DIRECTION	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x04E	GPIO_SET	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x04F	GPIO_CLEAR	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x050	GPIO_STATUS	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x051	GPIO_INT_MASK	0	0	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x052	CUSTOMIZED_INT	0	0	0	0	0	0	0	EN
0x054	PIN_PULLUP_EN	Tx	Rx	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x055	PIN_PULLDOWN_EN	Tx	Rx	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0x056	LOOPBACK	0	0	0	0	0	DTR_ DSR	RTS_ CTS	TX_ RX
0x057	IR_MODE	0	0	0	0	0	TX_ PULSE	RX_ I NVERT	EN
0x05F	REMOTE_WAKEUP	0	0	0	0	RX_EN	RI_EN	0	0
0x060	TX_FIFO_RESET	0	0	0	0	0	0	0	RST
0x061	TX_FIFO_FILL (MSB)	0	0	0	0	0	FILL[10:8]		
	TX_FIFO_FILL (LSB)	FILL[7:0]							
0x062	TX_WIDE_MODE	0	0	0	0	0	0	0	EN
0x063	RX_FIFO_RESET	0	0	0	0	0	0	0	RST
0x064	RX_FIFO_FILL (MSB)	0	0	0	0	0	FILL[10:8]		
	RX_FIFO_FILL (LSB)	FILL[7:0]							
0x065	RX_WIDE_MODE	0	0	0	0	0	0	0	EN
0x066	RX_CONTROL	0	0	0	0	0	0	MAX_ PKT_ SIZE	LOW_ LATENCY
0x067	FLOW_THRESHOLD (MSB)	0	0	0	0	0	THRESH [10:8]		
	FLOW_THRESHOLD (LSB)	THRESH [7:0]							
Miscellaneous Registers									
0x081	CUSTOM_DRIVER	0	0	0	0	0	0	0	ACTIVE

UART Register Descriptions

Note that all register reset default values are *0,* unless otherwise specified. All registers are 16 bits.

UART_ENABLE (0x040)—Read/Write

Table 12: UART_ENABLE

Bit	Default	Description
15:2	0x0000	**Reserved** These bits are reserved and should be written as *0.*
1	0	**Rx** ■ 0: Disable UART Rx. ■ 1: Enable UART Rx.
0	0	**Tx** ■ 0: Disable UART Tx. ■ 1: Enable UART Tx.

FORMAT (0x045)—Read/Write

Note that the `CDC_SET_LINE_CODING` command may be used to set the UART data format in addition to this register.

Table 13: FORMAT

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as *0.*
7	0	**Stop** ■ 0: 1 stop bit. ■ 1: 2 stop bits.
6:4	0	**Parity** ■ 000: No parity. ■ 001: Odd parity. ■ 010: Even parity. ■ 011: Mark parity. ■ 100: Space parity. All other values undefined, do not use.
3:0	0x8	**Data_Bits** ■ 0111: 7-bit characters. ■ 1000: 8-bit characters. ■ 1001: 9-bit characters. All other values undefined, do not use.

FLOW_CONTROL (0x046)—Read/Write

Table 14: FLOW_CONTROL

Bit	Default	Description
15:4	0x000	**Reserved.** These bits are reserved and should be written as *0*.
3	0	**Half-Duplex Mode** ■ 0: UART Rx receives data irrespective of UART Tx. ■ 1: UART Rx is disabled when UART Tx is transmitting data.
2:0	0	**Mode** ■ 000: None. ■ 001: Hardware. ■ 010: Software. ■ 011: Address match Rx. ■ 100: Address match Rx and Tx. All other values undefined, do not use.

XON_CHAR (0x047)—Read/Write

Table 15: XON_CHAR

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as *0*.
7:0	0x11	**Char** XON ASCII character received in hexadecimal format.

XOFF_CHAR (0x048)—Read/Write

Table 16: XOFF_CHAR

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved and should be written as *0*.
7:0	0x13	**Char** XOFF ASCII character received in hexadecimal format.

ERROR_STATUS (0x049)—Read-Only

Table 17: ERROR_STATUS

Bit	Default	Description
15:8	0x00	**Reserved** These bits are reserved.
7	0	**Break_Active** ■ 0: No break condition currently active. ■ 1: Break condition currently active.
6	0	**Overrun** ■ 0: No overrun error detected. ■ 1: Overrun error detected since last register read.
5	0	**Parity** ■ 0: No parity error detected. ■ 1: Parity error detected since last register read.
4	0	**Frame** ■ 0: No frame error detected. ■ 1: Frame error detected since last register read.
3	0	**Break** ■ 0: No break error detected ■ 1: Break error detected since last register read.
2:0	0	**Reserved** These bits are reserved and should be written as *0*.

TX_BREAK (0x04A)—Read/Write

Table 18: TX_BREAK

Bit	Default	Description
15:0	0x0000	**Value** This register controls transmission of break signal. Writing a non-zero value *N* to this register causes the MxL81434 to send a break signal on the UART Tx pin for *N* ms, for 0 < N < 0xFFFF. A counter decrements this value at 1ms intervals until the count reaches 0x0 at which time the break signal stops being sent. Writing a value of 0xFFFF causes a continuous break signal to be sent, until either a value of 0x0 is written or another non-zero value other than 0xFFFF is written which causes the break signal to stop after the new counter expires.

RS485_DELAY (0x04B)—Read/Write

Table 19: RS485_DELAY

Bit	Default	Description
15:4	0x000	**Reserved** These bits are reserved and should be written as *0*.
3:0	0X0	**Value** This value is the number of bit times the MxL81434 waits before de-asserting the corresponding channel's RTS#/RS485 pin when it is configured for automatic RS-485 half-duplex control.

GPIO_MODE (0x04C)—Read/Write

Table 20: GPIO_MODE

Bit	Default	Description
15:4	0x000	**Reserved** These bits are reserved and should be written as *0.*
3	0	**RS-485 Polarity** ■ 0: Active low auto. RS-485 half-duplex enable. ■ 1: Active high auto. RS-485 half-duplex enable.
2:0	0x0	**GPIO Mode** ■ 000: Mode 0—All GPIOs are used for general-purpose I/O. ■ 001: Mode 1—RTS#/RS485 and CTS# used for Auto RTS/CTS HW flow control. ■ 010: Mode 2—DTR# and DSR# used for Auto DTR/DSR HW flow control. ■ 011: Mode 3—RTS#/RS485 pin used for auto RS-485 half-duplex enable during transmit. ■ 100: Mode 4— RTS#/RS485 pin used for auto RS-485 half-duplex enable after address match. ■ 101 to 111: Reserved values, do not use.

GPIO_DIRECTION (0x04D)—Read/Write

Note that when setting direction of a UART GPIO to output, the `PIN_PULLUP_EN` for that I/O pin should also be disabled and when setting a UART GPIO pin to input, the `PIN_PULLUP_EN` for that I/O pin should also be enabled.

Table 21: GPIO_DIRECTION

Bit	Default	Description
15:6	0x000	**Reserved** These bits are reserved and should be written as *0.*
5:0	0x00	**GPIO[N] Direction** ■ 0: GPIO[N] is an input. ■ 1: GPIO[N] is an output.

GPIO_SET (0x04E)—Write-Only

Table 22: GPIO_SET

Bit	Default	Description
15:6	0x000	**Reserved** These bits are reserved and should be written as *0.*
5:0	0x00	**GPIO[N] Set** ■ 0: No effect. ■ 1: Set GPIO[N] if configured as an output to a logic *1.*

GPIO_CLEAR (0x04F)—Write-Only

Table 23: GPIO_CLEAR

Bit	Default	Description
15:6	0x000	**Reserved** These bits are reserved.
5:0	0x00	**GPIO[N] Clear** ■ 0: No effect. ■ 1: Clear GPIO[N] if configured as an output to a logic *0*.

GPIO_STATUS (0x050)—Read-Only

Table 24: GPIO_STATUS

Bit	Default	Description
15:6	0x000	**Reserved** These bits are reserved.
5:0	0x00	**GPIO[N] Status** Reading returns the current state of GPIO[N].

GPIO_INT_MASK (0x051)—Read/Write

Table 25: GPIO_INT_MASK

Bit	Default	Description
15:6	0x000	**Reserved** These bits are reserved and should be written as *0*.
5:0	0x00	**GPIO[N] Mask** Dictates whether a change in GPIO pin state causes the device to generate a USB interrupt packet. In either case, the GPIO status register still reports the pin's state when read, and if an interrupt packet is formed due to other interrupt trigger, the interrupt packet contains the current state of the pin. ■ 0: A change in the pin's state causes the device to generate an interrupt packet. ■ 1: A change in the pin's state does not cause the device to generate an interrupt packet.

CUSTOMIZED_INT (0x052)—Read/Write

Table 26: CUSTOMIZED_INT

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0*.
0	0	**Enable** Enables the customized interrupt packet format to report all GPIO status in the interrupt packet. ■ 0: Use standard interrupt packet. See Table 27 and Table 28 on page 24. ■ 1: Use customized interrupt packet. See Table 29 on page 25.

Table 27: Interrupt Packet Format

Offset	Field	Size (Bytes)	Value	Description
0	bmRequestType	1	8'b10100001	■ D7 = Device-to-host direction ■ D6-5 = Class type ■ D4-0 = Interface recipient
1	bNotification	1	8'h20	Defined encoding for SERIAL_STATE
2	wValue	2	16'h0000	-
4	wIndex	2	16'h0000	■ D15-8 = Reserved (0) ■ D7-0 = Interface number, 8'h00 for the CDC Command interface
6	wLength	Standard: 2 Customized: 4	16'h0002 For customized int_status size = 4 bytes Then, wLength should be 0x0004	Standard: 2 bytes of transferred data Customized: 4 bytes of transferred data
8	Data	Standard: 2 Customized: 4	Standard int_status (See Table 28) For customized int_status size = 4 bytes (See Table 29).	■ D15-7 = Reserved (0) ■ D6 = bOverRun ■ D5 = bParity ■ D4 = bFraming ■ D3 = bRingSignal (RI) ■ D2 = bBreak ■ D1 = bTxCarrier (DSR) ■ D0 = bRxCarrier (CD)

Table 28: Data Field of Standard Interrupt Packet

Bit	Field	Description
D15-7	-	Reserved (future use).
D6	bOverRun	Received data is discarded due to overrun in the device.
D5	bParity	A parity error has occurred.
D4	bFraming	A framing error has occurred.
D3	bRingSignal	State of ring signal detection of the device.
D2	bBreak	State of break-detection mechanism of the device.
D1	bTxCarrier	State of transmission carrier. This signal corresponds to V.24 signal 106 and RS-232 signal DSR.
D0	bRxCarrier	State of the receiver carrier-detection mechanism of the device. This signal corresponds to V.24 signal 109 and RS-232 signal DCD.

Table 29: Data Field of Customized Interrupt Packet—MaxLinear Vendor-Specific

Bit(s)	Description
31-20	Reserved (0)
19	Overrun
18	Parity Error
17	Frame Error
16	Break Status
15-14	Reserved (0)
13	RTS state
12	CTS state
11	DTR state
10	DSR state
9	CD state
8	RI state
7-6	Reserved (0)
5	RTS change
4	CTS change
3	DTR change
2	DSR change
1	CD change
0	RI change

Overrun, Parity Error, Frame Error, and Break all indicate that at least one event has occurred since the last interrupt message. *State* reflects the high/low state of the pin at the time the Interrupt Data IN packet is generated. *Change* indicates whether the level on the pin changed at least once since the last interrupt message.

PIN_PULLUP_EN (0x054)—Read/Write

Table 30: PIN_PULLUP_EN

Bit	Default	Description
15:8	0	**Reserved** These bits are reserved and should be written as *0*.
7	1	**UART Tx** ■ 0: Disable internal pull-up resistor on the UART Tx pin. ■ 1: Enable internal pull-up resistor on the UART Tx pin.
6	1	**UART Rx** ■ 0: Disable internal pull-up resistor on the UART Rx pin. ■ 1: Enable internal pull-up resistor on the UART Rx pin.
5:0	0x3F	**GPIO[N]** ■ 0: Disable internal pull-up resistor on the corresponding GPIO[N] pin. ■ 1: Enable internal pull-up resistor on the corresponding GPIO[N] pin.

PIN_PULLDOWN_EN (0x055)—Read/Write

Table 31: PIN_PULLDOWN_EN

Bit	Default	Description
15:8	0	**Reserved** These bits are reserved and should be written as *0*.
7	0	**UART Tx** ■ 0: Disable internal pull-down resistor on the UART Tx pin. ■ 1: Enable internal pull-down resistor on the UART Tx pin (not enabled if pull-up is already enabled).
6	0	**UART Rx** ■ 0: Disable internal pull-down resistor on the UART Rx pin. ■ 1: Enable internal pull-down resistor on the UART Rx pin (not enabled if pull-up is already enabled).
5:0	0	**GPIO[N]** ■ 0: Disable internal pull-down resistor on the corresponding GPIO[N] pin. ■ 1: Enable internal pull-down resistor on the corresponding GPIO[N] pin (not enabled if pull-up is already enabled).

LOOPBACK (0x056)—Read/Write

Table 32: LOOPBACK

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as *0*.
2	0	**DTR_DSR** ■ 0: Disable DTR-to-DSR internal loopback. ■ 1: Enable DTR-to-DSR internal loopback.
1	0	**RTS_CTS** ■ 0: Disable RTS-to-CTS internal loopback. ■ 1: Enable RTS-to-CTS internal loopback.
0	0	**TX_RX** When this bit is set, all transmitted UART data is looped back to the UART receiver. Note that when the internal loopback is enabled, the Tx data is disabled and Rx data is ignored. ■ 0: Disable Tx-to-Rx internal loopback. ■ 1: Enable Tx-to-Rx internal loopback.

IR_MODE (0x057)—Read/Write

Table 33: IR_MODE

Bit	Default	Description
15:3	0	**Reserved** These bits are reserved and should be written as *0*.
2	0	**TX_Pulse** ■ 0: Tx pulse width is 3/16 of the bit period. ■ 1: Tx pulse width is 4/16 of the bit period.
1	0	**RX_Invert** ■ 0: Rx input is not inverted before sampling. ■ 1: Rx input is inverted before sampling.

Table 33: IR_MODE

Bit	Default	Description
0	0	**En** ■ 0: Disable IR mode. ■ 1: Enable IR mode.

REMOTE_WAKEUP (0x05F)—Read/Write

Table 34: REMOTE_WAKEUP

Bit	Default	Description
15:4	0x000	**Reserved** These bits are reserved and should be written as *0.*
3	0	**RX_En** ■ 0: Rx pin remote wake-up is disabled. ■ 1: A high-to-low transition on the Rx pin causes a resume request to be sent to the USB host.
2	1	**RI_En** ■ 0: RI# pin remote wake-up is disabled. ■ 1: A high-to-low transition on the RI# pin causes a resume request to be sent to the USB host.
1:0	0x0	**Reserved** These bits are reserved and should be written as *0.*

TX_FIFO_RESET (0x060)—Write-Only

Table 35: TX_FIFO_RESET

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0.*
0	0	**Reset** ■ 0: No effect. ■ 1: Resets the Tx FIFO to empty.

TX_FIFO_FILL (0x061)—Read-Only

Table 36: TX_FIFO_FILL

Bit	Default	Description
15:11	0x00	**Reserved** These bits are reserved.
10:0	0x000	**Fill** Number of bytes in the Tx FIFO.

TX_WIDE_MODE (0x062)—Read/Write

Table 37: TX_WIDE_MODE

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0.*

Table 37: TX_WIDE_MODE

Bit	Default	Description
0	0	**EN** In wide mode, 2 bytes of data are used to transfer one character. This requires 2 bytes of FIFO space, therefore the FIFO can hold half as many characters in wide mode. In the Tx direction, bit 0 of the second byte is used as bit 8, the ninth bit of the character, if 9-bit mode is enabled. Bits 7:1 of the second byte are not used. ■ 0: Disable Tx wide mode. ■ 1: Enable Tx wide mode.

RX_FIFO_RESET (0x063)—Write-Only

Table 38: RX_FIFO_RESET

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0.*
0	0	**Reset** ■ 0: No effect. ■ 1: Resets the Rx FIFO to empty.

RX_FIFO_FILL (0x064)—Read-Only

Table 39: RX_FIFO_FILL

Bit	Default	Description
15:11	0x00	**Reserved** These bits are reserved.
10:0	0x000	**Fill** Number of bytes in the Rx FIFO.

RX_WIDE_MODE (0x065)—Read/Write

Table 40: RX_WIDE_MODE

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0.*
0	0	**EN** In wide mode, 2 bytes of bulk data are used to transfer one character. This requires 2 bytes of FIFO space, therefore the FIFO can hold half as many characters in wide mode. In 7 or 8 bit mode, bits [3:0] of the second byte in an Rx transfer contain the error flags associated with the character; bits [7:4] are unused. In 9-bit mode, the second byte is formatted differently. For the 9-bit mode configuration, see Figure 5 on page 12. ■ 0: Disable Rx wide mode. ■ 1: Enable Rx wide mode.

RX_CONTROL (0x066)—Read/Write

Table 41: RX_CONTROL

Bit	Default	Description
15:2	0	**Reserved** These bits are reserved and should be written as *0.*
1	0	**Max_Pkt_Size** ■ 0: Maximum bulk-in packet size is 512/64 bytes in hi-speed/full-speed mode respectively (normal operation). ■ 1: Maximum bulk-in packet size is 508/60 bytes in hi-speed/full-speed mode respectively (workaround for known Windows OS CDC-ACM driver issue).
0	0	**Low_Latency** ■ 0: Disable low latency mode. ■ 1: Enable low latency mode.

FLOW_THRESHOLD (0x067)—Read/Write

Table 42: FLOW_THRESHOLD

Bit	Default	Description
15:11	0x0	**Reserved** These bits are reserved and should be written as *0.*
10:0	0x2E0	**Thresh** If enabled, flow control (either hardware or software), is asserted when the Rx FIFO fill level exceeds the threshold value.

CUSTOM_DRIVER (0x081)—Read/Write

Table 43: CUSTOM_DRIVER

Bit	Default	Description
15:1	0x0000	**Reserved** These bits are reserved and should be written as *0.*
0	0	**Active** A custom driver should immediately enable this bit prior to using any CDC-ACM commands from the USB host, to ensure that the MxL81434 does not enter CDC mode and default to the values listed in Table 9 on page 10.

HID Reports

The I^{2}C and EDGE functions in the MxL81434 are HID functions. I^{2}C data can be read or written to/from the slave device using the interrupt-in and interrupt-out endpoints via HID input and output reports. Additionally, MxL81434 device register access using the control endpoint for both I^{2}C and EDGE functions is performed via HID feature reports. Reading uses indirect addressing such that for register reads, the register address must first be written and the register value can then be read. Both types of reports are described in the following sections.

Input and Output Reports

Input and output reports using the interrupt-in and interrupt-out endpoints follow the following format.

I2C_SLAVE_OUT

Transfer type: Interrupt-out

Transfer size: 37 bytes

The `I2C_SLAVE_OUT` report writes and/or reads up to 32 bytes of data on the I^{2}C interface. Note that all interrupt-out transfers are automatically followed by an interrupt-in transfer. For write-only transfers, the interrupt-in packet contains the status of the interrupt-out transfer. For read-only or write-and-read transfers, the interrupt-in packet contains the read data, as well as the status of the interrupt-out transfer. The following table lists the format of the interrupt-out packet.

Table 44: I2C_SLAVE_OUT

Field	Offset	Size	Value	Description
`Report ID`	0	1	0x00	Write, read, or write-and-read I^{2}C data.
`Flags`	1	1	Bitmap	Transfer options ■ D0: Prefix transfer with a start bit. ■ D1: Append a stop bit to the transfer. ■ D2: ACK last read to extend a read transfer (for example, if more than 32 bytes need to be read). The default is to NAK the last read in the transfer. This bit has no effect if `RdSize` is 0. ■ D3: Reserved. ■ D7-D4: Sequence number. This can help the host to correlate an IN response with a prior OUT command. This field is optional.
`WrSize`	2	1	Number	Number of data bytes to write. Valid values are 0 to 32. The 7-bit slave address should not be included in this total.
`RdSize`	3	1	Number	Number of bytes to read. Valid values are 0 to 32.
`SlaveAddr`	4	1	Number	The 7-bit slave address[1] to send. The MxL81434 automatically sets the I^{2}C read/write bit, so bit D0 of this field is ignored.
`Data`	5	32	Data	Data to be written to the slave. HID uses a fixed report size for each specific report ID so this field is always 32 bytes long. However, only the number of bytes specified in `WrSize` is written. Other bytes are ignored.

1. To support 10-bit addressing, the standard 7-bit address must be set to *1111 0xxB* where xx are the most significant bits of the 10-bit address. All four of these 7-bit addresses are reserved and are not used by any slaves with 7-bit only addresses. The least significant bit of the address byte still specifies the direction. For writes, the first data byte which is previously unformatted is now reserved for the least significant 8 bits of the 10-bit address. Additional data bytes remain unformatted. For reads, the write-then-read combined transfer format is always used. During the write portion of the combined transfer the master must send at least one data byte which contains the least significant eight bits of the 10-bit address. After all of the write data is sent the master then sends a restart bit. This is followed with an address byte which has the same 7-bit address 1111 0xxB as in the write portion. However, the direction bit is now 1 for reading. The slave then sends the read data as usual. The least significant eight bits of the 10-bit address are not sent again after the restart bit.

I2C_SLAVE_IN

Transfer type: Interrupt-in

Transfer size: 36 bytes

Interrupt-in packet status only, or status and read data from the I^2C interface.

Table 45: I2C_SLAVE_IN

Field	Offset	Size	Value	Description
Flags	0	1	Bitmap	Status of the requested transfer. ■ D0: Request Error. If 1, the OUT request had an error (for example, invalid size) and is not executed. ■ D1: A byte sent to a slave received an I^2C NAK response. The transfer is aborted. ■ D2: Arbitration is lost. The transfer is aborted. ■ D3: Timeout. Bus-free condition is not observed within 256ms or an individual byte transfer extended longer than 10ms. ■ D7-D4: Sequence number. This number matches the value provided in the corresponding OUT command packet.
WrSize	1	1	Number	Number of bytes written, 0 to 32.
RdSize	2	1	Number	Number of bytes read, 0 to 32.
Reserved	3	1	Number	This field is reserved.
Data	4	32	Data	The read data that is received from the slave. HID uses a fixed report size for each specific report ID, so this field is always 32 bytes long. However, only the number of bytes specified in RdSize are valid. Other bytes should be ignored.

Feature Reports

Access to the MxL81434 registers via HID feature reports along with the register descriptions are described in the following sections.

WRITE_HID_REGISTER

Transfer type: Control

Transfer size: 5 bytes

The WRITE_HID_REGISTER report writes 2 bytes of data to the specified register address.

Table 46: WRITE_HID_REGISTER

Field	Offset	Size	Value	Description
Report ID	0	1	0x3C	Write HID register.
Write Address LSB	1	1	-	Write address.
Write Address MSB	2	1	-	Write address.
Write Data LSB	3	1	-	Write data.
Write Data MSB	4	1	-	Write data.

SET_HID_READ_ADDRESS

Transfer type: Control

Transfer size: 3 bytes

The SET_HID_READ_ADDRESS report sets the address for the READ_HID_REGISTER report.

Table 47: SET_HID_READ_ADDRESS

Field	Offset	Size	Value	Description
Report ID	0	1	0x4B	Set address for HID register read.
Read Address LSB	1	1	-	Read address.
Read Address MSB	2	1	-	Read address.

READ_HID_REGISTER

Transfer type: Control

Transfer size: 3 bytes

The READ_HID_REGISTER report reads register data from the address set by the SET_HID_READ_ADDRESS report.

Table 48: READ_HID_REGISTER

Field	Offset	Size	Value	Description
Report ID	0	1	0x5A	Read HID register.
Read Data LSB	1	1	-	Read data.
Read Data MSB	2	1	-	Read data.

HID Register Map

Table 49: MxL81434 HID Register Map

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
I^2C Registers									
0x341	I^2C_SCL_LOW MSB [15:8]	VALUE (MSB)							
	I^2C_SCL_LOW LSB [7:0]	VALUE (LSB)							
0x342	I^2C_SCL_HIGH MSB [15:8]	VALUE (MSB)							
	I^2C_SCL_HIGH LSB [7:0]	VALUE (LSB)							
EDGE Registers									
0x3C0	EDGE_FUNC_SEL_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_FUNC_SEL_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C1	EDGE_DIR_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_DIR_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C2	EDGE_SET_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_SET_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C3	EDGE_CLEAR_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_CLEAR_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C4	EDGE_STATE_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_STATE_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C5	EDGE_TRI_STATE_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_TRI_STATE_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0

Table 49: MxL81434 HID Register Map (Continued)

Address	Register Name	Bit 7 (15)	Bit 6 (14)	Bit 5 (13)	Bit 4 (12)	Bit 3 (11)	Bit 2 (10)	Bit 1 (9)	Bit 0 (8)
0x3C6	EDGE_OPEN_DRAIN_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_OPEN_DRAIN_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C7	EDGE_PULL_UP_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_PULL_UP_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C8	EDGE_PULL_DOWN_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_PULL_DOWN_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3C9	EDGE_INTR_MASK_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_INTR_MASK_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3CA	EDGE_INTR_POS_EDGE_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_INTR_POS_EDGE_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3CB	EDGE_INTR_NEG_EDGE_0 [15:8]	E15	E14	E13	E12	E11	E10	E9	E8
	EDGE_INTR_NEG_EDGE_0 [7:0]	E7	E6	E5	E4	E3	E2	E1	E0
0x3CC	EDGE_FUNC_SEL_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_FUNC_SEL_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3CD	EDGE_DIR_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_DIR_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3CE	EDGE_SET_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_SET_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3CF	EDGE_CLEAR_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_CLEAR_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D0	EDGE_STATE_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_STATE_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D1	EDGE_TRI_STATE_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_TRI_STATE_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D2	EDGE_OPEN_DRAIN_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_OPEN_DRAIN_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D3	EDGE_PULL_UP_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_PULL_UP_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D4	EDGE_PULL_DOWN_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_PULL_DOWN_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D5	EDGE_INTR_MASK_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_INTR_MASK_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D6	EDGE_INTR_POS_EDGE_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_INTR_POS_EDGE_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D7	EDGE_INTR_NEG_EDGE_1 [31:24]	E31	E30	E29	E28	E27	E26	E25	E24
	EDGE_INTR_NEG_EDGE_1 [23:16]	E23	E22	E21	E20	E19	E18	E17	E16
0x3D8	EDGE_PWM0_CTRL MSB [15:8]	0	0	0	0	0	0	0	CMD[2]
	EDGE_PWM0_CTRL LSB [7:0]	CMD[1:0]		EN	PIN[4:0]				
0x3D9	EDGE_PWM0_HIGH MSB [15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM0_HIGH LSB [7:0]	VALUE [7:0]							
0x3DA	EDGE_PWM0_LOW MSB [15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM0_LOW LSB [7:0]	VALUE [7:0]							
0x3DB	EDGE_PWM1_CTRL MSB [15:8]	0	0	0	0	0	0	0	CMD[2]
	EDGE_PWM1_CTRL LSB [7:0]	CMD[1:0]		EN	PIN[4:0]				
0x3DC	EDGE_PWM1_HIGH MSB [15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM1_HIGH LSB [7:0]	VALUE [7:0]							
0x3DD	EDGE_PWM1_LOW MSB [15:8]	0	0	0	0	VALUE[11:8]			
	EDGE_PWM1_LOW LSB [7:0]	VALUE [7:0]							

HID Register Descriptions

Note that all register reset default values are *0*, unless otherwise specified. All registers are 16 bits.

I²C_SCL_LOW (0x341)—Read/Write

Table 50: I²C_SCL_LOW

Bit	Default	Description
15:0	0x0144	**Value** Specifies the number of periods that SCL is asserted low by the MxL81434 I²C master. Note that in clock stretching, the I²C slave may extend the SCL low period to delay the next transaction. For 100kbps transfer rate, this value must be at least 252 (0x00FC) and the sum of high and low periods must be at least 600 (0x0258). For 400kbps transfer rate, this value must be at least 78 (0x004E) and the sum of the high and low periods must be at least 150 (0x0096). Measured in 60MHz core clock periods, that is, approximately 16.7ns.

I²C_SCL_HIGH (0x342)—Read/Write

Table 51: I²C_SCL_HIGH

Bit	Default	Description
15:0	0x0114	**Value** Specifies the number of periods that SCL is asserted high by the MxL81434 I²C master. Note that another multi-master may assert SCL low before the MxL81434 high period is completed. For 100kbps transfer rate, this value must be at least 240 (0x00F0) and the sum of the high and low periods must be at least 600 (0x0258). For 400kbps transfer rate, this value must be at least 36 (0x0024) and the sum of the high and low periods must be at least 150 (0x0096). Measured in 60MHz core clock periods, that is, approximately 16.7ns.

EDGE_FUNC_SEL_0 (0x3C0)—Read/Write

Table 52: EDGE_FUNC_SEL_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: I/O is assigned to the UART/GPIO function. I/O pin controlled using UART registers. ■ 1: I/O is assigned to the EDGE function. I/O pin controlled using EDGE registers.

EDGE_DIR_0 (0x3C1)—Read/Write

Note that when setting direction of an EDGE I/O to output, the `EDGE_PULL_UP` for that I/O pin should also be disabled and when setting an EDGE I/O pin to input, the `EDGE_PULL_UP` for that I/O pin should also be enabled.

Table 53: EDGE_DIR_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: I/O pin assigned to EDGE function is configured as an input. ■ 1: I/O pin assigned to EDGE function is configured as an output.

EDGE_SET_0 (0x3C2)—Write-Only

Table 54: EDGE_SET_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: No effect. ■ 1: Set I/O pin assigned to EDGE function and configured as an output to a logic *1*.

EDGE_CLEAR_0 (0x3C3)—Write-Only

Table 55: EDGE_CLEAR_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: No effect. ■ 1: Clear I/O pin assigned to EDGE function and configured as an output to a logic *0*.

EDGE_STATE_0 (0x3C4)—Read/Write

Table 56: EDGE_STATE_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** Writing in this register sets or clears the EDGE I/O pin(s) configured as an output. Writing to an EDGE pin configured as an input has no effect. Reading this register returns the state of each I/O pin configured as an EDGE pin irrespective of whether it is configured as an input or output. Note that output transitions across multiple I/O pins may be slightly staggered. See "Enhanced Dedicated GPIO Entity (EDGE)" on page 16. ■ 0: Write clears the corresponding bit to a *0*. Read returns the current state. ■ 1: Write sets the corresponding bit to a *1*. Read returns the current state.

EDGE_TRI_STATE_0 (0x3C5)—Read/Write

Table 57: EDGE_TRI_STATE_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: I/O pin assigned to EDGE function and configured as an output is actively driven. ■ 1: I/O pin assigned to EDGE function and configured as an output is tri-stated.

EDGE_OPEN_DRAIN_0 (0x3C6)—Read/Write

Table 58: EDGE_OPEN_DRAIN_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** Note that MxL81434 open-drain outputs have a weak internal pull-up. ■ 0: I/O pin assigned to EDGE function and configured as an output is a push-pull output. ■ 1: I/O pin assigned to EDGE function and configured as an output is an open-drain output.

EDGE_PULL_UP_0 (0x3C7)—Read/Write

Table 59: EDGE_PULL_UP_0

Bit	Default	Description
15:0	0xFFFF	**E[15:0]** ■ 0: Disable internal pull-up resistor on I/O pin assigned to EDGE function and configured as an input. ■ 1: Enable internal pull-up resistor on I/O pin assigned to EDGE function and configured as an input.

EDGE_PULL_DOWN_0 (0x3C8)—Read/Write

Table 60: EDGE_PULL_DOWN_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** ■ 0: Disable internal pull-down resistor on I/O pin assigned to EDGE function and configured as an input. ■ 1: Enable internal pull-down resistor on I/O pin assigned to EDGE function and configured as an input.

EDGE_INTR_MASK_0 (0x3C9)—Read/Write

Table 61: EDGE_INTR_MASK_0

Bit	Default	Description
15:0	0x0000	**E[15:0]** Writing a *1* in this register enables the corresponding bit position EDGE I/O pin(s), when configured as an input, to generate an interrupt if the corresponding `EDGE_INTR_POS_EDGE` and/or `EDGE_INTR_NEG_EDGE` bit is enabled. An EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt.

EDGE_INTR_POS_EDGE_0 (0x3CA)—Read/Write

Table 62: EDGE_INTR_POS_EDGE_0

Bit	Default	Description
15:0	0xFFFF	**E[15:0]** Writing a *1* in this register enables an interrupt to be generated on the rising edge of the corresponding bit position EDGE I/O pin(s) configured as an input if the `EDGE_INTR_MASK` register is enabled for that pin. If the `EDGE_INTR_NEG_EDGE` register is also enabled, interrupts are generated on both edges. Writing to an EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt on rising edge. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt on rising edge if the corresponding `EDGE_INTR_MASK` bit is set.

EDGE_INTR_NEG_EDGE_0 (0x3CB)—Read/Write

Table 63: EDGE_INTR_NEG_EDGE_0

Bit	Default	Description
15:0	0xFFFF	**E[15:0]** Writing a *1* in this register enables an interrupt to be generated on the falling edge of the corresponding bit position EDGE I/O pin(s) configured as an input if the `EDGE_INTR_MASK` register is enabled for that pin. If the `EDGE_INTR_POS_EDGE` register is also enabled, interrupts are generated on both edges. Writing to an EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt on falling edge. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt on falling edge if the corresponding `EDGE_INTR_MASK` bit is set.

EDGE_FUNC_SEL_1 (0x3CC)—Read/Write

Table 64: EDGE_FUNC_SEL_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: I/O is assigned to the UART/GPIO function. I/O pin controlled using UART registers. ■ 1: I/O is assigned to the EDGE function. I/O pin controlled using EDGE registers.

EDGE_DIR_1 (0x3CD)—Read/Write

Note that when setting direction of an EDGE I/O to output, the `EDGE_PULL_UP` for that I/O pin should also be disabled and when setting an EDGE I/O pin to input, the `EDGE_PULL_UP` for that I/O pin should also be enabled.

Table 65: EDGE_DIR_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: I/O pin assigned to EDGE function is configured as an input. ■ 1: I/O pin assigned to EDGE function is configured as an output.

EDGE_SET_1 (0x3CE)—Write-Only

Table 66: EDGE_SET_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: No effect. ■ 1: Set I/O pin assigned to EDGE function and configured as an output to a logic *1*.

EDGE_CLEAR_1 (0x3CF)—Write-Only

Table 67: EDGE_CLEAR_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: No effect. ■ 1: Clear I/O pin assigned to EDGE function and configured as an output to a logic *0*.

EDGE_STATE_1 (0x3D0)—Read/Write

Table 68: EDGE_STATE_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** Writing in this register sets or clears the EDGE I/O pin(s) configured as an output. Writing to an EDGE pin configured as an input has no effect. Reading this register returns the state of each I/O pin configured as an EDGE pin irrespective of whether it is configured as an input or output. Note that output transitions across multiple I/O pins may be slightly staggered. See "Enhanced Dedicated GPIO Entity (EDGE)" on page 16. ■ 0: Write clears the corresponding bit to a *0*. Read returns the current state. ■ 1: Write sets the corresponding bit to a *1*. Read returns the current state.

EDGE_TRI_STATE_1 (0x3D1)—Read/Write

Table 69: EDGE_TRI_STATE_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: I/O pin assigned to EDGE function and configured as an output is actively driven. ■ 1: I/O pin assigned to EDGE function and configured as an output is tri-stated.

EDGE_OPEN_DRAIN_1 (0x3D2)—Read/Write

Table 70: EDGE_OPEN_DRAIN_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** Note that MxL81434 open-drain outputs have a weak internal pull-up. ■ 0: I/O pin assigned to EDGE function and configured as an output is a push-pull output. ■ 1: I/O pin assigned to EDGE function and configured as an output is an open-drain output.

EDGE_PULL_UP_1 (0x3D3)—Read/Write

Table 71: EDGE_PULL_UP_1

Bit	Default	Description
15:0	0xFFFF	**E[31:16]** ■ 0: Disable internal pull-up resistor on I/O pin assigned to EDGE function and configured as an input. ■ 1: Enable internal pull-up resistor on I/O pin assigned to EDGE function and configured as an input.

EDGE_PULL_DOWN_1 (0x3D4)—Read/Write

Table 72: EDGE_PULL_DOWN_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** ■ 0: Disable internal pull-down resistor on I/O pin assigned to EDGE function and configured as an input. ■ 1: Enable internal pull-down resistor on I/O pin assigned to EDGE function and configured as an input.

EDGE_INTR_MASK_1 (0x3D5)—Read/Write

Table 73: EDGE_INTR_MASK_1

Bit	Default	Description
15:0	0x0000	**E[31:16]** Writing a *1* in this register enables the corresponding bit position EDGE I/O pin(s), when configured as an input, to generate an interrupt if the corresponding EDGE_INTR_POS_EDGE and/or EDGE_INTR_NEG_EDGE bit is enabled. An EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt.

EDGE_INTR_POS_EDGE_1 (0x3D6)—Read/Write

Table 74: EDGE_INTR_POS_EDGE_1

Bit	Default	Description
15:0	0xFFFF	**E[31:16]** Writing a *1* in this register enables an interrupt to be generated on the rising edge of the corresponding bit position EDGE I/O pin(s) configured as an input if the EDGE_INTR_MASK register is enabled for that pin. If the EDGE_INTR_NEG_EDGE register is also enabled, interrupts are generated on both edges. Writing to an EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt on rising edge. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt on rising edge if the corresponding EDGE_INTR_MASK bit is set.

EDGE_INTR_NEG_EDGE_1 (0x3D7)—Read/Write

Table 75: EDGE_INTR_NEG_EDGE_1

Bit	Default	Description
15:0	0xFFFF	**E[31:16]** Writing a *1* in this register enables an interrupt to be generated on the falling edge of the corresponding bit position EDGE I/O pin(s) configured as an input if the EDGE_INTR_MASK register is enabled for that pin. If the EDGE_INTR_POS_EDGE register is also enabled, interrupts are generated on both edges. Writing to an EDGE pin configured as an output has no effect. ■ 0: I/O pin does not generate an interrupt on falling edge. ■ 1: I/O pin assigned to EDGE function and configured as an input generates an interrupt on falling edge if the corresponding EDGE_INTR_MASK bit is set.

EDGE_PWM0_CTRL (0x3D8)—Read/Write

Table 76: EDGE_PWM0_CTRL

Bit	Default	Description
15:9	0x00	**Reserved** These bits are reserved and should be written as *0*.
8:6	0x0	**Cmd** ■ 000: Idle. Output pin remains at same state. ■ 001: Undefined, do not use. ■ 010: Undefined, do not use. ■ 011: Undefined, do not use. ■ 100: Assert logic *0*. ■ 101: One-shot—If previous state is assert *0*, one-shot pulse is high. If previous state is assert *1*, one-shot pulse is low. ■ 110: Free run output. ■ 111: Assert logic *1*.
5	0	**Enable** ■ 0: PWM0 output is not enabled. ■ 1: PWM0 output is enabled on pin specified in `Pin` field using mode specified in `Cmd` field.
4:0	0x00	**Pin** Specifies which pin (E31–E0) is assigned to PWM0 output.

EDGE_PWM0_HIGH (0x3D9)—Read/Write

Table 77: EDGE_PWM0_HIGH

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as *0*.
11:0	0x001	**Value** This register specifies the high period for PWM0 in increments of 266.667ns. High period must be in the range of 1 to 4095 (266.667ns to 1.092ms).

EDGE_PWM0_LOW (0x3DA)—Read/Write

Table 78: EDGE_PWM0_LOW

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as *0*.
11:0	0x001	**Value** This register specifies the low period for PWM0 in increments of 266.667ns. Low period must be in the range of 1 to 4095 (266.667ns to 1.092ms).

EDGE_PWM1_CTRL (0x3DB)—Read/Write

Table 79: EDGE_PWM1_CTRL

Bit	Default	Description
15:9	0x00	**Reserved** These bits are reserved and should be written as *0.*
8:6	0x0	**Cmd** ■ 000: Idle. Output pin remains at same state. ■ 001: Undefined, do not use. ■ 010: Undefined, do not use. ■ 011: Undefined, do not use. ■ 100: Assert logic *0.* ■ 101: One-shot—If previous state is assert *0,* one-shot pulse is high. If previous state is assert *1*, one-shot pulse is low. ■ 110: Free run output. ■ 111: Assert logic *1.*
5	0	**Enable** ■ 0: PWM1 output is not enabled. ■ 1: PWM1 output is enabled on pin specified in `Pin` field using mode specified in `Cmd` field.
4:0	0x00	**Pin** Specifies which pin (E31–E0) is assigned to PWM1 output.

EDGE_PWM1_HIGH (0x3DC)—Read/Write

Table 80: EDGE_PWM1_HIGH

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as *0.*
11:0	0x001	**Value** This register specifies the high period for PWM1 in increments of 266.667ns. High period must be in the range of 1 to 4095 (266.667ns to 1.092ms).

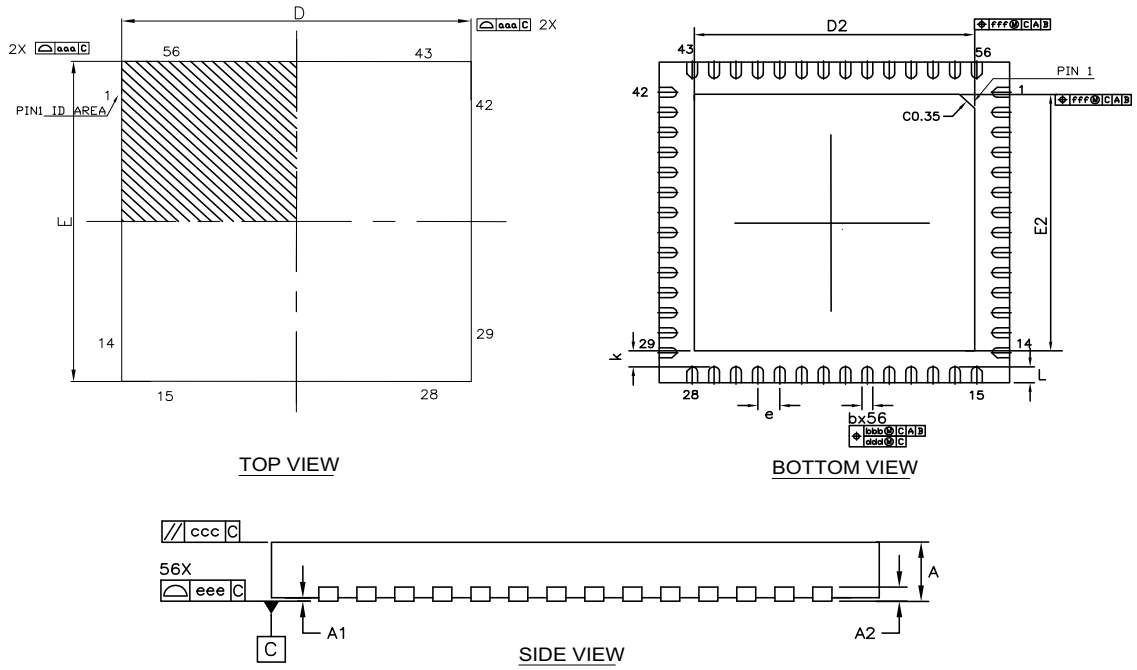
EDGE_PWM1_LOW (0x3DD)—Read/Write

Table 81: EDGE_PWM1_LOW

Bit	Default	Description
15:12	0x0	**Reserved** These bits are reserved and should be written as *0.*
11:0	0x001	**Value** This register specifies the low period for PWM1 in increments of 266.667ns. Low period must be in the range of 1 to 4095 (266.667ns to 1.092ms).

Mechanical Dimensions

56-Pin QFN



DIM / SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	---	0.20Ref	---
b	0.18	0.25	0.30
D		8.00 BSC	
E		8.00 BSC	
e		0.50 BSC	
D2	6.30	6.40	6.50
E2	6.30	6.40	6.50
L	0.30	0.40	0.50
K	0.40	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		56	

TERMINAL DETAILS

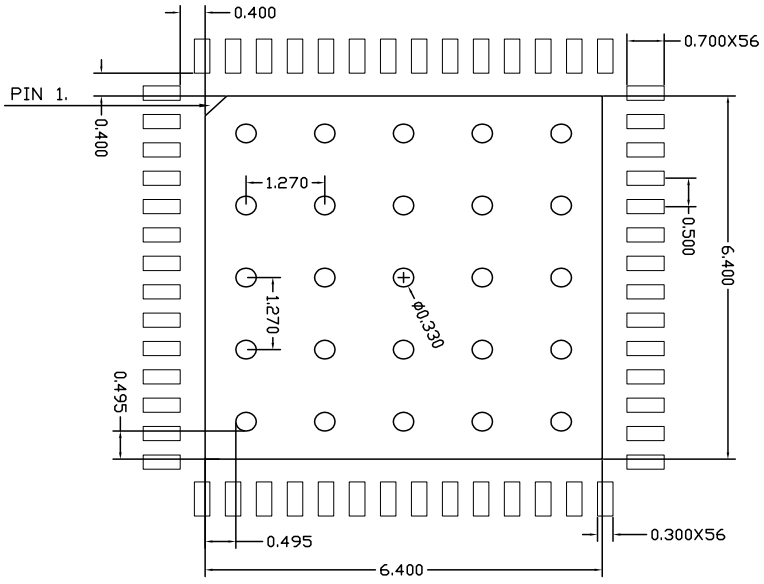
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

Drawing No.: POD-00000129
Revision: B

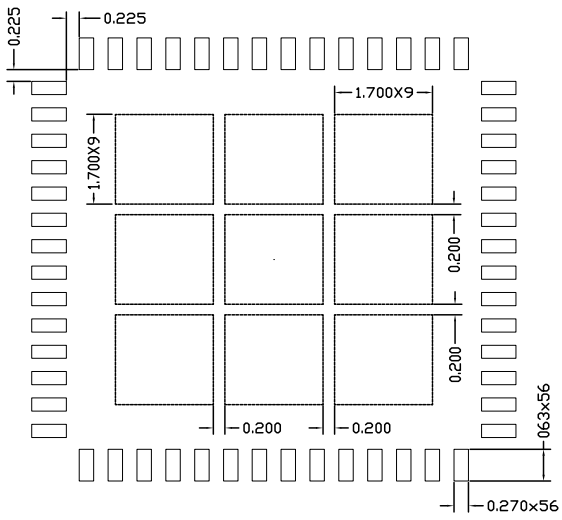
Figure 7: Mechanical Dimensions—56-Pin QFN

Recommended Land Pattern and Stencil

56-Pin QFN



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000129

Revision: B

Figure 8: Recommended Land Pattern and Stencil—56-Pin QFN

Ordering Information

Table 82: Ordering Information

Ordering Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
MXL81434I-AQB-R	–40°C to 85°C	Yes	56-Pin QFN	Tray
MXL81434I-AQB-EVK-1	MXL81434 Evaluation Kit			

Note: For more information about part numbers, as well as the most up-to-date ordering information and additional information on environmental rating, go to www.maxlinear.com/MxL81434.

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