SP7650

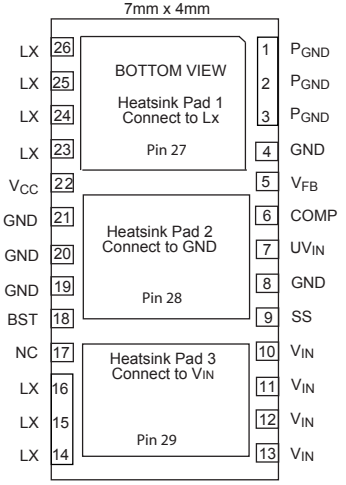
Wide Input Voltage Range 3A, 300kHz, Buck Regulator

PowerBlox™

FEATURES

- 2.5V to 28V Step Down Achieved Using Dual Input
- Output Voltage down to 0.8V
- 3A Output Capability
- Built in Low R_{DSON} Power Switches (40 mΩ typ)
- Highly Integrated Design, Minimal Components
- 300 kHz Fixed Frequency Operation
- UVLO Detects Both V_{CC} and V_{IN}
- Over Temperature Protection
- Short Circuit Protection with Auto-Restart
- Wide BW Amp Allows Type II or III Compensation
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than **95%** Possible
- Asynchronous Start-Up into a Pre-Charged Output
- Small 7mm x 4mm DFN Package
- U.S. Patent #6,922,041

SP7650
DFN PACKAGE
7mm x 4mm



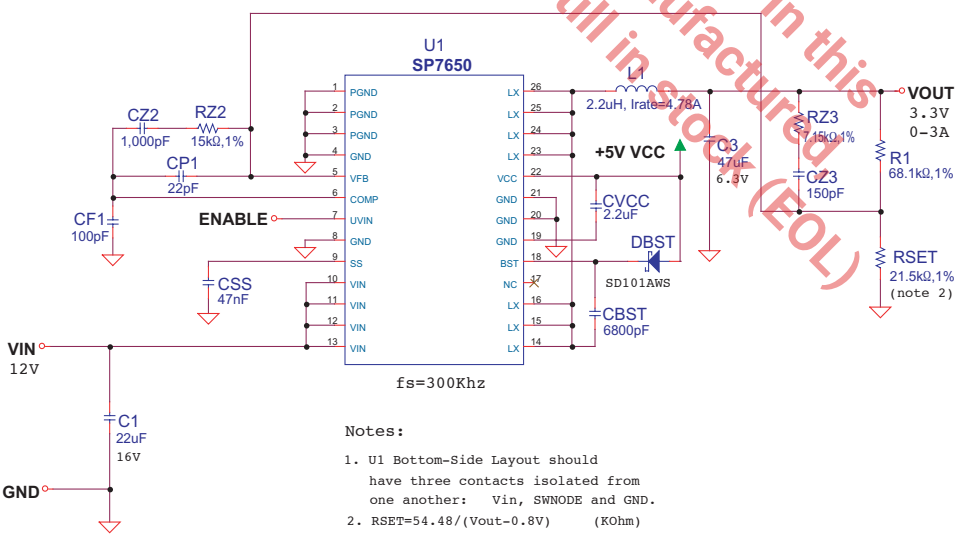
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DESCRIPTION

The SP7650 is a synchronous step-down switching regulator optimized for high efficiency. The part is designed to be especially attractive for dual supply, 12V or 24V distributed power systems stepped down with 5V used to power the controller. This lower V_{CC} voltage minimizes power dissipation in the part and is used to drive the top switch. The SP7650 is designed to provide a fully integrated buck regulator solution using a fixed 300kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown and output short circuit protection. The SP7650 is available in the space saving DFN package.

TYPICAL APPLICATION CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V
V_{IN} 30V
I_{LX} 5A
BST 35V
LX-BST ..... -0.3V to 7V
LX ..... -1V to 30V

All other pins ..... -0.3V to V_{CC}+0.3V

Storage Temperature ..... -65°C to 150°C
Power Dissipation ..... Internally Limited via OTP
ESD Rating ..... 2kV HBM
Thermal Resistance Θ_{JC} ..... 5°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: -40°C < T_{AMB} < 85°C, -40°C< Tj< 125°C, 4.5V < V_{CC} < 5.5V, 3V< Vin< 28V, BST=LX + 5V, LX = GND = 0.0V, UVIN = 3.0V, CV_{CC} = 1µF, C_{COMP} = 0.1µF, C_{SS} = 50nF, Typical measured at V_{CC} = 5V. The ♦ denotes the specifications which apply over the full temperature range, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
QUIESCENT CURRENT						
V_{CC} Supply Current (No switching)		1.5	3	mA		V_{FB} = 0.9V
V_{CC} Supply Current (switching)		4	6	mA	♦	
BST Supply Current (No switching)		0.2	0.4	mA		V_{FB} = 0.9V
BST Supply Current (switching)	4	4	6	mA	♦	
PROTECTION: UVLO						
V_{CC} UVLO Start Threshold	4.00	4.25	4.5	V		
V_{CC} UVLO Hysteresis	100	200	300	mV		
UV_{IN} Start Threshold	2.3	2.5	2.65	V	♦	
UV_{IN} Hysteresis	200	300	400	mV		
UV_{IN} Input Current			1	µA		UV_{IN} = 3.0V
ERROR AMPLIFIER REFERENCE						
Error Amplifier Reference	0.792	0.800	0.808	V		2X Gain Config., Measure V_{FB}; V_{CC} = 5 V, T = 25°C
Error Amplifier Reference Over Line and Temperature	0.788	0.800	0.812	V	♦	
Error Amplifier Transconductance		6		mA/V		
Error Amplifier Gain		60		dB		No Load
COMP Sink Current		150		µA		V_{FB}= 0.9V, COMP = 0.9V
COMP Source Current		150		µA		V_{FB}= 0.7V, COMP = 2.2V
V_{FB} Input Bias Current		50	200	nA		V_{FB}= 0.8V
Internal Pole		4		MHz		
COMP Clamp		2.5		V		V_{FB}= 0.7V, T_A = 25°C
COMP Clamp Temp. Coefficient		-2		mV/°C		

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ELECTRICAL SPECIFICATIONS

Unless otherwise specified: -40°C < T_{AMB} < 85°C, -40°C< Tj< 125°C, 4.5V < V_{CC} < 5.5V, 3V< Vin< 28V, BST=LX + 5V, LX = GND = 0.0V, UVIN = 3.0V, CV_{CC} = 1µF, C_{COMP} = 0.1µF, C_{SS} = 50nF, Typical measured at V_{CC} = 5V.
The ♦ denotes the specifications which apply over the full temperature range, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS		CONDITIONS
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH						
Ramp Amplitude	0.92	1.1	1.28	V		
RAMP Offset		1.1		V		T_A = 25˚C, RAMP COMP until GH starts Switching
RAMP offset Temp. Coefficient		-2		mV/˚C		
GH Minimum Pulse Width		90	180	ns	♦	
Maximum Controllable Duty Ratio	92	97		%		Maximum Duty Ratio Measured just before pulsing begins
Maximum Duty Ratio	100			%		Valid for 20 cycles
Internal Oscillator Ratio	240	300	360	kHz	♦	
TIMERS: SOFTSTART						
SS Charge Current:		10		µA		
SS Discharge Current:	1			mA	♦	Fault Present, SS = 0.2V
PROTECTION: SHORT CIRCUIT & THERMAL						
Short Circuit Threshold Voltage	0.2	0.25	0.3	V	♦	Measured V_{REF} (0.8V) - V_{FB}
Hiccup Timeout		200		ms		V_{FB} = 0.5V
Number of Allowable Clock Cycles at 100% Duty Cycle		20		Cycles		
Minimum GL Pulse After 20 Cycles		0.5		Cycles		V_{FB} = 0.7V
Thermal Shutdown Temperature		145		˚C		V_{FB} = 0.7V
Thermal Recovery Temperature		135		˚C		
Thermal Hysteresis		10		˚C		
OUTPUT: POWER STAGE						
High Side Switch R_{DSON}		40		mΩ		V_{CC} = 5V ; I_{OUT} = 3A; T_{AMB} = 25˚C
Synchrous Lowside Switch R_{DSON}		40		mΩ		V_{CC} = 5V ; I_{OUT} = 3A ; T_{AMB} = 25˚C
Maximum Output Current	3			A		

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PIN DESCRIPTION

Pin #	Pin Name	Description
1-3	P_{GND}	Ground connection for the synchronous rectifier
4,8,19-21	GND	Ground Pin. The control circuitry of the IC and lower power driver are referenced to this pin. Return separately from other ground traces to the (-) terminal of Cout.
5	V_{FB}	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever V_{FB} drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
6	COMP	Output of the Error Amplifier. It is internally connected to the inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or V_{FB} to stabilize the voltage mode loop.
7	UVIN	UVLO input for Vin voltage. Connect a resistor divider between V_{IN} and UV_{IN} to set minimum operating voltage.
9	SS	Soft Start. Connect an external capacitor between SS and GND to set the soft start rate based on the 10μA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
10-13	V_{IN}	Input connection to the high side N-channel MOSFET. Place a decoupling capacitor between this pin and PGND.
14-16,23-26	LX	Connect an inductor between this pinand V_{OUT}
17	NC	No Connect
18	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Typical Application Circuit on page 1. High side driver is connected between BST pin and SWN pin.
22	Vcc	Input for external 5V bias supply

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THEORY OF OPERATION

General Overview

The SP7650 is a fixed frequency, voltage mode, synchronous PWM regulator optimized for high efficiency. The part has been designed to be especially attractive for high voltage applications utilizing 5V to power the controller and 2.5V to 28V for step down conversion.

The heart of the SP7650 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference, present on the positive terminal of the error amplifier permits the programming of the output voltage down to 0.8V via the V_{FB} pin. The output of the error amplifier, COMP, compared to a 1.1V peak-to-peak ramp is responsible for trailing edge PWM control. This voltage ramp, and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 300kHz.

The SP7650 contains two unique control features that are very powerful in distributed applications. First, asynchronous driver control is enabled during start up, to prohibit the low side switch from pulling down the output until the high side switch has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side switch is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios.

The SP7650 also contains a number of valuable protection features. Programmable V_{IN} UVLO allows the user to set the exact value at which the conversion voltage can safely begin down conversion, and an internal V_{CC} UVLO which ensures that the controller itself has enough voltage to operate properly. Other protection

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features include thermal shutdown and short-circuit detection. In the event that either a thermal, short-circuit, or UVLO fault is detected, the SP7650 is forced into an idle state where the output drivers are held off for a finite period before a restart is attempted.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the positive terminal of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor.

$$I_{VIN} = C_{OUT} * (\Delta V_{OUT} / \Delta T_{SOFT\text{-}START})$$

The SP7650 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10uA pull up current present at the SS pin and the 0.8V reference voltage. Therefore, the excess source can be redefined as:

$$IV_{IN} = C_{OUT} * (\Delta V_{OUT} * 10\mu A / (C_{SS} * 0.8V)$$

Under Voltage Lock Out (UVLO)

The SP7650 contains two separate UVLO comparators to monitor the bias (V_{CC}) and conversion (V_{IN}) voltages independently. The V_{CC} UVLO threshold is internally set to 4.25V, whereas the V_{IN} UVLO threshold is programmable through the UVIN pin. When the UVIN pin is greater than 2.5V, the SP7650 is permitted to start up pending the removal of all other faults. Both the V_{CC} and V_{IN} UVLO comparators have been designed with hysteresis to prevent noise from resetting a fault.

Thermal and Short-Circuit Protection

Because the SP7650 is designed to drive large output current, there is a chance that the power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

A short-circuit detection comparator has also been included in the SP7650 to protect against an accidental short at the output of the power converter. This comparator constantly monitors the positive and negative terminals of the error amplifier, and if the V_{FB} pin falls more than 250mV (typical) below the positive reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP7650 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Handling of Faults:

Upon the detection of power (UVLO), thermal, or short-circuit faults, the SP7650 is forced into an idle state where the SS and COMP pins are pulled low and both switches are held off. In the event of UVLO fault, the SP7650 remains in this idle state until the UVLO fault is removed. Upon the detection of a thermal or short-circuit fault, an internal 200ms timer is activated. In the event of a short-circuit fault, a re-start is attempted immediately after the 200ms timeout expires. Whereas, when a thermal fault is detected the 200ms delay continuously recycles and a re-start cannot be attempted until the thermal fault is removed and the timer expires.

Error Amplifier and Voltage Loop

Since the heart of the SP7650 voltage error loop is a high performance, wide bandwidth transconductance amplifier. Because of the amplifier's current limited (+/-150µA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. If a simple, single pole, single zero response is

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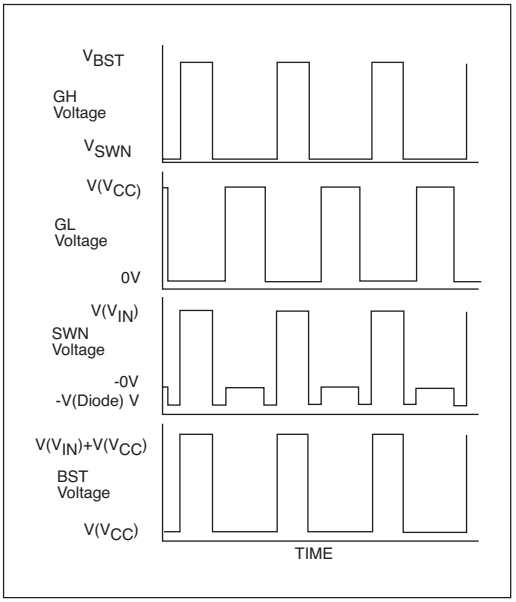
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desired, then compensation can be as simple as an RC circuit to Ground. If a more complex compensation is required, then the amplifier has enough bandwidth (45° at 4 MHz) and enough gain (60dB) to run Type III compensation schemes with adequate gain and phase margins at crossover frequencies greater than 50kHz.

The common mode output of the error amplifier is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.1V and 2.2V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is an asynchronous startup mode. Basically, the synchronous rectifier cannot turn on unless the high side switch has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes. The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the high side NFET is on for 20 continuous clock cycles, a reset is given to the PWM flip-flop half way through the 21st cycle. This forces GL to rise for the cycle, in turn refreshing the BST capacitor. The boost capacitor is used to generate a high voltage drive supply for the high side switch, which is 5V above V_{IN}.

Power MOSFETs

The SP7650 contains a pair of integrated low resistance N-channel switches designed to drive up to 3A of output current. Care should be taken to de-rate the output current based on the thermal conditions in the system such as ambient temperature, airflow and heat sinking. Maximum output current could be limited by thermal limitations of a particular application by taking advantage of the integrated-over-temperature protective scheme employed in the SP7650. The SP7650 incorporates a built-in over-temperature protection to prevent internal overheating.



Setting Output Voltages

The SP7650 can be set to different output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V. Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$V_{out} = 0.80V \left(R1 / R2 + 1 \right) \Rightarrow$$
$$R2 = R1 / \left[\left(V_{out} / 0.80V \right) - 1 \right]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of the R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that 50KΩ < R1 < 100KΩ for overall system loop stability.

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Inductor Selection

There are many factors to consider in selecting the inductor including core material, inductance vs. frequency, current handling capability, efficiency, size and EMI. In a typical SP7650 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and require more output capacitance to smooth out the larger ripple current. The inductor must be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} F_S K_r I_{OUT(\max)}}$$

where:

f_S = switching frequency

Kr = ratio of the AC inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT}(V_{IN(\max)} - V_{OUT})}{V_{IN(\max)} F_S L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current...

$$I_{PEAK} = I_{OUT(\max)} + \frac{I_{PP}}{2}$$

...and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable AC core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, although more expensive, and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss while the designer is only required to prevent saturation. In general, ferrite or molypermalloy materials are a better choice for all but the most cost sensitive applications.

Optimizing Efficiency

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetics vendor. Proper inductor selection can affect the resulting power supply efficiency by more than 15%!

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(Cu)} = I^2_{L(RMS)} R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(max)} \sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT(max)}}\right)^2}$$

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Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP7650 adjusts the inductor current to the new value.

In order to maintain V_{OUT}, the capacitance must be large enough so that the output voltage is held up while the inductor current ramps to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100%/0% duty cycle capability provided by the SP7650 when exposed to output load transients, the output capacitor is typically chosen for ESR, not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PK\text{-}PK}}$$

where:

ΔV_{OUT} = Peak to Peak Output Voltage Ripple

$I_{PK\text{-}PK}$ = Peak to Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{\left(\frac{I_{PP}\,(1-D)}{C_{OUT} F_S}\right)^2 + (I_{PP} R_{ESR})^2}$$

F_S = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. More accurately the current wave form is trapezoidal, given a finite turn-on and turn-off, switch transition slope. Most of this current is supplied by the input bypass capacitors. The RMS current handling capability of the input capacitors is determined at maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(RMS)} = I_{OUT(max)} \sqrt{D(1 - D)}$$

The worse case occurs when the duty cycle D is 50% and gives an RMS current value equal to $I_{OUT}/2$.

Select input capacitors with adequate ripple current rating to ensure reliable operation.

The power dissipated in the input capacitor is:

$$P_{CIN} = I^2_{CIN(rms)} R_{ESR(CIN)}$$

This can become a significant part of power losses in a converter and hurt the overall energy transfer efficiency. The input voltage ripple primarily depends on the input capacitor ESR and capacitance. Ignoring the inductor ripple current, the input voltage ripple can be determined by:

$$\Delta V_{IN} = I_{out(\max)} R_{ESR(CIN)} + \frac{I_{OUT(MAX)} V_{OUT} (V_{IN} - V_{OUT})}{F_S C_{IN} V_{IN}^2}$$

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The capacitor type suitable for the output capacitors can also be used for the input capacitors. However, exercise additional caution when tantalum capacitors are used. Tantalum capacitors are known for catastrophic failure when exposed to surge current, and input capacitors are prone to such surge current when power supplies are connected "live" to low impedance power sources. Although tantalum capacitors have been successfully employed at the input, it is generally not recommended.

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Loop Compensation Design

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to cross over at the desired frequency cut-off (FCO), the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate loop frequency response such that its crossover gain at 0db results in a slope of -20db/dec.

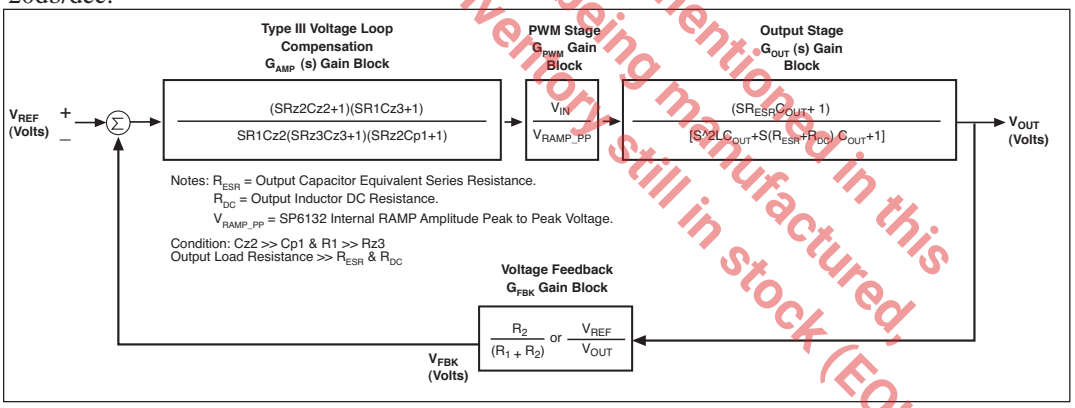
The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardizes the power supply stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency or 60kHz. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi\, C_{OUT}\, R_{ESR}}$$

The next step is to calculate the complex conjugate poles contributed by the LC output filter,

$$f_{P(LC)} = \frac{1}{2\pi \sqrt{L\, C_{OUT}}}$$

When the output capacitors are of a Ceramic Type, the SP7650 Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an underdamped resonance of the output filter at the double pole frequency.



SP7650 Voltage Mode Control Loop with Loop Dynamic

Definitions:

R_{ESR} = Output Capacitor Equivalent Series Resistance

R_{DC} = Output Inductor DC Resistance

R_{RAMP_PP} = SP7650 internal RAMP Amplitude Peak to Peak Voltage

Conditions:

C_Z2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> R_{ESR} and R_{DC}

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SP765X Thermal Resistance

The SP765X family has been tested with a variety of footprint layouts along with different copper area and thermal resistance has been measured. The layouts were done on 4 layer FR4 PCB with the top and bottom layers using 3oz copper and the power and ground layers using 1oz copper.

For the Minimum footprint, only about 0.1 square inch (of 3 ounces of) Copper was used on the top or footprint layer, and this layer had no vias to connect to the 3 other layers. For the Medium footprint, about 0.7 square inches (of 3 ounces of) Copper was used on the top layer, but vias were used to connect to the other 3 layers. For the Maximum footprint, about 1.0 square inch (of 3 ounces of) Copper was used on the top layer and many vias were used to connect to the 3 other layers.

The results show that only about 0.7 square inches (of 3 ounces of) Copper on the top layer and vias connecting to the 3 other layers are needed to get the best thermal resistance of 36°C/W. Adding area on the top beyond the 0.7 square inches did not reduce thermal resistance.

Using a minimum of 0.1 square inches of (3 ounces of) Copper on the top layer with no vias connecting to the 3 other layers produced a thermal resistance of 44°C/W. This thermal impedance is only 22% higher than the medium and large footprint layouts, indicating that space constrained designs can still benefit thermally from the Powerblox family of ICs. This indicates that a minimum footprint of 0.1 square inch, if used on a 4 layer board, can produce 44°C/W thermal resistance. This approach is still very worthwhile if used in a space constrained design.

The following page shows the footprint layouts from an ORCAD file. The thermal data was taken for still air, not with forced air. If forced air is used, some improvement in thermal resistance would be seen.

SP765X Thermal Resistance

4 Layer Board:
Top Layer 3ounces Copper
GND Layer 1ounce Copper
Power Layer 1ounce Copper
Bottom Layer 3ounces Copper

Minimum Footprint: 44°C/W
Top Layer: 0.1 square inch
No Vias to other 3 Layers

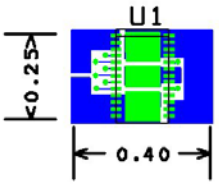
Medium Footprint: 36°C/W
Top Layer: 0.7 square inch
Vias to other 3 Layers

Maximum Footprint: 36°C/W
Top Layer: 1.0 square inch
Vias to other 3 Layers

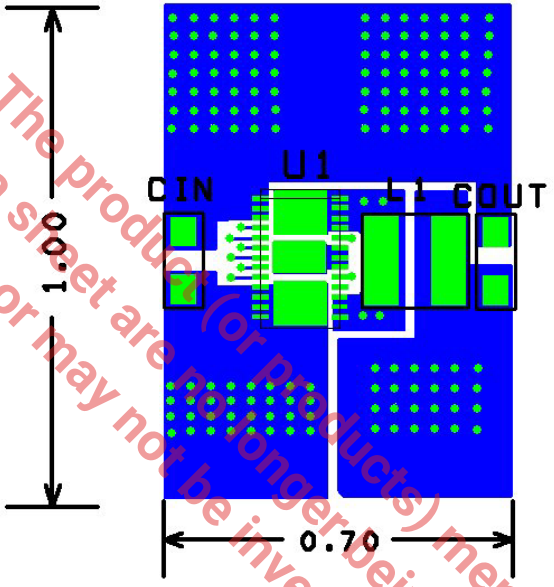
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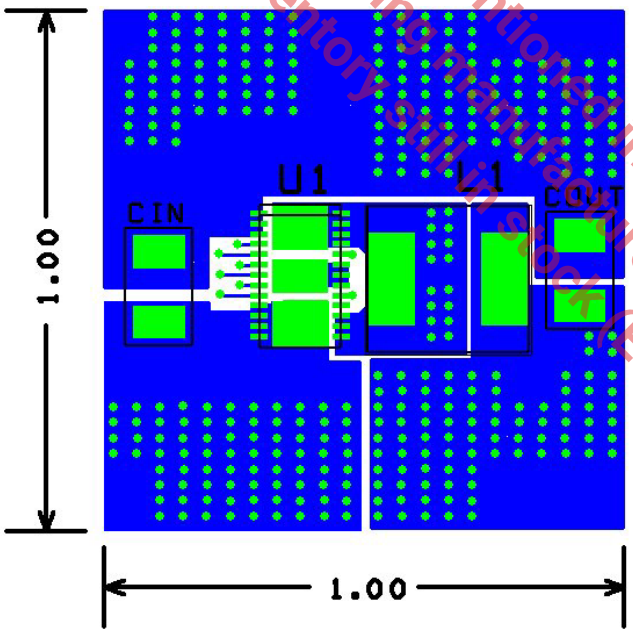
MINIMUM FOOTPRINT = 0.10 SQ IN.



MEDIUM FOOTPRINT = 0.70 SQ IN.

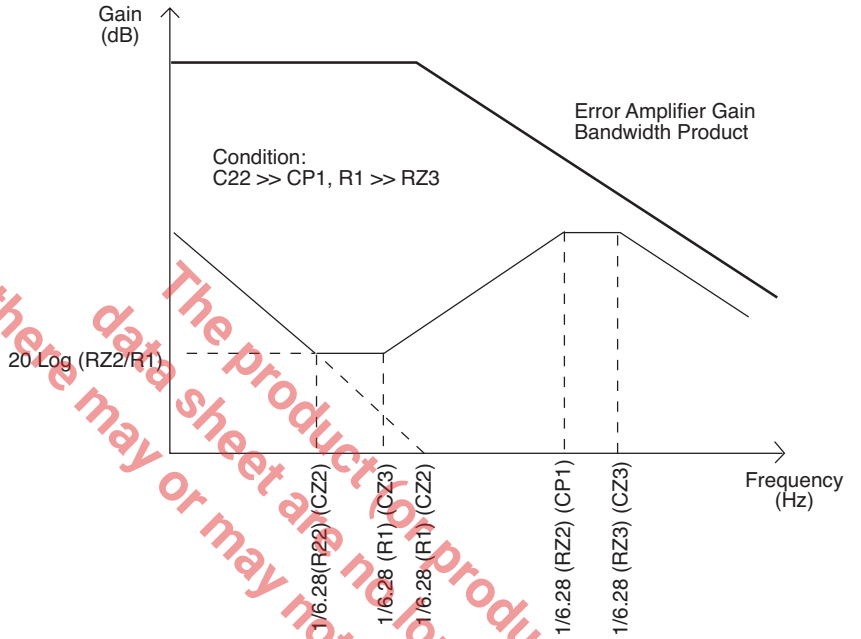


The product(s) mentioned in this data sheet are no longer being manufactured, there may or may not be inventory still in stock (EOL)



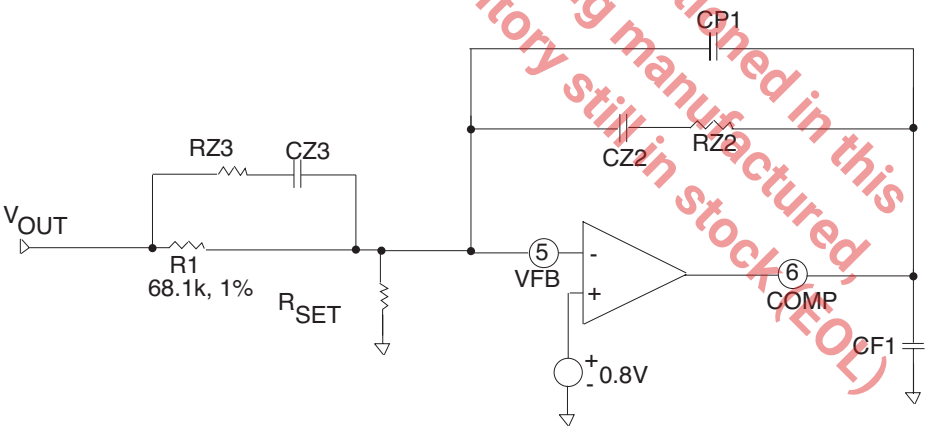
MAXIMUM FOOTPRINT = 1.0 SQ IN.

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Bode Plot of Type III Error Amplifier Compensation.

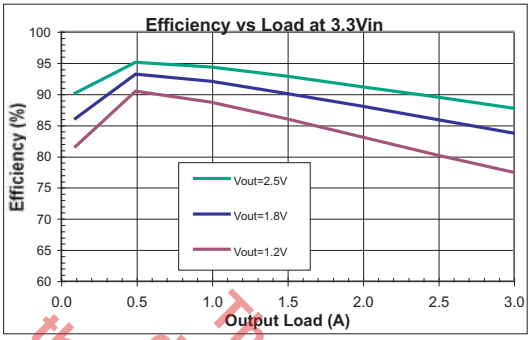
The product (or products) mentioned in this data sheet are no longer being manufactured, there may or may not be inventory still in stock (EOL)

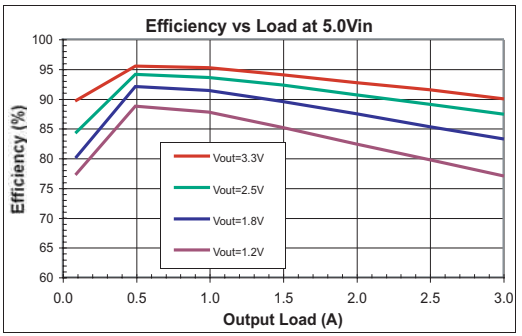


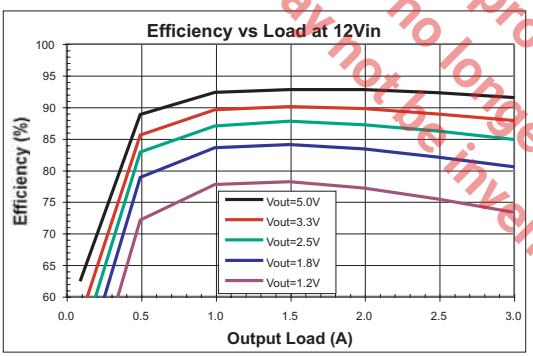
$$R_{SET} = 54.48/(V_{OUT} - 0.8) \quad (k\Omega)$$

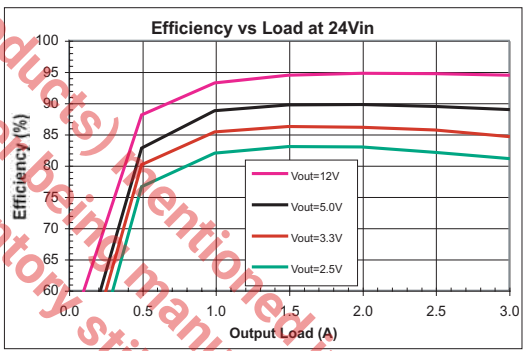
Type III Error Amplifier Compensation Circuit

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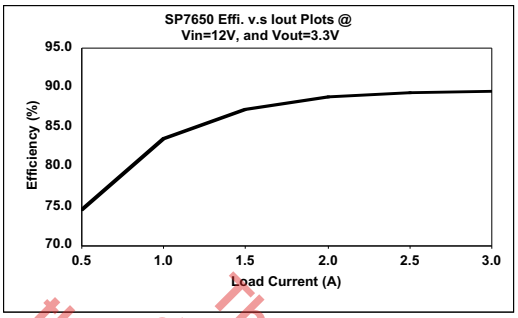


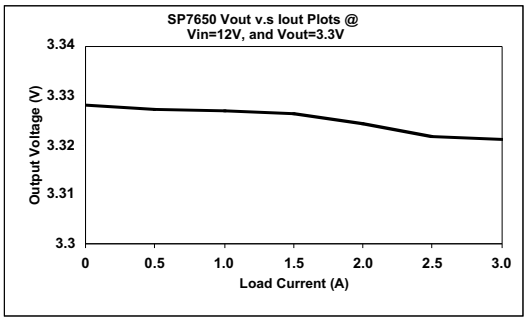




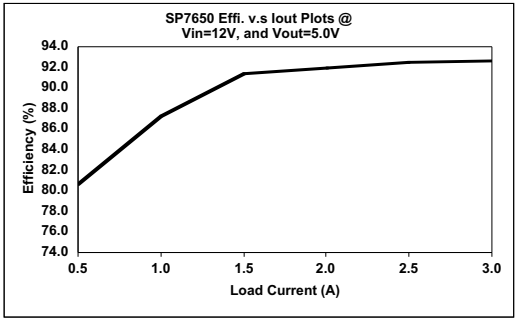
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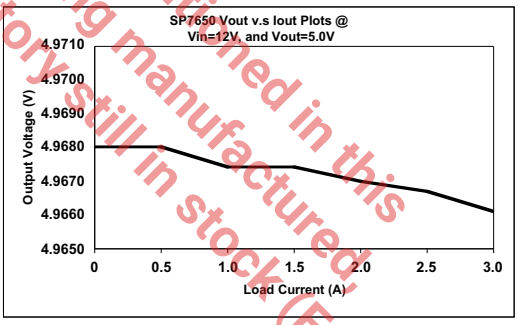
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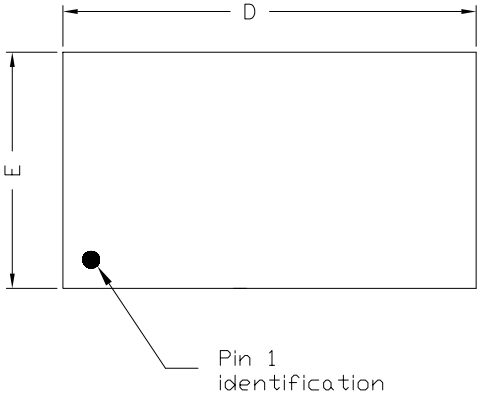




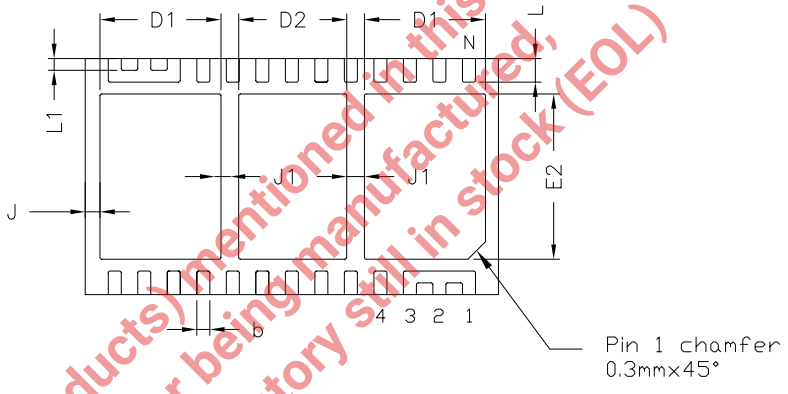
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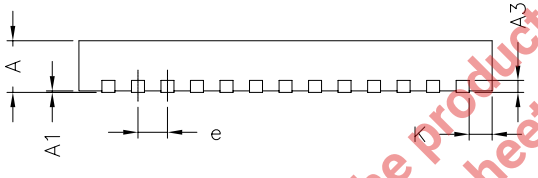
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	02/16/06	JL
B	DRAWING FORMAT MODIFICATION	05/22/06	JL

Top View



Bottom View





Side View

26LD 7 X 4 MM DFN -- (OPTION 1)*						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	—	0.05	0.000	—	0.002
A3	0.18	0.20	0.23	0.007	0.008	0.009
b	0.17	0.22	0.27	0.007	0.009	0.011
D	6.95	7.00	7.05	0.274	0.276	0.278
D1	2.00	2.05	2.10	0.079	0.081	0.083
D2	1.78	1.83	1.88	0.070	0.072	0.074
e	0.50 BSC			0.020 BSC		
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.73	2.78	2.83	0.108	0.109	0.111
J	0.20	0.25	0.30	0.008	0.010	0.012
J1	0.25	0.30	0.35	0.010	0.012	0.014
K	0.34	0.39	0.44	0.013	0.015	0.017
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.20 BSC			0.008 BSC		
N	26			26		

* Refer to product datasheet for POD option being used

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Solved by Sipex	SIPEX CORPORATION	
	26LD 7X4 DFN PACKAGE OUTLINE	
Packaging Approval:	Drawing No: 26LD 7x4 DFN	
By: JL / Date: 05/22/06	Revision: B	Sheet: 1 OF 3

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Part Number	Temperature	Package
SP7650ER	-40°C to +85°C	26 Pin 7 X 4 DFN
SP7650ER-L	-40°C to +85°C	(Lead Free) 26 Pin 7 X 4 DFN
SP7650ER/TR	-40°C to +85°C	26 Pin 7 X 4 DFN
SP7650ER-L/TR	-40°C to +85°C	(Lead Free) 26 Pin 7 X 4 DFN

Bulk Pack minimum quantity is 500.
/TR = Tape and Reel. Pack quantity is 3,000 DFN.

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Solved by Sipex™

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