XRT81L27

SEVEN CHANNEL E1 LINE INTERFACE UNIT WITH CLOCK RECOVERY

JULY 2001 REV. P1.0.3

GENERAL DESCRIPTION

The XRT81L27 is an optimized seven-channel, analog, 3.3V, line interface unit, fabricated using low power CMOS technology. The device contains seven independent E1 channels, including data and clock recovery circuits. It is primarily targeted towards the SDH multiplexers that accomodate TU12 Tributary Unit Frames. Line cards in these units mutiplex 21 E1 channels into higher SDH rates. Devices with seven E1 interfaces such as the XRT81L27 provide the most efficient method of implementing 21-channel line cards. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa.

The receiver input accepts transformer or capacitor coupled signals, while the transmitter is coupled to the line using a 1:2 step-up transformer. The same transformer configuration can be used for both balanced 120 Ω and unbalanced 75 Ω interfaces. The Receiver Loss of Signal Detection is compliant to G.775 and in Host Mode, the number of zeros received before LOS is declared can be increased to 4096 bits. This feature provides the user with the flexability to implement LOS specifications that require greater than G.775 requirements

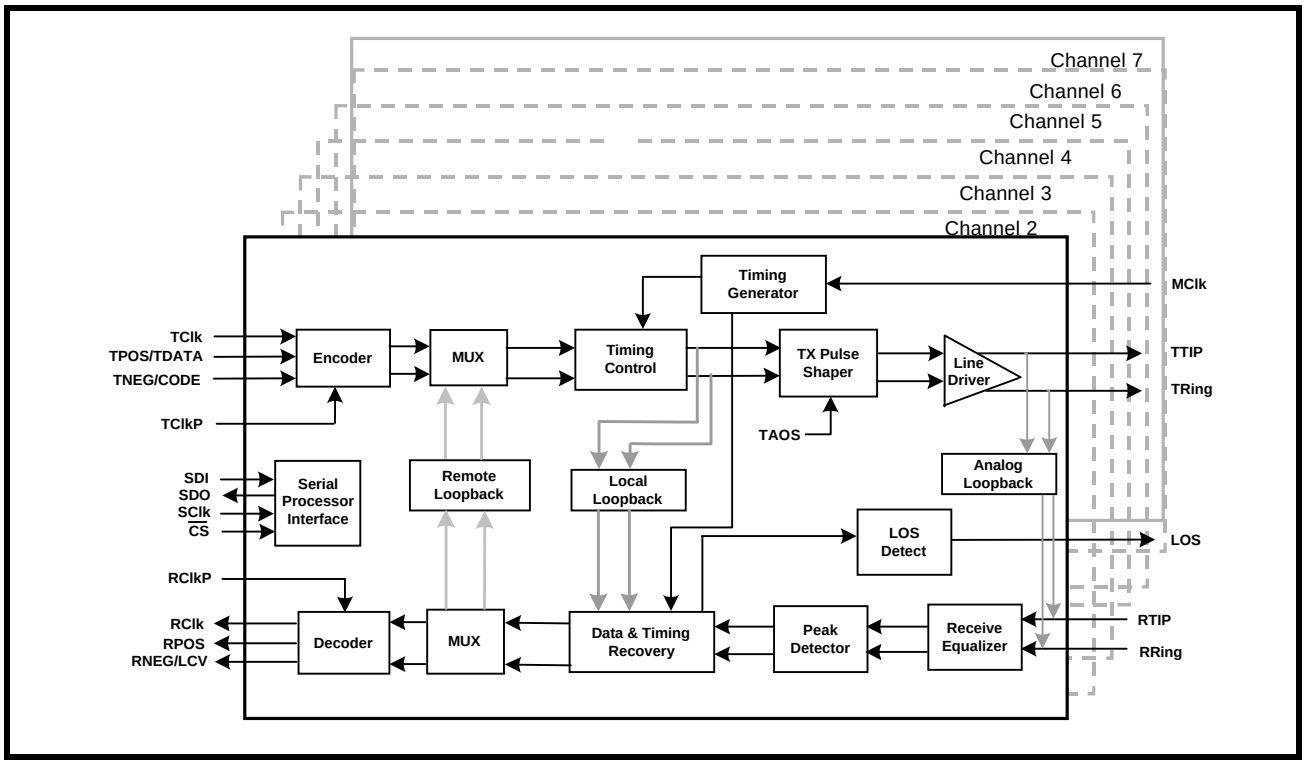
FEATURES

- Consists of Seven (7) Independent E1 (CEPT) Line Interface Units (Transmitter and Receiver)
- Generates Transmit Output Pulses that are Compliant with the ITU-T G.703 Pulse Template Requirement for 2.048Mbps (E1) Rates
- On-Chip Pulse Shaping for both 75Ω and 120Ω line drivers
- Receiver Can Either Be Transformer or Capacitive-Coupled to the Line
- Detects and Clears LOS (Loss of Signal) Per ITU-T G.775
- Compliant with the ITU-T G.823 Jitter Tolerance Requirements

APPLICATIONS

- IPDH Multiplexers
- SDH Multiplexers
- Digital Cross-Connect Systems
- DECT (Digital European Cordless Telephone) Base Stations
- CSU/DSU Equipment

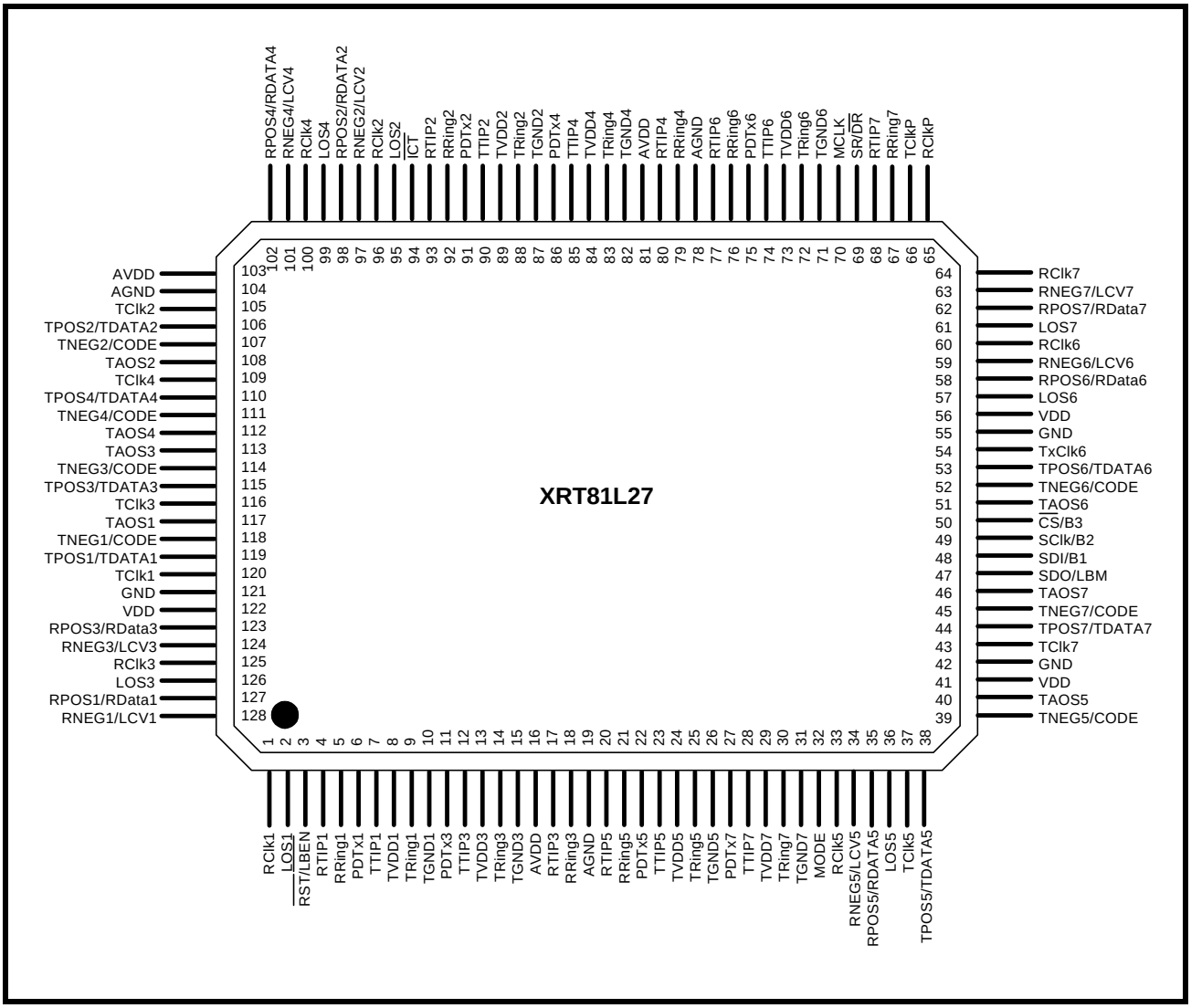
FIGURE 1. BLOCK DIAGRAM



ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT81L27IV	128 Lead TQFP	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT81L27



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PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
1	RClk1	O	**Receiver 1 Clock Output**
2	LOS1	O	**Receiver 1 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
3	$\overline{\text{RST}}$/$\overline{\text{LBEN}}$	I	**Reset (Active-low):** In **Host Mode**, tie this pin "Low" to reset the serial register contents to zero. Loop-back Enable (Active-low): In **Hardware Mode**, when this pin is tied "Low", Loop-back mode is enabled. ***NOTES:*** 1. *See description of pin 47 to pin 50 for Local or Remote Loop-back selection.* 2. *Internally pulled-high with 50KΩ.*
4	RTIP1	I	**Receiver 1 Bipolar Positive Input**
5	RRing1	I	**Receiver 1 Bipolar Negative Input**
6	PDTx1	I	**Powered-down Transmitter 1:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 1 transmitter and set TTIP1 and TRing1 output to high impedance. ***NOTE:*** *Internally pulled-high with 50KΩ.*
7	TTIP1	O	**Transmitter 1 Tip Output:** Positive bipolar data output to the line
8	TVDD1	****	**Transmitter 1 Positive Supply (3.3V± 5%)**
9	TRing1	O	**Transmitter 1 Ring Output:** Negative bipolar data output to the line.
10	TGND1	****	**Transmitter 1 Supply Ground**
11	PDTx3	I	**Powered-down Transmitter 3:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 3 transmitter and set TTIP3 and TRing3 output to high impedance. ***NOTE:*** *Internally pulled- high with 50KΩ.*
12	TTIP3	O	**Transmitter 3 Tip Output:** Positive bipolar data output to the line.
13	TVDD3	****	**Transmitter 3 Positive Supply(3.3V± 5%)**
14	TRing3	O	**Transmitter 3 Ring Output:** Negative bipolar data output to the line.
15	TGND	****	**Transmitter 3 Supply Ground**
16	AVDD	****	**Analog Positive Supply(3.3V± 5%)**
17	RTIP3	I	**Receiver 3 Bipolar Positive Input**
18	RRing3	I	**Receiver 3 Bipolar Negative Input**
19	AGND	****	**Analog Supply Ground**
20	RTIP5	I	**Receiver 5 Bipolar Positive Input**

PIN #	NAME	TYPE	DESCRIPTION
21	RRing5	I	**Receiver 5 Bipolar Negative Input**
22	PDTx5	I	**Powered-down Transmitter 5:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 5 transmitter and set TTIP5 and TRing5 output to high impedance. ***NOTE:*** *Internally pulled- high with 50KΩ.*
23	TTIP5	O	**Transmitter 5 Tip Output:** Positive bipolar data output to the line.
24	TVDD5	****	**Transmitter 5 Positive Supply(3.3V± 5%)**
25	TRing5	O	**Transmitter 5 Ring Output:** Negative bipolar data output to the line.
26	TGND5	****	**Transmitter 5 Supply Ground**
27	PDTx7		**Powered-down Transmitter 7:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 7 transmitter and set TTIP7 and TRing7 output to high impedance. ***NOTE:*** *Internally pulled- high with 50KΩ.*
28	TTIP7	O	**Transmitter 7 Tip Output:** Positive bipolar data output to the line.
29	TVDD7	****	**Transmitter 7 Positive Supply(3.3V± 5%)**
30	TRing7	O	**Transmitter 7 Ring Output:** Negative bipolar data output to the line.
31	TGND7	****	**Transmitter 7 Supply Ground**
32	MODE	I	**Mode Control Input:** This pin is used for selecting **Hardware Mode** or **Host Mode** control of the device. Left this pin unconnected or tie Low to select Host Mode and tie this pin High to select **Hardware mode**. ***NOTE:*** *Internally pulled-down with 50KΩ.*
33	RClk5	O	**Receiver 5 Clock Output**
34	RNEG5/LCV5	O	**Receiver 5 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
35	RPOS5/RDATA5	O	**Receiver 5 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 5 NRZ Data Output:** In single-rail mode, this signal is the receive output data
36	LOS5	O	**Receiver 5 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
37	TClk5	I	**Transmitter 5 Clock Input:** E1 rate at 2.048MHz ± 50ppm.

PIN #	NAME	TYPE	DESCRIPTION
38	TPOS5/TDATA5	I	**Transmitter 5 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 5. **Transmitter 5 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 5.
39	TNEG5/CODE	I	**Transmitter 5 Negative Data Input:** In dual-rail mode, this signal is the n-rail data input for transmitter 5. In single-rail mode (pin 69 = "1") and with this pin tied High, input data at the transmit input is encoded in HDB3 format and the substitution code in the corresponding receive channel will be removed. Tie this pin Low to enable AMI encoding and decoding. ***NOTE:*** *Internally pulled-down with 50KΩ.*
40	TAOS5	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled-down with 50KΩ.*
41	VDD	****	**Digital Positive Supply(3.3V± 5%).**
42	GND	****	**Digital Supply Ground.**
43	TClk7	I	**Transmitter 7 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
44	TPOS7/TDATA7	I	**Transmitter 7 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 7. **Transmitter 7 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 7.
45	TNEG7/CODE	I	**Transmitter 7 Negative Data Input:** In dual-rail mode, this signal is the n-rail data input for transmitter 7. See pin 39 description for single-rail mode operation. ***NOTE:*** *Internally pulled-down with 50KΩ.*
46	TAOS7	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled- down with 50KΩ.*
47	SDO/LBM	O	**Serial Data Output:** In **Host Mode**, this pin is the Serial Data Output port for the Microprocessor Serial Interface access. This pin serially outputs the contents of the specified Command Register during Read Operations. The data on this pin is updated on the falling edge of the SCLK input signal. This pin is tri-stated upon completion of data transfer. **Loop-back Mode:** In **Hardware Mode**, when this pin is tied High, Analog Local loop-back is selected. Connect this pin Low to select remote loop-back. Digital Local loop-back is not supported in **Hardware mode**.

<table>
<tr><th>PIN #</th><th>NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>48</td><td>SDI/B1</td><td>I</td><td>Serial Data Input Port for the Microprocessor Serial Interface:
In Host Mode, this pin is the serial data input port (see Figure 5).
This pin is used to read or write data into the Command Registers of the Microprocessor Serial Interface. The Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations are applied to this pin.
This input is sampled on the rising edge of the SCLK pin (pin 49).
In Hardware Mode, B1, together with B2 (pin49) and B3 (pin 50)are control bits used to select which one of the seven channels is to be placed in Loop-back mode. Analog or Remote Loop-back is determined by LBM (pin 47).

Loop-back Channel Control
<table><tr><th>B1</th><th>B2</th><th>B3</th><th>Chan. #</th></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>6</td></tr><tr><td>1</td><td>1</td><td>0</td><td>7</td></tr><tr><td>1</td><td>1</td><td>1</td><td>All</td></tr></table></td></tr>
<tr><td>49</td><td>SClk/B2</td><td>I</td><td>Microprocessor Serial Interface Clock:
In Host Mode, The data on the SDI pin is sampled on the rising edge of this clock signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal.
In Hardware Mode, B2, together with B1 and B3 are control bits to select which one of the seven channels to be placed in Loop-back mode, (see pin 48 description)</td></tr>
<tr><td>50</td><td>$\overline{CS}$/B3</td><td>I</td><td>Chip Select Input:
In Host Mode, this pin must be asserted Low in order to enable communication with the device via the Serial Interface.
In Hardware Mode, B3, together with B1 and B2 are control bits to select which one of the seven channels to be placed in Loop-back mode, (see pin 48 description)</td></tr>
<tr><td>51</td><td>TAOS6</td><td>I</td><td>Transmit All Ones:
This pin is set to insert AMI all ones data to the line using MCLK as reference.
In Host Mode, this pin can be left unconnected.
NOTE: Internally pulled-down with 50KΩ</td></tr>
<tr><td>52</td><td>TNEG6/CODE</td><td>I</td><td>Transmitter 6 Negative Data Input:
In dual-rail mode, this signal is the n-rail data input for transmitter 6.
See pin 39 description for single-rail mode operation.
NOTE: Internally pulled-down with 50KΩ.</td></tr>
<tr><td>53</td><td>TPOS6/TDATA6</td><td>I</td><td>Transmitter 6 Positive Data Input:
In dual-rail mode, this signal is the p-rail input data for transmitter 6.
Transmitter 6 NRZ Data Input:
In single-rail mode this signal is used as the NRZ input data for transmitter 6.</td></tr>
<tr><td>54</td><td>TClk6</td><td>I</td><td>Transmitter 6 Clock Input:
E1 rate at 2.048MHz ± 50ppm.</td></tr>
</table>

PIN #	NAME	TYPE	DESCRIPTION
55	GND	****	**Digital Supply Ground**
56	VDD	****	**Digital Positive Supply(3.3V± 5%)**
57	LOS6	O	**Receiver 6 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
58	RPOS6/RDATA6	O	**Receiver 6 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 6 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
59	RNEG6/LCV6	O	**Receiver 6 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
60	RClk6	O	**Receiver 6 Clock Output**
61	LOS7	O	**Receiver 7 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
62	RPOS7/RDATA7	O	**Receiver 7 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 7 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
63	RNEG7/LCV7	O	**Receiver 6 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
64	RClk7	O	**Receiver 7 Clock Output**
65	RClkP	I	**Receiver Clock Output Polarity:** In **Hardware Mode** and with this pin tied to Low, All channels RPOS /RDATA and RNEG/LCV output data are updated on the falling edge of RClk. Tie this pin High to select data update on rising edge of RClk. ***NOTE:*** *Internally pulled-down with 50KΩ.*
66	TClkP	I	**Transmit Clock Polarity:** In **Hardware Mode** and with this pin tied to Low, transmit input data is sampled using the falling edge of TClk. Tie this pin High to select rising edge of TClk for data sampling. ***NOTE:*** *Internally pulled-down with 50KΩ.*
67	RRING7	I	**Receiver 7 Bipolar Negative Input**
68	RTIP7	I	**Receiver 7 Bipolar Positive Input**
69	SR/$\overline{DR}$	I	**Single-rail/Dual-rail Select:** In **Hardware Mode** and with this pin tied to High, input transmit data and receive output data is selected for single-rail mode operation. Tie this pin Low to select dual-rail mode. ***NOTE:*** *Internally pulled-down with 50KΩ.*

PIN #	NAME	TYPE	DESCRIPTION
70	MClk	I	**Master Clock Input:** This signal is an independent 2.048MHz clock with accuracy better than ±50ppm and duty cycle within 40% to 60%. The function of MCLK is to provide timing source for the PLL clock recovery circuit, reference clock to insert All Ones data in the transmit as well as the receive paths.
71	TGND6	****	**Transmitter 6 Supply Ground**
72	TRing6	O	**Transmitter 6 Ring Output:** Negative bipolar data output to the line
73	TVDD6	****	**Transmitter 6 Positive Supply (3.3V± 5%)**
74	TTIP6	O	**TTIP6 O Transmitter 6 Tip Output:** Positive bipolar data output to the line.
75	PDTx6	I	**Powered-down Transmitter 6:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 6 transmitter and set TTIP6 and TRing6 output to high impedance.
76	RRing6	I	**Receiver 6 Bipolar Negative Input**
77	RTIP6	I	**Receiver 6 Bipolar Positive Input**
78	AGND	****	**Analog Supply Ground**
79	RRing4	I	**Receiver 4 Bipolar Negative Input**
80	RTIP4	I	**Receiver 4 Bipolar Positive Input**
81	AVDD	****	**Analog Positive Supply(3.3V± 5%)**
82	TGND4	****	**Transmitter 4 Supply Ground**
83	TRing4	O	**Transmitter 4 Ring Output:** Negative bipolar data output to the line.
84	TVDD4	****	**Transmitter 4 Positive Supply(3.3V± 5%)**
85	TTIP4	O	**Transmitter 4 Tip Output:** Positive bipolar data output to the line.
86	PDTx4	I	**Powered-down Transmitter 4:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 4 transmitter and set TTIP4 and TRing4 output to high impedance. ***NOTE:*** *Internally pulled- high with 50KΩ*
87	TGND2	****	**Transmitter 2 Supply Ground**
88	TRing2	O	**Transmitter 2 Ring Output:** Negative bipolar data output to the line.
89	TVDD2	****	**Transmitter 2 Positive Supply(3.3V± 5%)**
90	TTIP2	O	**Transmitter 2 Tip Output:** Positive bipolar data output to the line.

PIN #	NAME	TYPE	DESCRIPTION
91	PDTx2	I	**Powered-down Transmitter 2:** This pin is operational for both **Host** or **Hardware mode**, tie this pin High to power-down channel 2 transmitter and set TTIP2 and Tring2 output to high impedance. ***NOTE:*** *Internally pulled-high with 50KΩ.*
92	RRing2	I	**Receiver 2 Bipolar Negative Input**
93	RTIP2	I	**Receiver 2 Bipolar Positive Input**
94	$\overline{ICT}$	I	**In-Circuit Testing (Active Low):** When this pin is tied to Low, all output pins are forced to high impedance state for in-circuit testing. ***NOTE:*** *Internally pulled High with 50KΩ.*
95	LOS2	O	**Receiver 2 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
96	RClk2	O	**Receiver 2 Clock Output**
97	RNEG2/LCV2	O	**Receiver 2 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. Line Code Violation Output :In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
98	RPOS2/RDATA2	O	**Receiver 2 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. Receiver 2 NRZ Data Output: In single-rail mode, this signal is the receive output data.
99	LOS4	O	**Receiver 4 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
100	RClk4	O	**Receiver 4 Clock Output**
101	RNEG4/LCV4	O	**Receiver 4 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
102	RPOS4/RDATA4	O	**Receiver 4 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 4 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
103	AVDD	****	**Analog Positive Supply(3.3V± 5%)**
104	AGND	****	**Analog Supply Ground**
105	TClk2	I	**Transmitter 2 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
106	TPOS2/TDATA2	I	**Transmitter 2 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 2. **Transmitter 2 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 2.

PIN #	NAME	TYPE	DESCRIPTION
107	TNEG2/CODE	I	**Transmitter 2 Negative Data Input:** In dual-rail mode, this signal is the n-rail data input for transmitter 2. See pin 39 description for single-rail mode operation. ***NOTE:*** *Internally pulled-down with 50KΩ.*
108	TAOS2	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled-down with 50KΩ.*
109	TClk4	I	**Transmitter 4 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
110	TPOS4/TDATA4	I	**Transmitter 4 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 4. **Transmitter 4 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 4.
111	TNEG4/CODE	I	**Transmitter 4 Negative Data Input:** In dual-rail mode, this signal Is the n-rail data input for the transmitter 4. See pin 39 description for single-rail mode operation. ***NOTE:*** *Internally pulled-down with 50K Ω*
112	TAOS4	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled-down with 50KΩ.*
113	TAOS3	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pull-down with 50KΩ.*
114	TNEG3/CODE	I	**Transmitter 3 Negative Data Input:** In dual-rail mode, this signal is the n-rail data input for transmitter 3. See pin 39 description for single-rail mode operation. ***NOTE:*** *Internally pulled-down with 50KΩ.*
115	TPOS3/TDATA3	I	**Transmitter 3 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 3. **Transmitter 3 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 3.
116	TClk3	I	**Transmitter 3 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
117	TAOS1	I	**Transmit All Ones:** This pin is set to insert AMI all ones data to the line using MCLK as reference. In Host Mode, this pin can be left unconnected. ***NOTE:*** *Internally pulled-down with 50KΩ.*
118	TNEG1/CODE	I	**Transmitter 1 Negative Data Input:** In dual-rail mode, this signal is the n-rail data input for transmitter 1. See pin 39 description for single-rail mode operation. ***NOTE:*** *Internally pulled-down with 50KΩ.*

PIN #	NAME	TYPE	DESCRIPTION
119	TPOS1/TDATA1	I	**Transmitter 1 Positive Data Input:** In dual-rail mode, this signal is the p-rail input data for transmitter 1. **Transmitter 1 NRZ Data Input:** In single-rail mode, this signal is used as the NRZ input data for transmitter 1.
120	TClk1	I	**Transmitter 1 Clock Input:** E1 rate at 2.048MHz ± 50ppm.
121	GND	****	**Digital Supply Ground**
122	VDD	****	**Digital Positive Supply(3.3V± 5%)**
123	RPOS3/RDATA3	O	**Receiver 3 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 3 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
124	RNEG3/LCV3	O	**Receiver 3 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.
125	RClk3	O	**Receiver 3 Clock Output**
126	LOS3	O	**Receiver 3 Loss of Signal:** This signal is asserted High to indicate loss of signal at the receive input.
127	RPOS1/RDATA1	O	**RPOS1/RDATA1 O Receiver 1 Positive Data Output:** In dual-rail mode, this signal is the receive p-rail output data. **Receiver 1 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
128	REG1/LCV1	O	**Receiver 1 Negative Data Output:** In dual-rail mode, this signal is the receive n-rail output data. **Line Code Violation Output:** In single-rail mode, this signal output High for one clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go High.

TABLE 1: RECEIVER ELECTRICAL CHARACTERISTICS

(Vdd=3.3V ± 5%, T_a= -40°C to +85°C unless otherwise Specified)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Receiver loss of signal:					
Number of consecutive zeros before **LOS** is set	----	32	----	bit	Cable attenuation @1024KHz
Number of consecutive Zeros before **EXLOS** is set	----	4096	----	bit	
Input signal level at **LOS**	12	16	----	dB	
LOS Delay	10	-------	255	bit	ITU-G.775, ETSI 300 233
Hysteresis	----	2	2	dB	
Receiver Sensitivity	11	13	----	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Interference Margin	-18	-14	----	dB	With 6dB cable loss.
Input Impedance	10	----	----	KΩ	Between RTIP or RRing to ground
Jitter Tolerance: 20 Hz 700Hz 10KHz ¾100KHz	 10 5 0.3	----	----	UIpp	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	----	36	---- 0.5	KHz dB	ITU G.736
Return Loss: 51KHz -- 102KHz 102KHz -- 2048KHz 2048KHz -- 3072KHz	 14 20 16	 ---- ---- ----	 ---- ---- ----	 dB dB dB	ITU-G.703

TABLE 2: TRANSMITTER ELECTRICAL CHARACTERISTICS

(Vdd=3.3V ± 5%, T_a= -40°C to +85°C unless otherwise Specified)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.13 2.70	 2.37 3.0	 2.60 3.30	 V V	Use transformer with 1:2 ratio and 9.1Ω resistor in series with each end of primary.
Output Pulse Width	224	244	264	ns	
Output Pulse With Ratio	0.95	----	1.05	----	ITU-G.703
Output Pulse Amplitude Ratio	0.95	----	1.05	----	ITU-G.703
Output Return Loss: 51KHz --102KHz 102KHz--2048KHz 2048KHz--3072KHz	 8 14 10	 TBD TBD TBD	 ---- ---- ----	 dB dB dB	ETSI 300 166, CHPTT

FIGURE 3. TRANSMIT INPUT TIMING

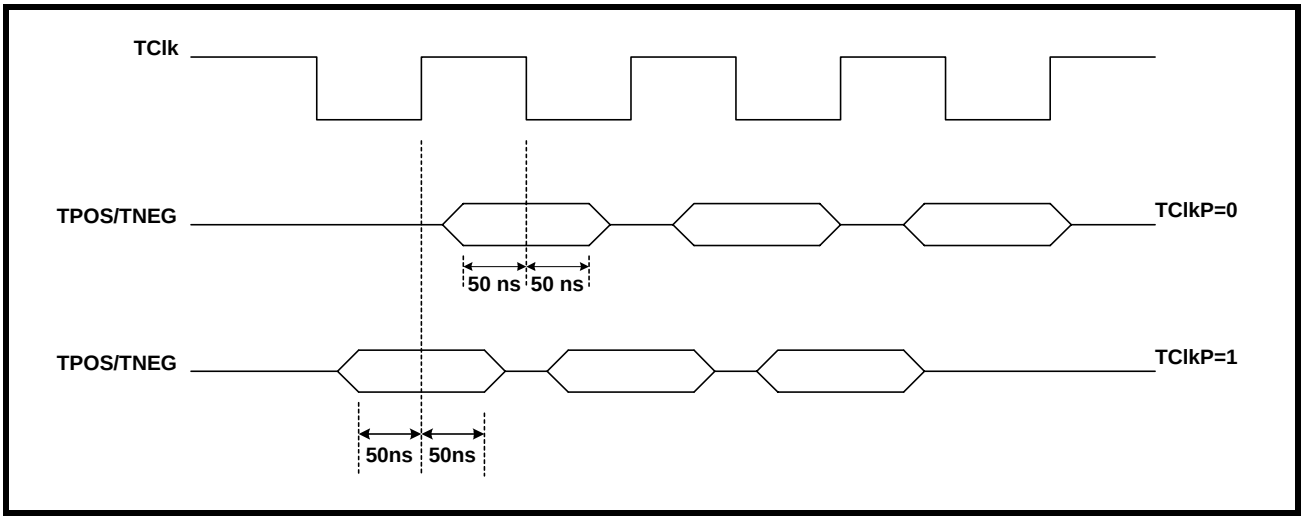


FIGURE 4. RECEIVE OUTPUT TIMING

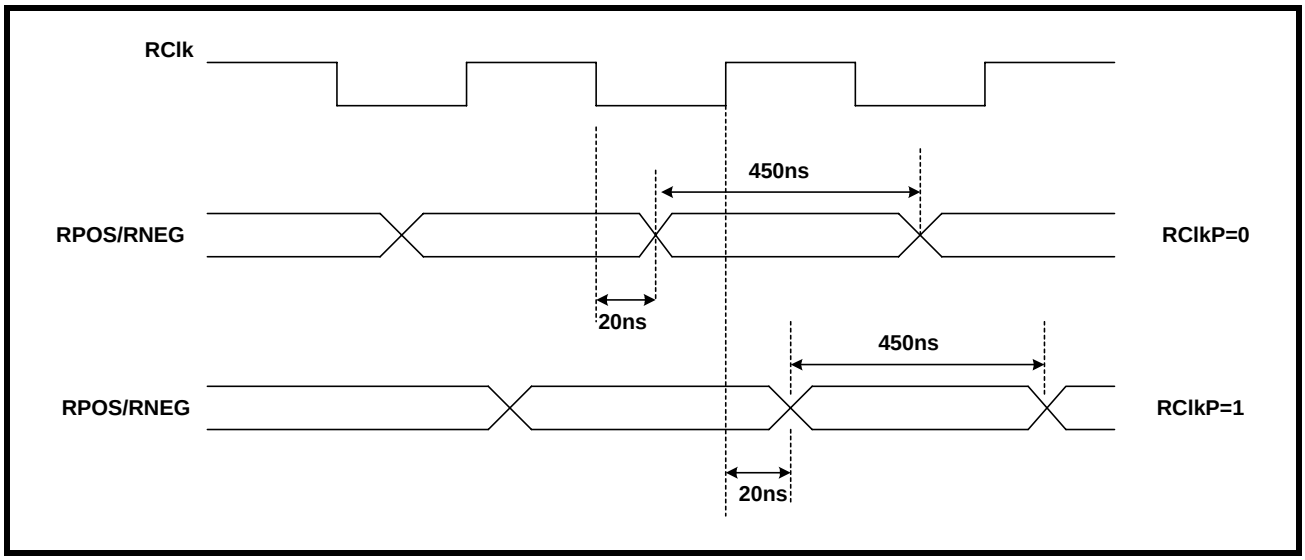


TABLE 3: DC ELECTRICAL CHARACTERISTICS

(Vdd=3.3V ± 5%, T_a= -40°C to +85°C unless otherwise Specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage	V_{DD}	3.13	3.3	3.46	V
Input High Voltage	V_{IH}	2.0	----	5.0	V
Input Low Voltage	V_{IL}	-0.5	----	0.8	V
Output High Voltage @ IOH = 5mA	V_{OH}	2.4	----	3.5	V
Output Low Voltage @ IOL = 5mA	V_{OL}	-0.5	----	0.4	V
Input Leakage Current (except input pins with pull-up or pull-down resistors)	I_L	----	----	± 10	µA
Input Capacitance	C_I	----	5.0	----	pF
Output Load Capacitance	C_L	----	----	25	pF

The HOST Mode

To configure the XRT81L27 to operate in the HOST Mode, connect the MODE input pin (pin 32) to Ground or leave unconnected.

When the XRT81L27 is operating in the HOST Mode, the Microprocessor Serial Interface block is enabled. Many configuration selections are made by writing the appropriate data into the on-chip Command Registers via the Microprocessor Serial Interface.

1.0 THE MICROPROCESSOR SERIAL INTERFACE

The on-chip Command Registers of the XRT81L27 E1 Line Interface Unit IC are accessed to configure the XRT81L27 into a variety of modes. This section describes the Command Registers and how to use the Microprocessor Serial Interface.

1.1 DESCRIPTION OF THE COMMAND REGISTERS

A listing of these Command Registers, their Addresses and their Bit-Formats are listed in Table 4

TABLE 4: MICROPROCESSOR REGISTER ADDRESS AND CONTROL

REGISTER ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMMAND CONTROL REGISTER (READ/WRITE)								
0000	reserved	ARAOS	EXLOS	MUTE	SR/DR	CODE	RClkP	TClkP
		Reset=0	Reset=0	Reset=0	Reset=0	Reset=0	Reset=0	Reset=0
CHANNEL CONTROL REGISTERS (READ/WRITE)								
0001	reserved	LLB7	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1
0010	reserved	RLB7	RLB6	RLB5	RLB4	RLB3	RLB2	RLB1
0011	reserved	ALB7	ALB6	ALB5	ALB4	ALB3	ALB2	ALB1
0100	reserved	TAOS7	TAOS6	TAOS5	TAOS4	TAOS3	TAOS2	TAOS1
0101	reserved	RAOS7	RAOS6	RAOS5	RAOS4	RAOS3	RAOS2	RAOS1
0110	reserved	PDTx7	PDTx6	PDTx5	PDTx4	PDTx3	PDTx2	PDTx1
		Reset=0	Reset=0	Reset=0	Reset=0	Reset=0	Reset=0	Reset=0
0111	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

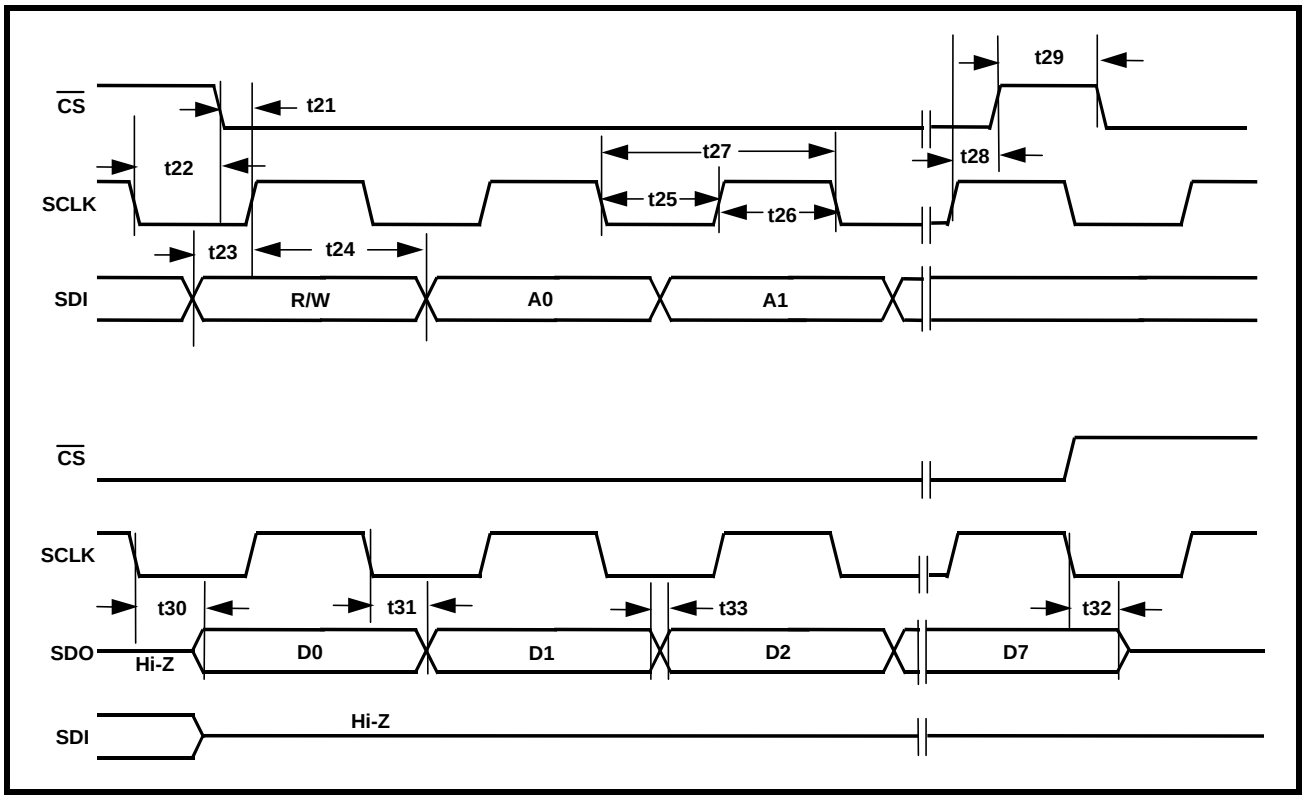
TABLE 5: REGISTER CONTROL BIT DESCRIPTION

BIT NO.	NAME	FUNCTION	REGISTER TYPE
COMMAND CONTROL REGISTER (COMMON TO ALL SEVEN CHANNELS) ADDRESS: 0000			
7	Reserved	This bit position is reserved.	R/W
6	ARAOS	Automatic Receive All Ones: Writing a "1" to this bit globally enables receive all one data insertion at RPOS/RNEG upon receive LOS condition. The setting of this bit has priority over the "MUTE" function of bit 4.	R/W
5	EXLOS	Extended LOS: Writing a "1" to this bit extends the number of zeros at the receive input to 4096 bits before LOS is declared.	R/W
4	MUTE	Receive Output Muting: Writing a "1" to this bit mutes the receive data output at RPOS/RNEG/LCV to a Low state upon LOS condition. The setting of this bit is only active when AROAS is = "0".	R/W
3	SR/DR	Single-rail/Dual-rail: Writing a "1" to this bit selects single-rail mode operation for transmit input and receive output. In single-rail mode, TPOS is the input data for the transmitter and RPOS is the receiver output data. RNEG is the Line Code Violation output pin. Writing a "0" to select dual-rail mode operation.	R/W
2	CODE	Coding and Decoding: This bit is only active when SR/DR is ="1". With single-rail mode selected, writing a "1" to this bit selects HDB3 encoding and decoding, writing a "0" to select AMI encoding and decoding.	R/W
1	RClkP	Receive Clock Polarity: Writing a "1" to this bit selects receive output data to be updated on the rising edge of RCLK and a "0" to update on the falling edge of RClk.	R/W
0	TClkP	Transmit Clock Polarity: Writing a "1" to this bit selects input data to be sampled on the rising edge of TClk and a "0" to sample on the falling edge of TClk.	R/W
LOCAL LOOP-BACK REGISTERS ADDRESS: 0001			
7	reserved	This bit position is reserved.	R/W
0-6	LLB1-LLB7	Local Loop-back: Writing a "1" to this bit enables Local Loop-back for the channel selected. During Local loop-back, transmit input data continues to be sent to the line unless overridden by TAOS request.	R/W
REMOTE LOOP-BACK REGISTERS ADDRESS: 0010			
7	reserved	This bit position is reserved	R/W
0-6	RLB1-RLB7	Remote Loop-back: Wring a "1" to this bit enables Remote Loop-back for the channel selected. During Remote Loop-back, receive output data is available at RPOS/RNEG unless overridden by RAOS request.	R/W

TABLE 5: REGISTER CONTROL BIT DESCRIPTION

BIT NO.	NAME	FUNCTION	REGISTER TYPE
ANALOG LOOP-BACK REGISTERS ADDRESS: 0011			
7	reserved	This bit position is reserved	R/W
0-6	ALB1-ALB7	Analog Loop-back: Writing a "1" to this bit enables Analog Local Loop-back for the channel selected. Analog Loop-back ignores input data on RTIP and RRing and internally route data at TTIP and TRing back to the receive input. This loop-back mode exercises most of the functional blocks. Analog Loop-back has priority over other Loop-back, TAOS and RAOS requests.	R/W
TAOS REGISTERS ADDRESS: 0100			
7	reserved	This bit position is reserved	
0-6	TAOS1-TAOS7	Transmit All Ones: Writing a "1" to this bit enables an AMI encoded all ones data to be transmitted to the line for the channel selected. Transmit input data is ignored when TAOS bit is set to a "1". Remote Loop-Back has priority over TAOS request.	R/W
RAOS REGISTERS ADDRESS: 0101			
7	reserved	This bit position is reserved.	R/W
0-6	RAOS1-RAOS7	Receive All Ones: Writing a "1" to this bit enables all ones data to be inserted on the receive side for the channel selected. In single-rail mode, all ones data is a continuous High signal at RPOS output and in dual-rail mode, a "1010 " pattern is sent to RPOS and RNEG while receive input signal at RRTIP and RRing is ignored. Local Loop-Back has priority RAOS and ARAOS request.	R/W
PDTX REGISTERS ADDRESS: 0110			
7	reserved	This bit position is reserved.	R/W
0-6	PDTx1-PDTx7	Power-down Transmitter: Writing a "1" to this bit shut down the transmitter channel selected and placed TTIP/TRing in high impedance mode. Individual pin control is also available to switch off the transmitter for fast redundancy application both in **Host** and **Hardware mode**.	R/W

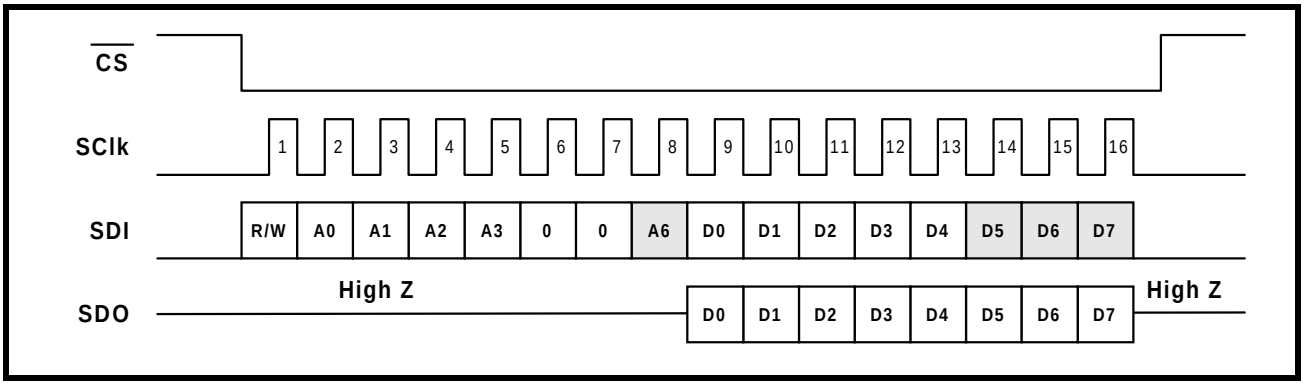
FIGURE 5. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



MICROPROCESSOR SERIAL INTERFACE TIMING (SEE FIGURE 5)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SCLK Setup Time	50			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SCLK Hold Time	20			ns
t_{23}	SDI to Rising Edge of SCLK Setup Time	50			ns
t_{24}	SDI to Rising Edge of SCLK Hold Time	50			ns
t_{25}	SCLK “Low” Time	240			ns
t_{26}	SCLK “High” Time	240			ns
t_{27}	SCLK Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SCLK Hold Time	50			ns
t_{29}	$\overline{CS}$ Inactive Time	250			ns
t_{30}	Falling Edge of SCLK to SDO Valid Time			200	ns
t_{31}	Falling Edge of SCLK to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SCLK or Rising Edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

FIGURE 6. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



Notes:

- Denotes a "don't care" value

A4 and A5 are always "0".
R/W = "1" for "Read" Operations
R/W = "0" for "Write" Operations

TABLE 6: AC ELECTRICAL CHARACTERISTICS

(Vdd=3.3V ± 5%, T_a= -40°C to +85°C unless otherwise Specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
TCLK Clock Period	T_1	-	488	-	ns
TCLK Duty Cycle	T_2	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	50	-	-	ns
TCLK Rise Time(10%/90%)	T_R	-	-	40	ns
TCLK Fall Time(90%/10%)	T_F	-	-	40	ns
Receive Data Rise Time	R^{tr}	-	-	40	ns
Receive Data Fall Time	R_{tf}	-	-	40	ns
Receive Data Prop. Delay	R_{pd}	-	75	-	ns
Receive Data Pulse Width	R_{xpw}	450	488	-	ns

TABLE 7: PER CHANNEL POWER CONSUMPTION INCLUDING LINE POWER DISSIPATION, TRANSMISSION AND RECEIVE PATHS ALL ACTIVE

(Vdd=3.3V ± 5%, T_a= -40°C to +85°C unless otherwise Specified)

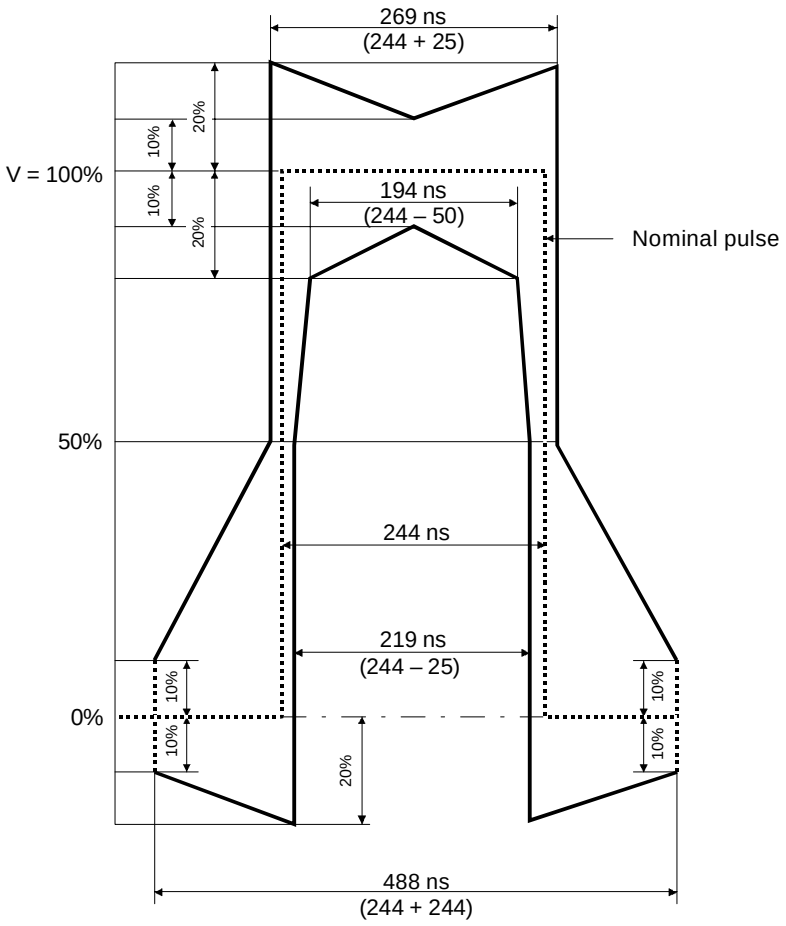
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Power Consumption	PC	-	90	107	mW	75Ω load, operating at 50% Mark Density
Power Consumption	PC	-	85	92	mW	120Ω load, operating at 50% Mark Density.
Power Consumption	PC	-	150	180	mW	75Ω load, operating at 100% Mark Density.
Power Consumption	PC	-	120	155	mW	120Ω load, operating at 100% Mark Density.
Power Consumption	PC	-	20	-	mW	Transmitter in Powered-down mode.

ABSOLUTE MAXIMUM RATINGS:

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
ESD Rating	>4000V on all pins[2]
Supply Voltage	-0.5 to 3.465V

NOTE: *[2] Human Body Model, 100pF capacitor discharged through a 1.5KΩ resistor*

FIGURE 7. ILLUSTRATION OF THE ITU-T G.703 PULSE TEMPLATE FOR E1 APPLICATIONS



Note – V corresponds to the nominal peak value.

2.0 THE PULSE SHAPING CIRCUIT

The purpose of the "Transmit Pulse Shaping" Circuit is to generate Transmit Output pulses that comply with the ITU-T G.703 Pulse Template Requirements for E1 applications, even with TClk duty cycle between 30 and 70%.

As a consequence, each channel (within the XRT81L27 device) will take each mark (which is provided to it via the Transmit Input Interface block, and will generate a pulse that complies with the pulse template, presented in Figure 6, (when measured on the secondary-side of the Transmit Output Transformer).

2.1 INTERFACING THE TRANSMIT SECTIONS OF THE XRT81L27 TO THE LINE

In both applications (75Ω or 120Ω), the user is advised to interface the Transmitter to the Line, in the manner as depicted in Figure 8 and Figure 9, respectively.

FIGURE 8. ILLUSTRATION OF HOW TO INTERFACE THE TRANSMIT SECTIONS OF THE XRT81L27 TO THE LINE (FOR 75Ω APPLICATIONS)

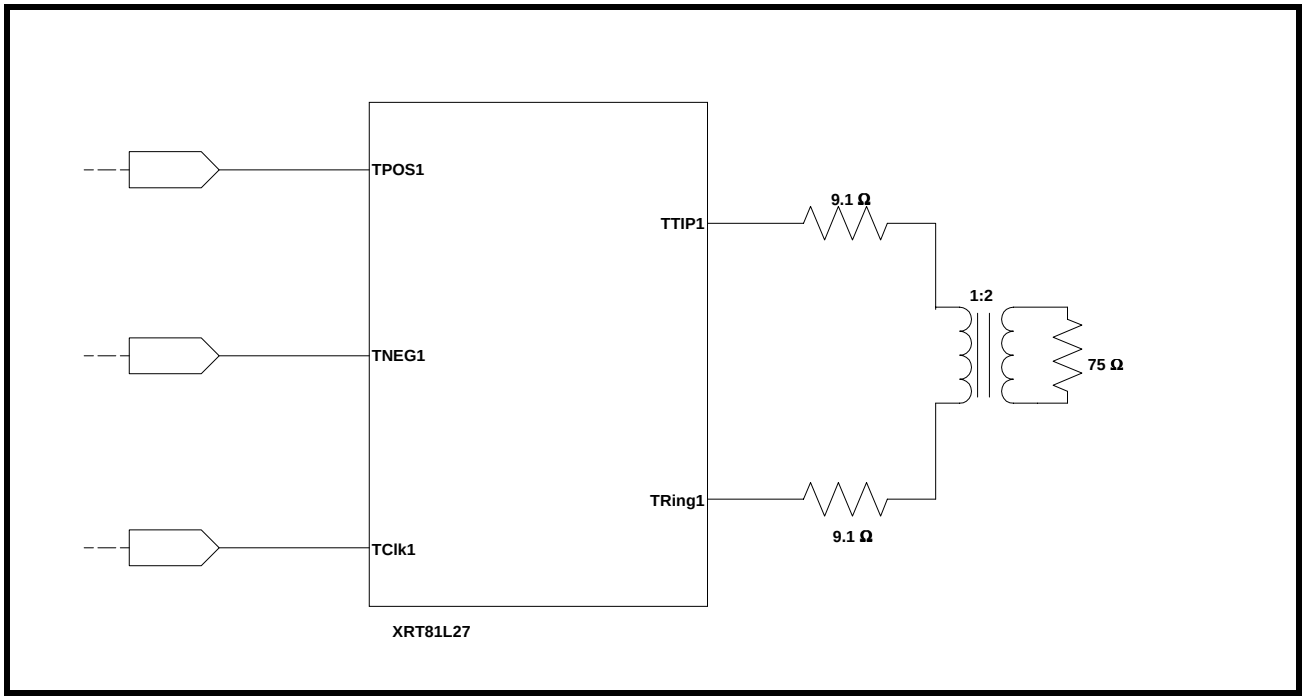
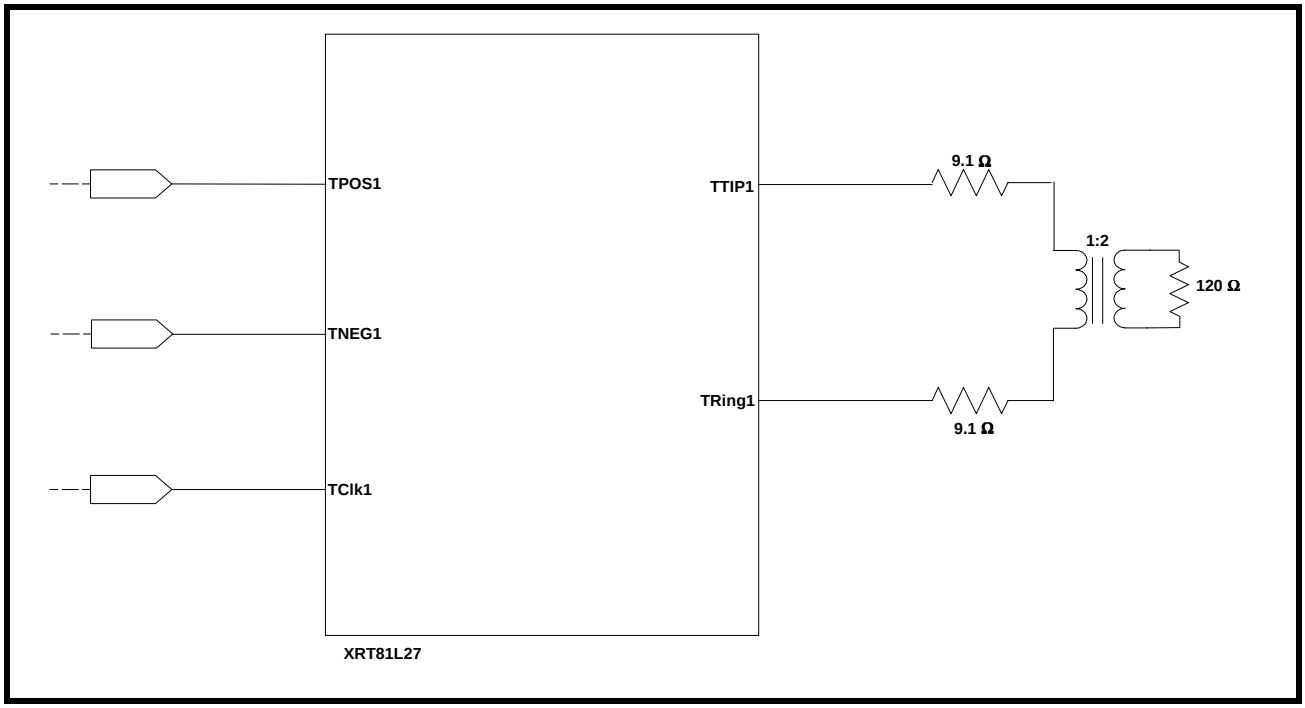


FIGURE 9. ILLUSTRATION OF HOW TO INTERFACE THE TRANSMIT SECTIONS THE XRT81L27 TO THE LINE (FOR 120Ω APPLICATIONS)



3.0 THE RECEIVE SECTION

The Receive Sections of the XRT81L27 consists of the following blocks:

- The Receive Equalizer block
- The Peak Detector and Slicer block
- The LOS Detector block
- The Receive Output Interface block

3.1 INTERFACING THE RECEIVE SECTIONS TO THE LINE

The design of each channel (within the XRT81L27 device) permits the user to transformer-couple or capacitive-couple the Receive Section to the line. Additionally, as mentioned earlier, the specification documents for E1 specify 75Ω termination loads, when transmitting over coaxial cable, and 120Ω loads, when transmitting over twisted-pair. Figure 10, Figure 11and Figure 12 present the various methods that can be employ to interface the Receivers (of the XRT81L27) to the line.

FIGURE 10. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE FOR 75Ω APPLICATIONS (TRANSFORMER-COUPLING)

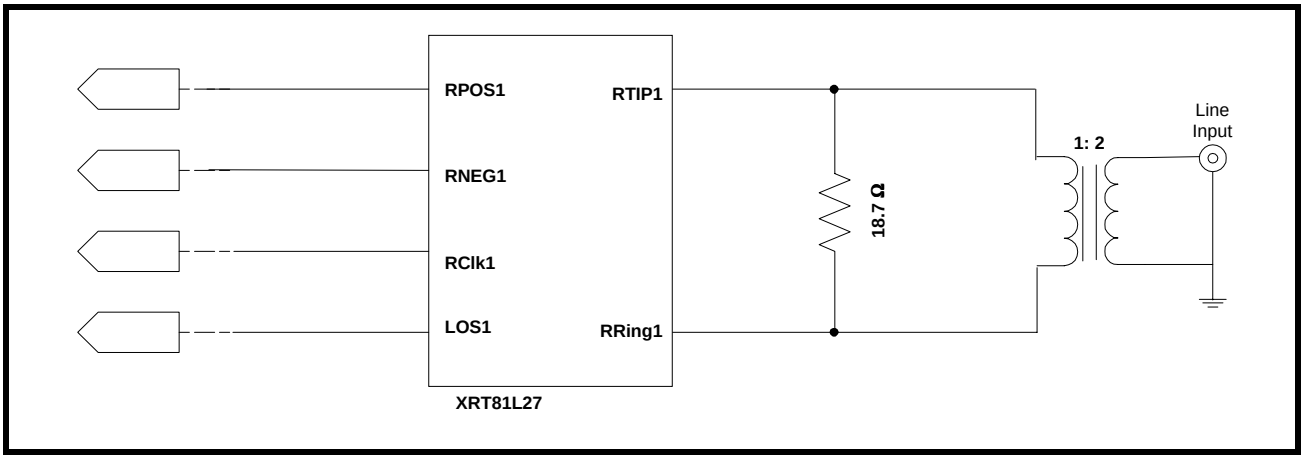
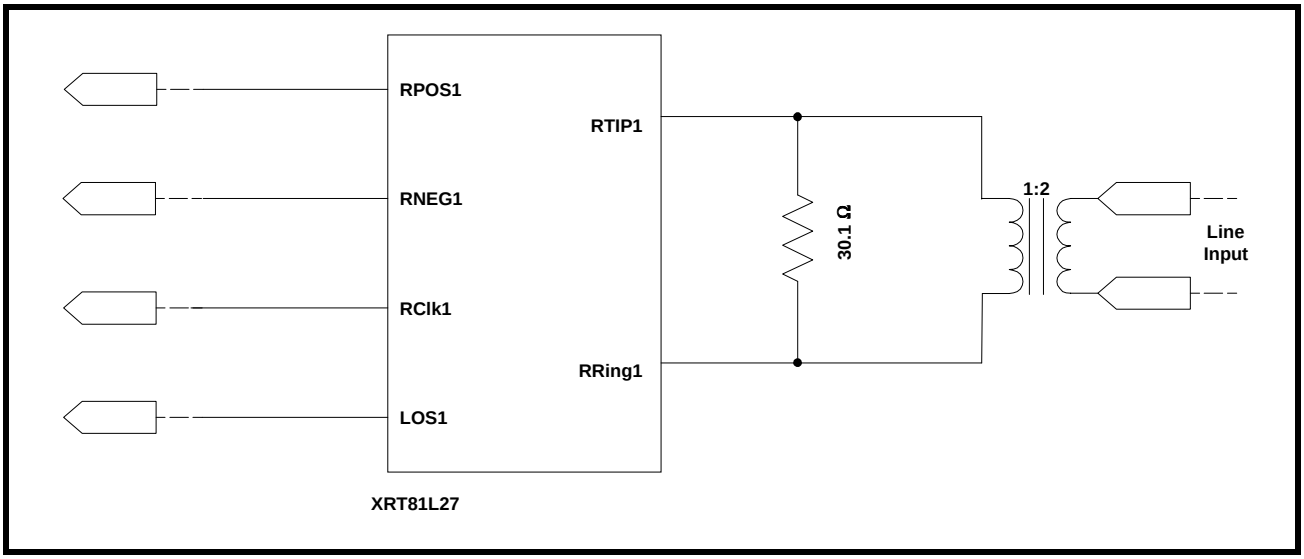


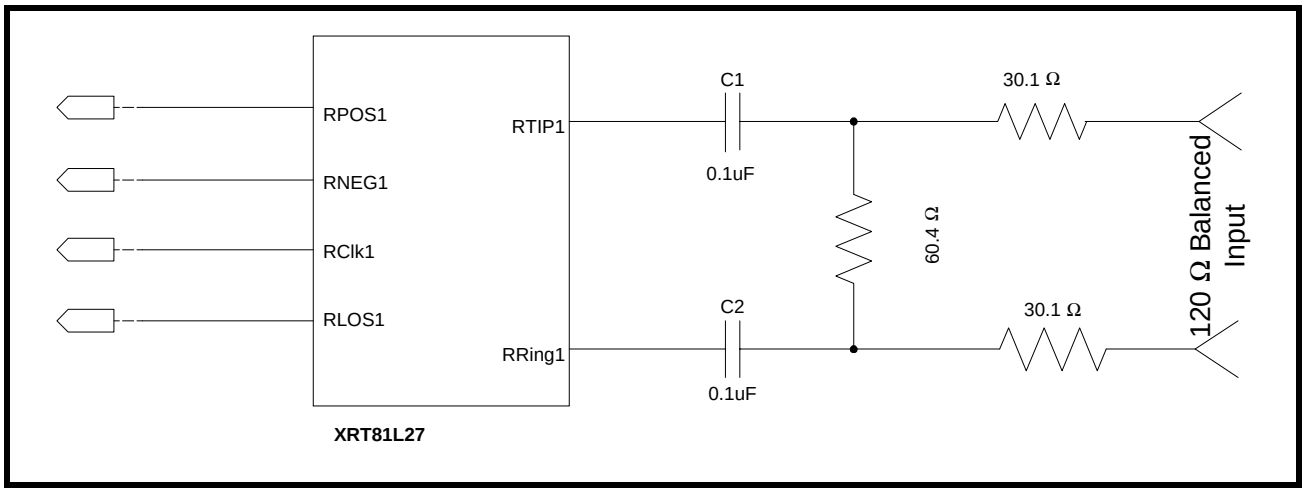
FIGURE 11. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE FOR 120Ω APPLICATIONS (TRANSFORMER-COUPLING)



Capacitive-Coupling the Receiver to the Line

Figure 12, presents a recommended method to use when capacitive-coupling the Receive Section to the line.

FIGURE 12. RECOMMENDED SCHEMATIC FOR INTERFACING THE RECEIVE SECTIONS OF THE XRT81L27 TO THE LINE FOR 120Ω APPLICATIONS (CAPACITIVE-COUPLING)



3.2 THE RECEIVE EQUALIZER BOCK

After a given Channel (within the XRT81L27) has received the incoming line signal, via the RTIP_n (where _n is the channel number) and RRing_n input pins, the first block that this signal will pass through is the Receive Equalizer block.

As the line signal is transmitted from a given Transmitting terminal, the pulse shapes (at that location) are basically square. Hence, these pulses consist of a combination of low and high frequency Fourier components. As this line signal travels from the transmitting terminal (via the coaxial cable or twisted pair) to the receiving terminal, it will be subjected to frequency-dependent loss. The higher frequency components of the signal will be subjected to a greater amount of attenuation than the lower frequency components. If this line signal travels over reasonably long cable lengths, then the shape of the pulses (which were originally square) will be distorted and with inter-symbol interference increases.

The purpose of this block is to equalize the incoming distorted signal, due to cable loss. In essence, the Receive Equalizer block accomplishes this by subjecting the received line signal to frequency-dependent amplification (which attempts to counter the frequency-dependent loss that the line signal has experienced). By doing this, the Receive Equalizer is attempting to restore the shape of the line signal so that the received data can be recovered reliably.

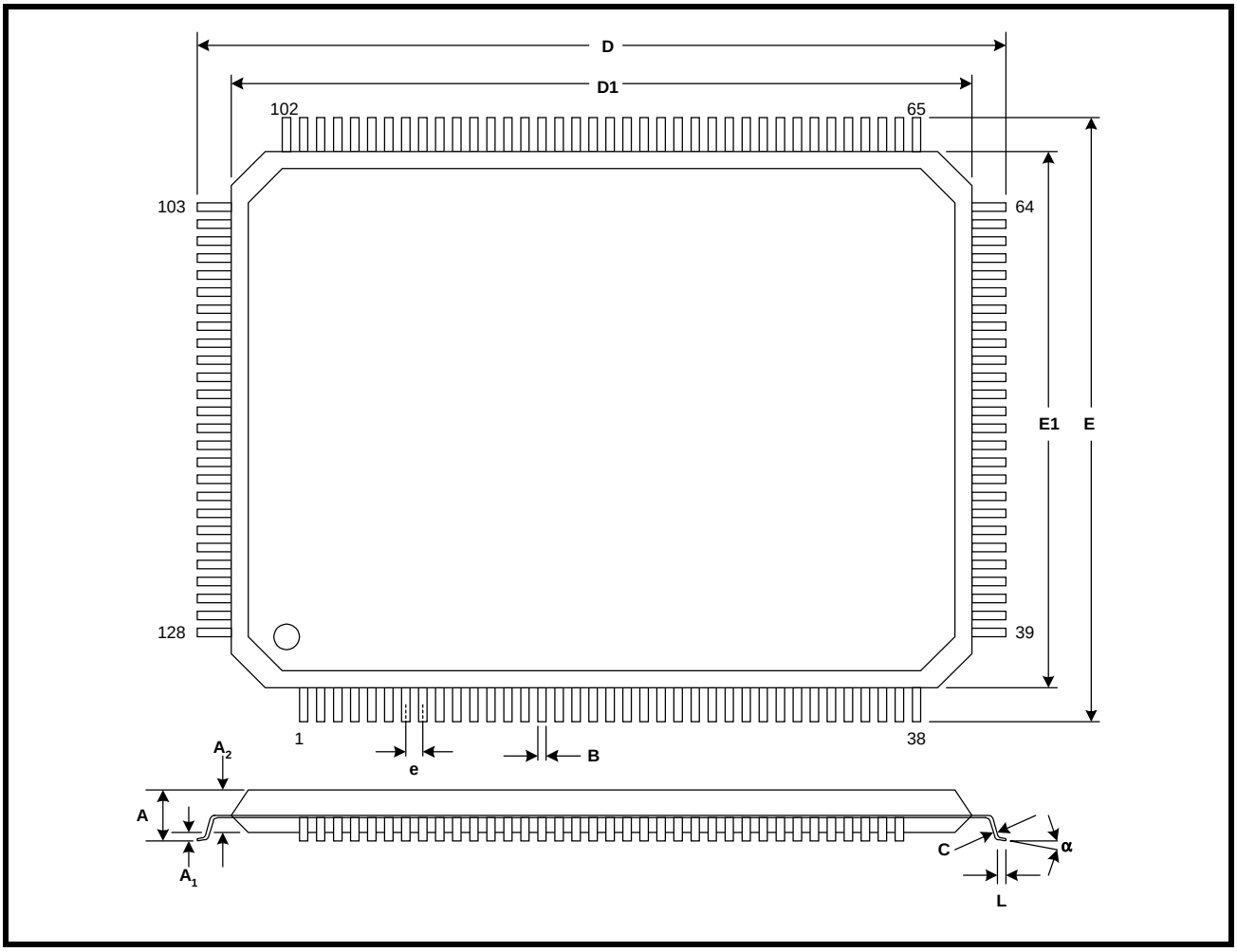
3.3 THE PEAK DETECTOR AND SLICER BLOCK

After the incoming line signal has passed through the Receive Equalizer block, it will next be routed to the Slicer block. The purpose of the Slicer block is to quantify a given bit-period (or symbol) within the incoming line signal as either a “1” or a “0”.

3.4 THE LOS DETECTOR BLOCK

The LOS Detector block, within each channel (of the XRT81L27) was specifically designed to comply with the LOS Declaration/Clearance requirements per ITU-T G.775. As a consequence, the channel will declare an LOS Condition, (by driving the LOS output pin “High”) if the received line signal amplitude drops to –20dB or below. Further, the channel will clear the LOS Condition if the signal amplitude rises back up to –15dB typically, or above. The XRT81L27 was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, the XRT81L27 will declare an LOS between 10 and 255 UI (or E1 bit periods) after the actual time the LOS condition occurred. Further, the XRT81L27 will clear the LOS indicator within 10 to 255 UI after restoration of the incoming line signal.

FIGURE 13. PACKAGE OUTLINE DRAWING



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D_1	0.783	0.791	19.90	20.10
E	0.622	0.638	15.80	16.20
E_1	0.547	0.555	13.90	14.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISIONS

Rev. 1.0.1 changed package from 14x14mm 128 pins to 14x20mm 128 pins.

Rev. 1.0.2 Added info on serial processor interface. Corrected pin out for pins 33, 34, 35, 36, 37, 38, 97, 98, 101 and 102.

Rev. 1.0.3 Corrected typos in pin list (pin 29, 51, 64 and 118) and Pin out diagram (pins 47, 48 and 69).