T1/E1 Essentials

WHITE PAPER

Darren Pool

Manager, SONET Aggregation and T/E Carrier Applications Group

XRWP00001

TABLE OF CONTENTS

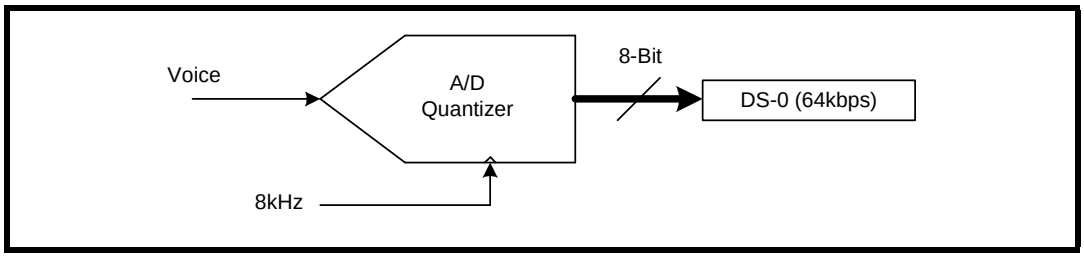
1.0 INTRODUCTION TO T1

Digital cross connect systems transport T1 lines deployed in North America and Canada. The T1 signal is the basic standard of PDH and is discussed in this section.

1.1 A Brief History of the Emergence of the Digital Signal Hierarchy

The need to transmit analog voice over digital transmission medium resulted in the formation of the Digital Signal Hierarchy in North America in the early 1960's. The DS0 constitutes the smallest fundamental unit in the Digital Signal Hierarchy. Human hearing is able to sufficiently discern voice intelligibly between a 300 Hz to 3300 Hz range resulting in a 4kHz voice baseband in telephony. To meet the Nyquist minimum sampling theorem of the 4kHz voice baseband signal, the DS0 must be sampled or repeated at an 8kHz interval using an 8-bit Quantization A/D. This yields (8bits x 8kHz) 64kbps.

FIGURE 1. VOICE TO DS-0 USING AN 8-BIT QUANTIZER



To generate the DS1 framing structure, 24 DS0 channels are multiplexed in addition to 1 Overhead Bit resulting in 193 bits per DS1 frame. Therefore, a given DS1 channel bit-rate runs at 1.544 Mbps (193bits x 8kHz).

TABLE 1: DIGITAL SIGNAL HIERARCHY

DIGITAL SIGNAL LEVEL	BIT RATE	NUMBER OF VOICE CHANNELS	EQUIVALENT
DS0	64 kbps	1	-
DS1	1.544 Mbps	24	24 DS0's
DS2	6.312 Mbps	96	4 DS1's
DS3	44.736 Mbps	672	7 DS2's

1.2 Summary of DS1 General Specifications

The following is a summary of DS1 specifications.

TABLE 2: SUMMARY OF DS1 SPECIFICATIONS

Parameter	Specification
Nominal Bit Rate	1,544 kbps
Line Rate Accuracy	+/- 32 ppm
Line Code	AMI or B8ZS
Medium	One balanced twisted pair for each direction.
Test Load	100 Ohms +/- 5%
Pulse Amplitude	The amplitude of an isolated pulse shall be between 2.4v and 3.6v.

1.3 Bit Stream Encoding/Decoding

For all digital bit streams rates, sufficient energy must exist such that network elements can maintain timing extraction from the incoming data, known as Loop Timing Systems. As such, too many consecutive zeros can lead to timing extraction issues and cause a distruption in timing events and synchronization. In DS1, the line coding used is B8ZS (Bipolar With 8 Zero Substitution). This method utilizes "violation" pulses so that the recovering circuitry can distinguish between data and an encoded signal.

In B8ZS encoding, any sequence of eight consecutive zeros is replaced with {000VB0VB}. The polarity of the V pulses are the same as its preceding pulse. Therefore, there are two possibilities for its substitution.

TABLE 3: EXAMPLES OF B8ZS CODING

Case 1	Preceding Pulse	Next 8 Bits
Input	+	00000000
B8ZS Substitution		000VB0VB
Output	+	000+-0-+
Case 2		
Input	-	00000000
B8ZS Substitution		00VB0VB
Output	-	000-+0+-

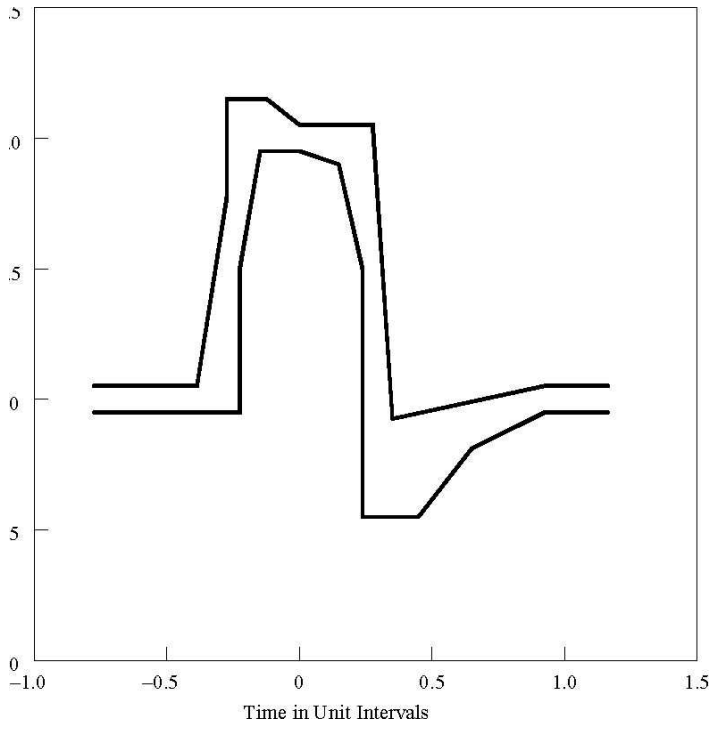
1.4 Pulse Template Requirements

An isolated pulse preceded by 4 consecutive zeros must fit within the pulse template shown below. In addition, there are five LBO (Line Build Out) settings for short haul specifications. Here are the five LBO settings:

TABLE 4: LBO SHORT HAUL SPECIFICATIONS

0 - 133 feet
133 - 266 feet
266 - 399 feet
399 - 533 feet
533 - 655 feet

FIGURE 2. T1 PULSE TEMPLATE



1.5 Digital Equipment Timing Jitter Requirements

Timing jitter is the short term variation (phase oscillations) from a digital signal's ideal positions. Jitter is commonly measured in peak-to-peak in unit intervals, (UIpp). There are three types of jitter in DS1 applications.

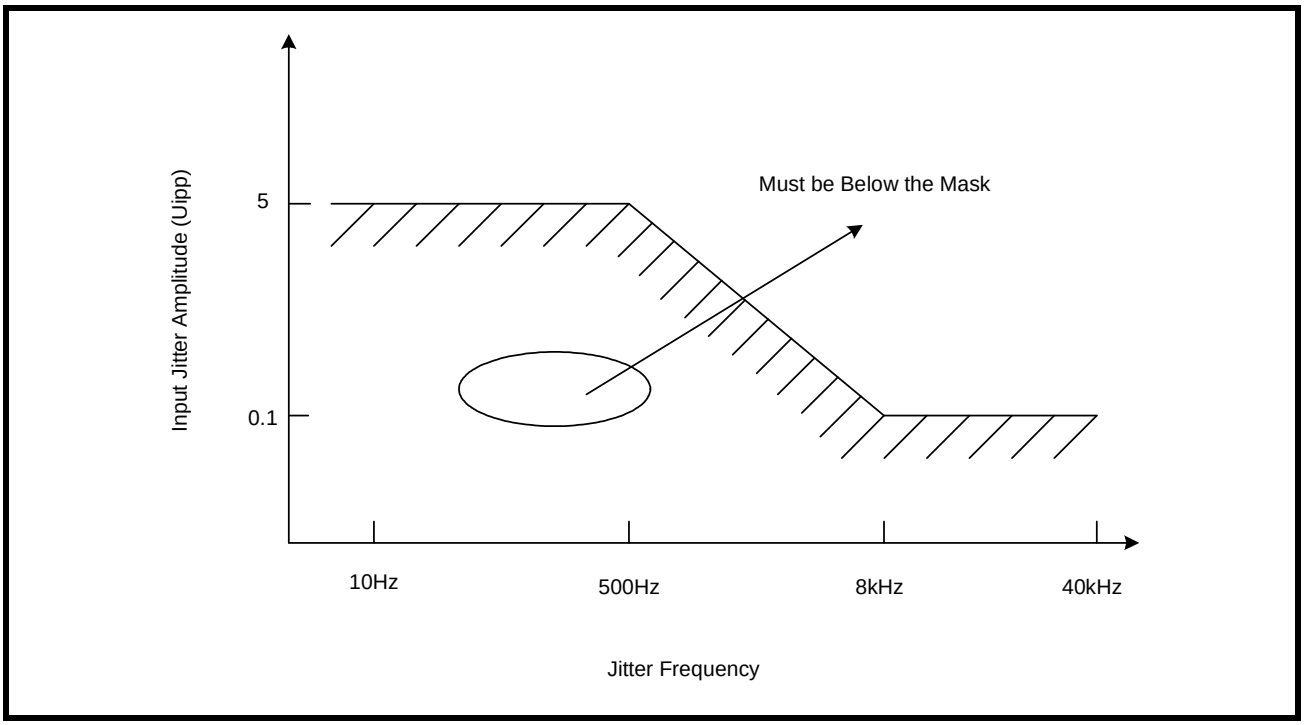
- Jitter Tolerance
- Jitter Transfer
- Jitter Generation

NOTE: *DS1's extracted from higher rate signals are subject to Category II (or GR-253-Core if demapped from Sonet/SDH in Virtual Tributary VT1.5 applications).*

1.6 Jitter Tolerance

Input jitter tolerance is defined as the minimum amplitude of sinusoidal jitter at a given frequency that, when modulating the signal, results in more than 2 erred seconds in a 30 second interval. Requirements on input jitter tolerance are then given in terms of a jitter tolerance mask, which represents the minimum acceptable jitter tolerances for a specified range of jitter frequencies.

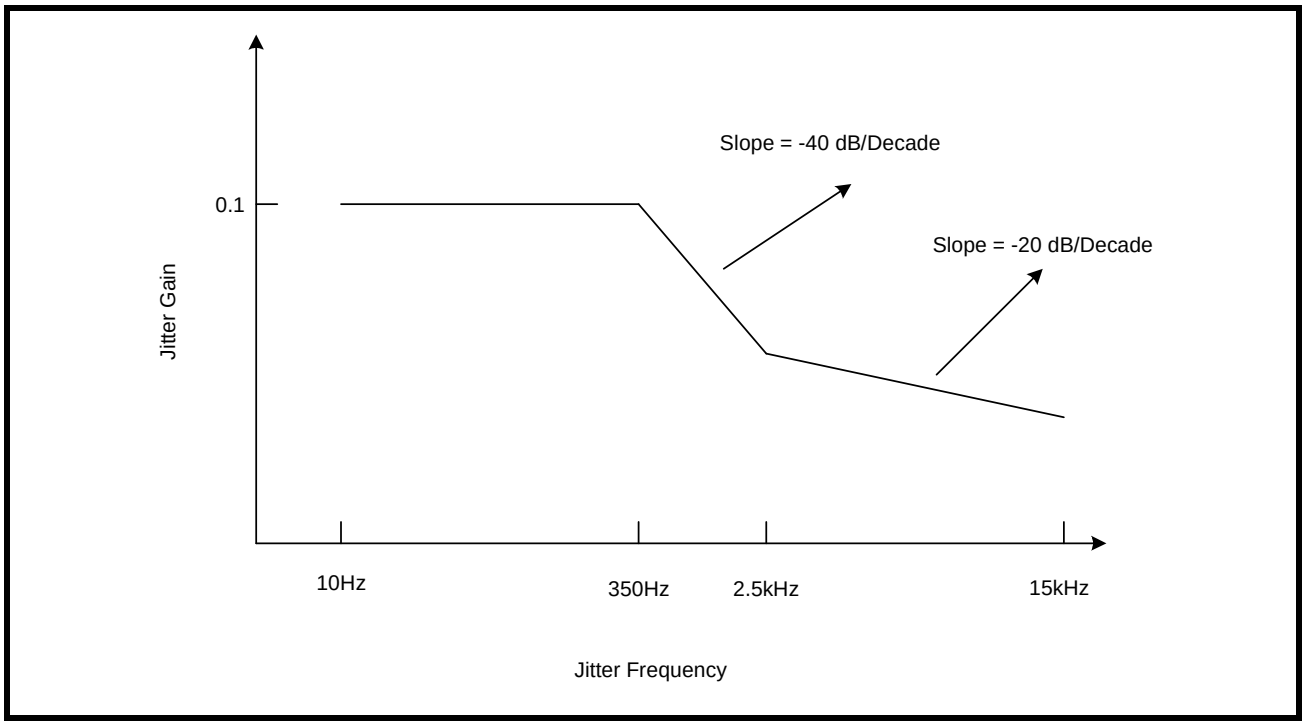
FIGURE 3. JITTER TOLERANCE MASK



1.7 Jitter Transfer

Transfer of jitter is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. The gain of jitter over frequency must be within 0.1UIpp.

FIGURE 4. JITTER TRANSFER CURVE



1.8 Jitter Generation

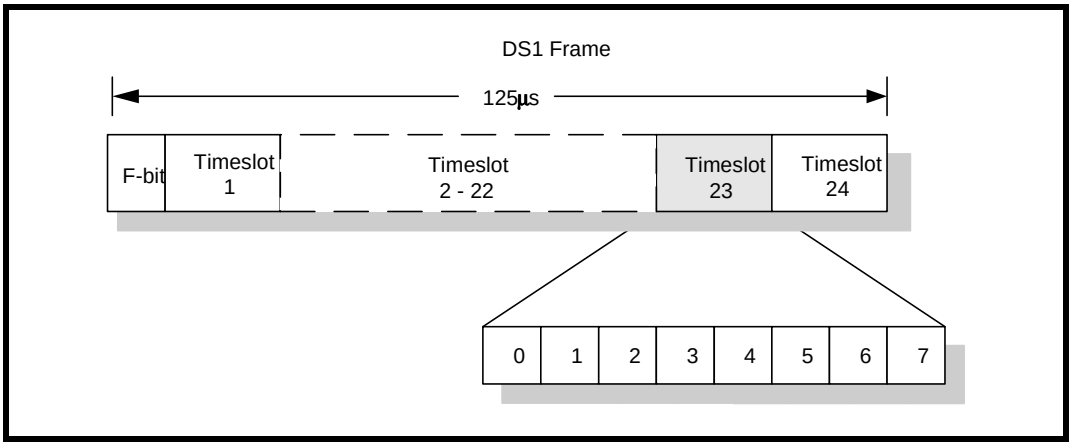
Jitter generation is the measure of pure output jitter with no input jitter applied. As where jitter transfer is a measure of jitter gain (equipment adds jitter in the process), jitter generation is a measure of the digital equipment without the influence added jitter during the measurement process.

2.0 THE DS1 FRAMING STRUCTURE

With all the advances in T1 carrier over the years, it is still important to support legacy T1 framing formats. When a T1 line card is deployed in a network, it must have the capability to recognize and communicate to any one of the five available framing formats. EXAR's stand alone framers and Framer+LIU (One chip solution) support legacy framing in addition to the latest features T1 has to offer.

A single T1 frame is 193 bits long and is transmitted at a frame rate of 8kHz. This results in an aggregate bit rate of 1.544 Mbit/s. Basic frames are divided into 24 timeslots numbered 1 thru 24 and a framing bit as shown in **Figure 5**. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. This results in a single timeslot data rate of 8 bits x 8,000/sec = 64 kbit/s.

FIGURE 5. T1 FRAME FORMAT



2.1 T1 Super Frame Format (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF) as shown in **Figure 6** and **Table 5**. This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating ones and zeros (101010) in odd frames that defines the boundaries so that one timeslot may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

FIGURE 6. T1 SUPERFRAME PCM FORMAT

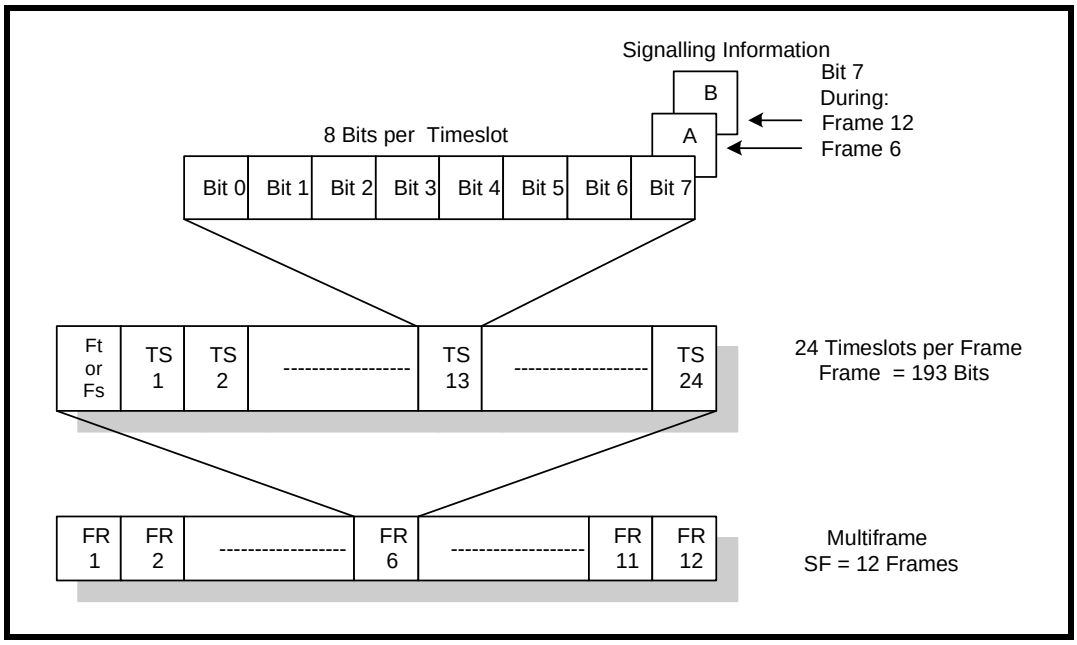


TABLE 5: SUPERFRAME FORMAT

FRAME	BIT	F-BITS		BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL
		TERMINAL FRAMING FT	TERMINAL FRAMING FS	TRAFFIC	SIG	
1	0	1	----	1-8	----	----
2	193	----	0	1-8	----	----
3	386	0	----	1-8	----	----
4	579	----	0	1-8	----	----
5	772	1	----	1-8	----	----
6	965	----	1	1-7	8	A
7	1158	0	----	1-8	----	----
8	1351	----	1	1-8	----	----
9	1544	1	----	1-8	----	----
10	1737	----	1	1-8	----	----
11	1930	0	----	1-8	----	----
12	2123	----	0	1-7	8	B

2.2 T1 Extended Superframe Format (ESF)

In Extended Superframe Format (ESF), as shown in **Figure 7** and **Table 6**, the multiframe structure is extended to 24 frames. The timeslot structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit) and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1.Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2.Facility Data Link (FDL), which allows data such as error-performance to be passed within the T1 link.
3.Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

FIGURE 7. T1 EXTENDED SUPERFRAME FORMAT

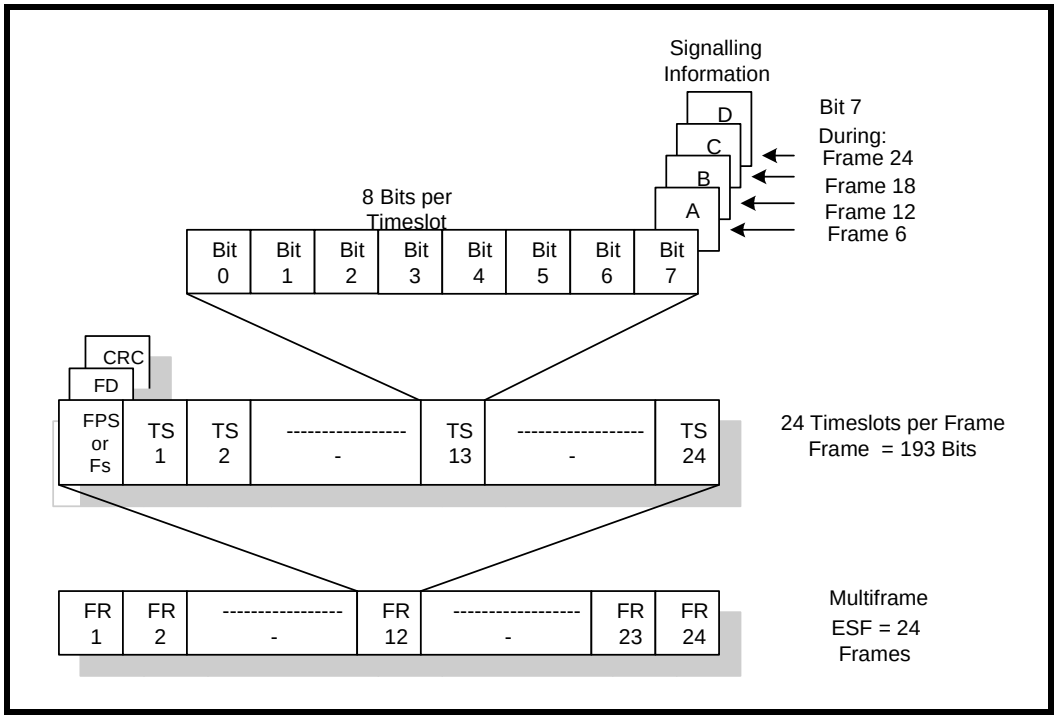


TABLE 6: EXTENDED SUPERFRAME FORMAT

FRAME	BIT	F-BITS			BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL		
		FPS	DL	CRC	TRAFFIC	SIG	16	4	2
1	0	----	m	----	1-8	----	----	----	----
2	193	----	----	C1	1-8	----	----	----	----
3	386	----	m	----	1-8	----	----	----	----
4	579	0	----	----	1-8	----	----	----	----
5	772	----	m	----	1-8	----	----	----	----
6	965	----	----	C2	1-7	8	A	A	A
7	1158	----	m	----	1-8	----	----	----	----
8	1351	0	----	----	1-8	----	----	----	----
9	1544	----	m	----	1-8	----	----	----	----
10	1737	----	----	C3	1-8	----	----	----	----
11	1930	----	m	----	1-8	----	----	----	----
12	2123	1	----	----	1-7	8	B	B	A
13	2316	----	m	----	1-8	----	----	----	----
14	2509	----	----	C4	1-8	----	----	----	----
15	2702	----	m	----	1-8	----	----	----	----
16	2895	0	----	----	1-8	----	----	----	----
17	3088	----	m	----	1-8	----	----	----	----
18	3281	----	----	C5	1-7	8	C	A	A
19	3474	----	m	----	1-8	----	----	----	----
20	3667	1	----	----	1-8	----	----	----	----
21	3860	----	m	----	1-8	----	----	----	----
22	4053	----	----	C6	1-8	----	----	----	----
23	4246	----	m	----	1-8	----	----	----	----
24	4439	1	----	----	1-7	8	D	B	A

NOTES:

1. *FPS indicates the Framing Pattern Sequence (...001011...)*
2. *DL indicates the 4kb/s Data Link with message bits m.*
3. *CRC indicates the cyclic redundancy check with bits C1 to C6*
4. *Signaling options include 16 state, 4 state and 2 state.*

2.3 T1 Non-Signaling Frame Format

The Non-Signaling (N) framing format is a simplified version of the T1 super frame. The N-Frame consists of four frames with two Fs bits and two Ft bits. The Fs bits can be used as a proprietary 4kbps data link transmission. Signaling is not supported in this framing format.

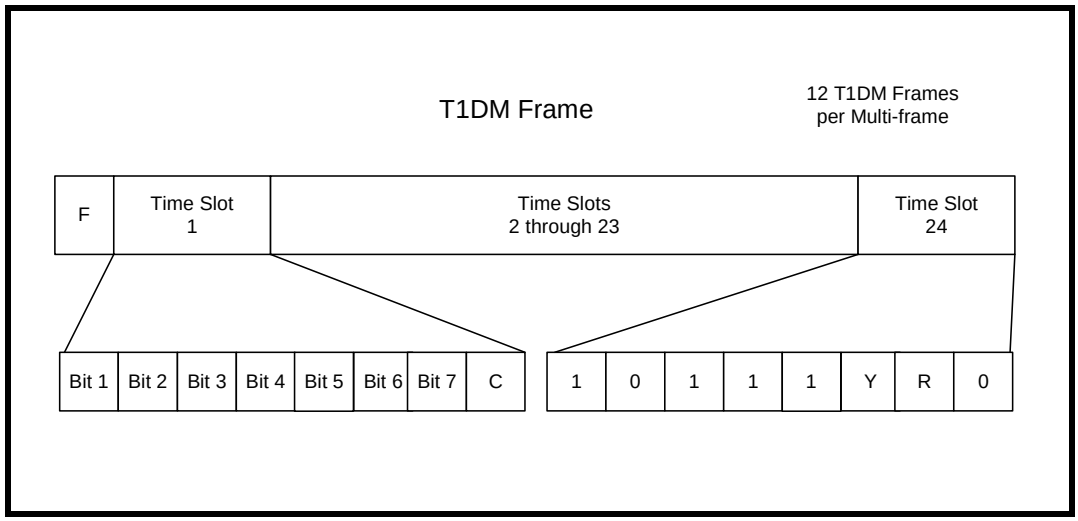
TABLE 7: NON-SIGNALING FRAMING FORMAT

FRAME	BIT	F-BITS	
		TERMINAL FRAMING FT	TERMINAL FRAMING FS
1	0	1	----
2	193	----	X
3	386	0	----
4	579	----	X

2.4 T1 Data Multiplexed Framing Format (T1DM)

T1DM uses a similar framing structure as the SF (D4), such that the Fs and Ft bits on the individual frame boundaries remain the same. The differentiation between T1DM and SF is within the payload time slots. Time slot 24 cannot be used for data when configured for T1DM. Time slot 24 is dedicated for a special synchronization byte as shown in **Figure 8**. The Y-bit is to carry the status of the Yellow Alarm. The R-bit is dedicated for a remote signaling bit typically not used. However, the framer allows this bit to carry an HDLC message. Time slots 1 through 23 are used to carry the seven bit word from each of the 23 DS-0 signals.

FIGURE 8. T1DM FRAME FORMAT



2.5 SLC-96 Format (SLC-96)

SLC framing mode allows synchronization to the SLC®96 data link pattern. This pattern described in Bellcore TR-TSY-000008, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern. See Table 8.

TABLE 8: SLC®96 FS BIT CONTENTS

FRAME #	FS BIT	FRAME #	FS BIT	FRAME #	FS BIT
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

NOTES:

1. *The SLC®96 frame format is similar to that of SF as shown in Table 5 with the exceptions shown in this table.*
2. *C1 to C11 are concentrator bit fields.*
3. *M1 to M3 are Maintenance bit fields.*
4. *A1 and A2 are alarm bit fields.*
5. *S1 to S4 are line switch bit fields.*
6. *The Fs bits in frames 46, 48 and 70 are spoiler bit switch are used to protect against false multiframing.*

3.0 INTRODUCTION TO E1

E1 is the European counter part to T1 which is supported everywhere in the world except North America, Canada, and Japan. Although its structure is slightly different, it deploys the same concepts when transmitting data from one locality to another.

3.1 Summary of E1 General Specifications

The following is a summary of E1 specifications.

TABLE 9: SUMMARY OF E1 SPECIFICATIONS

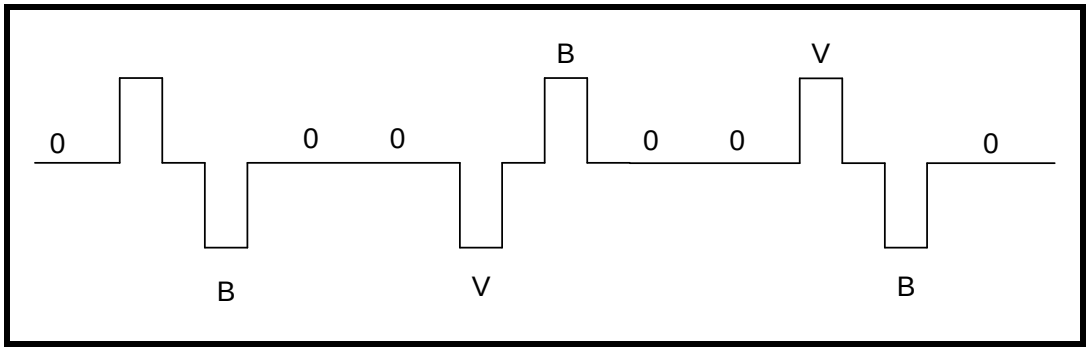
Parameter	Specification	
Nominal Bit Rate	2,048 kbps	
Line Rate Accuracy	+/- 50 ppm	
Line Code	HDB3	
Medium	Balanced Pair	Coax Cable
Test Load	120 Ohms	75 Ohms
Pulse Amplitude	3.0v	2.37v

3.2 Bit Stream Encoding/Decoding

For all digital bit streams rates, sufficient energy must exist such that network elements can maintain timing extraction from the incoming data, known as Loop Timing Systems. As such, too many consecutive zeros can lead to timing extraction issues and cause a distruption in timing events and synchronization. In E1, the line coding used is HDB3 (High Density Bipolar With 3 Zero Substitution). This method utilizes "violation" pulses so that the recovering circuitry can distinguish between data and an encoded signal.

In HDB3 encoding, any sequence of four consecutive zeros will be replaced by 000V or B00V. The choice is made so that the number of B pulses between consecutive V pulses is odd. Successive V pulses are of alternate polarity to avoid the possibility of a DC component.

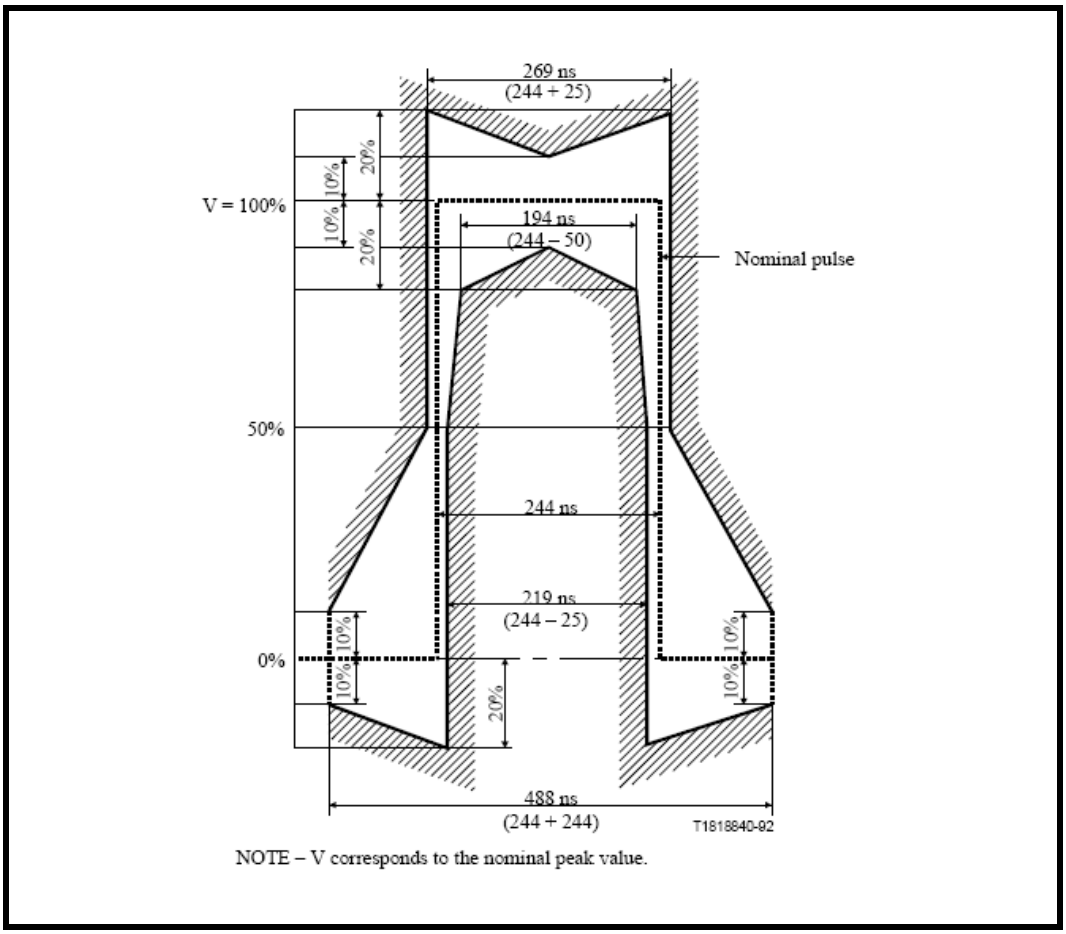
FIGURE 9. EXAMPLE OF HDB3 FOR AN ALL ZERO BIT STREAM



3.3 Pulse Template Requirements

All marks of a valid signal must conform to the pulse mask shown below. The value V corresponds to the nominal amplitude of the pulse. For Coax 75Ω, the nominal voltaga is 2.37v. For balanced twisted pair 120Ω, the nominal voltage is 3.0v.

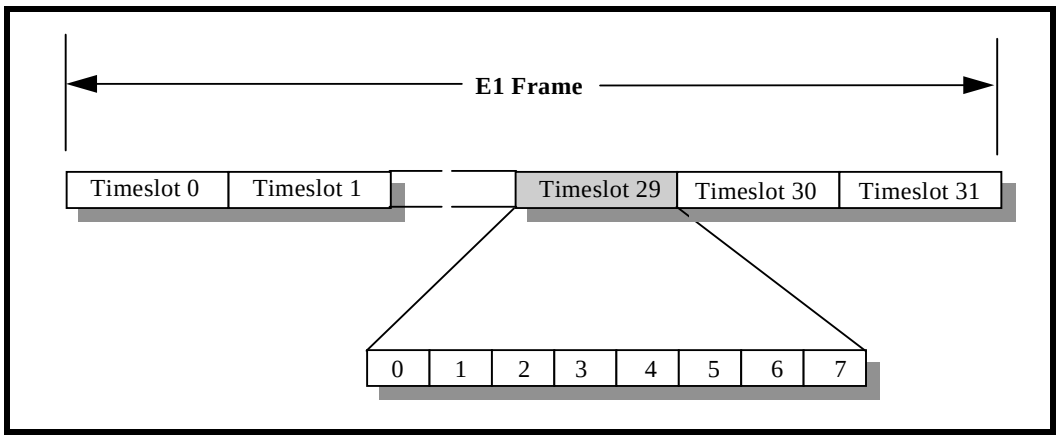
FIGURE 10. E1 PULSE TEMPLATE



4.0 THE E1 FRAMING STRUCTURE

A single E1 frame consists of 256 bits which is created 8,000 times per second. This yields a bit-rate of 2.048Mbps. The 256 bits within each E1 frame are grouped into 32 octets or timeslots. These timeslots are numbered from 0 to 31. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. **Figure 11** presents a diagram of a single E1 frame.

FIGURE 11. SINGLE E1 FRAME DIAGRAM



Not all of these timeslots are available to transmit voice or user data. For instance, timeslot 0 is always reserved for system use and timeslot 16 is sometimes used (reserved) by the system. Hence, within each E1 frame, either 30 or 31 of the 32 timeslots are available for transporting user or voice data. In general, there are two types of E1 frames, FAS and Non-FAS. In any E1 data stream, the E1 frame begins with a FAS frame followed by Non-FAS frame and then alternates between the two.

4.1 FAS Frame

Timeslot 0 within the FAS E1 frame contains a framing alignment pattern and therefore supports framing. The bit-format of timeslot 0 is presented in **Table 10**. The Si bit within the FAS E1 Frame typically carries the results of a CRC-4 calculation. The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) will be used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes.

TABLE 10: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A FAS E1 FRAME

BIT	0	1	2	3	4	5	6	7
Value	SI	0	0	1	1	0	1	1
Function	International Bit	Frame Alignment Signaling (FAS) Pattern						
Description-Operation	In practice, the Si bit within the FAS E1 Frame carries the results of a CRC-4 calculation.	The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) is used by the Receive E1 Framer at the Remote terminal for frame synchronization/ alignment purposes.						

4.2 Non-FAS Frame

Timeslot 0 within the non-FAS E1 frame contains bits that support signaling or data link message transmission. The bit-format of timeslot 0 is presented in **Table 11**. The Si bit in the Non-FAS frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.

TABLE 11: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A NON-FAS E1 FRAME

BIT	0	1	2	3	4	5	6	7
Value	Si	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
Function6	International Bit	Fixed Value	Yellow Alarm	National bits				
Description-Operation	International Bit The Si bit within the non-FAS E1 Frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.	Fixed at “1” Bit-field “1” contains a fixed value “1”. This bit-field will be used for FAS framing synchronization/alignment purposes by the Remote Receive E1 Framer.	FAS Frame Yellow Alarm Bit This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to “0” during normal conditions, and is set to “1” whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.	National Bits These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.				

4.3 The E1 Multi-frame Structure

There are two types of E1 Multi-frame structures, CRC Multi-frame and CAS Multi-frame. The CAS Multi-frame can be considered a subset of the CRC Multi-frame, in that CAS is an option to carry signaling information within the CRC Multi-frame structure.

4.3.1 The CRC Multi-frame Structure

A CRC Multi-frame consists of 16 consecutive E1 frames, with the first of these frames being a FAS frame. From a Frame Alignment point of view, timeslot 0 of each of these E1 frames within the Multi-frame are the most important 16 octets. **Table 12** presents the bit-format for all timeslot 0 octets within a 16 frame CRC Multi-frame.

TABLE 12: BIT FORMAT OF ALL TIMESLOT 0 OCTETS WITHIN A CRC MULTI-FRAME

SMF	FRAME NUMBER	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
2	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

The CRC Multi-frame is divided into 2 sub Multi-Frames. Sub-Multi-Frame 1 is designated as SMF1 and Sub-Multi-Frame 2 is designated as SMF2. SMF1 and SMF2 each consist of 8 E1 frames having 4 FAS frames and 4 non-FAS frames. There are two interesting things to note in **Table 12**. First, all of the bit-field 0 positions within each of the FAS frames (within each SMF) are designated as C1, C2, C3 and C4. These four bit-fields contain the CRC-4 values which have been computed over the previous SMF. Hence, while the Transmit E1 Framer is assembling a given SMF, it computes the CRC-4 value for that SMF and inserts these results into the C1 through C4 bit-fields within the very next SMF. These CRC-4 values ultimately are used by the Remote Receive E1 Framer for error detection purposes.

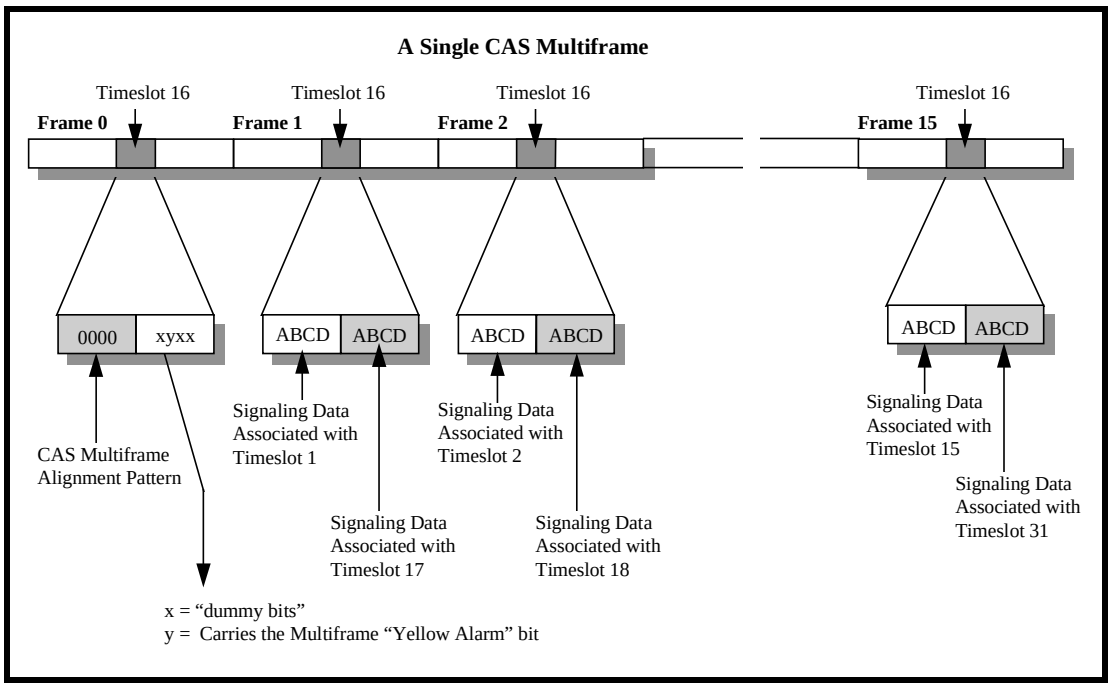
NOTE: *This framing structure is referred to as a CRC Multi-Frame because it permits the remote receiving terminal to locate and verify the CRC-4 bit-fields.*

The second interesting thing to note regarding **Table 12** is that the bit-field 0 positions within each of the non-FAS frames (within the entire MF) are of a fixed 6-bit pattern 0, 0, 1, 0, 1, 1 along with two bits, each designated as “E”. This 6-bit pattern is referred to as the CRC Multi-Frame alignment pattern, which can ultimately be used by the Remote Receive E1 Framer for CRC Multi-Frame synchronization/alignment. The "E" bits are used to indicate that the Local Receive E1 framer has detected errored sub-Multi-Frames.

4.4 Channel Associated Signaling

If the user operates an E1 channel in Channel Associated Signaling, then timeslot 16 octets within each E1 frame will be reserved for signaling. Such signaling would convey information such as On-Hook, Off-Hook conditions, call set-up, control, etc. In CAS, this type of signaling data that is associated with a particular voice channel will be carried within timeslot 16 of a particular E1 frame within a CAS Multi-Frame. The CAS is carried in a Multi-Frame structure which consists of 16 consecutive E1 frames. The framing/byte format of a CAS Multi-Frame is presented in **Figure 12**.

FIGURE 12. FRAME/BYTE FORMAT OF THE CAS MULTI-FRAME STRUCTURE



Timeslot 16 within frame 0 is a special octet that is used to convey CAS Multi-Frame alignment information, and to convey Multi-Frame alarm information to the Remote Terminal. The bit-format of timeslot 16 within frame 0 of a CAS Multi-Frame is 0000 xyxx. The upper nibble of this octet contains all zeros and is used to identify itself as the CAS Multi-Frame alignment signal. If CAS is used, then the user is advised to insure that none of the other timeslot 16 octets contain the value "0000". The lower nibble of this octet contains the expression "xyxx". The x-bits are the spare bits and should be set to "0" if not used. The y-bit is used to indicate a Multi-Frame alarm condition to the Remote terminal. During normal operation, this bit-field is cleared to "0". However, if the Local Receive E1 Framer detects a problem with the incoming Multi-Frames, then the Local Transmit E1 Framer will set this bit-field within the next outbound CAS Multi-Frame to "1".

NOTE: *The Local Transmit E1 Framer will continue to set the y-bit to "1" for the duration that the Local Receive E1 Framer detects this problem.*

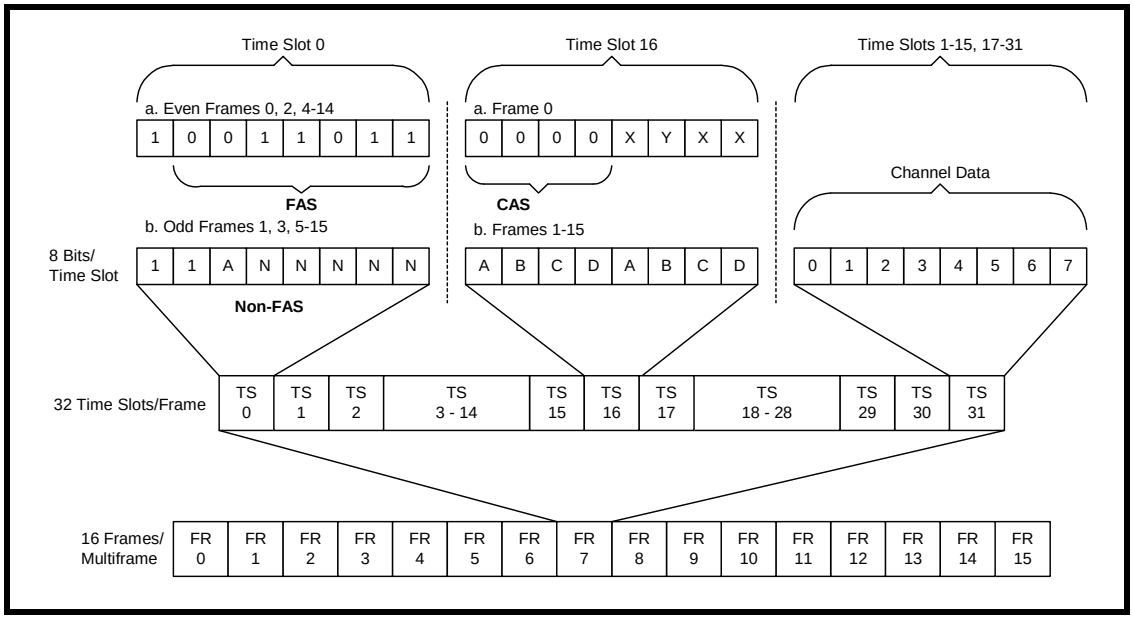
Timeslot 16 within Frame 1 of the CAS Multi-Frame contains 4 bits of signaling data for voice channel 1 and 4 bits of signaling data for voice channel 17. Timeslot 16 within Frame 2 contains 4 bits of signaling data for voice channel 2 and 4 bits of signaling data for voice channel 18, and this continues for all E1 frames.

4.5 Common Channel Signaling (CCS)

Common Channel Signaling is an alternative form of signaling from CAS. In CCS, whatever signaling data which is transported via the outbound E1 data stream, carries information that applies to all of the voice channels as a set (e.g., timeslots 1 through 15 and 17 through 31) in the E1 frame. There are numerous other variations of Common Channel Signaling that are available. Some of these are listed below.

- 31 Voice Channels with the common channel signaling being transported via the National Bits.
- 30 Voice Channels with the common channel signaling data being transported via the National Bits and CAS data being transported via timeslot 16.
- 30 Voice Channels with the Common Channel Signaling being processed via timeslot 16. (e.g., Primary Rate ISDN Signaling).

FIGURE 13. E1 FRAME FORMAT



5.0 REFERENCES

1. Bellcore Generic Requirements GR-499-CORE

   Transport Systems Generic Requirements (TSGR): Common Requirements

2. International Telecommunications Union ITU-T G.703

   Series G: Transmission Systems and Media, Digital Systems and Networks: Digital Terminal Equipments - General