ENVISIONING • EMPOWERING • EXCELLING

MAXLINEAR

# XR791xx Family Layout Recommendations

## Application Note AN-230

# Revision History

| Revision | Release Date | Change Description |
|---|---|---|
| 230ANR00 | 12/20/19 | Initial release of document. |

# Table of Contents

# List of Figures

# Introduction

When it comes to PCB layout, it is very important to follow a few simple guidelines in order to achieve and maintain optimum performance. This Application Note will cover guiding principles for component placement and ground planes around the XR791xx Family of Power Modules, including the XR79103, XR79106, and XR79110.

# General Information

The layout must be as neat and compact as possible by placing all the components close to their associated pins. This practice reduces the amount of parasitic inductances in the return path, which helps minimize the ON and OFF current loops shown in Figure 1 and Figure 2. During the ON time, the high side FET (QH) is turned ON, while the low side (QL) is OFF. The current flow is from $C_{IN}$ through QH, inductor L, output capacitor $C_{OUT}$ and back into $C_{IN}$ as shown in Figure 1.

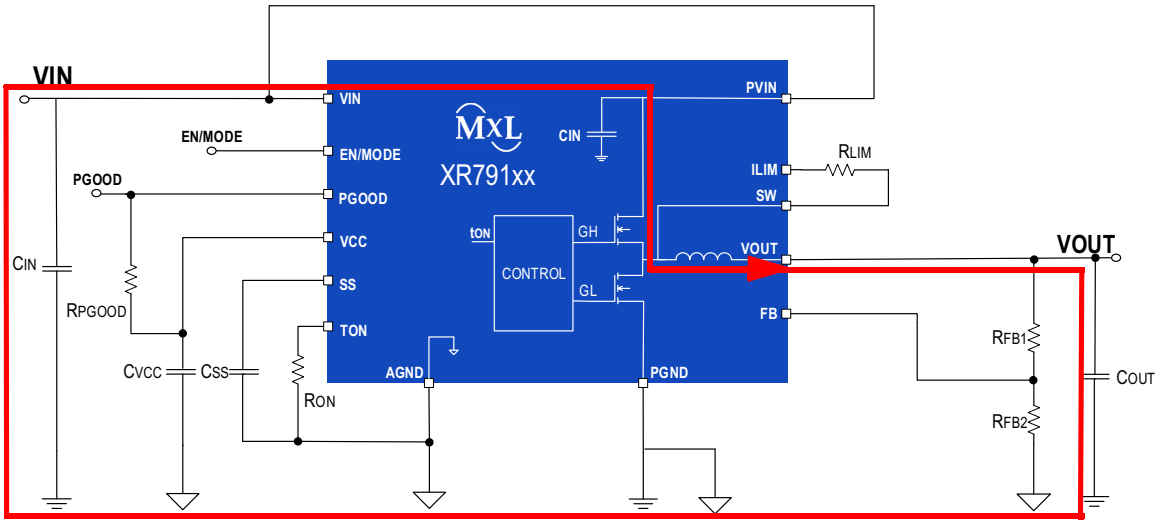


**Figure 1: Current Flow During ON Time**

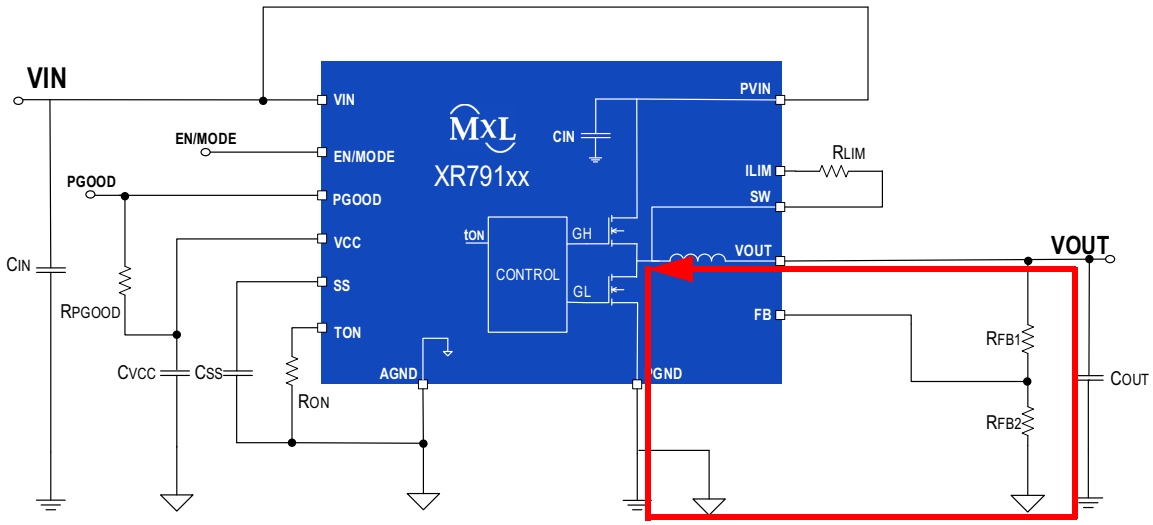


**Figure 2: Current Flow During OFF Time**

During the OFF time, QH is OFF and QL is ON forming the second current loop. Since QH is OFF, the return current path is now through the source of QL, which is connected to PGND. The current flow is through the low side switch QL, inductor L, capacitor $C_{OUT}$ and back to QL as shown in Figure 2.

## Switch Nodes

As shown in Figure 1 and Figure 2 above, there are two major current loops in a synchronous buck converter. These loops share a common switching node (SW) which connects the high side switch QH, low side switch QL and inductor L. Since this node experiences voltage swings from GND to $V_{IN}$, it is critical that it be kept away from sensitive lines to avoid noise coupling into those lines. Current in the switching node can switch at several amps per microsecond. For this reason, charge reservoir capacitors $C_{IN}$ and $C_{OUT}$ need to be placed close to the device input and output pins, respectively, to supply instantaneous power requirements. For this reason, large capacitors (10µF – 100µF) should be placed no more than 1 inch away from the power module's input and output pins. High frequency capacitors (0.01µF – 0.1µF) should be placed as closed to the pins as allowed, to reduce noise. This practice helps to minimize the effects of EMI from the PCB.

## Ground

The ground is the point with which all the signals are referenced against on a PCB. On the XR79103, there are two such references, AGND and PGND. Maxlinear recommends the use of an AGND island directly under the device. This AGND island should be the reference for all small signal components. The rest of the ground plane should be treated as the power stage reference (PGND).

**AGND** → IC analog reference GND. AGND serves as reference for small-signal components. Components referenced to AGND are $C_{VCC}$, $R_{ON}$, $C_{SS}$ and $V_{OUT}$ resistor divider $R_{FB2}$.

**PGND** → Power stage reference ground. It is the return path for the module's low side driver and should be connected to low side FET source. For the example of the XR79103, the high side and low side FETs are co-packaged within the module. $C_{IN}$, as well as pins 7, 9-14, and 29-30 should be connected to, and share the power stage reference (PGND).

Both **AGND** and **PGND** signals should then be joined to each other with a single low impedance connection, away from the VIN input pins and close to the VOUT pins (see Figure 4). Figure 3 below shows the 2 ground planes isolated from each other and joined by a single connection.

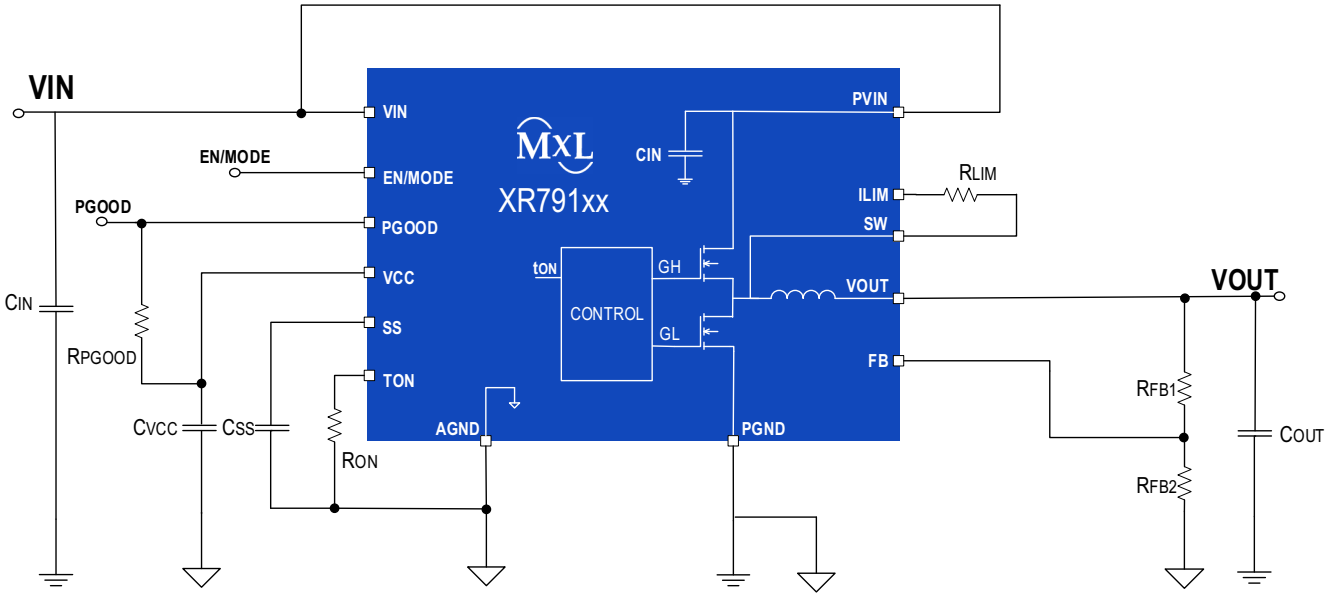


**Figure 3: Typical Application Circuit**

Figure 4 and Figure 5 below, show the recommended layout example for joining AGND and PGND in an area away from the input pins VIN.

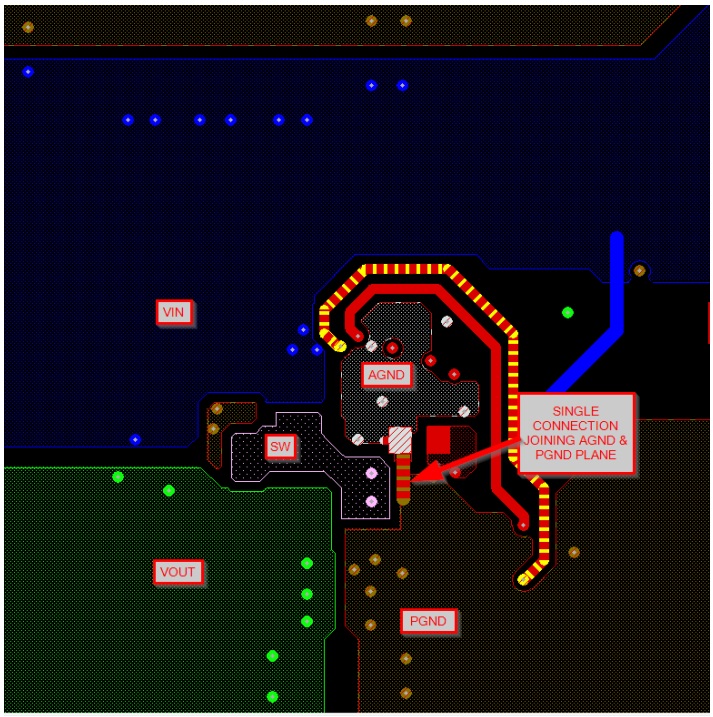


**Figure 4: Single Connection Joining AGND and PGND on Bottom Layer of XR79103 Evaluation Board**

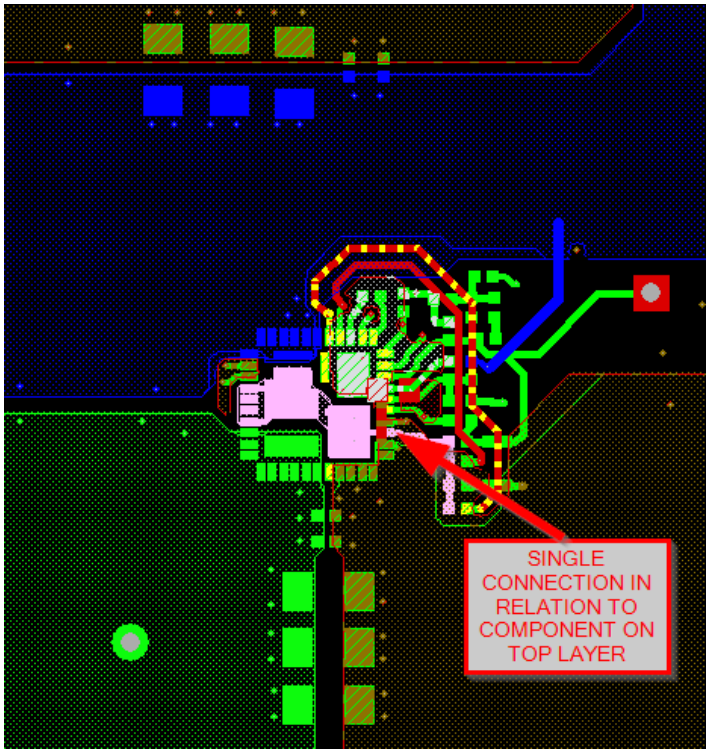


**Figure 5: Top and Bottom Layers, Single Connection in Relation to Components**

This layout example shows what NOT to do with the placement of input and output capacitors $C_{IN}$ and $C_{OUT}$. As it can be seen, the input capacitor placement is too far with respect to the associated VIN pins. Although this will work, performance cannot be guaranteed for all applications. For best results, it is recommended they be placed close to the device as shown in Figure 6 below.

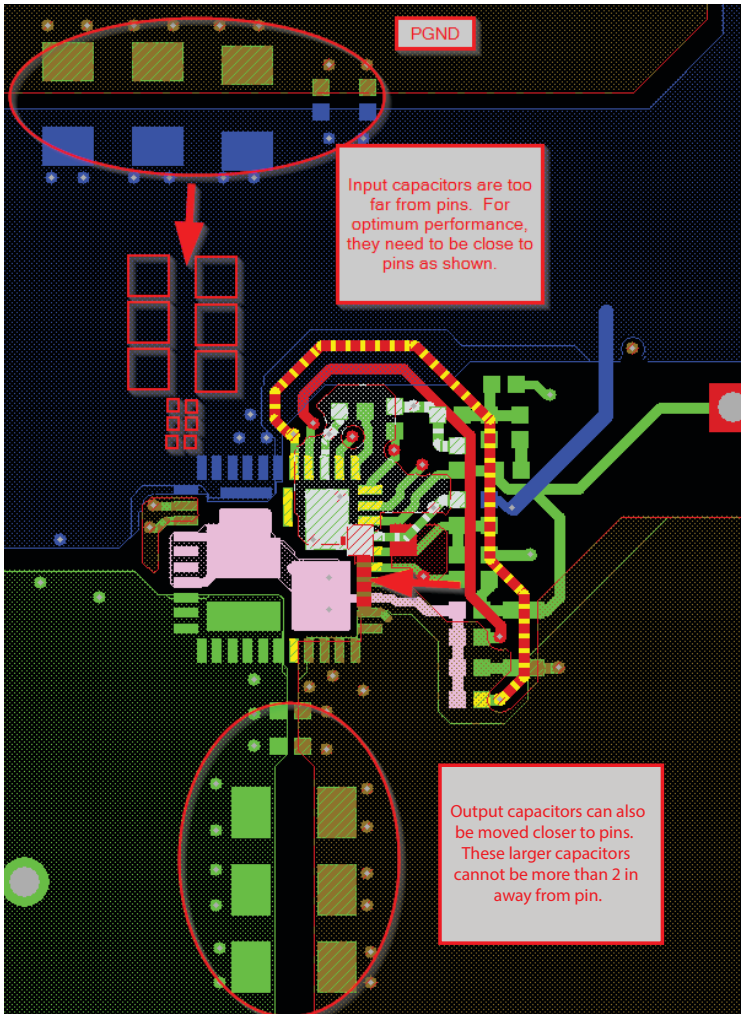


**Figure 6: Input Capacitor Placement on XR79103 Evaluation Board**

# Power Plane

Maxlinear recommends the use of a power plane for the main power supplies. This plane must be low impedance to reduce losses and improve efficiency. Input and output decoupling capacitors should be used to decouple the power plane, and these capacitors should be placed as close as possible to associated pins to reduce line inductance and series resistance between the decoupling components and the device.

## Vias

PCB vias are inductive at high frequencies and will therefore increase the ground impedance. Having multiple vias in place will reduce this effect as the inductances are in parallel. Maxlinear recommends the use of ground-fill for the remaining layers. When using ground-fill, it is important that there are plenty of vias connecting this fill to the main ground plane. The vias must be placed in a way as to not cut-up the plane excessively.

**MaxLinear, Inc.**
**5966 La Place Court, Suite 100**
**Carlsbad, CA 92008**
**760.692.0711 p.**
**760.444.8598 f.**

www.maxlinear.com