# SP507 SERIES MULTI-PROTOCOL RS-232 LATCH-UP PREVENTION

## 1.0 INTRODUCTION

The purpose of this application note is to alert users of the SP504, SP505, SP506 and SP507 of an application condition that can lead to a latch-up of the device.

Note: SP508E and SP510E are not affected by this application issue.

## 2.0 DESCRIPTION

The condition is defined as a latch-up upon power-up of a device that is connected together in a DCE/DTE configuration in V.28/RS-232 mode.

In the following example the application is two SP507's connected together in a DCE/DTE configuration. The DCE SP507 is powered on and the DTE SP507 is not powered on. The DCE SP507 is configured in RS-232 mode with the decoder M2-M0 set to 110.

Part of this configuration is shown in Figure 1 below. The RS-232 outputs (SD(a) and TR(a)) of the DCE SP507 should be +/-9V depending upon the state of their respective inputs.

**FIGURE 1. PORTION OF DCE/DTE CONFIGURATION**

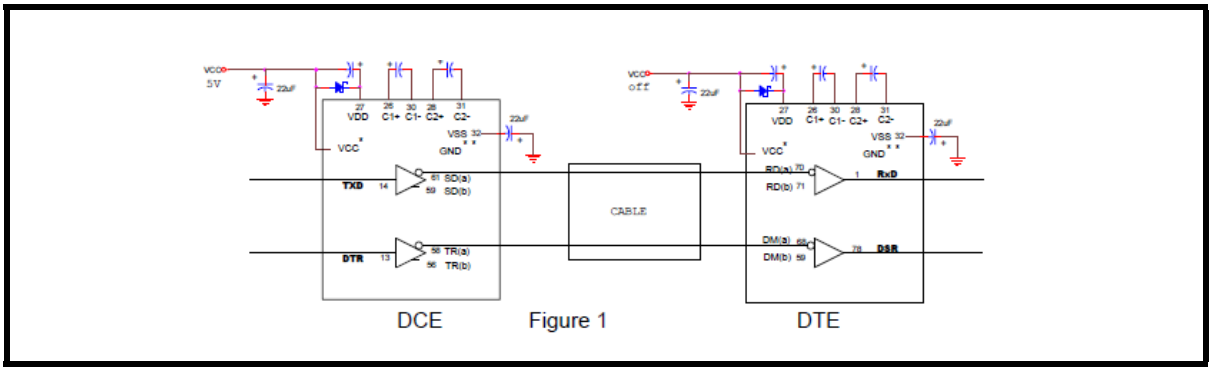


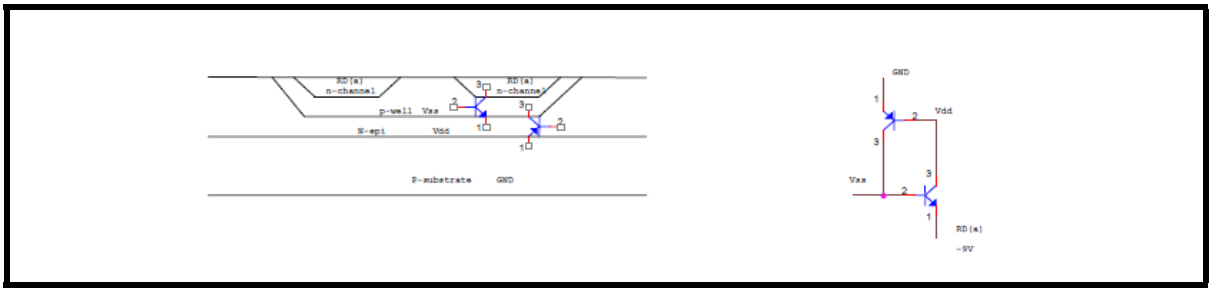
Figure 1

To create the latch condition the DTR line of the DCE SP507 Receiver input is a logic 1 which translates to the TR(a) output being -9V and the TxD line is a logic 0 with the SD(a) output at +9V. These voltages are then present on the un-powered DTE SP507 Receiver inputs DM(a) and RD(a) respectively.

In this scenario a parasitic SCR is triggered on by the +9V and -9V differential on the RD(a) and SD(a) inputs which causes the SD(a) output to RD(a) input to go to a level of -2.5V and the supply current on the DCE SP507 to rise to >100mA. When the DTE SP507 is powered on the supply current will draw as much as 600mA and the device will catastrophically fail.

The SCR structure that is connected to an n-channel source/drain (RD(a)), a floating P-well (Vss), an n-epi layer (Vdd) and the P-substrate (ground). Part of the SCR is connected to Vdd which in the DTE SP507 is floating since it is un-powered. The gate of the SCR is connected to the P-well, which is also floating. Figure 2 is a representation of the parasitic's.

**FIGURE 2. PARASITIC SCR REPRESENTATION**



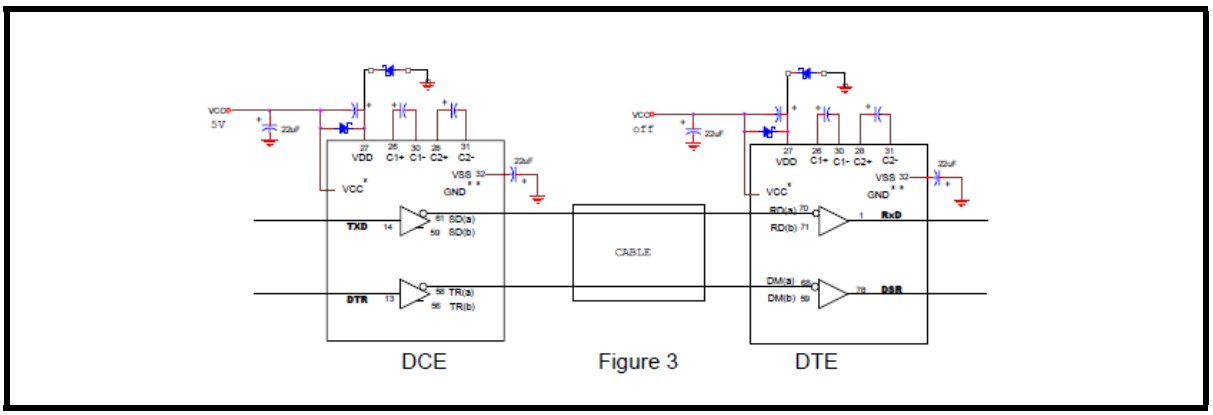

When the SCR is turned on the supply current of the DCE SP507 increases. With this SCR is triggered when the DTE SP507 is powered a latch condition occurs with the supply current increasing to >600mA.

## 3.0 LATCH PREVENTION

By biasing Vdd to ground during start-up the SCR is not allowed to turn on in most cases. This has been verified by grounding Vdd of the un-powered DTE SP507 and seeing if the supply current of the DCE increases and if the SD(a) to RD(a) connection goes to -2.5V

Grounding Vdd during start-up can be accomplished by adding an additional schottky diode between Vdd and ground. Figure 3 shows this arrangement.

**FIGURE 3. VDD SCHOTTKY DIODE ARRANGEMENT**




The anode of the Schottky is tied to ground and the cathode to Vdd

Prior to powering on the DTE SP507 the Vdd pin will be at ground preventing the triggering of the SCR. Once the SP507 has started Vdd will rise to a normal level and latch-up will not occur in most cases.

Upon examining this arrangement further it was determined that a latch-up can still occur when an entire DCE/ DTE setup is made on the bench with multiple drivers and receivers connected. The latch-up occurred when the power from the DCE SP507 turned on and then off again. The reason for this latch-up is the transitions of the multiple receiver outputs from one state to another triggers noise into more than one SCR structure and the

Vdd Schottky diode to ground is not strong enough to overcome this. Adding an additional Schottky diode from Vss to ground overcomes this by tying the gate of the SCR to ground.

The Schottky diode should be connected to both SP507's as the same phenomenon can occur any time an SP507 is powered off and voltages are present on the receiver inputs.

Figure 4 shows the configuration of the Schottky diodes that will prevent latch-up in the RS-232 mode

**FIGURE 4. VSS SCHOTTKY DIODE ARRANGEMENT**

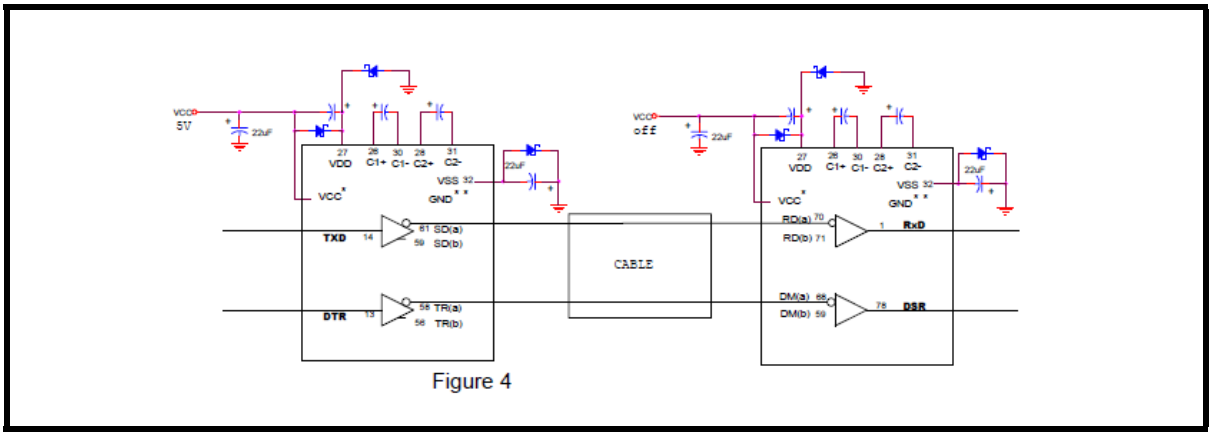


Figure 4

## 4.0 SUMMARY

The latch condition exists on the SP504, SP505, SP506 and SP507. The latch condition from the V.28/RS-232 lines does not affect SP508E or SP510E. The suggested Schottky diode for this latch prevention is 1N5819. The 1N5819 has a very low forward voltage rating at <100mA and has been used for this examination. Only V.28/RS-232 lines have the output level capable of triggering the SCR. All other modes of operation are not affected by this application note. It shall be noted that the triggering of the SCR does not occur when the SP504, SP505, SP506 or SP507 is powered on and then the V.28/RS-232 signals are applied to the receiver inputs. The SCR is also not triggered when the V.28 signals are removed from the receiver inputs before the SP504, SP505, SP506 or SP507 is powered off. To ensure the device does not enter a latch condition always have the SP504, SP505, SP506 or SP507 powered on before connecting V.28/R-232 signals to the receiver inputs or removing V.28/RS-232 signals from the receiver inputs.

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