APPLICATION NOTE ANI6

Connecting the SP504 Multiprotocol Transceiver to the 85C30 Universal Enhanced Serial Communications Controller (ESCC)

INTRODUCTION

The Sipex SP504 is a cost-effective, flexible and robust physical interface solution for standard Serial Interface Controllers. Like the other Sipex multiprotocol devices in the SP50x family, the SP504 contains multiple line drivers and line receivers that are electrically configurable for either single ended or differential physical interface. The device has built in configurations that implement several of the most popular standard serial port types on a single chip. The SP504 also incorporates a simplified termination scheme when used in V.35 mode. It is also configurable with all seven drivers and seven receivers configured for RS-485, making it ideal for industrial-network, fieldbus or SCSI applications.

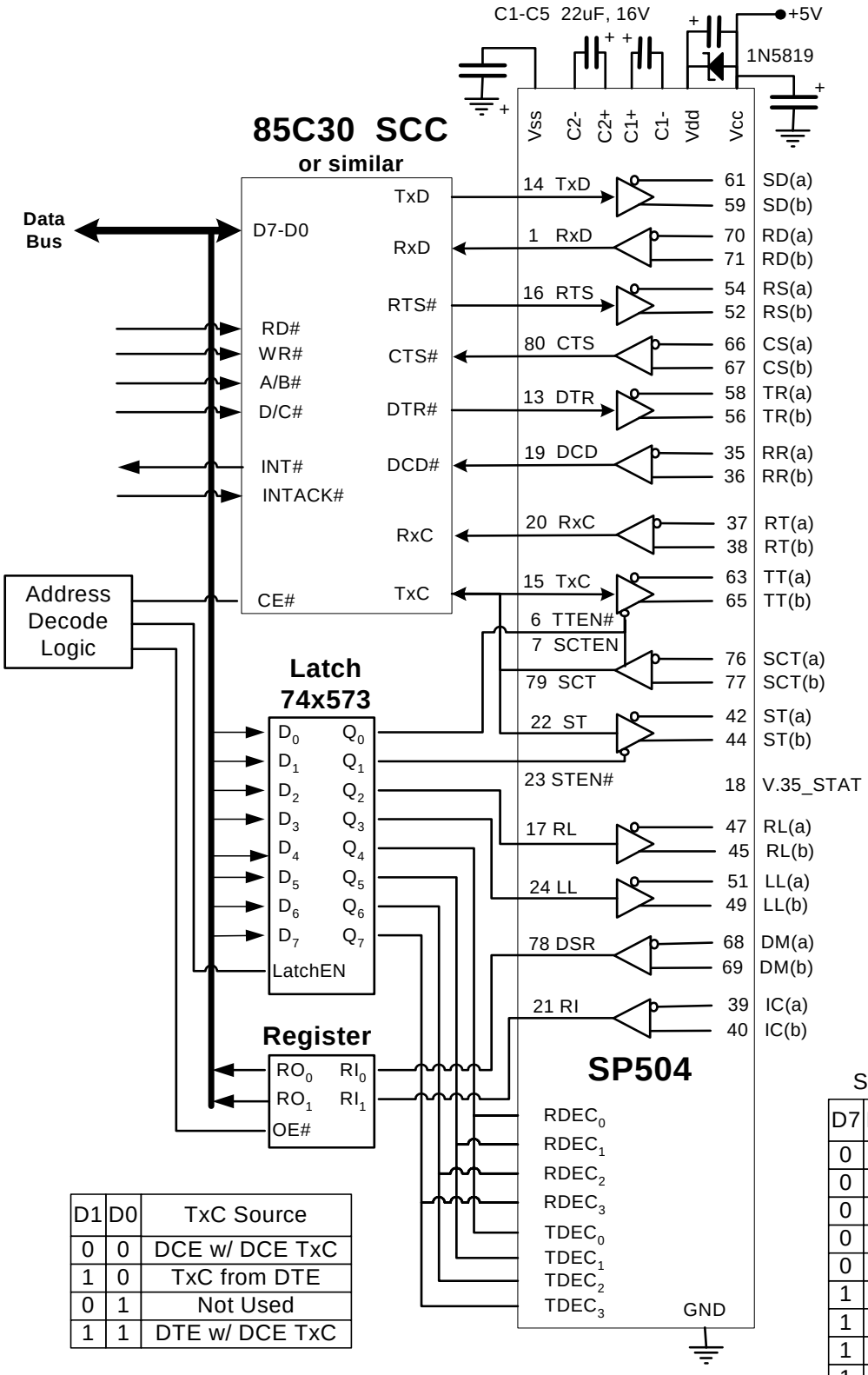
A Serial Communications Controller (SCC) converts parallel data from the microprocessor into a serial format and then packages that data into frames according to the appropriate protocol. Most SCCs are also capable of sending serial data over synchronous (clocked) links, unlike the simpler UART (Universal Asynchronous Receiver Transmitter). UARTs and SCCs may exist as standalone devices or integrated onto other logic. Typical controllers have CMOS or TTL inputs and outputs and rely on external analog line drivers and receivers to generate and receive signals for data cables. At the receiving end, the physical signals are recovered, decoded and converted back into parallel format.

The 85C30 and its derivatives are among the most widely implemented Serial Communications Controller (SCC) architectures. The original (NMOS) Am8530 was used as the serial port controller on Apple Macintosh™ and was widely used in routers, Frame Relay and communications servers. Later, the CMOS 85C30 improved on the original design. There are now a number of 85C30 equivalent devices in the market as discrete chips, silicon IP or programmable macros. Many communications ICs include SCCs that remain compatible with the basic 85C30 design.

An attractive feature of the 85C30 is its flexibility. It is configurable to support asynchronous or synchronous HDLC, SDLC or BISYNC frames and performs NRZI encode/decode, bit stuffing, baud rate generation, parity, CRC and error detection. The SP504 is an equally flexible device that includes seven line-drivers and seven line-receivers that are electrically re-configurable in-system. When the 85C30 and SP504 are paired, they enable mid to high speed data transfer between many types of telecommunications, data-network, computing and control-systems.

The schematic diagram below shows an example connection between an 85C30 or similar SCC and a Sipex SP504 multiprotocol transceiver. The SCC supports two data signals (TxD, RxD), four control signals and two clock signals (RxC, TxC). TxC can be either input or output. All other signals are one directional. By convention all signals from the SCC are labeled for DTE operation but the 85C30 can also function as a DCE controller. In the example schematic, several control and diagnostic signals, not supported by the SCC, are driven to or from the system data bus using a discrete latch and register. These control and diagnostic circuits are not speed critical and will typically hold level value throughout a communications session.

Example Multiprotocol Circuit with SP504 and 85C30 SCC



Suggested Signals			
DTE		DCE	
EIA	ITU	EIA	ITU
BA	103	BB	104
BB	104	BA	103
CA	105	CB	106
CB	106	CA	105
CD	108	CC	107
CF	109	RL	140
DD	115	DA	113
DA	113	DD	115
DB	114	-	-
-	-	DB	114
RL	140	CF	109
LL	141	TM	142
CC	107	CD	108
TM	142	LL	141

D1	D0	TxC Source
0	0	DCE w/ DCE TxC
1	0	TxC from DTE
0	1	Not Used
1	1	DTE w/ DCE TxC

SP504 Decoder Inputs

D7	D6	D5	D4	Port Config
0	0	0	0	Tri-State
0	0	1	0	RS-232
0	1	0	0	RS-422
0	1	0	1	RS-485
0	1	1	0	V.36
1	1	0	0	RS-449
1	1	0	1	EIA-530
1	1	1	0	V.35
1	1	1	1	EIA-530-A

DTE or DCE Operation

The 85C30 and SP504 can operate as either a DTE or DCE device. By convention, the pin labels on SCC and Sipex devices reflect the signal assignments used in a DTE configuration. To operate as a DCE, these pin assignments are "crossed over" to corresponding signals appropriate to the DCE. Suggested signal connections are shown next to the SP504 driver output and receiver inputs. SP504 pins are labeled with pin number and pin mnemonic. Suggested signals are identified for either DTE or DCE operation and are labeled with both TIA/EIA mnemonic and ITU-T (CCITT) signal names.

SP504 Transceiver Decode Pins

The SP504 is programmable into eight different port modes and a tri-state shutdown mode using its decoder inputs. There are four receiver-decoder inputs and four transmitter-decode inputs. For any of the pre-defined modes, the driver and receiver decode values are aligned so they can share input signals ($RDEC_0$ tied to $TDEC_0$, $RDEC_1$ to $TDEC_1$ etc.). Decoder inputs are not latched internally.

Clock Signals

Two drivers and two receivers on the SP504 are intended for driving or receiving timing signals (clocks). For a DTE implementation, the receive-data timing (RxC) is provided from the DCE. Transmitted-data timing may be provided either by the DTE or the DCE. Received-data timing and transmitted-data timing are implemented on independent pins, even if the signals are both sourced from the DCE. This allows the DTE to adapt to skew between sent and received data.

For a DCE implementation, the situation is a mirror image of the DTE case. The DCE may provide both timing signals or only one. The 85C30 has only one clock output per SCC channel, so when configured as a DCE, this signal is fed to both the RxC and TxC cable connectors.

In the example schematic, latched outputs D0 and D1 configure the SP504 for four possible timing scenarios. The RxC receiver on the SP504 is always enabled and is connected to the RxC input on the SCC. TxC is configured as either an input or output on the SCC and connects to TxC and ST drivers and the SCT receiver. D0 and D1 control whether the receiver or one or both drivers are active on the SP504. System designers should ensure that the timing source configuration of the SP504 is set consistent to what is configured in the SCC.

D1, D0	Transmit-data timing source
0,0	DCE mode, provide timing on 115 & 114, receive on 113
1,0	Either DTE or DCE mode, provide outbound-timing
0,1	Not used
1,1	DTE mode, receive all timing from DCE

Octal Latch

In the example circuit a single octal latch (74LS573 or similar) is sufficient to latch signals for the transceiver decode inputs, the timing-source enable pins and two signal outputs (RL and LL). The latch enable pin is enabled when activated by the address decode logic, allowing the 74LS573 to latch a configuration word off a shared data bus.

Polled Signals

Output signals that are not supported by the SCC are driven from the SP504 into a register. The register can then be polled periodically by the system CPU. In the example schematic, the two signals polled while connected as a DTE are DCE Ready (also called Data Set Ready or DSR) and Test Mode Indication. When connected as a DCE, the two signals are Data Terminal Ready (DTR) and Local Loopback. Typically, these signals are not speed critical and hold level values throughout a communications session.

Cable-Connectors

An example cable-connector signal routing for EIA-530 is shown below. The example shows signal routing from the SP504 to both male (DTE) and female (DCE) DB-25 (ISO/IEC2110) connectors. The DB-25 connector is specified for several popular serial standards such as RS-232, V.24, X.21bis, EIA-530 and EIA-530-A. Since the DB-25 is inexpensive and widely available, some standards such as V.35, V.36 are also sometimes implemented using the DB-25, even though those standards were defined for use over other connectors.

Although many different standards use the DB-25 as a connector they are not interoperable at the physical layer. For example, RS-232 uses single ended drivers and receivers for all signals. Receivers must tolerate voltages ranging between +15V to -15V. Other standards use a mix of differential and single-ended signals. Higher priority signals are carried on a differential pair, lower priority signals on single-wire, unbalanced lines that rely on a common return.

Supporting these electrical differences over multiple protocols is normally a difficult task. Designers might require multiple sets of physical transceivers and some way to select between them. Sipex multiprotocol transceivers, like SP504, solve this problem by being configurable to support many different physical protocols all in a single chip solution. This gives the system designer a cost effective way to add flexibility and improved functionality to their system.

V.35 Termination

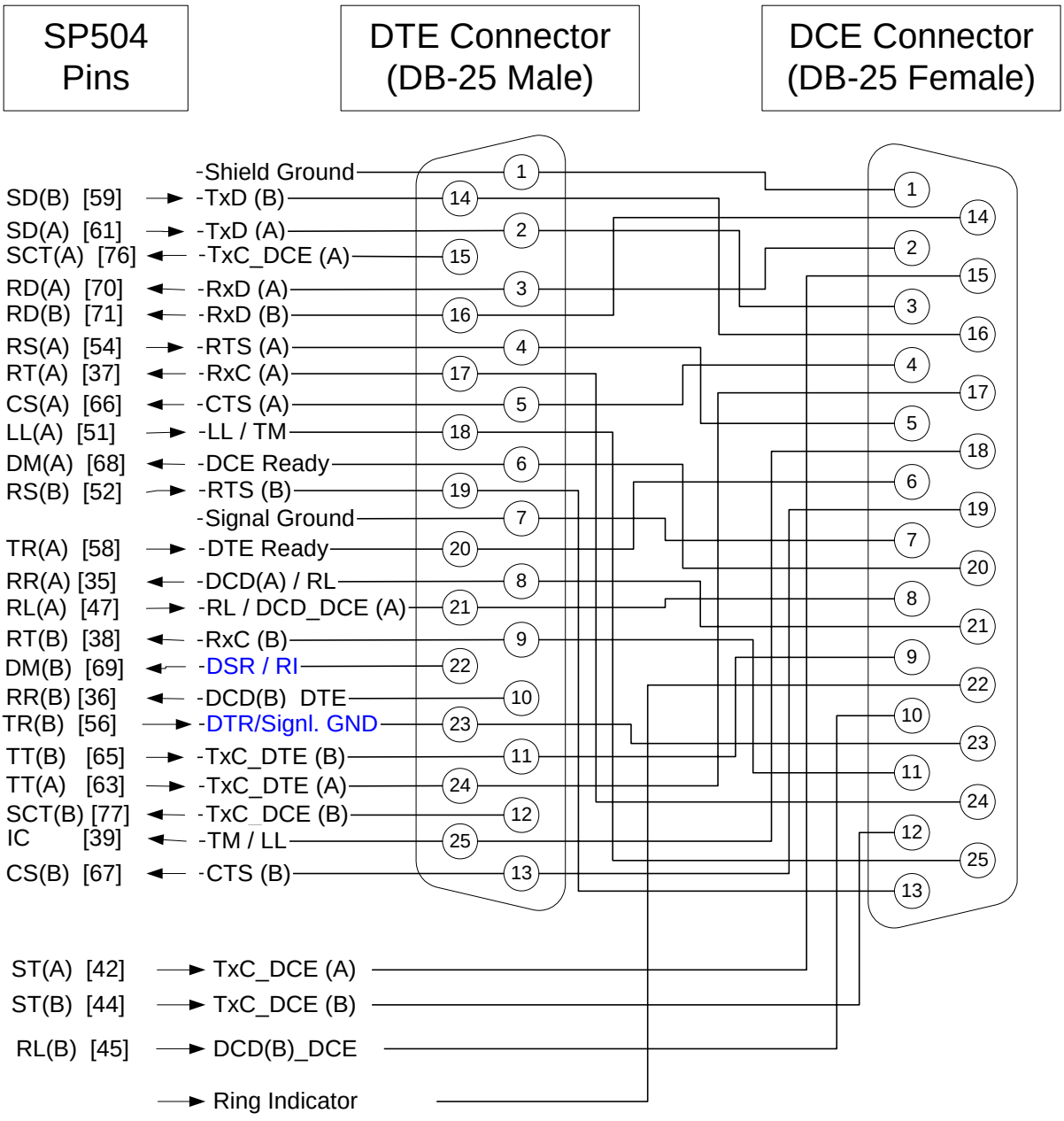
The SP504 implements a simplified termination for V.35 mode. Comité Consultatif International Téléphonique et Télégraphique (CCITT) recommendation V.35, appendix II, defines use of differential drivers and receivers with tightly controlled source and load

impedance to carry clock and data signals. Normally a V.35 compliant port would require adding external resistor networks to meet these impedance requirements. Several options for implementation of the V.35 termination are explained in Sipex SP504 Applications note, http://www.sipex.com/products/pdf/SP504_an.pdf.

It should also be noted that the International Telecommunication Union – Telecommunication Sector (ITU-T), the parent organization for CCITT, has officially rescinded the V.35 standard and replaced it with V.36. However, many V.35 connections still exist on installed equipment worldwide. V.36 may be implemented using the same 34-pin connector as V.35 but uses standard V.11 type drivers and receivers without a special impedance network. Also, it is quite common for people to refer to any use of the M34 connector as a "V.35" port even though electrically it may really be V.36. SP504 mode 0110 is appropriate for V.36 implementation using standard connectors.

Example Connection for TIA/EIA-530

Also valid for RS-232, V.35 and V.36



Ring Indication (RI) or Calling Indicator (circuit 125)

The seven drivers and seven receivers in the SP504 support the complete set of signals used in EIA-530. The revised EIA-530 (called EIA-530-A) adds a provision for a Ring Indication signal (RI) and reserves pin 22 on the cable connector for RI. The SP504 includes both an RS-530 mode (1101) and an RS-530-A mode (1111) but would require

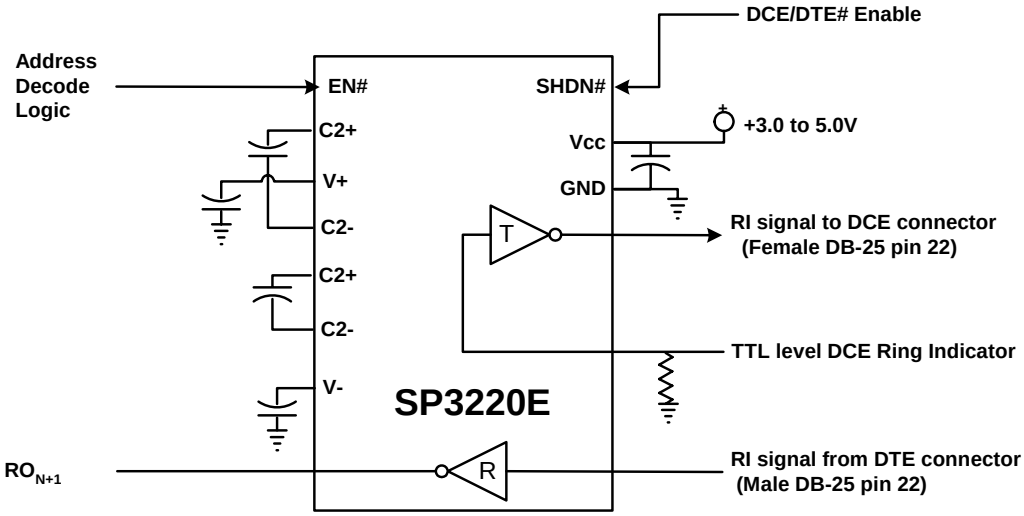
eight receivers (DTE) or eight drivers (DCE) to support RI function. Some other protocols such as V.36, RS-232 and RS-449 also allow for RI.

Ring Indicate is typically used in circuit-switched (dial-up) connections to flag when an inbound call is ringing. Permanently connected circuits or connectionless circuits will not normally use the RI signal.

Ring Indicate is always a single ended signal, either V.28 or V.10. A single transceiver such as SP3220E is ideal for adding RI capability. The SP3220E transmitter outputs are regulated to +5.5V and -5.5V regardless of the supply voltage (V_{CC}) over a +3.0V to +5.5V range. This allows the SP3220E to safely drive signals that are compatible with either V.10 or V.28. The SP3220E's receiver threshold of 1.5V should also be sufficient to detect a low data-rate RI signal.

For DTE operation, only the receiver is required. The SP3220E features a low power shutdown mode that disables much of its onboard circuitry. The receiver is always active independent of this shutdown mode. Receiver output is controlled using the receiver output enable (EN#) pin. This allows the SP3220E to coexist on a shared bus without extra buffers or registers.

For DCE mode, the SHDN# pin should be driven high (active.) RI is normally held at logic 0 (off) except when a calling signal is being received from the modem.



Some protocols such as RS-232 and RS-449 allow for secondary data channels and also include a number of other diagnostic signals. Use of these additional channels and signals is rare. But if they are required they must be implemented using additional external transceivers.