RS-485 Isolated Interface

INTRODUCTION

The SP1481E/SP1485E and SP1490E/1491E series transceivers with SP6652 high efficiency high frequency current mode PWM buck regulator together allow creating an isolated RS-485 interface with up to 2kVrms isolation and can support up to 15Mbps data rate communication.

FEATURES

- +5V Single Supply Operation
- ESD Protection for Bus-pins (±15kV Air-Gap Discharge and Human Body Model and ±8kV Contact Discharge)
- True Failsafe Receiver

APPLICATION

- Low Power RS485/RS-422 Systems
- DTE-DCE Interface
- Local Area Networks
- Industrial Process Control
- Building Automation

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage (Vcc) …... + 6.0V
Input voltage at control input pins ($\overline{RE}$, DE) …. - 0.3V to + 6V
Driver input voltage (DI) ….- 0.3V to + 6V
Driver output voltage (A, B, Y, and Z) ……-7.5V to +12.5V
Receiver input voltage (A, B) … ……- 7.5V to +12.5V

All other parameters are limited by used components and should be checked at appropriate data sheets.

GENERAL DESCRIPTION

The Sipex's family of RS-485 transceivers contains full-duplex and half-duplex devices. All half-duplex devices allow enable and disable both driver and receiver independently. The bus-pin outputs of disabled modules are in high impedance state. The bus-pins of all powered down devices are in high impedance state too. The high impedance driver output is maintained over the entire common-mode voltage range from -7 to +12V.

The schematic diagrams in Figures 1 — 4 show the component connection for full-duplex and half-duplex isolated interface. Table 1 contains information about components value and manufacturers.

The full-duplex interface contains isolated power supply on the base of SP6652 PWM buck regulator and 10Base-T/Ethernet isolation transformer EP9531-6 from PCA or any other manufacturer with primary inductance 100±20uH (PE64503 from Pulse or T-10905 from Rhombus Industries in a DIP16 package or EP9531G-X from PCA or identical in SMD package). The primary voltage at the output of SP6652 is set to 2.5V that create a stable 5V output voltage in the second winding of transformer. Zener diode D2 is used to protect transceiver from over voltage in a sleep mode.

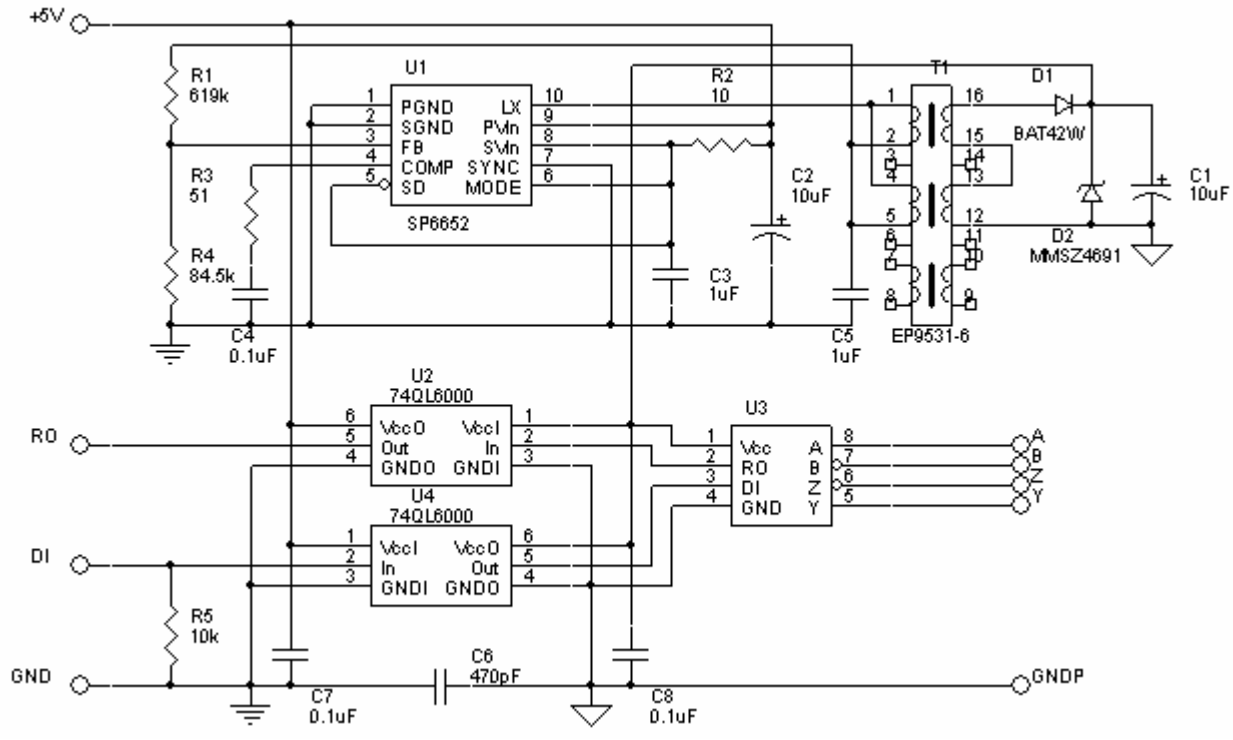

Figure 1. Full-duplex interface schematic diagram for 15Mbps data rate

Capacitor C8 is used to protect device from ESD discharge between primary and secondary grounds and should be rated at 2kV or higher voltage.

Optocouplers 74OL6000 with buffered input/output are TTL compatible and can support up to 15Mbps data rate communication.

The type of RS-485 driver U3 depends from desirable data rate and can been selected from the following list:

U3 Type*	Data rate, Mbps	Comments
SP1490E/SP1491E	15	Limited by 74OL6000
SP490E/SP491E	10	
SP490/SP491	5	

*) SP491, SP1491, and SP1491E have additional driver/receiver tri-state enable lines and should be connected according schematic diagram in Figure 2.

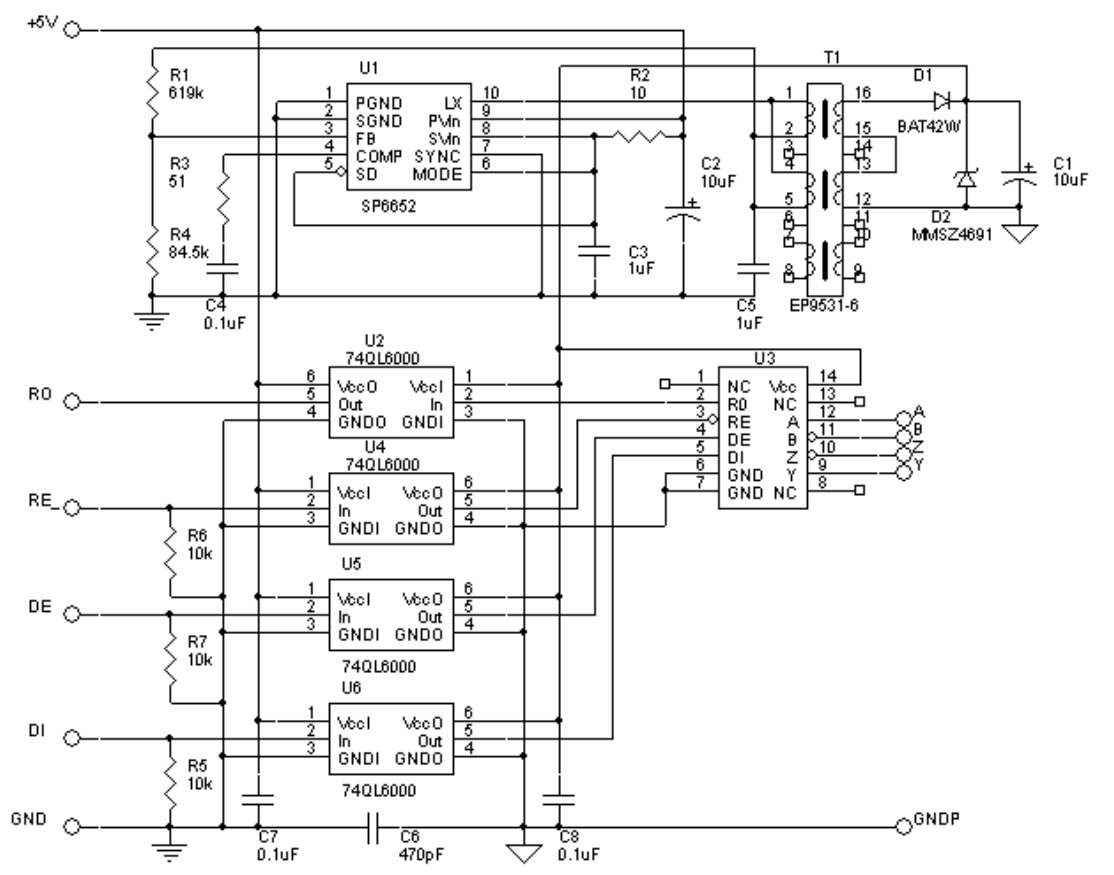

Figure 2. Full-duplex interface schematic diagram for 15Mbps data rate with additional driver/receiver tri-state enable lines

The schematic of the interface in Figure 2 is identical to the previous example except connection of the driver and two additional optocouplers that allow transmit driver/receiver enable signals into secondary stage of the driver.

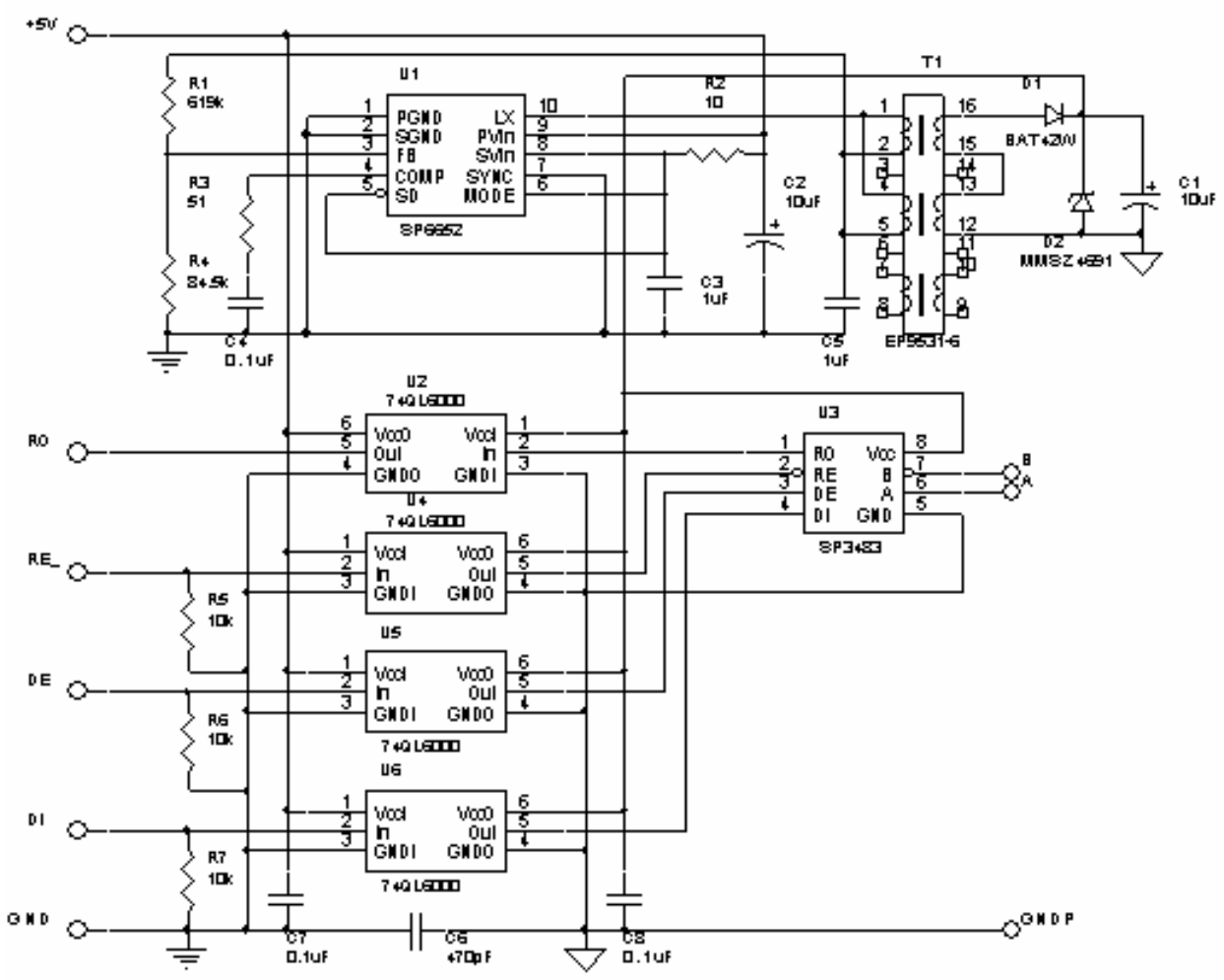

Figure 3. Half-duplex interface schematic diagram

The half-duplex interface uses the same components as a full-duplex interface except for driver. The type of RS-485 driver U3 depends from desired data rate and can been selected from the following list.

U3 Type	Data rate, Mbps	Comments
SP1481E/SP1485E	15	Limited by 74OL6000
SP481E/SP485E	10	
SP481/SP485	5	
SP481R/485R	5	
SP483	0.25	

At low speed data rate (up to 5Mbps) instead of 74OL6000 optocouplers may be used SFH6701, SFH6711, SFH6720T, and SFH6721T optocouplers from Vishay Semiconductors. The schematic diagram of a full-duplex interface with these optocouplers is shown in Figure 4.

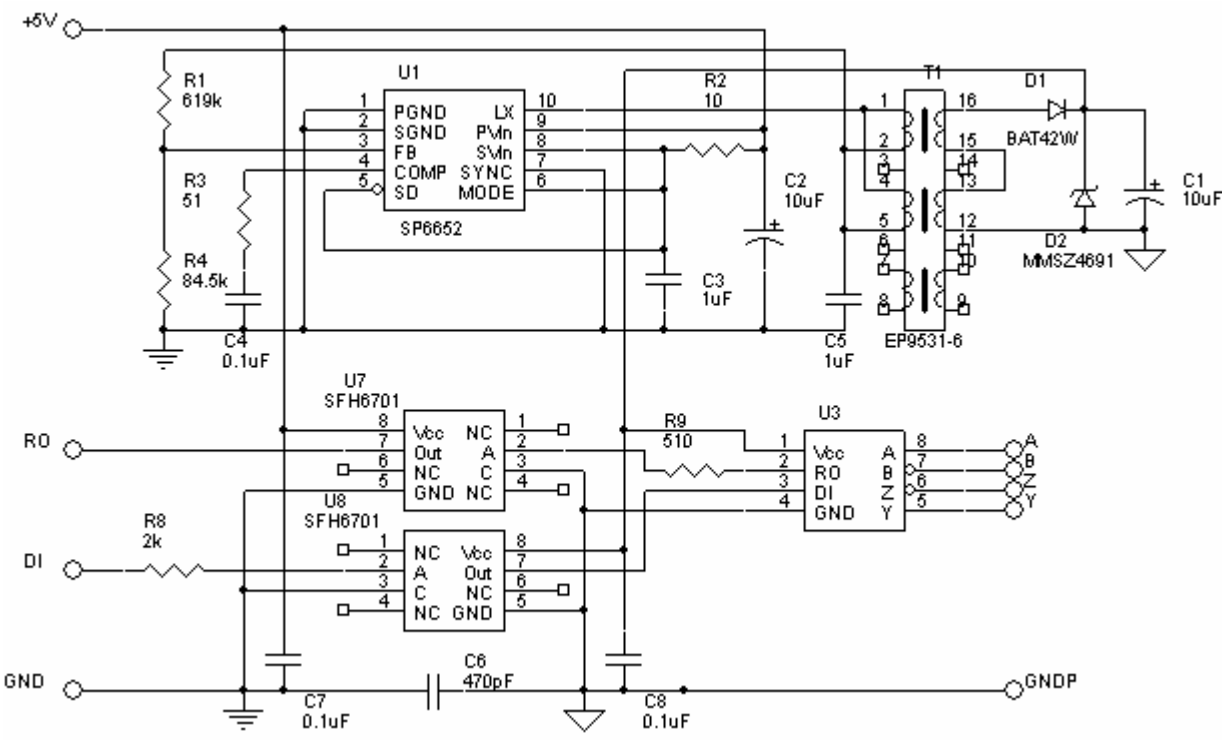

Figure 4. Full-duplex interface schematic diagram for 5MBbps data rate

Item	Quantity	Reference	Value	Manufacturer	Comments
1	2	C2, C1	10uF		Tantalum
2	2	C5, C3	1uF		Ceramic
3	3	C4, C7, C8	0.1uF		Ceramic
4	1	C6	470pF x 2kV		Ceramic
5	1	D1	BAT42W	Diodes Inc.	
6	1	D2	MMSZ4691	Vishay Semiconductor	
7	1	R1	619k ±1%		0.063W
8	1	R2	10 ohm ±10%		0.125W
9	1	R3	51 ohm ±10%		0.063W
10	1	R4	84.5k ohm ±1%		0.063W

11	3	R5, R6, R7	10k ohm ±10%		0.063W
12	1	R8	2k ±10%		0.063W
13	1	R9	510 ohm ±10%		0.063W
14	1	T1	EP9531-6	PCA Electronics Inc.	
15	1	U1	SP6652	Sipex Corp.	
16	4	U2, U4, U5, U6	74OL6000	Fairchild Semiconductor	
17	2	U7, U8	SFH6701	Vishay Semiconductor	

Table 1. Components Specification

BOARD LAYOUT AND GROUNDING

To obtain the best performance of transceiver, a printed circuit board with ground planes is required. Primary and secondary ground planes should be separated with a wide enough space to prevent high voltage breakdown.
Ground pins of IC and optocouplers should be connected to the appropriate ground plane. High quality, low series resistance ceramic 0.1uF bypass capacitors C4, C7, and C8 should be used at the Vcc pins. These capacitors must be located as close to the pins as possible. The traces connecting the pins to the ground plane, Vcc, and bypass capacitors must be kept short and should be made as wide as possible.

The suggested layout of printed circuit board for a full-duplex interface is shown in Figure 5.

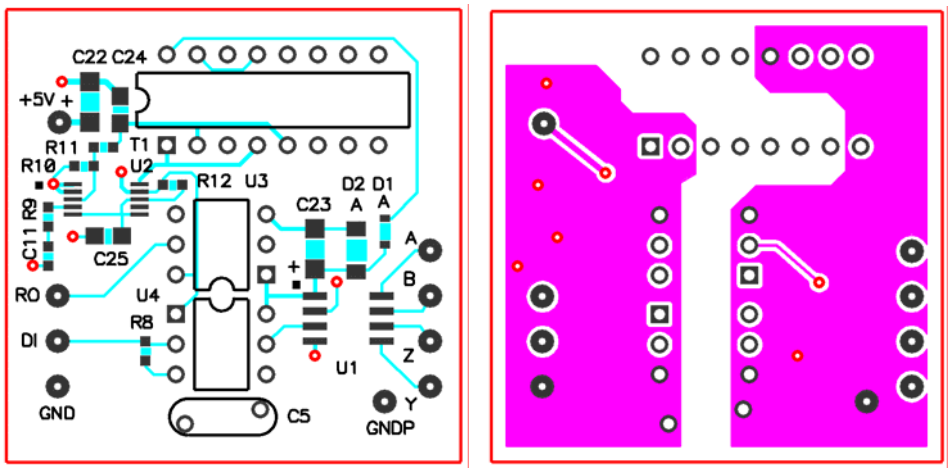

Figure 5. Top and bottom layers of full-duplex interface evaluation board

For further assistance:

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