Design Guide for Multi-Protocol Serial Ports ANI16

Many of today's routers and access equipment are being designed with Wide Area Network (WAN) serial ports which are able to support various physical interface protocols or standards. The WAN serial port may contain EIA-530, V.35 or V.36 electrically compliant signals.

As compared with older configurations, a "multi-protocol" serial port eliminates the need for stocking different hardware as well as duplicate manufacturing of the same equipment with different serial port connectors.

In order to allow for this flexibility, one set of transceivers must provide the EIA-530 signals and another set must provide the V.35 signals. This typically requires six or more transceiver ICs, depending on the number of physical protocols implemented as well as the signaling requirements used. There are a variety of transceiver IC manufacturers that offer EIA-232, EIA-422, EIA-423 or V.35 compliant transceivers. All of these transceivers are configured to

the serial connector and programmed to only offer the physical protocol selected. The connector can vary from a DB-25 for EIA-232 and EIA-530 to a ISO-2593 for V.35 or a custom high density connector for all available physical protocols. Programming the desired protocol can either be done through hardware or software.

There are many configurations in which one can implement multiple physical protocols on one serial port. In terms of serial transceivers, there are discrete drivers and receivers which are dedicated for each physical layer protocol. A combination of them are needed to support the necessary protocols. The easiest method is to group various transceivers into a single integrated circuit. **Sipex** offers single IC transceivers for the multi-protocol applications which require multiple physical standards on the WAN port. The **SP500** family allows four or more physical interface protocols to be programed on a single IC.
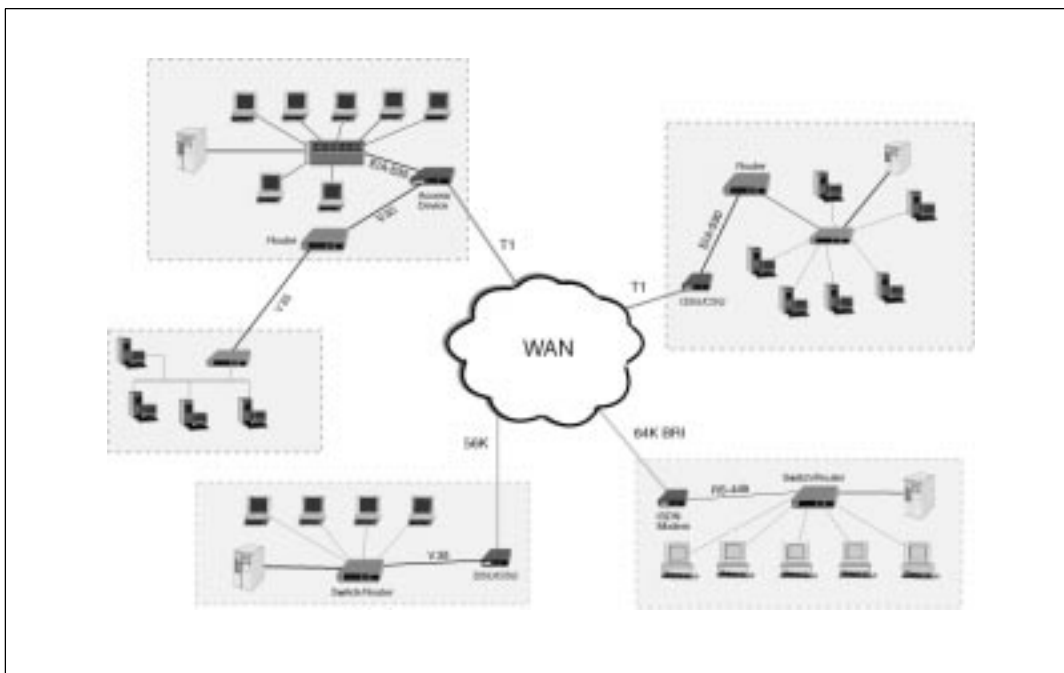

Figure 1. Typical WAN Environment

Multi-Protocol Serial Port Approaches

I. Using a "daughter board":

One method of designing and manufacturing a WAN serial port is to create separate "daughter" cards for each physical protocol offering. For example, a system needing a EIA-449 serial port will contain a daughter board with V.11 and V.10 compliant transceivers. The daughter board may also contain the DB-37 connector or may interface with a dedicated EIA-449 back-panel with the connector. The daughter board and/or the back-panel is then assembled to the chassis.

A system offering EIA-232, EIA-449 and V.35 would require three separate daughter boards and/or three different back-panels for the system. The appropriate back-panel for the V.35 serial protocol would have the ISO-2593 connector for V.35 physical connections. The actual system cost of this approach is relatively inexpensive. If one requires a V.35 configuration for the equipment, any costs associated with V.11 or V.10 transceivers are eliminated in the actual equipment. The serial transceiver count on the daughter board would consist of the V.35 transceiver ICs for clock and data signals, their associated V.35 termination resistor networks, and the V.28 transceivers for handshaking signals. The cons of this approach are the tedious material management task of keeping inventory for each type of transceiver ICs, daughter PCBs, and the separate back-panels with the appropriate connector.

II. Common Connector w/ "daughter" cables:

Another method is to have a single motherboard with a common connector supporting the different transceivers for the multiple serial protocols needed. One tedious design issue is dealing with the different connectors required by each serial protocol. The EIA-232 and EIA-530 protocols specify a DB-25 type connector, while a V.35 protocol specifies the ISO-2593 connector. For this technique, the actual physical link is connected via a translator or "daughter" cable. The cable routes the relevant signals from the common connector to the appropriate connector for the proper physical link to the other equipment. There are two basic configurations using this method.

a) Using a high density connector

The first configuration uses a high density connector to support all the signals required. This allows all of the transceiver I/O lines to have separate connections to a pin. Each group of pins would support signals for each serial protocol. For example, pins 1 through 15 can support V.11 signals (TxD, RxD, RTS, CTS, DTR, DSR, etc.) for EIA-449, EIA-530, V.36, X.21, etc. Pins 16 through 30 can support the same
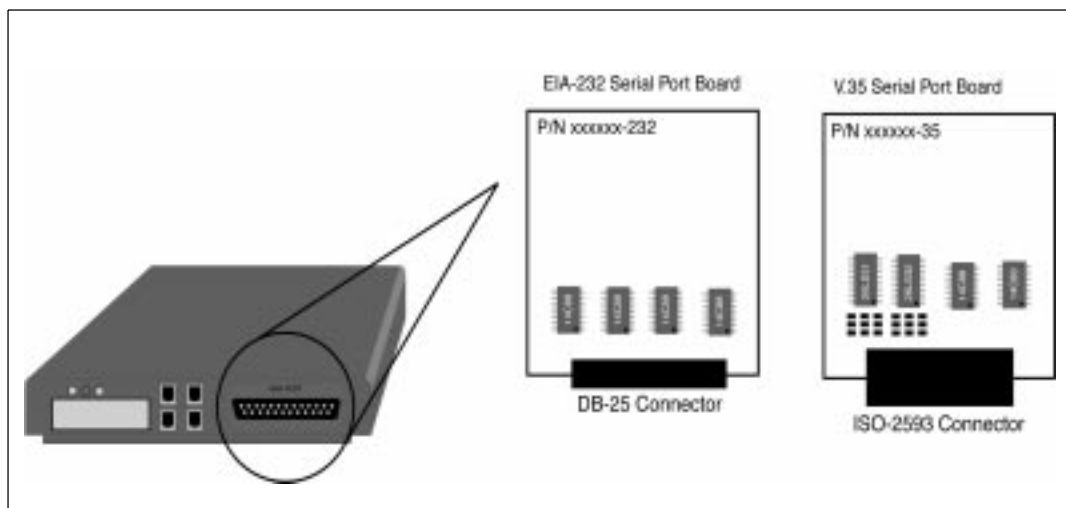

Figure 2. Daughter Board Approach for Multi-Protocol Serial Ports.

signals for V.35, and so on. For a system requiring EIA-232 (V.28), V.35, EIA-449, EIA-530 and X.21; CTS for example, can be allocated to pins 1 and 2 for the CS(a) and CS(b) signals. These two pins would have V.11 electrical characteristics and are used when EIA-449, EIA-530, and X.21 interfaces are selected. The CTS signal for EIA-232 would be assigned to another pin. This pin would be used for EIA-232 and V.35 interfaces. Other signals such as TxD, RxD, etc. would also have similar allocations. The ITU-T (formerly CCITT) V.24 Standard lists the definitions of interchange circuits between the data terminal equipment (DTE) to the data communications equipment (DCE).

The transceiver configuration is relatively straightforward. The V.11 transceivers used for EIA-449, EIA-530, V.36, and X.21 can connect directly to the assigned V.11 pins on the connector. The V.28, V.10, and V.35 transceivers will also go to their respective pin assignments. This configuration simplifies bus contention issues since the driver output and receiver input pins of each transceiver are exclusive of each other.

b) Using a D-sub or low-density connector
The other technique uses a small low density connector such as a DB-25 or µDB-26. Since synchronous serial ports support most of the

signals specified in ITU-T V.24, a connector pin count of twenty five is adequate for most of the serial interface protocols. However, supporting the EIA-232, EIA-449, EIA-530, V.35, and V.36 protocols will require more connector pins for the V.24 signals. How are the Transmit Data signals, SD(a) and SD(b), going to be supported for V.28 and V.11?

The transceiver configuration must address the pin shortage for the smaller connector. The most sensible way is allocating a common pin for each signal regardless of physical protocol. The TxD signal for EIA-232, EIA-449, EIA-530, V.35, and V.36 would go to the same connector pin(s). The SD(a) signal connects to pin 2 and the SD(b) signal connects to pin 14. These pins represent the Transmit Data signal for all these protocols. Specifically, SD(a) would be valid as the V.28 driver output (for a DTE) and also the inverting V.11 driver output. SD(b) is only valid for V.11 because V.28 signals are single-ended. This is similar for the other V.24 recommended signals as well.

To perform this, the transceiver I/Os must be common with each other. For example, an EIA-232 driver IC will be dedicated for Transmit Data and connected to pin 2 of the DB-25. In addition, a V.11 differential (RS-422) driver, dedicated for EIA-530, EIA-449, and V.36; will
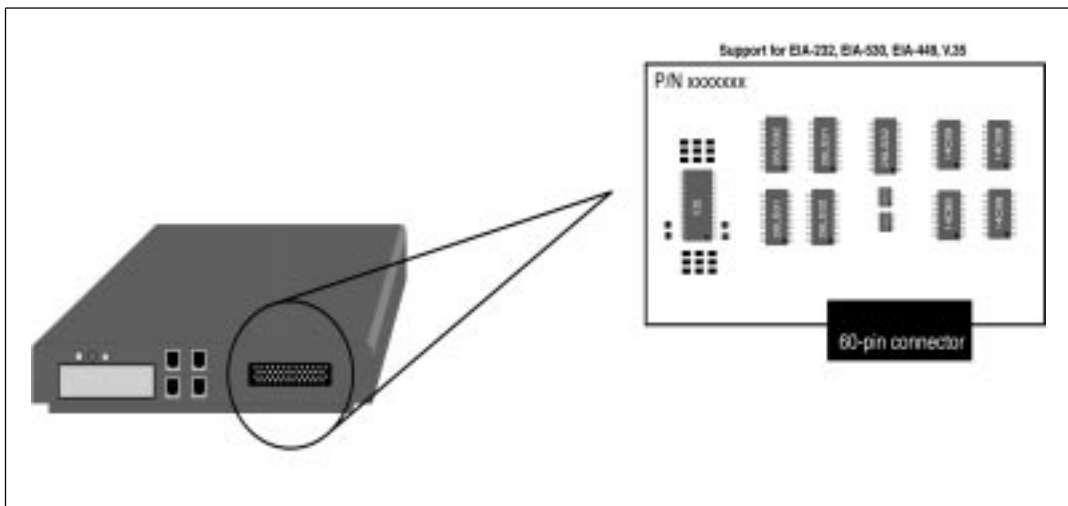

Figure 3. Separate I/O Lines Through a High-Density Connector Approach for Multi-Protocol Serial Ports.

connect to pins 2 and 14. Also, to support V.35, a V.35 differential driver must connect to the same two pins. The drivers in this configuration must have tri-state capability in order to disable the unused outputs. If EIA-530 is the protocol used, the V.35 and EIA-232 drivers are disabled to avoid any bus contention. The same applies for the other protocols.

Be aware that using this method requires that the transceiver I/Os will have low tri-state leakage current when disabled, specifically over the V.28 operating voltage range of ±15V. It is now rare for RS-232 drivers to produce ±15V output rails given that there are either +5V-only charge pumped RS-232 transceivers or ±12V supplied RS-232 transceivers. The worse case operating output rails from the two transceivers are approximately ±9.9V and ±11.8V, respectively. During tri-state of a V.11 driver, the tri-state driver output leakage must be low enough so that the V.28 signal to the same serial connector pin, with a potential output swing of ±12V, is not affected. If switches are used to isolate the driver outputs and receiver inputs, the same leakage considerations must be used as well.

This approach is commonly used for smaller printed circuit boards or smaller equipment applications where a higher density connector occupies more than the desired space given the design needs.

A block representation of the two approaches is shown on *Figures 3 and 4*. The high density connector pinout scheme is taken from a popular 60-pin serial connector configuration. The other method uses a DB-25 connector.

The daughter cables for each of the supporting serial interface protocols must be included with the equipment. The actual physical connection must adhere to the physical layer standard. For example, EIA-232 and EIA-530 uses a DB-25 connector as specified in each of their respective specifications. More details on the cabling scheme are discussed in the following section.

III. Cabling Approaches
A separate daughter cable is needed for either connector approach. As mentioned previously, the individual serial communication standards specify an actual physical connection. *Page 5* lists the signals used for synchronous serial communications and illustrates the connectors for some of the standards.

Using an example with a DB-25 connector as the backpanel serial port connector, the daughter cables are illustrated in *Figures 5* through *11* for EIA-530, RS-232, RS-449, and V.35. The cables can either be wired as a DTE or DCE.
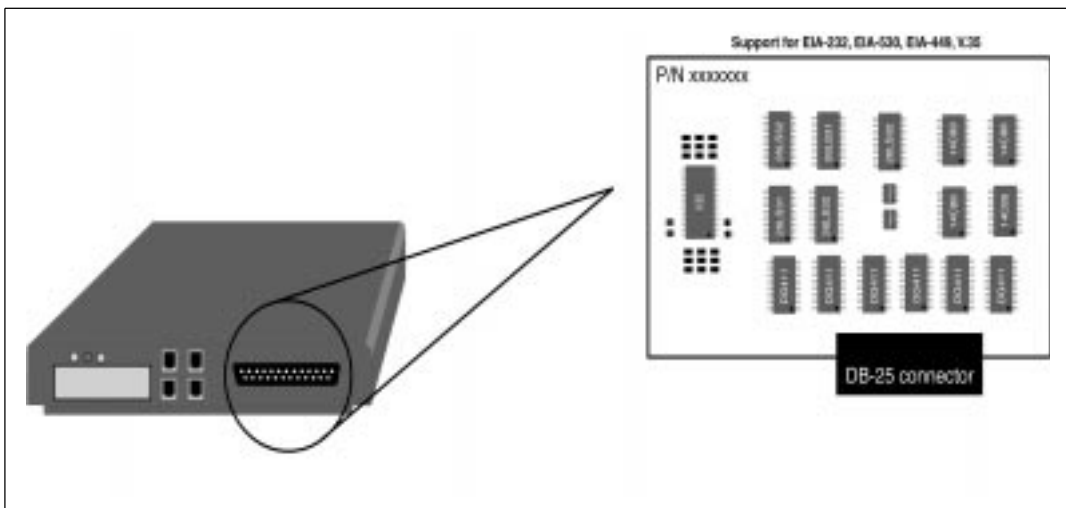

Figure 4. Common I/O Lines Through a Low-Density Connector Approach for Multi-Protocol Serial Ports.

| Signal Name	Source	EIA-232		EIA-530		EIA-449		V.35		X.21	
		Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin
Shield	—	—	1	—	1	—	1	—	A	—	1
Transmitted Data	DTE	BA	2	BA (A)	2	SD (A)	4	103	P	Circuit T(A)	2
				BA (B)	14	SD (B)	22	103	S	Circuit T(B)	9
Received Data	DCE	BB	3	BB (A)	3	RD (A)	6	104	R	Circuit R(A)	4
				BB (B)	16	RD (B)	24	104	T	Circuit R(B)	11
Request To Send	DTE	CA	4	CA (A)	4	RS (A)	7	105	C	Circuit C(A)	3
				CA (B)	19	RS (B)	25			Circuit C(B)	10
Clear To Send	DCE	CB	5	CB (A)	5	CS (A)	9	106	D	Circuit I(A)	5
				CB (B)	13	CS (B)	27			Circuit I(B)	12
DCE Ready (DSR)	DCE	CC	6	CC (A)	6	DM (A)	11	107	E		
				CC (B)	22	DM (B)	29				
DTE Ready (DTR)	DTE	CD	20	CD (A)	20	TR (A)	12	108	H *		
				CD (B)	23	TR (B)	30				
Signal Ground	—	AB	7	AB	7	SG	19	102	B	Circuit G	8
Recv. Line Sig. Det. (DCD)	DCE	CF	8	CF (A)	8	RR (A)	13	109	F		
				CF (B)	10	RR (B)	31				
Trans. Sig. Elemt. Timing	DCE	DB	15	DB (A)	15	ST (A)	5	114	Y	Circuit B(A)**	7
				DB (B)	12	ST (B)	23	114	AA	Circuit B(B)**	14
Recv. Sig. Elemt. Timing	DCE	DD	17	DD (A)	17	RT (A)	8	115	V	Circuit S(A)	6
				DD (B)	9	RT (B)	26	115	X	Circuit S(B)	13
Local Loopback	DTE	LL	18	LL	18	LL	10	141	L *		
Remote Loopback	DTE	RL	21	RL	21	RL	14	140	N *		
Ring Indicator	DCE	CE	22	—	—	—	—	125	J *		
Trans. Sig. Elemt. Timing	DTE	DA	24	DA (A)	24	TT (A)	17	113	U *	Circuit X(A)**	7
				DA (B)	11	TT (B)	35	113	W *	Circuit X(B)**	14
Test Mode	DCE	TM	25	TM	25	TM	18	142	NN *		

* - Optional signals
** - Only one of the two X.21 signals, Circuit B or X, can
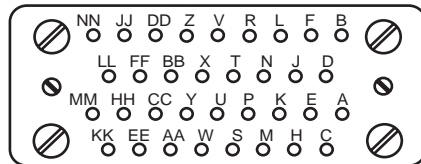   be implemented and active at one given time.
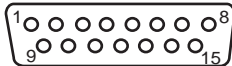
X.21 Connector (ISO 4903)
DTE Connector — DB-15 Pin Male
DCE Connector — DB-15 Pin Female
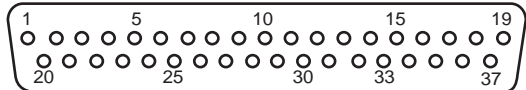
RS-449 Connector (ISO 4902)
DTE Connector Face — DB-37 Pin Male
DCE Connector Face – DB-37 Pin Female
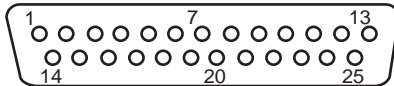
RS-232 & EIA-530 Connector (ISO 2110)
DTE Connector — DB-25 Pin Male
DCE Connector — DB-25 Pin Female

V.35/ISO 2593 Connector
DTE Connector Face — 34 Pin Male
DCE Connector Face — 34 Pin Female

Note: Connector drawings not drawn to scale.

Given which signals are drivers and which signals are receivers, the pin allocations can be swapped for a DCE configuration. First, the backpanel connector pinout must be defined. In these cases, the backpanel connector is a DB-25 in DTE mode. For example using TxD for RS-449 mode, the output on the DB-25 is pin 2 for SD(a) and pin 14 for SD(b). Remember, these pins (2 & 14) are always being driven by a transmitter (RS-232, V.11, or V.35). RxD for the DB-25 connector is mapped to pin 3 for RD(a) and pin 16 for RD(b). These pins will also be permanent such as they are connected to a receiver (RS-232, V.11, or V.35).

The other end will contain a DB-37 (ISO-4903) connector. For a DTE, the RS-449 pin assignment for SD(a) is pin 4 and SD(b) is pin 22. The TxD signal fanout is configured from pins 2 and 14 of the DB-25 to pins 4 and 22 of the DB-37, respectively. The direction of the signal will be constant (driving). The RxD is configured from the DB-25 on pins 3 and 16 to pins 6 and 24, respectively. The RD(a) and RD(b) signals are receiving.

Inversely, a DCE connection will require that pins 4 and 22 are configured as receive pins. Since the DB-25 connector is permanently configured as a DTE, the DCE cable will be mapped such that the TxD signal on pins 2 and 14 will now connect to pins 6 and 24 of the DB-37, respectively. The RxD signal on pins 3 and 16 will connect to pins 4 and 22 of the DB-37, respectively. Notice that the output from the DB-25 is still consistent regardless of DTE or DCE operation, but the end pinout on the daughter cable now defines the system as a DTE or DCE. The same method is repeated for the other signals and also the physical layers offered.

The approach with a high density connector on the backpanel is similar. The difference is how the internal transceivers are configured to the connector. *Figures 12* and *13* illustrate an example of a DB-60 high density connector with daughter cables to the ISO-2593 V.35 connector for both DTE and DCE. The driver signals in DTE configuration are receive signals in a DCE configuration, and vice versa.
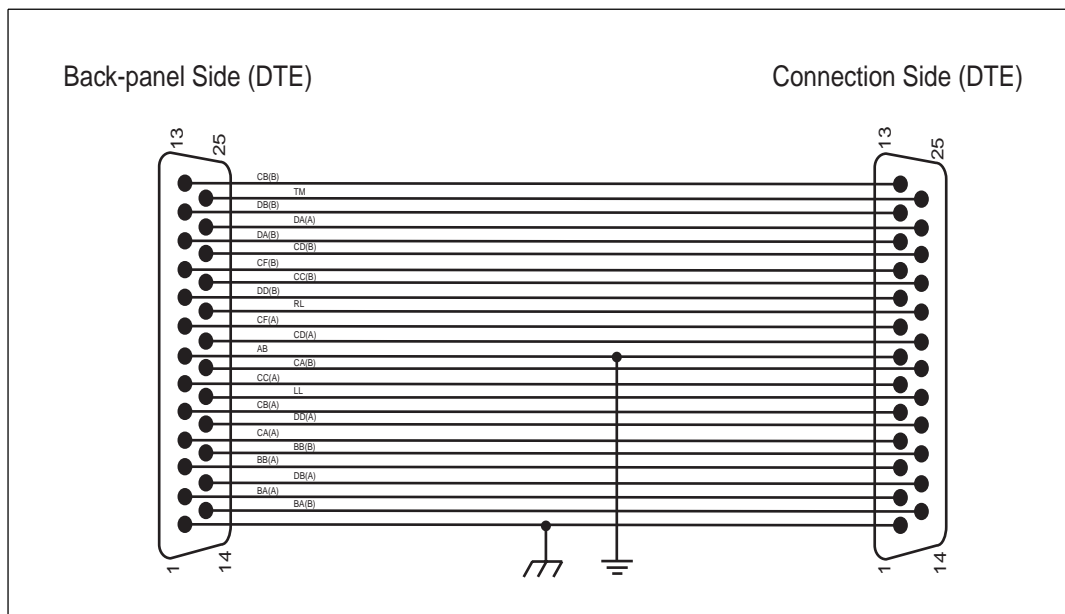

Figure 5. Daughter Cable - EIA-530 DTE Configuration (not necessary since back-panel connector conforms to EIA-530 pinout)
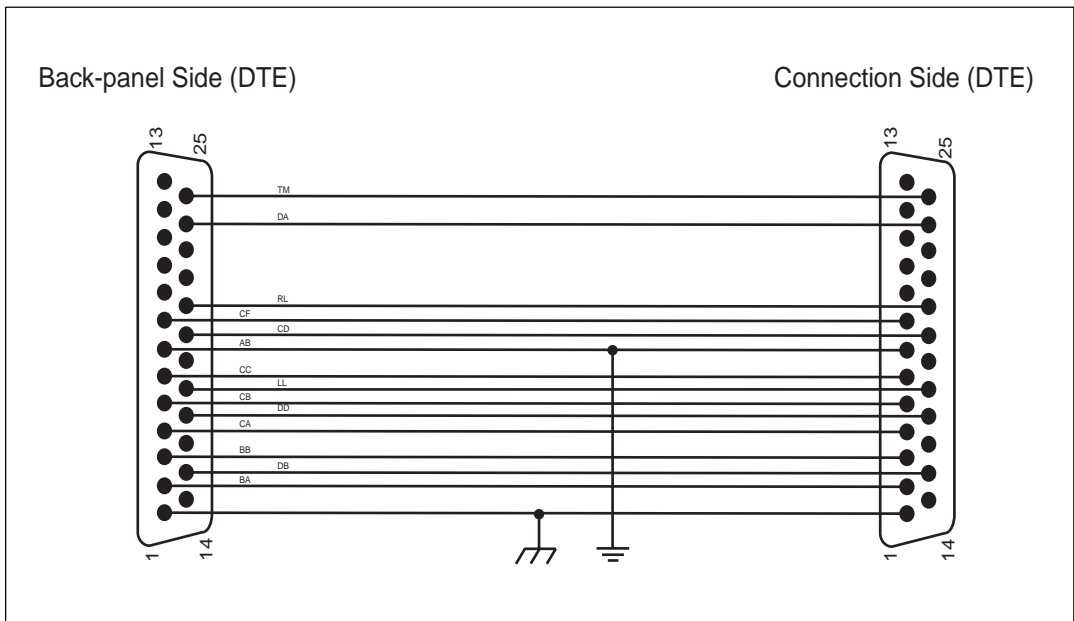
Back-panel Side (DTE)

Connection Side (DTE)

Figure 6. Daughter Cable - RS-232 DTE Configuration

Back-panel Side (DTE)

Connection Side (DCE)

Note: Signal DB (ITU#114) is bidirectional. The direction of the signal in DCE mode is ⇒, where ⇒ is driving the signal. The transceiver configuration must be implemented such that a driver is active for DCE and a receiver is active for DTE through pin 15 on the back-panel connector.
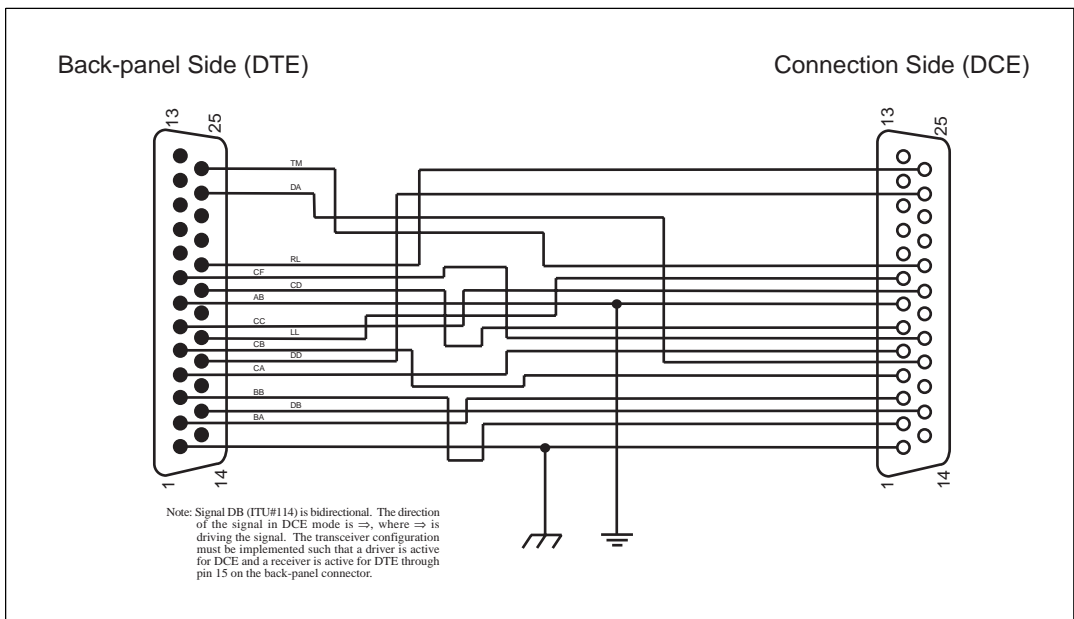
Figure 7. Daughter Cable - RS-232 DCE Configuration
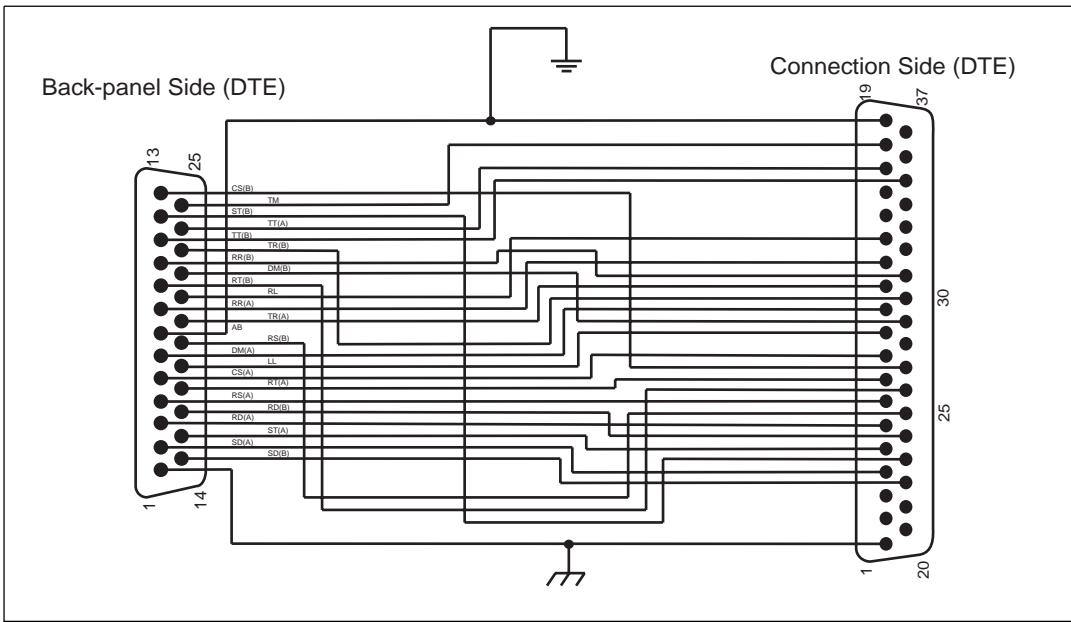
Figure 8. Daughter Cable - RS-449 DTE Configuration

Note: Signals RR, LL, and ST are bidirectional. The direction of the signals in DCE mode are: ⇒, ⇐, and ⇒, respectively. (⇒ is driving and ⇐ is receiving) The transceiver configuration must be implemented such that the appropriate drivers are active for DCE and vice versa, through the same pin on the back-panel connector.
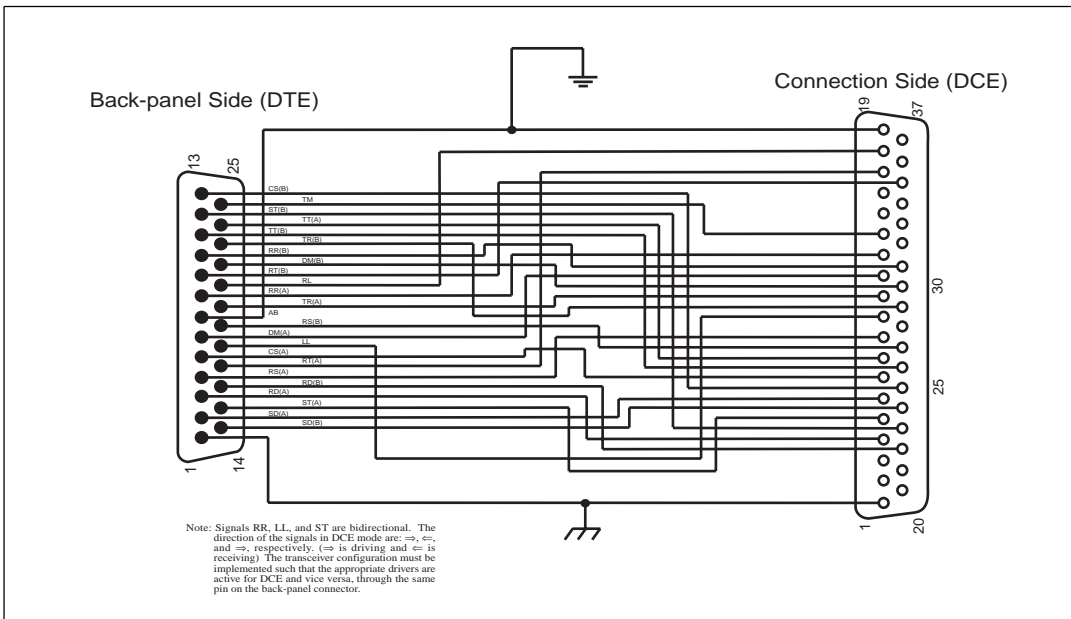
Figure 9. Daughter Cable - RS-449 DCE Configuration
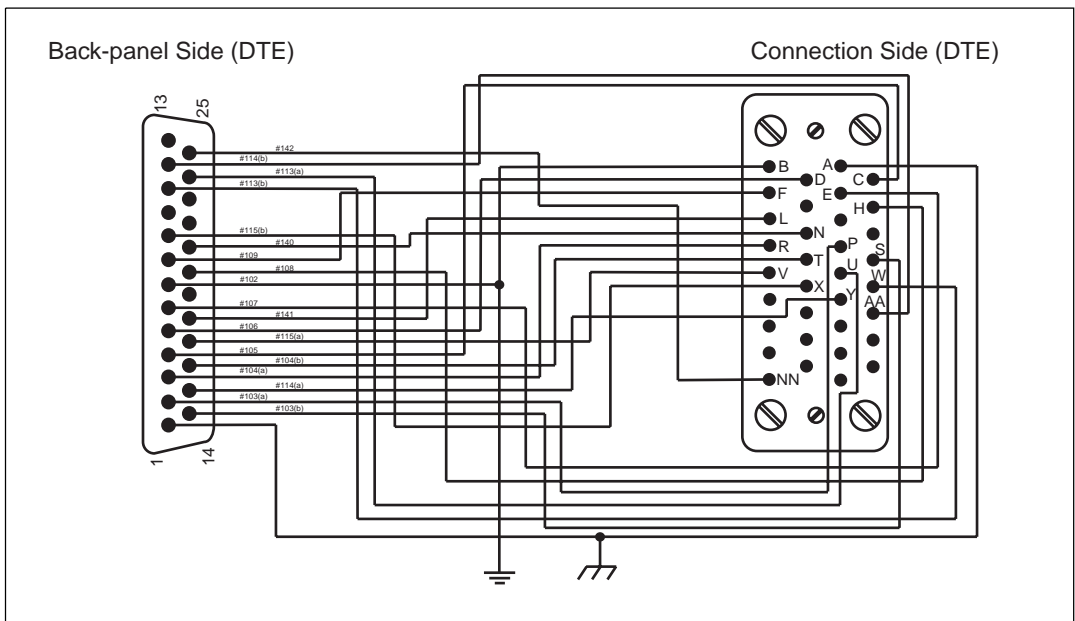
Figure 10. Daughter Cable - V.35 DTE Configuration

Note: Signal ITU#114 is bidirectional. The direction of the signal in DCE mode is ⇒, where ⇒ is driving the signal. The transceiver configuration must be implemented such that a driver is active for DCE and a receiver is active for DTE through pins 15 & 12 on the back-panel connector.
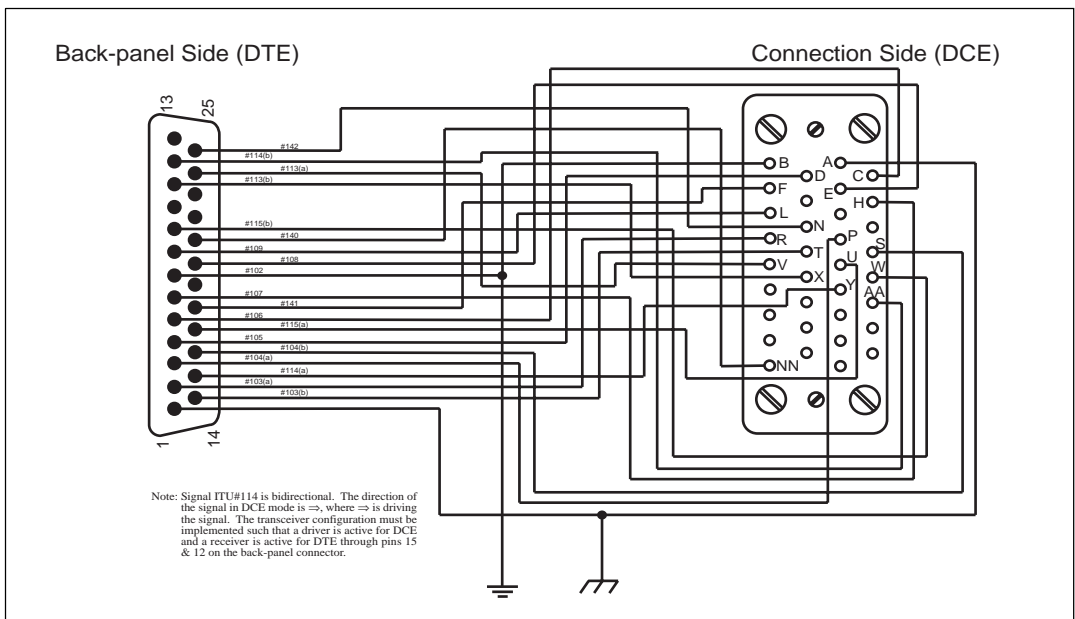
Figure 11. Daughter Cable - V.35 DCE Configuration
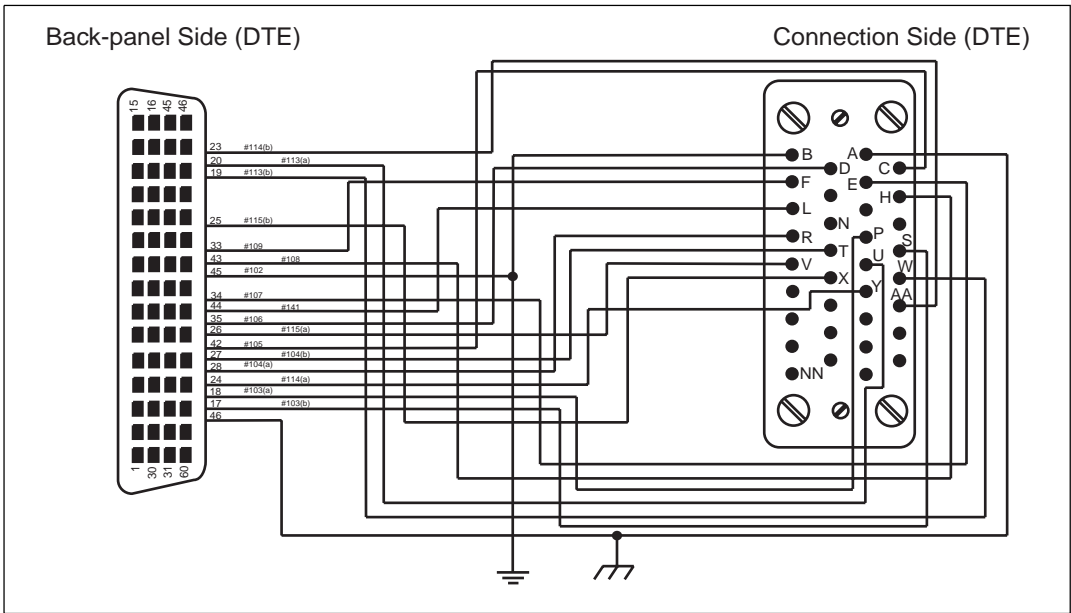
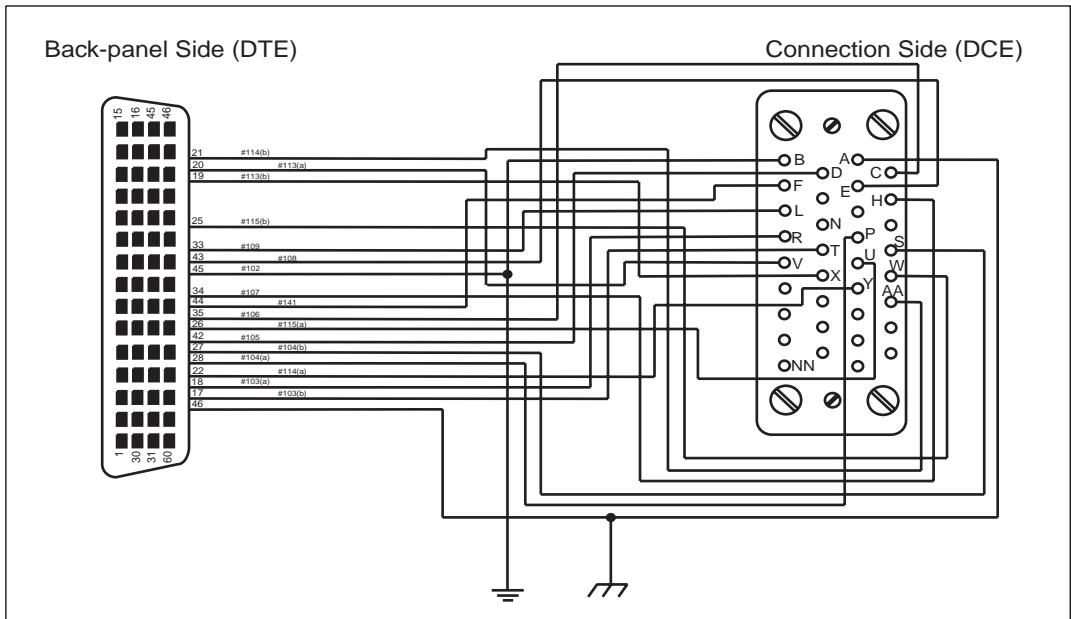*Figure 12. High-Density Daughter Cable - V.35 DTE Configuration*

Figure 13. High-Density Daughter Cable - V.35 DCE Configuration

Multi-Protocol Serial Port Transceiver Approaches

a) *Using discrete transceivers*

Implementing a serial port is relatively easy if you are dealing with one physical layer protocol. Dealing with more than one protocol will require transceivers for each appropriate physical layer. Each protocol will require transceiver ICs such as the traditional DS1488 or SP208 for RS-232 and DS26LS31 for V.11, etc. The design must also have enough drivers and receivers for the signals needed. This may require several ICs for RS-232, RS-422, and V.35.

For designs using a high-density cable, the transceiver I/Os are directly connected to an assigned pin on the connector. The RS-232 transceivers for TxD, RxD, CTS, DTR, etc. will go to preassigned pins on the connector. The RS-422 transceivers for the same signals will go to another set of pins on the connector. The same will go for the V.35 transceivers.

For the low-density connector where a pair of pins may define one signal for all protocols, the transceiver I/Os must be combined into the connector. The drivers must have tri-state capability to avoid bus contention when connecting the driver outputs together. When the serial port is selected in V.35 mode, the RS-232 and RS-422 driver outputs must be tri-stated or disconnected. Also, the RS-422 and V.35 drivers must tolerate the $\pm V_{OUT}$ swing from the RS-232 driver without producing any excessive leakage current. With $\pm12V$ supplied to the RS-232 drivers (DS1488 or MC145406), the range is $\pm12V$. The charge-pumped type RS-232 drivers (SP211 or MAX232) produce only up to $\pm10V$. Typical driver output leakage currents are in the $10\mu A$ to $500\mu A$ range. If the leakage current is at 1mA, the loading at 5V is 5kΩ. When the driver is connected to the receiver at the other end, the impedance caused by leakage from the disabled driver will combine the receiver input impedance in parallel and further load the driver output. It will also change the overall driver output V_{OH} and V_{OL} characteristics.

- ➥ Power Supplies Required: +5V, –5V, +12V, –12V

- ➥ Number of Transceiver ICs: 12

- ➥ Physical Layer Protocols Supported: RS-232, RS-422, RS-449, EIA-530, V.35, V.36

- ➥ Method of Protocol Selection: Hardware jumpers or switches/relays

- ➥ Board Space: Huge, real estate necessary for 15 active components and other supporting hardware.

- ➥ Overall Power Consumption: Approx. 1W

- ➥ Power Supplies Required: +5V Only

- ➥ Number of Transceiver ICs: 1

- ➥ Physical Layer Protocols Supported: RS-232, RS-422, RS-485, RS-449, EIA-530, EIA-530A, V.35, V.36

- ➥ Method of Protocol Selection: Software or hardware through internal decoder.

- ➥ Board Space: Very small compared to discrete method.

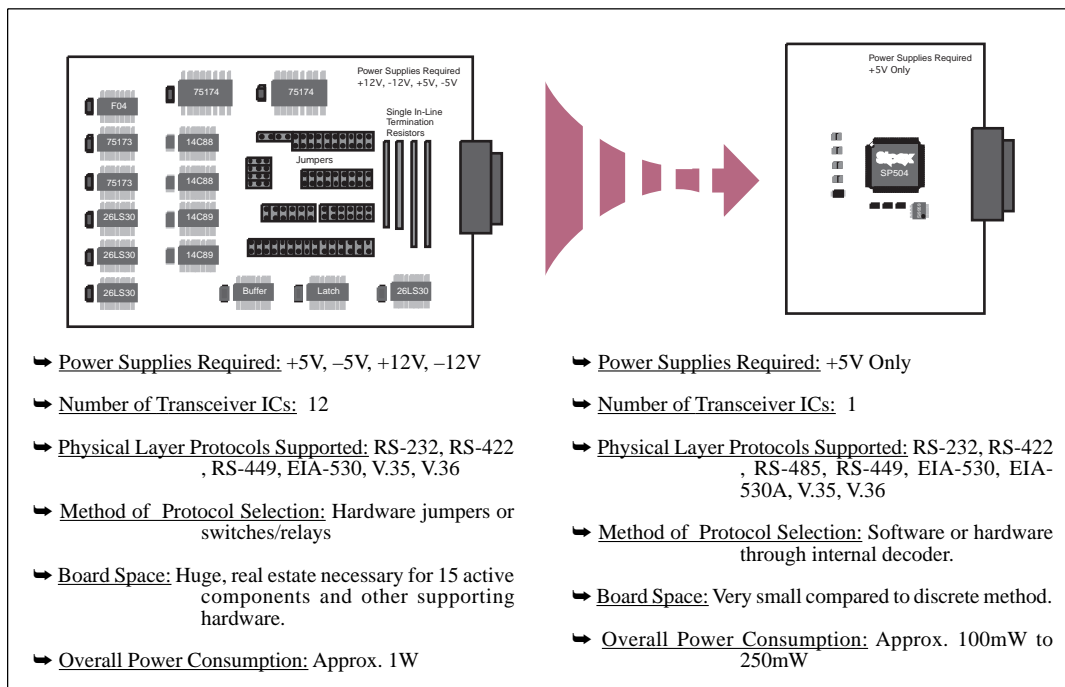- ➥ Overall Power Consumption: Approx. 100mW to 250mW

Figure 14. Comparison One-Chip Integration for Multi-Protocol Support (RS-232, X.21, EIA-530, RS-449, and V.35)

V.35 transceivers are especially difficult because of external termination networks necessary for V.35. These resistor networks for both drivers and receivers must be disconnected during other interfaces. Usual V.35 driver networks have a "Y" configuration where a 124Ω resistor is connected between two 51Ω resistors. The other end of the 124Ω resistor is connected to ground, and the network is connected between the A and B outputs of the driver. The termination network must be switched out when all other interfaces are selected. Switching mechanisms must be carefully considered since the switches will also have to tolerate the RS-232 voltage swings (±5V to ±15V). Typical analog switches do not have the analog signal range to support up to ±15V unless powered by ±15V supplies, which may not be available in most systems. Solid-state or mechanical relays are preferred for these types of applications. Opto-isolated FETs such as "Photo-MOS" FETs from Aromat or International Rectifier can be used for this application as well. These FETs require a gate current generated by a +5V supply through a series resistor to activate the device and can tolerate ranges of ±15V.

Incorporating the termination in the V.35 cable is another option. Although this is costly for the cable, it is a more direct solution since the V.35 termination is only used in conjunction with the V.35 connector. There are no switching complexities since the termination network is not on the board. The V.35 receiver termination is the same as the driver's network and can be configured similarly with switches or in the V.35 cable.

The connection from the transceivers to the HDLC controller must also be carefully considered. Logic outputs to the driver inputs of the transceiver are less critical and can go to multiple transceiver inputs. The RTS function of the HDLC device would go to the V.28 and V.11 driver input. Since the driver outputs go to their own pin allocation on the connector, there is no contention. Be sure that the HDLC device can drive multiple fanouts from its logic outputs. If not, a TTL buffer may be needed to increase the drive of the HDLC output. The receiver output connection to the HDLC device is tricky since there are multiple transceivers used for a particular signal. For example, CTS would be a TTL/CMOS output from the receiver. Since CTS is supported by X.21, EIA-232, V.35, EIA-530, etc., the CTS output is generated by a V.11 receiver and a V.28 receiver. Regardless of a receiver input, the output will produce a logic "0" or "1" which will contend with the other receiver output.
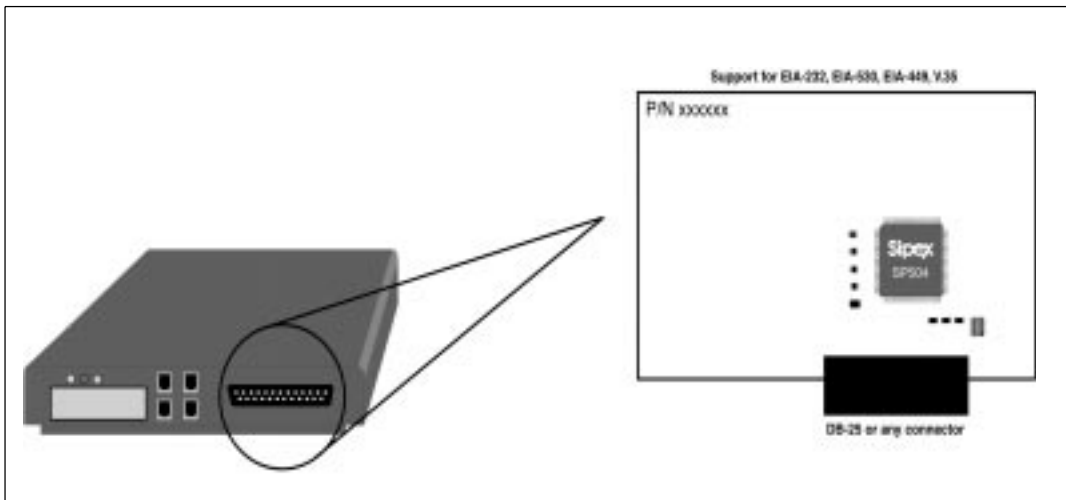

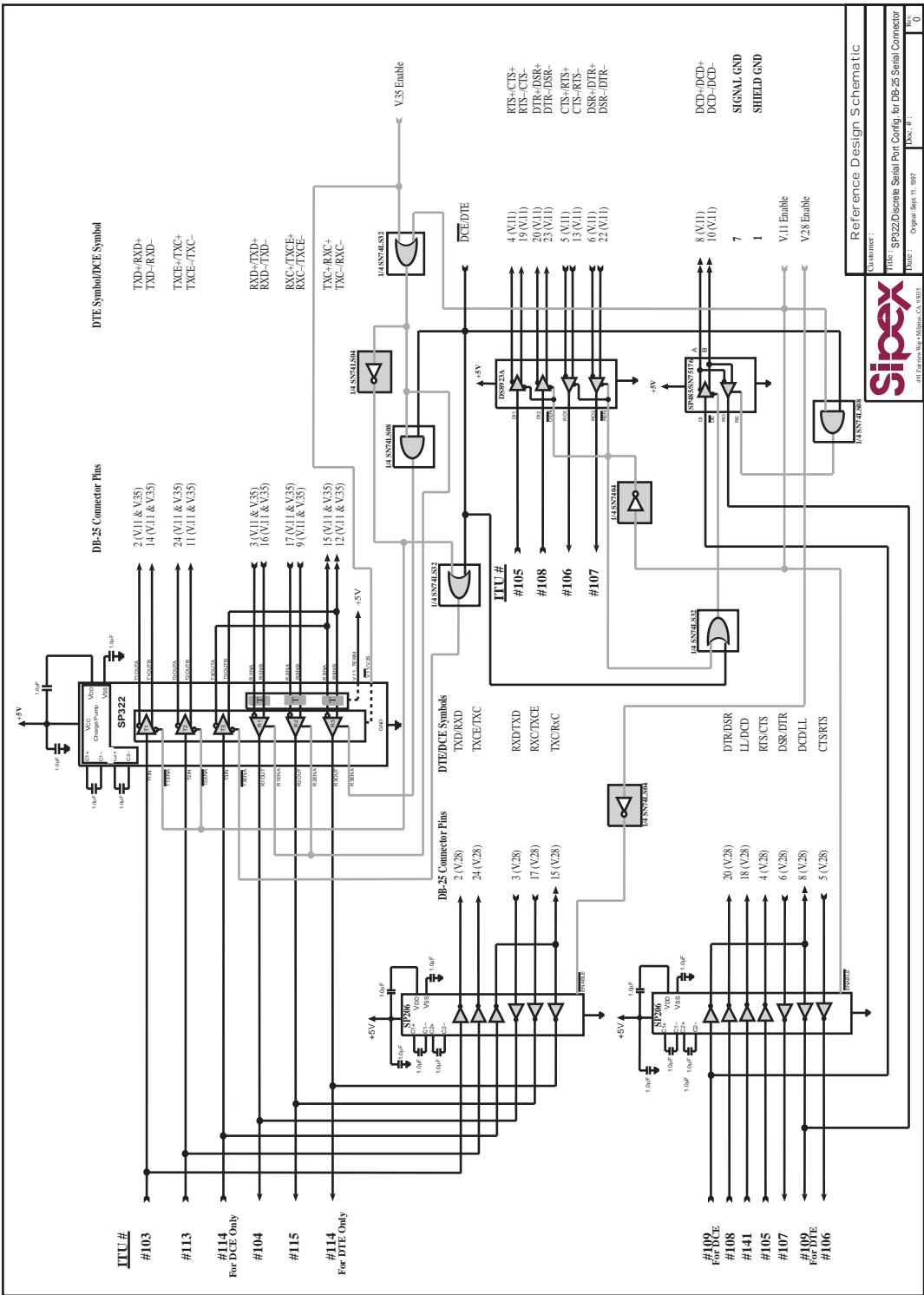*Figure 15. Configuration for Multi-Protocol Serial Ports Using the SP500 Multi-Protocol Transceiver.*

Figure 16. Discrete Configuration Using a DB-25 Serial Connector

Figure 17. SP322 Configuration Using a DB-25 Serial Connector

Figure 18. Configuration for Multi-Protocol Serial Port Using the SP322 and SP526 Transceivers.

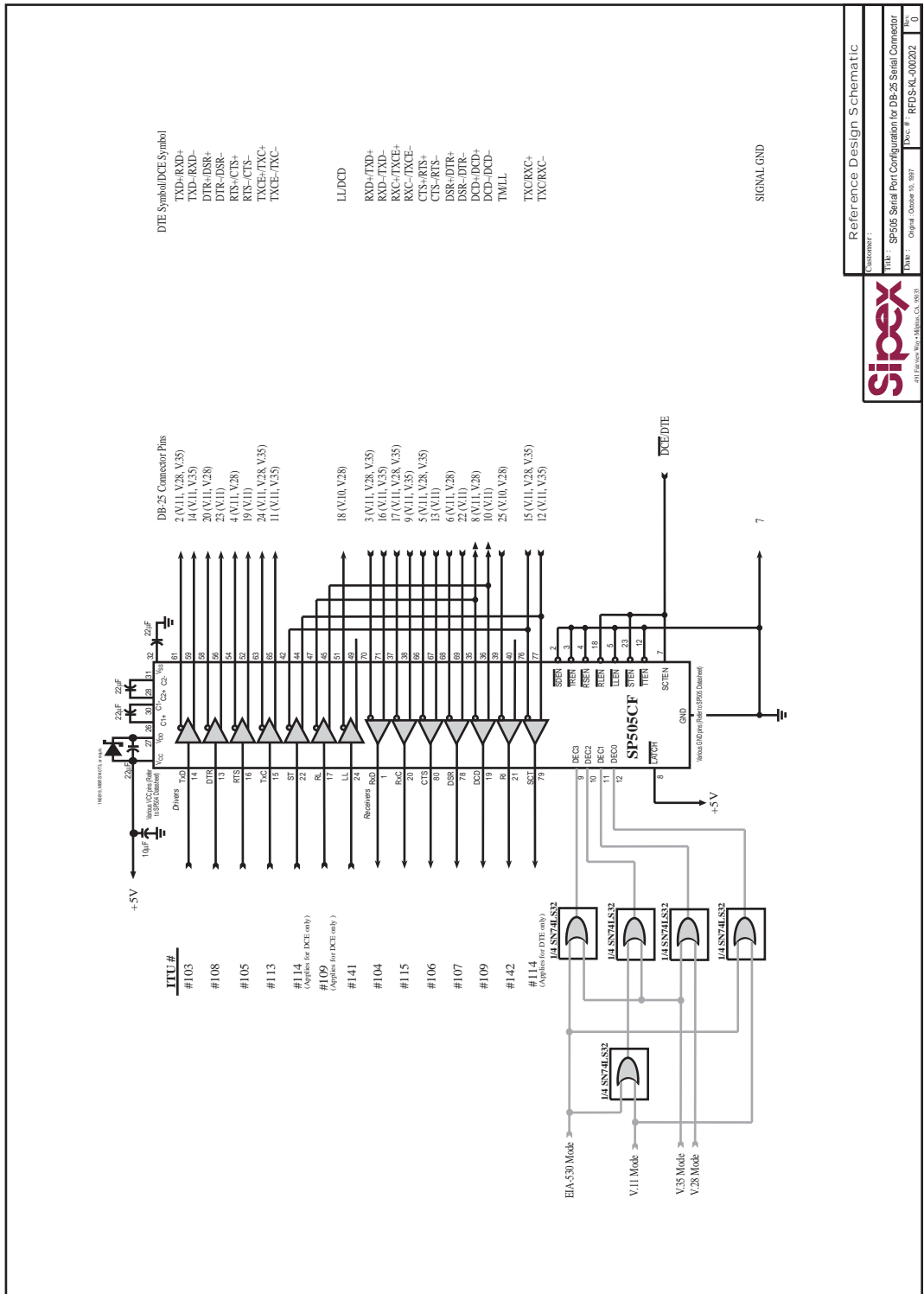*Figure 19. Configuration for Multi-Protocol Serial Port Using the SP504 Transceiver.*

Figure 20. Configuration for a Multi-Protocol Serial Port Using the SP505 Transceiver w/ the DB-25 Serial Connector

This problem is eliminated when a receiver's output can be disabled. Many discrete transceivers will have disabling features on the receiver which will tri-state the output on command. Be sure to select a transceiver which has a disable option on the receiver outputs. Another option is to use a multiplexer which will select the appropriate receiver output. For example, the RxD signal will originate from three different transceivers; EIA-232, V.11, and V.35. These outputs will route to the mux inputs (3:1 mux) and the output of the mux is selected by the interface selection logic. Thus, in V.35 mode, the V.35 RxD signal is valid through the mux and to the HDLC device.

b)   Integration

There are some transceiver manufacturers now producing multi-protocol transceiver ICs. Sipex was the first in the industry to introduce the SP301 RS-232/RS-422 software configurable IC. The multi-protocol transceiver basically combines the electrical characteristics of RS-232 and RS-422 transceivers into one single integrated circuit. *Figure 18* compares the two different implementations. There are more complete multi-protocol transceivers now offering more than four physical layer protocols in one chip. The newer transceivers include termination resistors for both V.35 as well as V.11 cable termination for the receivers.

In terms of disabling drivers and worrying about driver output leakage, the multi-protocol device is much easier to deal with. When configured to a specific protocol through control lines, the electrical parameters on the drivers and receivers will adhere to the appropriate electrical specifications. The integrated circuit internally handles the driver output levels, receiver input thresholds, driver & receiver impedance values, and common mode ranges for each physical layer protocol. The only change needed when choosing a serial protocol will be the physical connection to the other equipment. Again, this can be done by daughter cables.

The connection to the HDLC device is also simpler. Additional logic such as multiplexers can be removed between the receiver outputs and the HDLC inputs, since the multi-protocol transceiver will contain a dedicated receiver output for RxD or CTS, etc. The receivers are not required to have tri-state capability since only one RxD output will go to the RxD input of the HDLC, similar with the other signals.

DTE-DCE Capability on Serial Ports

a)   Cabling Techniques

Many systems may require the serial port to be configured as either a DTE or DCE. DTE/DCE configurations can be performed with cable options as discussed in *Multi-Protocol Serial Port Approaches; III. Cabling Approaches*. This technique for DTE/DCE flexibility is the easiest for reduced transceiver complexity. As mentioned previously, the DTE/DCE choice is done via the appropriate daughter cable. *Figures 7, 9, 11,* and *13* show the DCE configuration. This is the most straightforward approach to incorporating DTE/DCE options on a system. The schematics shown on *Figures 16* through *20* are configured as a DTE to the DB-25 serial port connector but can be easily changed to a DCE configuration by a DCE daughter cable. As mentioned previously, the driver output pins on the DB-25 serial port are now receiver inputs, and vice versa.

b)   Transceiver Configurations

Discrete transceiver designs or multi-protocol transceivers can be configured to support DTE or DCE on the serial port. Either approach will require dedicated transceivers for DTE and dedicated transceivers for DCE. The key is to isolate the DTE transceivers from the DCE transceivers.

Using the schematic illustrated in *Figure 16*, the discrete design shows a DTE configuration. The transceiver configuration is duplicated to support the DCE option. The driver outputs of the

DTE transceivers are connected back into the receiver inputs of the DCE transceivers, and the receiver inputs of the DTE transceivers are common with the driver outputs of the DTE transceivers. The common input/output lines can be routed to the connector and used as either driver outputs or receiver inputs. To control either DTE or DCE, the driver and receiver outputs must have tri-state capability. Extra considerations must be taken since now there are multiple driver outputs tied together with multiple receiver inputs, all routing to the serial connector. For three different serial protocols, TxD, for example, will have driver outputs from a RS-232, V.11 and V.35 transceiver. For DCE, the same outputs will have to connect to dedicated DCE receiver inputs for RxD for each protocol. There can be as many as eight drivers and eight receivers used for synchronous signaling which means, if quad-transceivers are used, as many as twelve transceivers are needed to support DTE/DCE for the three serial protocols.

The output leakage concern during tri-state is also more important now since one pin on the connector will be common with three driver outputs (RS-232, V.11, V.35) and three receiver inputs (RS-232 w/ 5kΩ Z_{IN}, V.11 w/120Ω Z_{IN}, and V.35 w/ 100Ω Z_{IN}). Without the DCE implementation, the pin only has three driver connections. The most complicated of transceivers are the V.35 drivers where the "Y" termination network is switched out from the output bus in other modes. However with DCE, the switching scheme is more elaborate since the V.35 "Y" network for the V.35 receivers and the V.11 120Ω cable termination between the receiver inputs are now attached to the same bus and must be switched out during the other protocols. Furthermore, the switches on the receiver inputs must tolerate more than the incoming RS-232 voltage swing which can be as high as ±15V.

The connection to the HDLC device will also require multiple connections from the various transceivers. The TxD pin of the HDLC will fanout to all the transceivers (RS-232, V.11, V.35 drivers for both DTE & DCE) which have a driver dedicated to TxD on the bus, similar to other synchronous signals.

When the two multi-protocol devices are connected, one device must be disabled while the other is transmitting and receiving data. Disabling one of the devices allows the other to communicate over the serial bus. One is dedicated to a DTE configuration to the serial port and the other is a dedicated DCE device. Disabling the DTE device implies that the serial port will be configured as a DCE, and vice versa.

Using the SP505 as an example shown in *Figure 21*, one device is dedicated for DTE and the other for DCE. Both have common I/O lines to the connector and communicate with the other side. For this case, a DTE configuration is selected and the DCE SP505 is disabled. The SP505 driver and receiver outputs can be tri-stated by writing "0000" into the decoder (DEC_X) lines. The receiver's input impedance is relatively high ($\geq$10kΩ) and will not affect the signals on the driver outputs.

Best of all, the V.35 termination resistors and the V.11 receiver cable termination are internal within the SP505. The resistor networks conveniently switch out when not used for their respective protocols. When disabled, the leakage is low enough so that there is no interference with signals and with various impedance and current testing for the drivers or receivers in V.28, V.11 and V.35 modes.

For the complexity of DTE and DCE flexibility while supporting the various physical layer protocols desired, using a multi-protocol serial transceiver simplifies the configuration, real estate, and design task, necessary when using many discrete components.
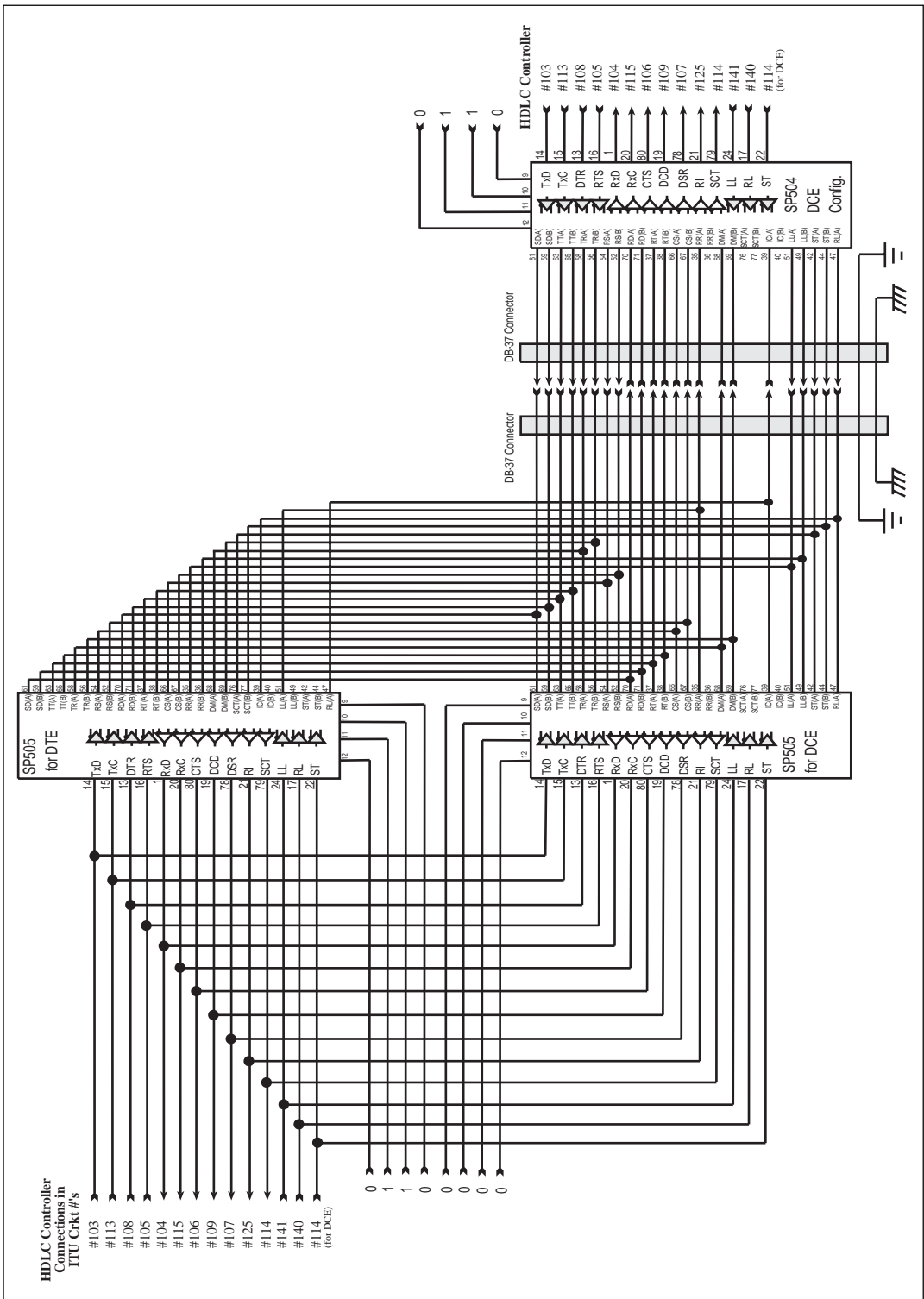
Figure 21. DTE/DCE Configuration on Board Using Two SP505 Multi-Protocol Transceivers

NET1/NET2 European Compliancy Testing

Compliancy testing is becoming more of a requirement for networking equipment. Many system designers are concerned with attaining the European certification and approval necessary for connecting the equipment to the European public networks. Some of the system designers may not fully be aware of what this testing entails.

Telecom certification and approval are performed in accordance with the NET (Norme Européenne de Télécommunication) which is a specification written by ETSI (European Telecommunications Standards Institute) that specifies the approval requirements for data terminal equipment (DTE) connecting to public data networks. Testing the NET requirements involve all seven layers of the OSI model (Physical, Data Link, Network, ... Application Layers) as well as EMC (electromagnetic compatibility) and various safety tests. The purpose of the NET is to ensure interworking of terminal equipment, protection of public telecom networks from harm and user/operator safety. NET testing can be performed by anyone but can only be certified by an approved test lab.

NET1 specifies approval requirements for the DTE to connect to circuit switched public data networks and leased circuits using ITU Recommendation X.21. NET2 specifies approval requirements for the DTE to connect to packet switched public data networks using ITU Recommendation X.25. Some test labs may adhere to test methods and techniques described by the ETSI specification, TBR (Technical Basis for Regulation). In the past, the TBR may be used to pass the serial port for NET1/2.

The configuration of serial transceiver circuitry impacts the NET1/NET2 physical layer testing. The serial transceiver IC is directly tested to ensure meeting the electrical requirements as specified by the NET. The physical layer proto-col for NET1 is V.11 (RS-422). The physical layer protocols for NET2 are V.11, V.28 (RS-232), V.35, and V.36 (combination of V.10 and V.11). Depending on the system, only two or three of these protocols may be implemented. The International Telecommunications Union (ITU, formerly CCITT) Series V Recommendations (Data Communication Over The Telephone Network) can be used for reference on the electrical specifications.

The testing methodology prescribed by the TBR apply simple circuit theory principles to the test the transmitter outputs and the receiver inputs. ***The following test procedures and illustrations are not meant as standards for testing per the ETSI NET1/NET2 and the TBR specifications but summarizes all the electrical physical layer testing performed on the serial port of the equipment as prescribed by the NET.*** The actual testing is usually performed through the appropriate interface cable connected to the serial port of the equipment. The NET1/NET2 and TBR documents should be referenced when performing compliancy testing. It is always good practice to do a "pre-compliancy" test prior to taking the equipment for certification testing. Any problems can be detected in the lab before going to the certified test house and investing the cost for the NET testing only to discover that the system may not pass.

Transceivers will usually adhere to the physical layer standards like V.28, V.11, V.35, etc. as specified in their datasheets. But as a safety precaution, examine the transceiver electrical specifications and compare to the ITU V. Recommendations (V.28, V.10, V.11, V.35) and ETSI NET1/2 documents.

ELECTRICAL SPECIFICATIONS PER ITU V. RECOMMENDATIONS

(Refer to the following *Figures* for more accurate test circuits on the electrical specifications.)

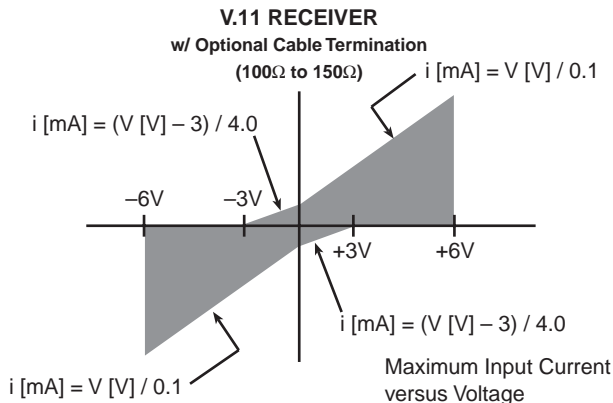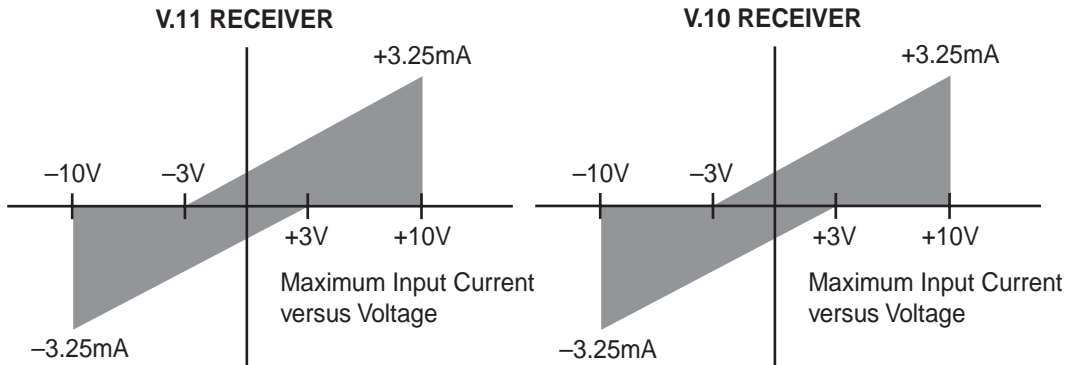|	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.10 DRIVER Output Voltage					
✔Open Circuit, V_{OC}	±4.0		±6.0	Volts	R_L=3.9kΩ
✔Test-Terminated, V_T	$0.9V_{OC}$			Volts	R_L=450Ω
Output Current					
✔Short Circuit, I_{SC}			±150	mA	V_{OUT} = 0V
✔Power Off, I_X			±100	µA	V_{CC} = 0V, V_{OUT}= ±0.25V
✔Rise Time, $+t_r$, $-t_r$			$0.3t_b$	µs	t_b = pulse width of signal < 1ms
			300	µs	$t_b \geq$ 1ms
					Measured between 10% to 90%
V.10 RECEIVER					
✔Input Current	−3.25		+3.25	mA	Refer to V.10 Receiver input graph
Receiver Sensitivity			±0.3	Volts	V_{IN} = +7V to −7V
Input Voltage Range	−10		+10	Volts	Functional test; no damage for either binary state.
Input Balance					Functional test; detect change in binary state while input is varied.
V.11 DRIVER Output Voltage					
✔Open Circuit, VO			±6.0	Volts	R_L=3.9kΩ
✔Test-Terminated, V_T	±2.0			Volts	R_L=50Ω
	$0.5V_O$		$0.67V_O$	Volts	
✔Offset, V_{OS}			+3.0	Volts	R_L=50Ω
✔Balance			±0.4	Volts	$\mid V_{T\,(logic\,"1")} \mid - \mid V_{T\,(logic\,"0")} \mid$
Output Current					
✔Short Circuit, I_{SC}			±150	mA	V_{OUT} = 0V
✔Power Off, I_{XA}, I_{XB}			±100	µA	V_{CC} = 0V, V_{OUT} = ±0.25V
✔Rise Time, $+t_r$, $-t_r$			20	ns	t_b = pulse width of signal < 200ns
			$0.1t_b$	ns	$t_b \geq$ 200ns
					Measured between 10% to 90%
V.11 RECEIVER					
✔Input Current	−3.25		+3.25	mA	Refer to V.11 Receiver input graph. Tested for power-on and power-off conditions.
✔Input Current w/ Termination	−60.75		+60.75	mA	With 100Ω minimum between inputs Power-on and power-off conditions.
Receiver Sensitivity			±0.3	Volts	V_{CM} = +7V to −7V
Common Mode Range	−10.0		+10.0	Volts	
Input Balance					Functional test; detect change in binary state while inputs are varied.
V.28 DRIVER Output Voltage					
✔Open Circuit, VO			±25	Volts	
✔Loaded, V_T	±5			Volts	R_L=3kΩ
✔Loaded, V_T			±15	Volts	R_L=7kΩ
Output Current					
✔Short Circuit Current			±500	mA	R_L=0.5Ω, for either binary state
✔Power Off Impedance	300			Ω	V_{CC} = 0V, V_{OUT} = ±2.0V
✔Instantaneous Slew Rate			30	V/µs	R_L=7kΩ; ≤ 20kbps
✔Transition Time			$0.03t_b$	µs	R_L=3kΩ, C_L=2500pF; ≤ 20kbps Measured between ±3V.

ELECTRICAL SPECIFICATIONS PER ITU V. RECOMMENDATIONS (continued)

(Refer to the following *Figures* for more accurate test circuits on the electrical specifications.)

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V28 RECEIVER					
✔Open Circuit Load Voltage			+2.0	Volts	
Valid Transition Range	+3.0		+15.0	Volts	"ON" state; Receiver V_{OUT} = logic "0"
	−15.0		−3.0	Volts	"OFF" state; V_{OUT} = logic "1"
✔Input Impedance	3		7	kΩ	V_{IN} = +15V to −15V
✔Input Shunt Capacitance			2500	pF	
V.35 DRIVER					
Output Voltage					
✔Differential Output	±0.44		±0.66	Volts	R_L= 2 x 50Ω in series
✔Voltage Output Offset	−0.6		+0.6	Volts	
✔Source Impedance	50	100	150	Ω	
✔Short-Circuit Impedance	135	150	165	Ω	V_{OUTA} = V_{OUTB} = −2V to +2V
✔Transition Time			40 or 0.1t_b	ns	R_L=100Ω; t_b = pulse width of signal Measured between 10 % and 90%
V.35 RECEIVER					
✔Input Impedance	90	100	110	Ω	
✔Short-Circuit Impedance	135	150	165	Ω	V_{IN} = +2V to −2V

✔ - **Tested parameters during NET1/NET2 Conformance Testing**

RECEIVER INPUT GRAPHS

V.11 RECEIVER

+3.25mA

−10V −3V +3V +10V

Maximum Input Current versus Voltage

−3.25mA

V.10 RECEIVER

+3.25mA

−10V −3V +3V +10V

Maximum Input Current versus Voltage

−3.25mA

V.11 RECEIVER
w/ Optional Cable Termination
(100Ω to 150Ω)

i [mA] = V [V] / 0.1

i [mA] = (V [V] − 3) / 4.0

−6V −3V +3V +6V

i [mA] = (V [V] − 3) / 4.0

i [mA] = V [V] / 0.1

Maximum Input Current versus Voltage

I. V.28 RECOMMENDATION *(ANNEX B IN NET2)*

ANNEX B.1 – GENERATOR CHARACTERISTICS

B.1.1 *Protection against short-circuit conditions.*
   The generator shall not be damaged by the application when the output is short-circuited.

B.1.2 *Generator Output Current Limit.*
   The output current of the generator with a short-circuit applied between the generator output pin and ground shall not exceed 0.5A in any binary state. Test circuit is shown on *Figure 22*. The output can either be connected directly to ground or through a 0.5Ω resistor.
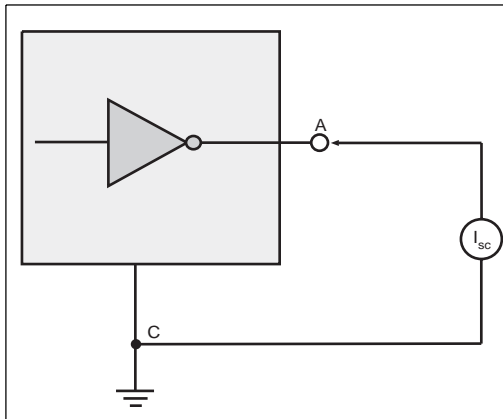
Figure 22. Generator Output Current Limit

B.1.3 *Generator Output Voltage open-circuit.*
   The open-circuit generator voltage shall not exceed 25V. Test circuit is shown on *Figure 23*. V_{OC} can be measured directly using a digital voltmeter (DVM).
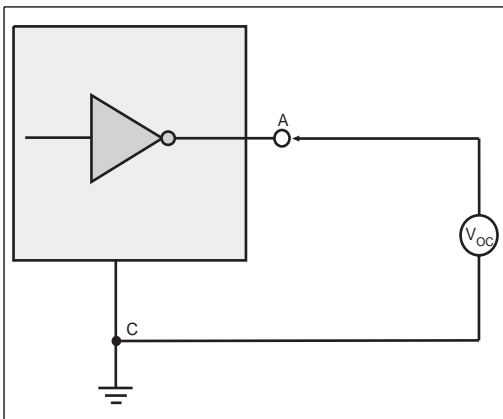
Figure 23. Generator Output Voltage Limit

B.1.4 *Generator Output Voltage limit under maximum load conditions.*
   The generator output voltage shall not be less than $\pm 5V$ in either binary state when terminated with a resistance of $3k\Omega$. Test circuit is shown on *Figure 24*. V_T can be measured directly using a DVM at the interchange point (output) to ground.

B.1.5 *Generator Output Voltage limit under minimum load conditions.*
   The generator output voltage shall not exceed $\pm 15V$ in either binary state when terminated with a resistance of $7k\Omega$. Test circuit is shown on *Figure 25*. V_T can be measured directly using a DVM at the output to ground.
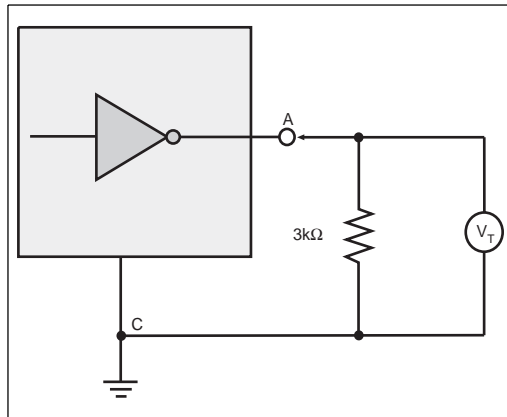
Figure 24. Generator Output Voltage – Maximum Load
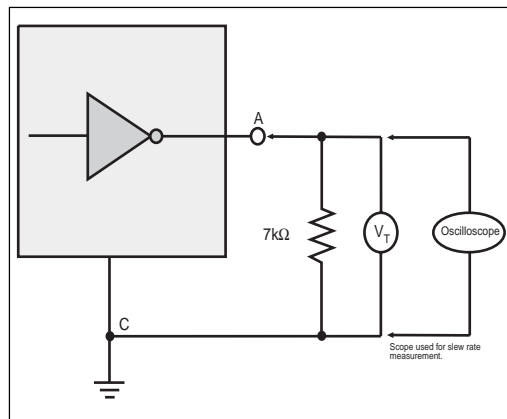
Figure 25. Generator Output Voltage – Minimum Load

B.1.6 *Generator Output Power.*
   The generator shall have sufficient output power to supply current through all of the capacitance on the generator side plus an additional capacitance of 2500pF.

ANNEX B.2 – LOAD CHARACTERISTICS

B.2.1 *Load Resistance Conditions.*

The load resistance shall have a minimum value of 3kΩ and a maximum value of 7kΩ over an input range of ±15V. Test circuit is shown on *Figure 26 and 27*. The testing will be performed at 3V and 15V. The current will be measured between the interchange point A and the test voltage of the supply (±3V or ±15V). The input impedance is calculated:
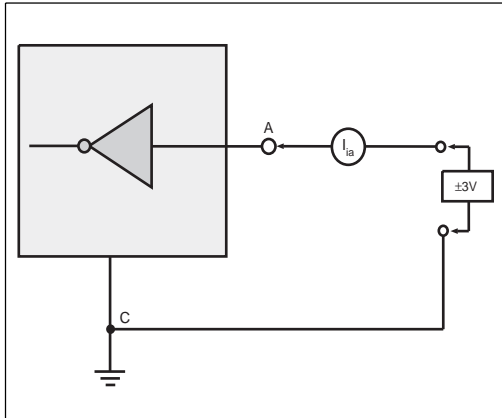
Figure 26. Load Resistance – 3V Test Voltage
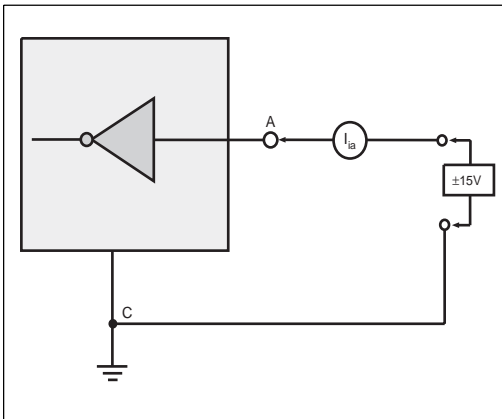
Figure 27. Load Resistance – 15V Test Voltage

V_{TEST} / I_{ia}.

B.2.2 *Maximum Load open-circuit voltage.*

The open-circuit of the load shall not exceed 2V when disconnected from the generator. Test circuit is shown on *Figure 28*. V_{OC} can be measured directly using a DVM at the interchange point (input) to ground.
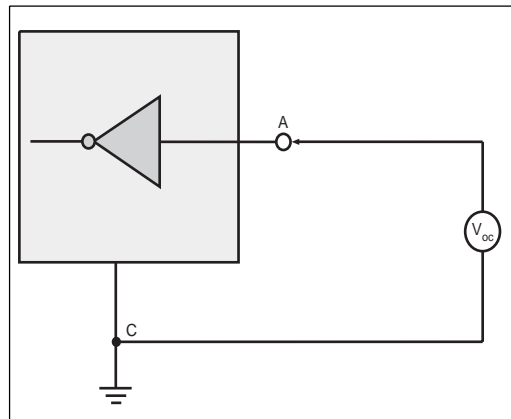
Figure 28. Load Open-Circuit Voltage
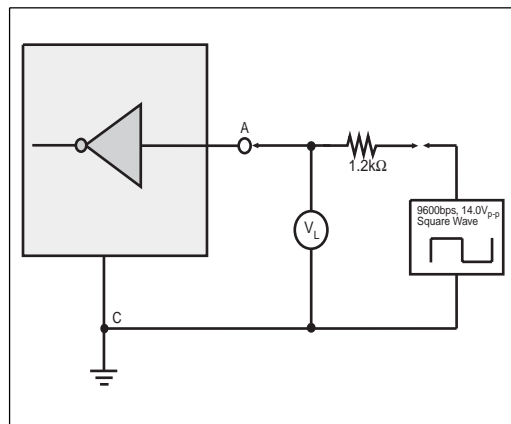
Figure 29. Load Shunt Capacitance

B.2.3 *Maximum load shunt capacitance.*

The total effective load shunt capacitance measured at the interchange point shall not exceed 2500pF. Test circuit is shown on *Figure 29*. The shunt capacitance is calculated using the effective R_{LOAD}. The R_{LOAD} is equal to $(1200 * V_{LOAD})/(14.0 – V_{LOAD})$. The V_{LOAD} is measured at the interchange point A with respect to ground. The shunt capacitance is equal to:

$C = T/(R_{LOAD} * Ln[(V_{LOAD} – V_1)/(V_{LOAD} – V_2)]$

where T is the transition time. V_1 and V_2 are measured during transition at –1.0V and +1.0V, respectively.

B.2.4 *Load impedance.*

The reactive component of the load impedance shall be capacitive as measured at the interchange point with an open-circuit condition. The frequency range is 0-20kHz.

B.3.1 *Wave form.*

Interchange signals entering the transition region shall proceed through this region to the opposite signal state in a monotonic progression. For example, a transition from –3V to +3V shall have no negative going component in the waveform, and vice versa. The test is done with both a) only a 7kΩ resistive load on the generator output *(Figure 25)*, and b) a resistive load of 3kΩ in parallel with a capacitive load of 2500pF *(Figure 30)*. Measurement in both conditions is performed with an oscilloscope. The output signal is measured at +3V to -3V of the waveform.
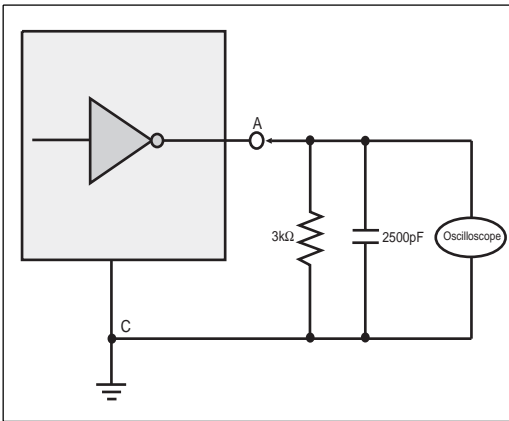
Figure 30. Transition Time and Slew Rate Test.

B.3.2 *Maximum transition time on control interchange circuits.*

The time required for the signal to cross the transition region during a change in signal state shall not exceed 1ms. Test circuit is shown on *Figure 30*. The output signal is measured at +3V to -3V of the waveform.

B.3.3 *Maximum transition time on data and timing interchange circuits.*

The time required for the signal to cross the transition region during a change in signal state shall not exceed 1ms or 3% of the nominal element period on the interchange circuit, whichever is lesser. Test circuit is shown on *Figure 30*. The output signal is measured at +3V to -3V of the waveform.
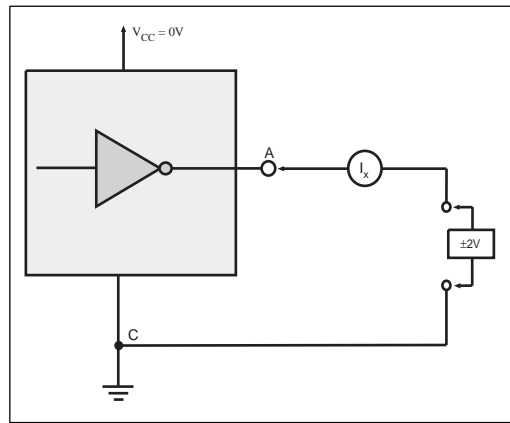
Figure 31. Generator Output Power-Off Impedance

B.3.4 *Maximum Instantaneous rate of voltage change.*

It shall not be possible for an interchange circuit to have a slew rate of more than 30V per microsecond. Test circuit is shown on *Figure 25*. The output signal is measured between 10% to 90% of the waveform.

B.4 *Power off condition with minimal load.*

In the power off state, the generator shall have an output impedance greater than 300Ω when referenced to the common return. Test circuit is shown on *Figure 31*. The current I_X is measured from the ±2V supply to the generator output. The resultant impedance is $2V / I_X$.

ANNEX B.5 – SHORT-CIRCUIT TESTS

a) Generator in the binary "0" (ON) state. The following tests shall be applied sequentially for 10 minutes.

i.) The generator output (A) connected to the common return (ground).

ii.) The generator output shall be connected to a load of 3kΩ, where the open-circuit voltage of the load is –2V.

b) Generator in the binary "1" (OFF) state. The following tests shall be applied sequentially for 10 minutes.

i.) The generator output (A) connected to the common return.

ii.) The generator output shall be connected to a load of 3kΩ, where the open-circuit voltage of the load is +2V.

Note 1: Detection of damage or high current can be performed by using an ammeter connected at point A to measure the steady state

maximum current for each test.

Note 2: B.5 tests do not represent the worst case where multiple short circuits occur.

Note 3: Where the generator would not normally produce a particular binary state for a period of 10 minutes, the tests in that state need not be performed.

B.7 – TEST EQUIPMENT REQUIREMENTS

a)   The digital voltmeter shall have a minimum internal resistance of 5MΩ.

b)   The oscilloscope shall have a slew rate greater than 50V/μs and an input impedance greater than 5MΩ.

II. V.10 RECOMMENDATION *(SECTION 5 IN ITU)*

SECTION 5 – GENERATOR CHARACTERISTICS

5.1   *Output Impedance.*
   The total dynamic generator output impedance shall be less than or equal to 50Ω.

5.2.1   *Open-circuit voltage measurement.*
   The open-circuit voltage measurement is made with a 3.9kΩ resistor connected at the interchange point A with respect to the common return (ground). For either binary state, the magnitude of the output voltage shall be between 4.0V and 6.0V, inclusive. Test circuit is shown on *Figure 32*.
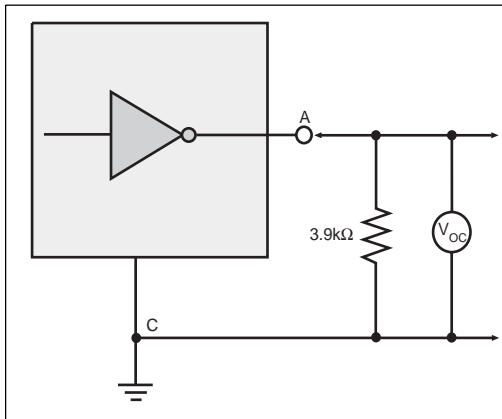
Figure 32. Generator Open-Circuit Voltage

5.2.2   *Test termination measurement.*
   The test terminated voltage measurement is made with a 450Ω resistor connected at the interchange point A with respect to the common return (ground). For either binary state, the magnitude of the output voltage shall be

greater than or equal to 0.9 (90%) of the magnitude of V_{OC}. Test circuit is shown on *Figure 33*.

5.2.3   *Short-circuit measurement.*
   The generator current in a short-circuited condition to the common return (ground) in either binary state shall not exceed 150mA. Test circuit is shown on *Figure 34*. An ammeter is used between the interchange point A and ground.
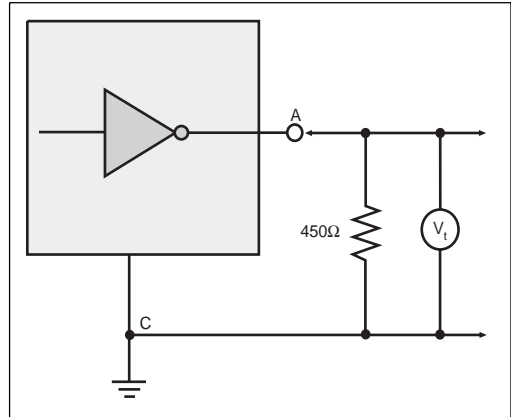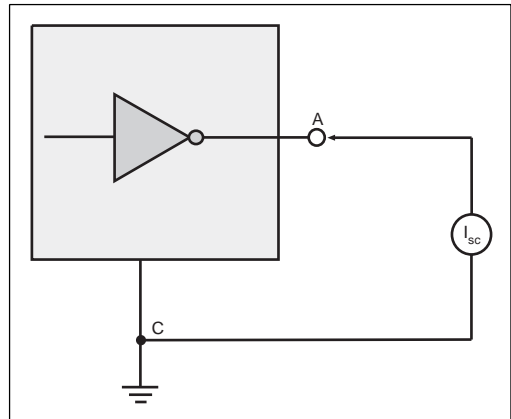

Figure 33. Generator Test Terminated Voltage

Figure 34. Generator Output Short-Circuit Current

5.2.4   *Power-off measurement.*
   Under a power-off condition, the magnitude of the generator output leakage current shall not exceed 100μA while a voltage of ±0.25V is applied. Test circuit is shown on *Figure 35*. An ammeter is connected between the test voltage and the interchange point A.
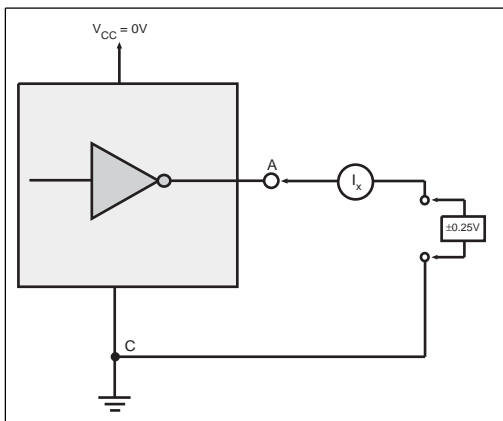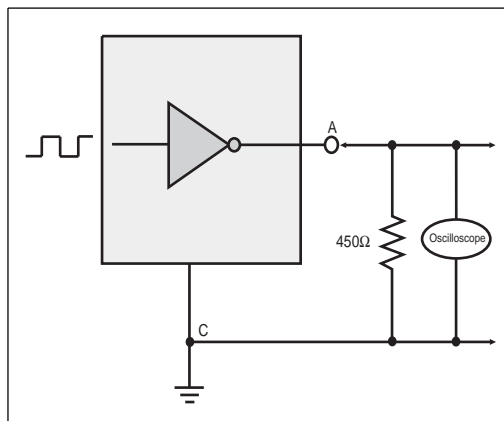
Figure 35. Power-Off Output Current

Figure 36. Generator Output Rise-Time Measurement

5.3.1 *Generator output rise-time measurement – Waveform.*

The waveform shall be observed using a 450Ω resistor connected between A and ground. A test signal with a pulse width or signal duration of t_b and composed of alternate binary 0's and 1's shall be applied to the input (i.e. function generator applying a TTL signal to the input). The change in amplitude of the output signal during transitions from one binary state to the other binary state shall be monotonic between 10% and 90% of the voltage difference between steady state signal conditions (V_{SS}).

5.3.2 *Generator output rise-time measurement – Waveshaping.*

The rise time of the output waveform shall be controlled to ensure that the signal reaches $0.9V_{SS}$ between 0.1 and 0.3 of the signal element duration, t_b, for signalling rates greater than 1 kbps. The rise shall be between $100\mu s$ and $300\mu s$ at signalling rates of 1 kbps or less. Test circuit is shown on ***Figure 36***.

SECTION 6 – LOAD CHARACTERISTICS

6.2 *Receiver input voltage – current.*

With a voltage of V_{ia} (or V_{ib}) ranging between $-10V$ and $+10V$, while V_{ib} (or V_{ia}) is held at 0V, the resultant input current for either I_{ia} or I_{ib} shall remain within the shaded region as shown in the V.10 Receiver Input Graph on ***Figure 17***. The current limit at 10V is 3.25mA. The measurements apply to both power-on and power-off conditions. Test circuit is shown on ***Figure37***.

6.3 *DC input sensitivity measurement*

For a common mode range (V_{CM}) of $\pm7V$, the receiver shall not require a differential input voltage (V_i) of more than 300mV to assume the correct binary state on the output. Reversing the polarity of the input shall cause the receiver output to assume the opposite binary state. The maximum voltage, including the common mode, present between either receiver input and receiver ground shall not exceed 10V. The receiver shall tolerate a maximum differential voltage of 12V applied across its input terminals without being damaged.

6.4 *Input balance test*

The balance of the receiver input resistances and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the following conditions:

a) with $V_i = +720mV$ and V_{CM} is varied between $\pm7V$

b) with $V_i = -720mV$ and V_{CM} is varied between $\pm7V$

c) with $V_i = +300mV$ and V_{CM} is a $1.5V_{P-P}$ square wave at the highest applicable signalling rate.

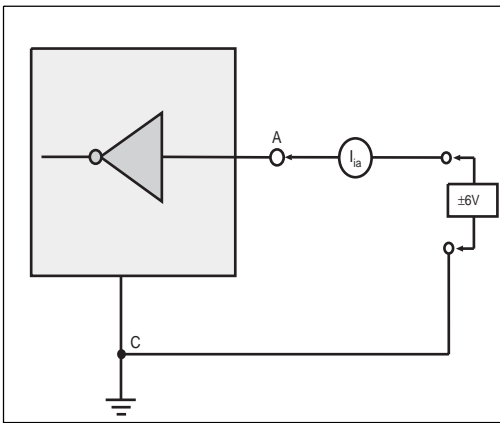d) with $V_i = -300mV$ and V_{CM} is a $1.5V_{P-P}$ square wave at the highest applicable signalling rate.

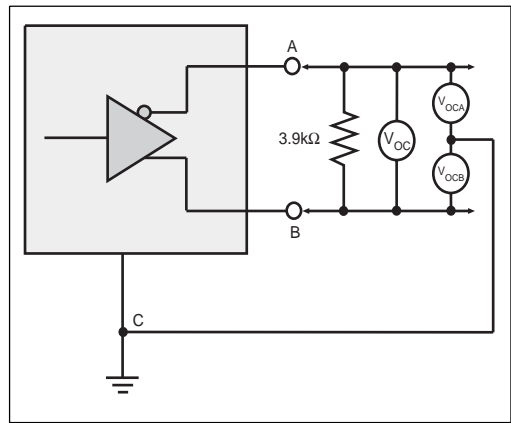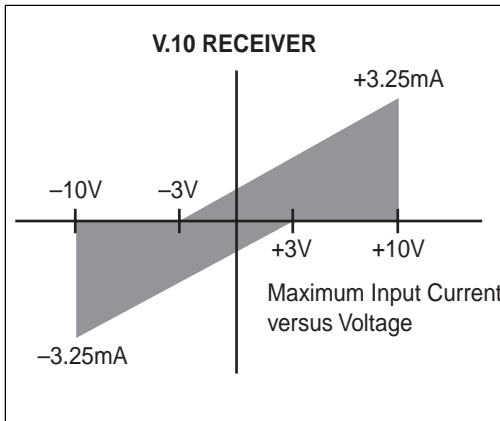Figure 37. Load/Receiver Input Current

Figure 38. V.10 Receiver Input Graph

III. V.11 RECOMMENDATION *(SECTION 5 IN ITU)*

SECTION 5 – GENERATOR CHARACTERISTICS

5.1   *Resistance and DC offset voltage.*
        The total generator resistance between inter-
        change points A and B shall be in the range of
        50Ω to 100Ω and adequately balanced with
        respect to the common return, C. The magni-
        tude of the generator DC offset shall not
        exceed 3V under all operating conditions.
        (The DC offset is also specified in 5.2.2)

5.2.1 *Open-circuit voltage measurement.*
        The open-circuit voltage measurement is made
        with a 3.9kΩ resistor connected between the
        interchange points A and B. For either binary
        state, the magnitude of the differential output
        voltage shall not exceed 6.0V, nor shall the
        magnitude of V_{OCA} and V_{OCB} be more than
        6.0V. Test circuit is shown on *Figure 39*.

Figure 39. Generator Open-Circuit Voltage

5.2.2 *Test termination measurement.*
        The test terminated voltage measurement is
        made with two 50Ω resistors connected in
        series between the interchange points A and
        B. For either binary state, the differential
        output voltage (V_T) shall not be less than 2.0V
        or 50% of the magnitude of V_{OC}, whichever is
        greater. For the opposite binary state, the
        polarity of V_T shall be reversed ($-V_T$). The
        difference in magnitudes of V_T and $-V_T$ shall
        be less than 0.4V. The magnitude of the
        generator offset voltage (V_{OS}) measured be-
        tween the center point of the two 50Ω in series
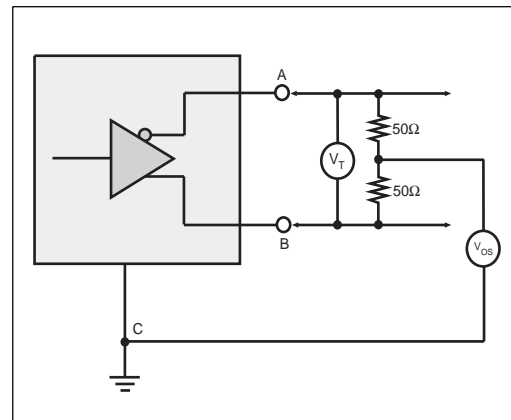   and the common return (point C) shall not be

Figure 40. Generator Test Terminated Voltage

greater than 3.0V. The magnitude of the
difference in values of V_{OS} for either binary
state shall be less than 0.4V. Test circuit is
shown on *Figure 40*.

5.2.3 *Short-circuit measurement.*

With both output points A and B short-circuited to point C, the current flowing through each of the output points A and B for both binary states shall not exceed 150mA. Test circuit is shown on *Figure 41*. An ammeter is used between the interchange point A and ground.
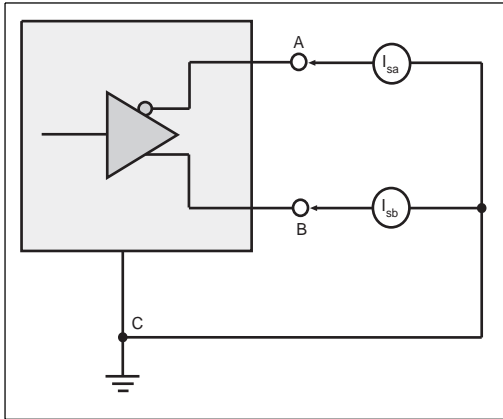

Figure 41. Generator Output Short-Circuit Current

5.2.4 *Power-off measurement.*

Under a power-off condition with voltages ranging between ±0.25V applied each output point and pointC, the magnitude of the output leakage current shall not exceed 100μA. Test circuit is shown on *Figure 42*. An ammeter is connected between the test voltage and the tested interchange point while the other point is open.

5.3.1 *Dynamic voltage balance and rise-time measurements.*

A waveform shall be applied to the input of the generator with a signal duration of t_b and composed of alternate binary 0's and 1's. The change in amplitude of the output signal during transitions from one binary state to the other binary state shall be monotonic between 0.1 and 0.9 of the voltage difference between steady state signal conditions (V_{SS}) within 0.1 of the signal element duration, t_b, or 20ns, whichever is greater. Thereafter, the signal voltage shall not vary more than 10% of its steady state value. Test circuit is shown on *Figure 43*.
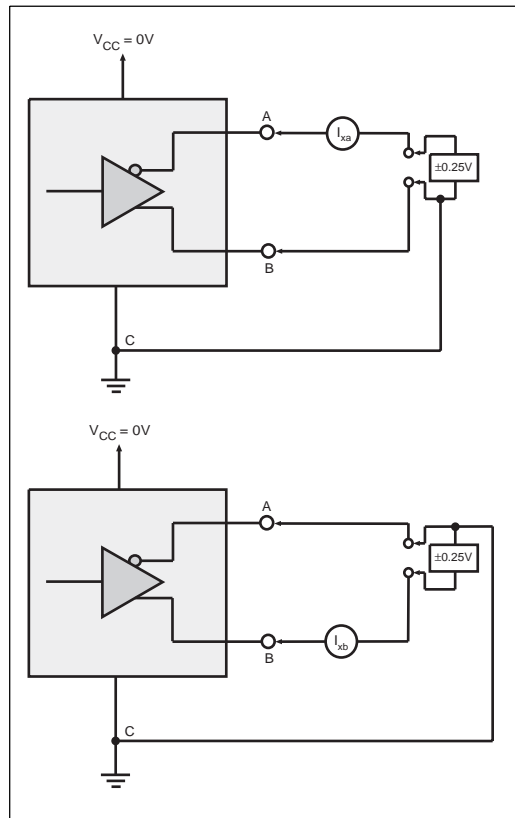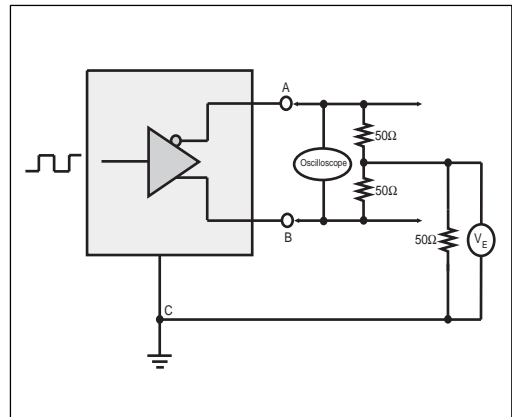

Figure 42. Power-Off Current Measurement

Figure 43. Generator Output Rise-Time Measurement

SECTION 6 – LOAD CHARACTERISTICS

6.2   *Receiver input voltage – current.*

With a voltage of V_{ia} (or V_{ib}) ranging between –10V and +10V, while V_{ib} (or V_{ia}) is held at 0V, the resultant input current for either I_{ia} or I_{ib} shall remain within the shaded region as shown in the V.10 Receiver Input Graph on **Figure 45**. The input current limit at ±10V is 3.25mA. The measurements apply to both power-on and power-off conditions. Test circuit is shown on **Figure 44**.

6.3   *DC input sensitivity measurement*

For a common mode range (V_{CM}) of ±7V, the receiver shall not require a differential input voltage (V_i) of more than 300mV to assume the correct binary state on the output. Reversing the polarity of the input shall cause the receiver output to assume the opposite binary state. The maximum voltage, including the common mode, present between either receiver input and receiver ground shall not exceed 10V. The receiver shall tolerate a maximum differential voltage of 12V applied across its input terminals without being damaged.
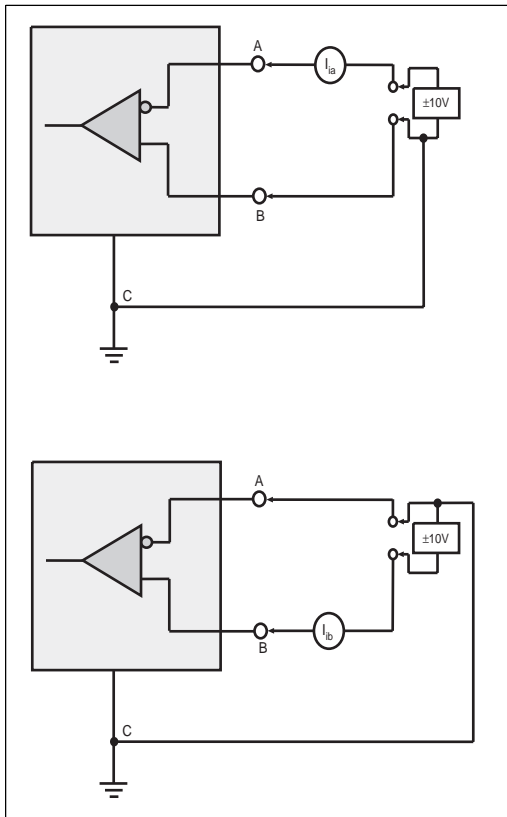
6.4   *Input balance test*

The balance of the receiver input resistances and internal bias voltages shall be such that the receiver shall remain in the intended binary state under the following conditions:

a) with V_i = +720mV and V_{CM} is varied between ±7V

b) with V_i = –720mV and V_{CM} is varied between ±7V

c) with V_i = +300mV and V_{CM} is a 1.5V_{P-P} square wave at the highest applicable signalling rate.

d) with V_i = –300mV and V_{CM} is a 1.5V_{P-P} square wave at the highest applicable signalling rate.

6.5   *Terminator*

The use of a cable terminating impedance (Zt) is optional depending upon the specific environment in which the interchange circuit is used. The total load resistance shall be greater than 100Ω. **Figures 46** and **47** show the receiver input test circuit and receiver input current range with the termination resistor, respectively. The maximum receiver input current for a terminated receiver input shall be less than or equal to 60.75mA over the voltage range of ±6V.

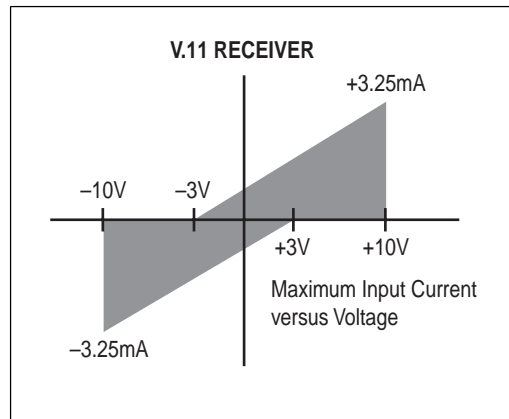**Figure 44. Load/Receiver Input Current**

Figure 45. V.11 Receiver Input Graph

11/15/05   Ani16: Multiprotocol Design Manual   © Copyright 2005 Sipex Corporation
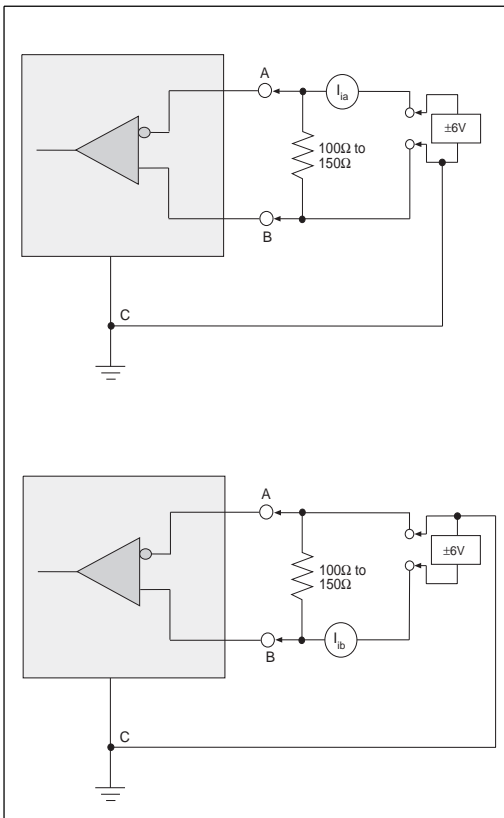
31

Figure 46. V.11 Receiver Input Test w/ Termination
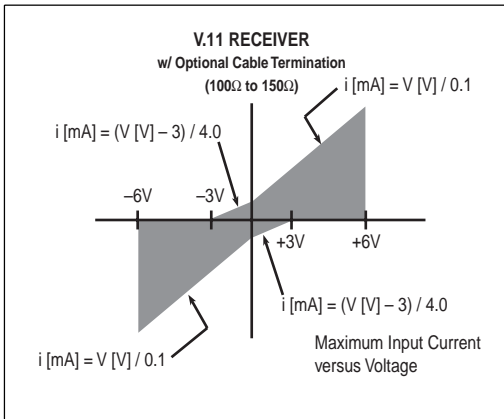

Figure 47. V.11 Receiver Input Graph w/ Termination

IV. V.35 RECOMMENDATION *(ANNEX C IN NET2)*

<u>SECTION C.1 – GENERATOR CHARACTERISTICS</u>

C.1.1 *Source impedance.*

The source impedance of the generator shall be 100Ω with a tolerance of $\pm 50\Omega$ at the applied signalling rate. Test circuit is shown on *Figure 48*. A sine wave with characteristics of $0.55V_{P-P}$ and 24kHz is applied to the generator output as shown. The sine wave is connected to one end of the 50Ω and the reference of the sine wave (usually the ground connection from the function generator output) is connected to the B interchange point. The other end of the 50Ω resistor is connected to the A interchange point. V_1 is the AC voltage measured across the 50Ω resistor. V_2 is the AC voltage measured across the inter-
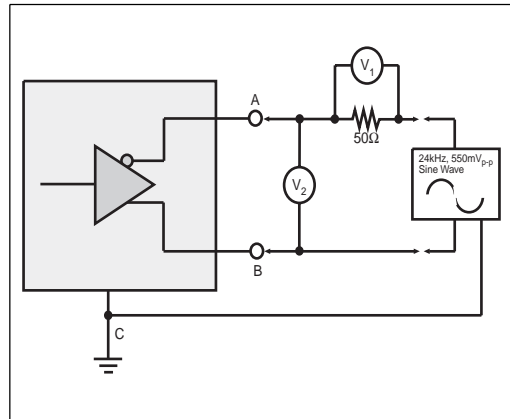

Figure 48. Generator Source Impedance

change points A and B. The source impedance is calculated by: $Z_S = (V_2/V_1)*50$.

C.1.2 *Short-circuit impedance.*

With a voltage range of $\pm 2V$ applied to the between short-circuited terminals A and B and the common return, the resistance shall be $150\Omega \pm 15\Omega$. Test circuit is shown on *Figure 49*. An ammeter is used to measure the current between the short-circuited point AB and the $\pm 2V$ supply. The short-circuited impedance is calculated by: $Z_{SC} = \pm 2V / I_{SC}$. In some cases, the offset voltage may be calculated into the equation by: $Z_{SC} = (\pm 2V - V_{OS})/I_{SC}$ where V_{OS} is the voltage measured between the short-circuited point AB and the common
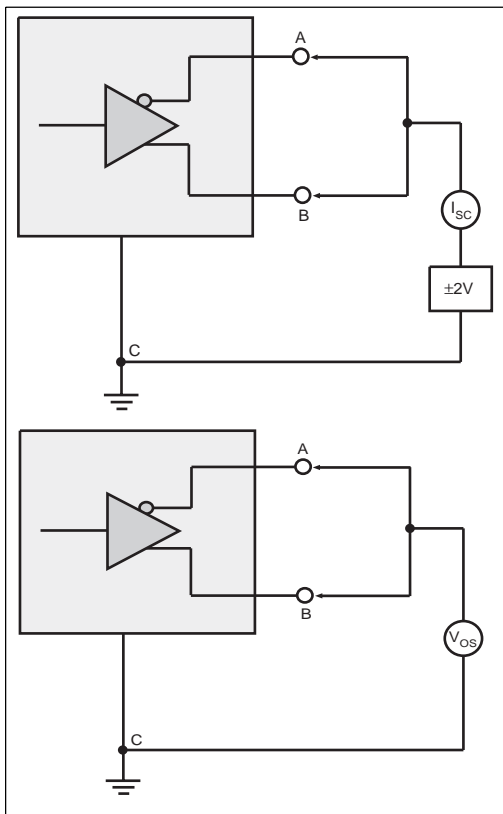
Figure 49. Generator Source Impedance

Figure 50. Generator Differential Voltage

Figure 51. Generator Rise Time Measurement

return, C prior to applying the test voltage.

C.1.3 *Test termination measurement.*

The terminal-to-terminal voltage between the interchange points A and B with a total resistive load of 100Ω (two 50Ω resistors in series.) Shall be 0.550V ±20% in either binary state. Test circuit is shown on **Figure 50**. A DVM can be used to measure the differential voltage.

C.1.4 *Rise time measurement.*

A waveform shall be applied to the input of the generator with a signal duration of t_b and composed of alternate binary 0's and 1's. The change in amplitude of the output signal during transitions from one binary state to the other binary state shall be monotonic between 0.1 and 0.9 of the voltage difference between steady state signal conditions (V_{SS}) within 0.1 of the signal element duration, t_b, or 40ns, whichever is greater. Thereafter, the signal voltage shall not vary more than 10% of its steady state value. Test circuit is shown on **Figure 51**.
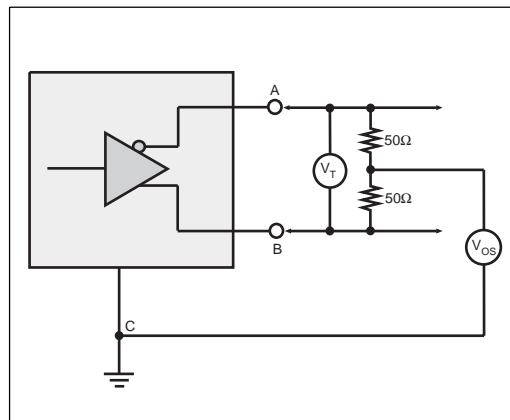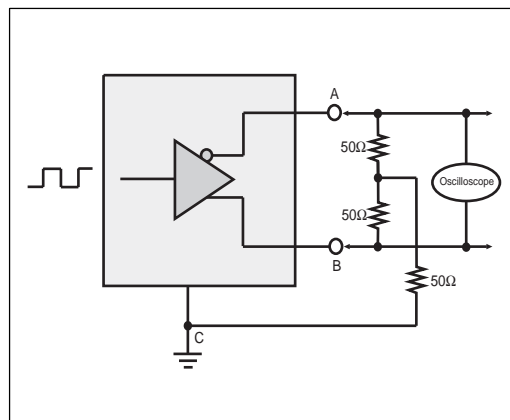
Section C.3 – Receiver Characteristics

C.3.1 *Source impedance.*

The input impedance of the receiver shall be 100Ω with a tolerance of $\pm$10Ω. Test circuit is shown on *Figure 52*. A sine wave with characteristics of $0.55V_{P-P}$ and 24kHz is applied to the receiver input as shown. The sine wave is connected to one end of the 50Ω and the reference of the sine wave (usually the ground connection from the function generator output) is connected to the B interchange point. The other end of the 50Ω resistor is connected to the A interchange point. V_1 is the AC voltage measured across the 50Ω resistor. V_2 is the AC voltage measured across the interchange points A and B. The input impedance is calculated by: $Z_S = (V_2/V_1)*50$.

C.3.2 *Short-circuit impedance.*

With a voltage range of $\pm$2V applied to the between short-circuited terminals A and B and the common return, the resistance shall be 150Ω $\pm$15Ω. Test circuit is shown on *Figure 53*. An ammeter is used to measure the current between the short-circuited point AB and the $\pm$2V supply. The short-circuited impedance is calculated by: $Z_{SC} = \pm2V/I_{SC}$. The receiver input open circuit bias may also be calculated into the equation by: $Z_{SC} = (\pm2V - V_{OS})/I_{SC}$ where V_{OS} is the voltage measured between the short-circuited point AB and the common return, C.
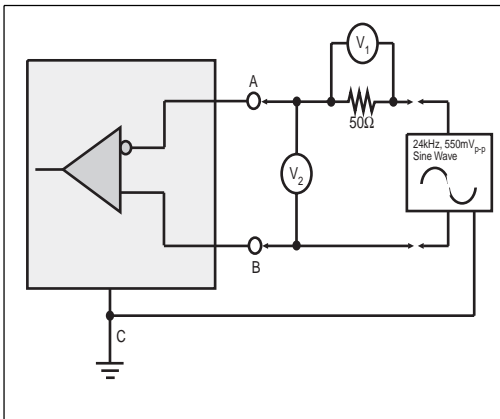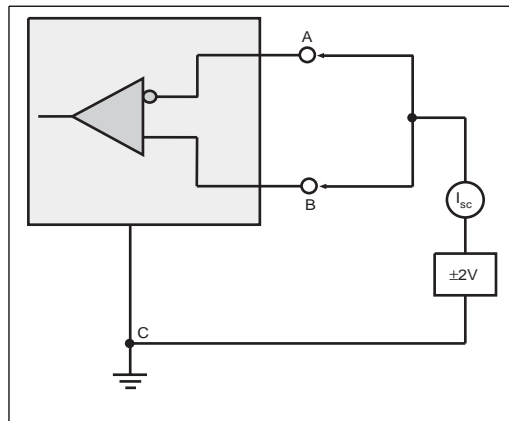

Figure 53. Receiver Short-Circuit Impedance

Figure 52. Receiver Input Impedance

LIST OF SIPEX MULTI-PROTOCOL TRANSCEIVERS

	Description/Physical layer Support	Tx/Rx Count
DUAL-PROTOCOL		
SP301	Programmable RS-232 and RS-422 Transceiver	2/2 for V.28; 2/2 for V.11
SP302	Programmable RS-232 and RS-422 Transceiver	4/4 for V.28; 2/2 for V.11
SP303	Programmable RS-232 and AppleTalk Transceiver	4/4 for V.28; 2/2 for Apple
SP304	Same as SP302 w/ Additional Drive Capability	4/4 for V.28; 2/2 for V.11
SP306	Programmable RS-422 and RS-423 Transceiver	2/2 for V.10; 2/2 for V.11
SP320	Complete V.35 Transceiver with RS-232 Control Lines	4/4 for V.28; 3/3 for V.35
SP322	Programmable +5V Only V.11 and V.35 Transceiver w/ Internal V.11 Cable and V.35 Termination, Individual Tri-State Control	3/3 for V.11; 3/3 for V.35
SP331	Programmable +5V Only RS-232 and RS-485 Transceiver w/ Tx Enable	4/4 for V.28; 2/2 for V.11
SP332	Programmable +5V Only RS-232 and RS-422 Transceiver	4/4 for V.28; 2/2 for V.11
SP333	Programmable +5V Only RS-232 and AppleTalk Transceiver	3/5 for V.28; 2/2 for Apple
SP334	Programmable +5V Only RS-232 and RS-485 Transceiver w/ Tx Enable	3/5 for V.28; 2/2 for V.11
MULTI-PROTOCOL		
SP502	+5V Only, Programmable RS-232, RS-422, RS-449, EIA-530, RS-485, V.35 DTE Configured	6/7 Total
SP503	Same as SP502 with Additional Driver for DTE or DCE Applications	7/7 Total
SP504	Same as the SP503 with Additional EIA-530A and V.36 Support Simplified V.35 Termination, Internal V.35 Receiver Termination	7/7 Total
SP505	Same as the SP504 with All V.35 and V.11 Termination Internally Contained Includes Individual Driver Tri-State Control, Decoder Latch, Internal Loopback	7/7 Total
SP506	20Mbps upgrade to the SP505	7/7 Total
SP507	Similar to SP506 but includes termination disable function, four drivers and receivers with disable/3-state capability, and 3-bit decoder.	7/7 Total
SP522	Programmable RS-232, RS-422 and RS-423 Transceiver, Individual Tri-State	2/2 Total
SP524	Programmable RS-232, RS-422 and RS-423 Transceiver, Individual Tri-State	4/4 Total
SP526	Programmable V.10. V.11, and V.28 transceiver. Supports handshaking signals in synchronous serial ports and mates with SP322 for full multi-protocol support.	4/4 Total

Sipex
Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

Headquarters and
Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com

Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600