Application Note ANP6

PowerBlox™ in Distributed Power Architectures

Introduction

The challenges in designing POL converters for distributed power architectures (see Figure 1) in telecom systems are many. System boards are very space constrained and the power solution must occupy minimal PCB real estate. Efficiency is of great importance to improve the throughput efficiency of the system as well as to minimize temperature rise in components and ensure long life. Also, the loads on the system board require complex and unique protocols that are provided in the ASIC or NPU manufacturer specifications. This sequencing function is usually done using a proprietary IC and high current MOSFETs on the output of each rail. These MOSFETs are 100% duty cycle switches that lower the efficiency of the system, generate heat and increase the cost of the system.

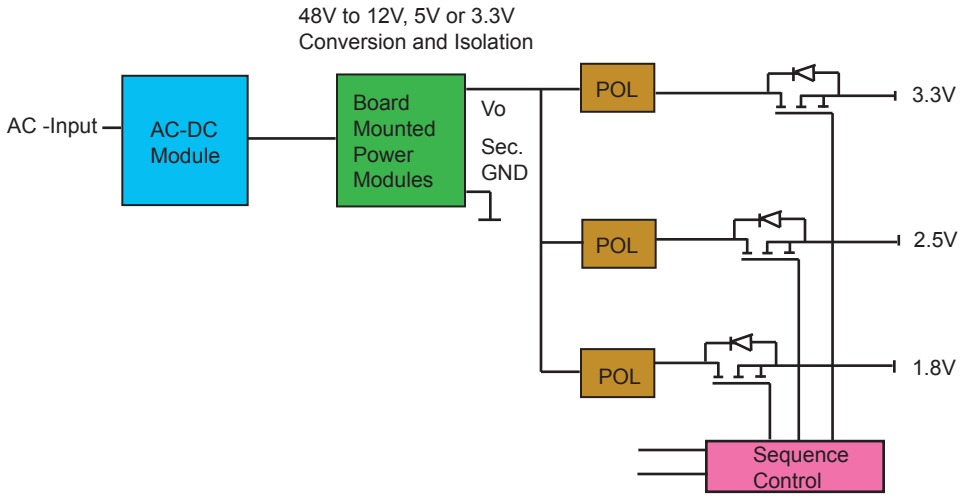

Figure 1. Distributed Power Architecture in a Telecommunications System

The PowerBlox™ Solution

Sipex has introduced a family of high current regulators called PowerBlox™ that address these system level requirements. The PowerBlox™ family of products are available in a range of output current levels from 3A to 8A and switching frequencies from 300kHz to 1.2MHz. An example of such a device is the SP7652 available in a space saving 7mm x 4mm DFN package. It is capable of accepting a wide input voltage and can provide up to 6A at output voltages as low as 0.8V. Since the switching frequency of the SP7652 is 600kHz, output filter size is reduced, enabling a very small solution ideal for applications where PCB real estate is at a premium. The built in low RDS(on) FETs enable high efficiency. Figure 2 shows the SP7652 delivering over 92% efficiency over the entire load range.

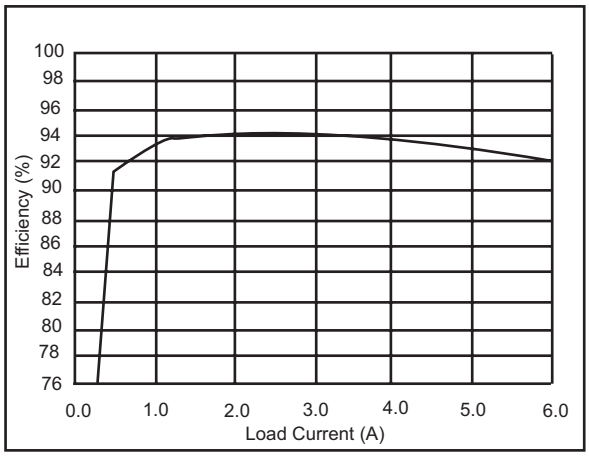

Figure 2. Efficiency versus Load Current for SP7652 at 5V_{IN} and 3.3V_{OUT}

The SP7652 includes protection features such as UVLO on both V_{CC} and V_{IN} pins, programmable soft start and thermal shutdown. The SP7652 also has short circuit protection with auto-restart. This auto-restart feature is key in today's end telecom or networking systems, many of which are in remote locations. Auto-restart capabilities increase up-time and reduce maintenance costs thereby improving QoS.

Implementing Power-Up Protocols

One of the most compelling reason for using this part in telecom systems is the ability to easily implement power-up protocols.

There are essentially three types of power-up protocols used in distributed power architectures: Sequential, ratiometric, and simultaneous (or output tracking). These protocols are described below.

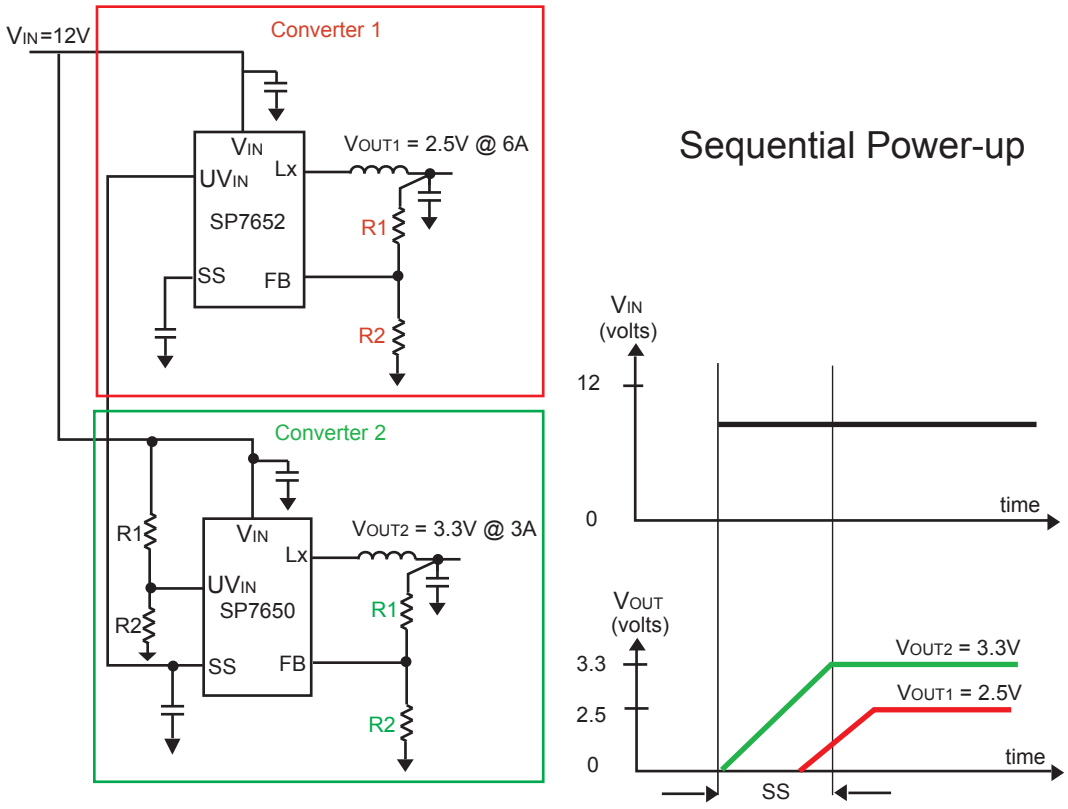

Figure 3. Sequential Power-up Implemented with PowerBlox™

1. Sequential Power-up

In sequential power-up, one voltage rail is turned on and, after a predetermined interval, the second voltage is turned on. Sequential power-up is required in systems where the core voltage rail must turn on before the I/O or chipset rails are turned on. This start up protocol can be easily implemented using the PowerBlox™ chips, by connecting the UVIN of one converter to the soft start of the other as shown in Figure 3.

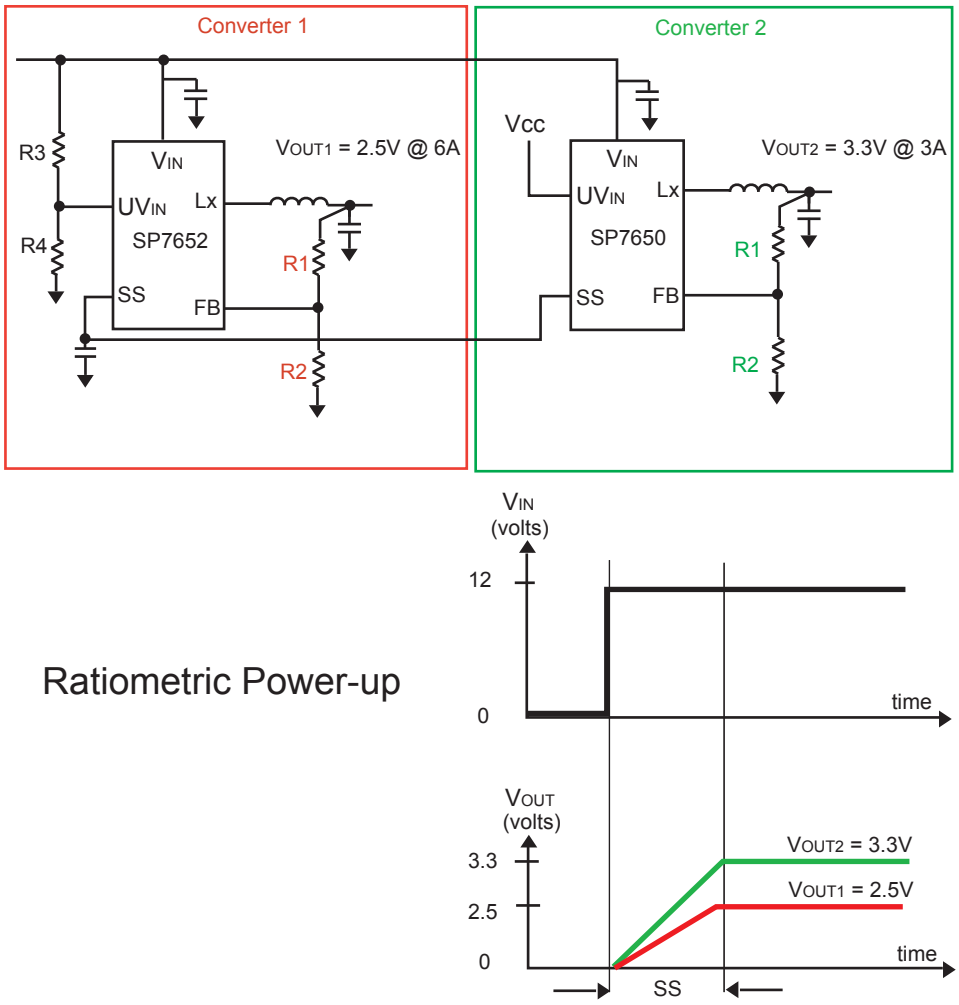

Figure 4. Ratiometric Power-up Using PowerBlox™

2. Ratiometric Power-Up

The second type of start-up is the ratiometric method: The two supplies are turned on simultaneously, reaching regulation at their respective set-points at the same time. In this method, the two rails are controlled with different slew rates, so that the two different voltages are realized at the same time. Figure 4 shows how to implement ratiometric power up simply by tying the soft start pins together.

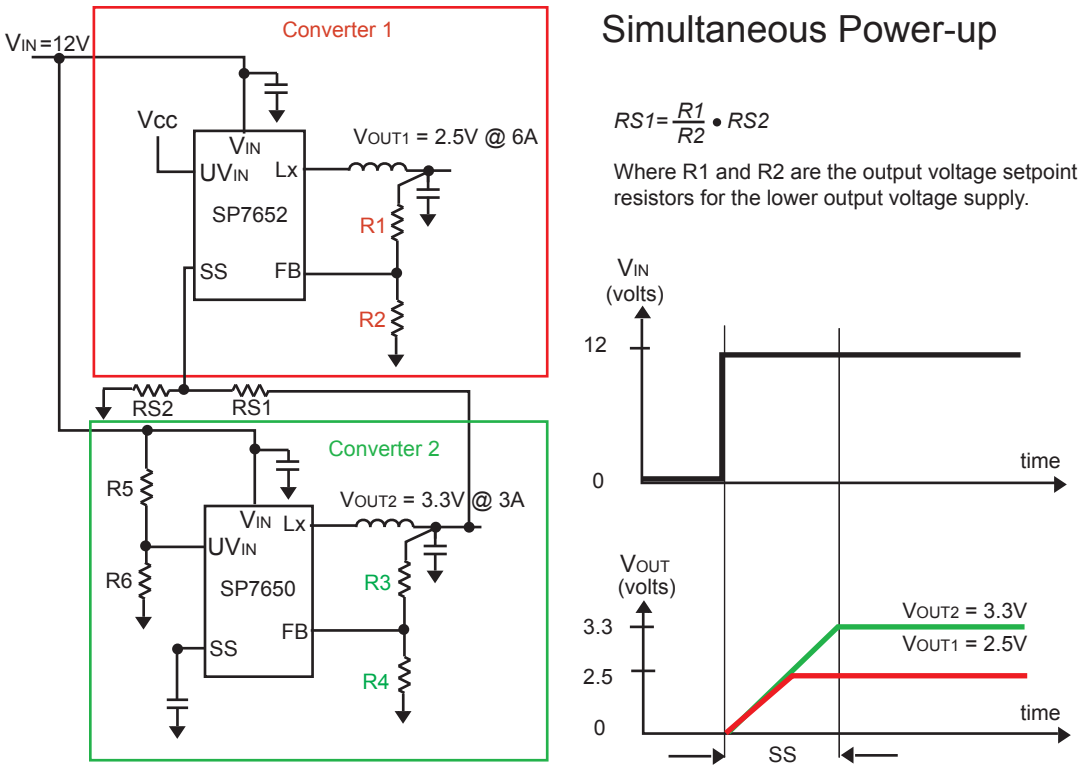

Figure 5. Simultaneous Power-up Using PowerBlox™

3. Simultaneous (Output Tracking) Power-up

The simultaneous power-up sequence is the third approach to power sequencing. Both the rails start up simultaneously and rise at the same slew rate. As a result, the lower voltage rail reaches regulation first, and the higher rail reaches regulation later. In order to implement simultaneous power-up using PowerBlox™, the output of the converter with the higher output voltage is tied through a resistor divider to the soft start of the other converter. The formula for calculating the resistor divider values is shown along with the application diagram in Figure 5. Note that RS2 should be set to 8kΩ.

Thus, the soft start and UVIN pins can be used in various configurations to provide simultaneous, sequential or ratiometric power up as required by the system. This eliminates the use of sequencing control ICs and MOSFETs on the output of each rail, simplifying system design and reducing costs at the same time.