APPLICATION NOTE ANP9

Using SP6652 For a Positive to Negative Buck Boost Converter

Introduction

The SP6652 is an integrated FET synchronous PWM buck regulator ideal for low input voltage applications. Although most standard circuits will use this device for simple synchronous step down conversion, this device is also capable of performing in a buck-boost topology for a positive voltage to negative voltage converter. In this application note we will show how to implement the SP6652 in the negative buck boost topology as well as simple design steps that are needed for proper component selection.

Principle of Operation

The simplified form of a buck boost regulator is shown below in Figure 1. The basic principle of operation relies on the principle of energy storage in the inductor L. When the switch S is conducting, diode D becomes reverse biased; thus all of the current goes into inductor L which will ramp up linearly until switch S is turned off. At this point the inductor reverses the polarity, thereby forward biasing the diode D and the energy stored in the inductor will be transferred to the load as well as the output capacitor C_{out}.

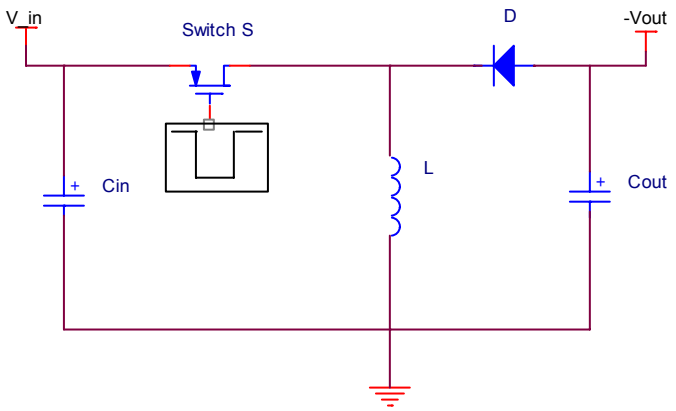


Figure 1

One advantage of using the SP6652 is the integration of the synchronous FET into the device, thus eliminating the need for the free wheeling diode D. This helps reduce the part count as well as increase the efficiency of the overall circuit. Below in Figure 2 is the switch configuration of the SP6652 showing how the synchronous switch Sync_FET replaces the free wheeling diode D.

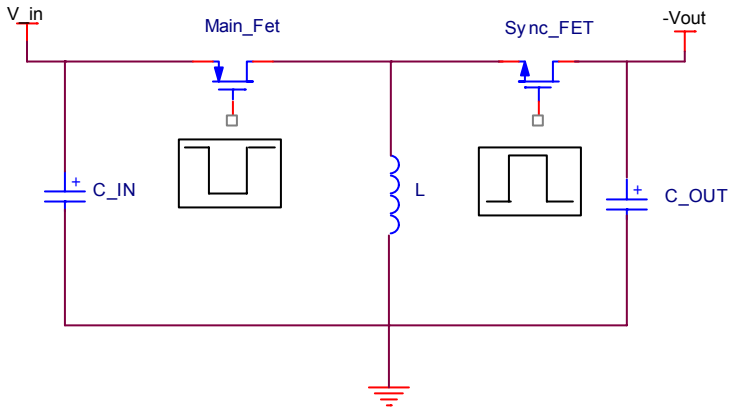


Figure 2

Design Considerations

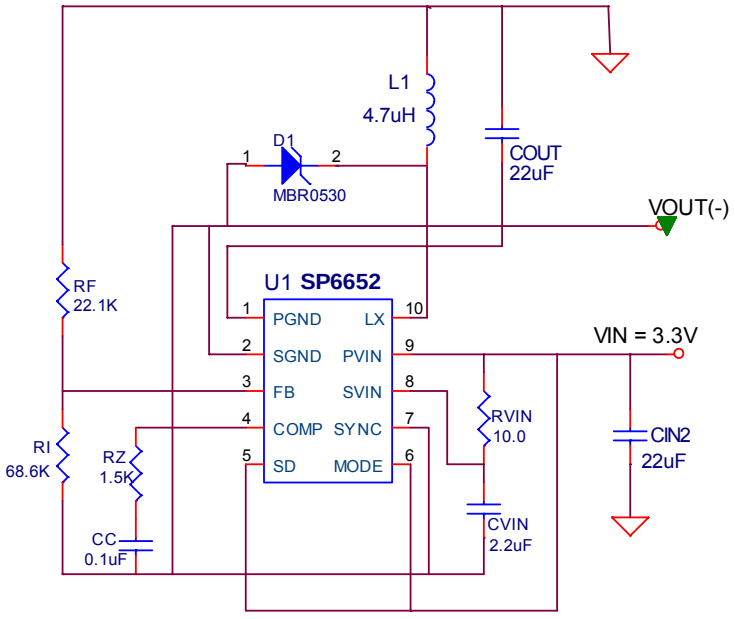


Figure 3

Figure 3 shows a typical configuration for a positive to negative voltage converter using the SP6652 including all supporting components needed for operation. One thing to note is that the GND of the SP6652 is connected to the V_{out} of the converter. Because of this connection to GND there are some further considerations that will be addressed in this application note. Also remember to connect any polarized components in the proper orientation as not to damage them since GND of the circuit on the output is more positive than V_{out}.

Component Selection

The next section will deal with proper component selection for this type of application.

Inductor Selection

The duty cycle is calculated as follows.

$$D = \frac{|V_{out}| + (I_{out} \cdot Rdson_{sync})}{V_{in} + |V_{out}| + (I_{out} \cdot Rdson_{sync}) - (I_L \cdot Rdson_{main})} \quad (1)$$

Where
$Rdson_{sync}$ is the switch resistance of the synchronous FET
$Rdson_{main}$ is the main switch resistance
I_L is the average Inductor current
I_{out} is the load current.

The average inductor current I_L

$$I_L = \frac{I_{out}}{1 - D} \quad (2)$$

One thing to notice about the set of formulae is that the duty cycle sets the amount of I_L. This creates a problem since the current I_L is not fixed in this converter configuration and can significantly vary with the duty cycle. A good assumption in the case of the SP6652 is to take the maximum current that the inductor could see, which is approximately 1.3A, set by the current limit of the device, and use this number as the starting point for inductor selection for max I_L.

It is also recommended to use equation 3 for duty cycle calculation as a good starting point.

$$D = \frac{|V_{out}|}{V_{in} + |V_{out}|} \quad (3)$$

The inductor can be defined as:

$$L = \frac{V_{in} \cdot D}{f \cdot \Delta I_L} \quad (4)$$

By substituting the duty cycle Equation 1 into the inductor equation 4 you get the following result:

$$L = \frac{V_{in}(|V_{out}| + (Rdson_{sync} \cdot I_{out}))}{f \cdot \Delta I_L \cdot (V_{in} + |V_{out}| + (Rdson_{sync} \cdot I_{out}) - (I_L \cdot Rdson_{main}))} \quad (5)$$

The typical choice for ΔI_L is 20 to 40 percent of (I_{out} + I_{in}) although the larger the inductor value the smaller the output voltage ripple of the converter with the same amount of output ESR. Current ripple can also considerably affect the current limit in some devices; this will be discussed further in this document. In most designs it is acceptable to use equation 4 for calculating the inductor value. Formula 5 is just a detailed equation that can be used as well to calculate inductance with switch losses included.

Output Capacitor selection

The desired output capacitor is chosen mainly for its ESR characteristics which dictate the amount of output voltage ripple ΔV_{out} the output of the converter will have.

The following formula calculates the amount of Equivalent Series Resistance (ESR) needed for a desired output voltage ripple. The ESR needs to be able to sustain a ripple current of the inductor peak current since the load sees a square pulse of current every cycle during when the inductor discharges.

$$ESR = \frac{\Delta V_{out}}{I_{L\ peak}} \quad (6)$$

There is also a need for a minimum output capacitance. This will ensure that the entire output voltage ripple is ESR related and not due to voltage drop due to lack of capacitance.

$$Cout = \frac{I_{Load} \cdot D}{f \cdot \Delta V_{out}} \quad (7)$$

Input capacitor selection

The input capacitor is selected mainly for its ESR characteristics which gives the input capacitor a high value of Root Mean Square (RMS) current rating. The RMS of the input current is approximated by the following formula.

$$RMS = \frac{I_{out}}{1-D} \cdot \sqrt{D \cdot (1-D)} \quad (8)$$

IC Device Ratings and considerations for the SP6652

There are several considerations that need to be addressed when choosing an IC, One is the maximum voltage under which the IC will be expected to operate; two is the current limit; and three is the maximum power dissipation of the device.

Due to the IC ground being tied to the output voltage of the system, the maximum voltage that the IC sees is:

$$V_{\max} = V_{in} + \left|V_{out}\right| \quad (9)$$

This tends to limit the total voltage range of V_{in}.

The other consideration is the current limit of the device. In the SP6652 the internal current limit sensed across the PMOS Main_FET of the device. The current limit has a typical value of 1.3A with the minimum value of 1.2A. During the design process a the minimum value for current limit needs to be used to assure that the device does not go into current limit before full load is achieved. The peak current seen across the PMOS FET is also the peak inductor current I_{Lpeak} which can be determined as follows:

$$I_{Lpeak} = I_L + \frac{\Delta I_L}{2} \quad (10)$$

This translates to

$$I_{Lpeak} = I_{in} + I_{out} + \frac{\Delta I_L}{2} \quad (11)$$

Because I_L has a duty cycle relationship to I_{out} -- making the effective I_{peak} current in the inductor equal to I_{out}+I_{in} plus the peak ripple -- there are times that this part will not be able to deliver the full output current of 1A as listed in the part description over the whole possible range of input and output voltages. The following graph gives output current verses duty cycle with some compensation for switch losses which affect the duty cycle.

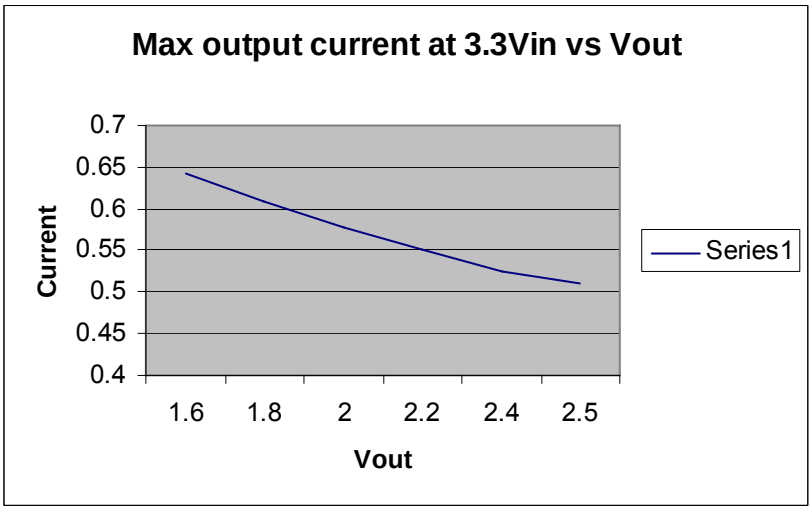


Figure 4

It might also be noted that because the current limit is fixed, it might be advantageous to use a smaller inductor value to get higher ripple current to limit the current in designs where the needed amount of output current is small. This will sacrifice some total efficiency of the system due to larger peak currents, but it

will limit the total amount of output current to a more reasonable level during fault conditions.

The last consideration is the total power dissipation of the IC. There are two components to the total power P_{total} dissipation of the IC. The first component is the power dissipated by the control logic of the Ic. The second component is the power dissipation of the actual switches. The following formula combines the two components for total power dissipation:

$$P_{total} = I_c \cdot V_{in} + \left(I_L{}^2 \cdot Rdson_{main} \cdot D\right) + \left(I_L{}^2 \cdot Rdson_{sync} \cdot 1 - D\right) \quad (12)$$

For the SP6652 application $Rdson_{main}$ and $Rdson_{sync}$ are both equal.

The P_{total} is an important first check to see if the Sp6652 can handle the total power dissipation over a wide temperature range without causing the IC to shut down due to the Thermal shutdown limit. It is important to note that this is only the first step and the temperature of the IC needs to be taken to verify the theoretical values since there can be a large variation in thermal performance due to layout and airflow conditions.

Efficiency

The efficiency of the system can be given by:

$$\eta = \frac{P_{in}}{P_{out}} \cdot 100 \quad (13)$$

The efficiency of the converter switches **only** is given by:

$$\eta_{converter\_switches} = \frac{V_{in} - I_L \cdot Rdson_{main}}{V_{out} + I_{Load} \cdot Rdson_{sync}} \cdot \frac{V_{out}}{V_{in}} \quad (14)$$

One thing to note that in this negative buck boost configuration, the duty cycle will have an effect on the efficiency of the converter more so than in a buck configuration. Another major loss in the circuit that contributes to the total efficiency of the system is the inductor resistance loss. In the end it is always better to measure the input and output power to get the best results for efficiency.

Design Example

The following is a design example with the SP6652 for a 3.3V to -1.8V out 500mA regulator.

A good starting point is to take ΔI_L to be .3 of I_L

$$D = \frac{|-1.8V|}{3.3V + |-1.8V|} \quad \text{From Equation 3}$$

$$D=.35$$

$$I_L = \frac{300mA}{1-.35} \text{ From Equation 2}$$

$$I_L=769mA$$

$$\Delta I_L = .4 \cdot I_L$$

$$\Delta I_L = 230mA$$

The Rdson of the FETs was taken from the data sheet.

$$L = \frac{V_{in} \cdot D}{f \cdot \Delta I_L} \quad (4)$$

$L = 3.58$ µH calculated, 4.2µH was chosen rated at 1.5A

Output Capacitor ESR Calculation

$$ESR = \frac{.02V}{..553A} \text{ From Equation 6}$$

ESR is 36mΩ

Minimum Capacitance

$$C_{out} = \frac{.5A \cdot .35}{1.4MHz \cdot .02V} \quad \text{From Equation 7}$$

$$C_{out}=6.25\mu F$$

Since you need about 10-22uF to get the proper ESR, the minimum capacitance requirement will be fulfilled due to ESR requirements.

The Input capacitor RMS current rating

$$RMS = \frac{500mA}{1-.35} \cdot \sqrt{.35 \cdot (1-.35)} \text{ From Equation 8}$$

RMS=.370 A

Total power dissipation of the IC

$$P_{total} = 1mA \cdot 5.1V + \left(.769^2 A \cdot .6\Omega \cdot .35\right) + \left(.769^2 A \cdot .6\Omega \cdot \left(1-.35\right)\right) \text{ From Equation 12}$$

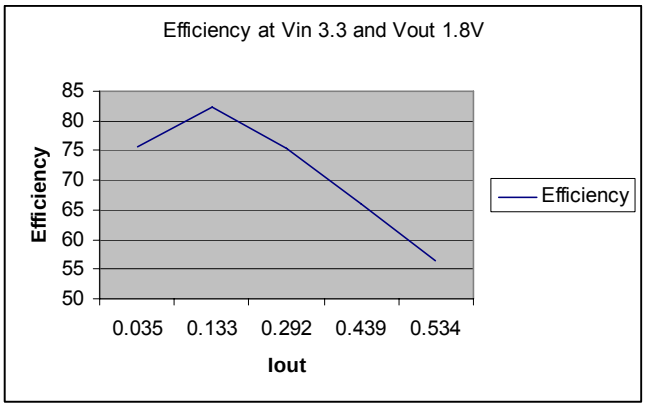
P_{total}=.355W

PCB Layout

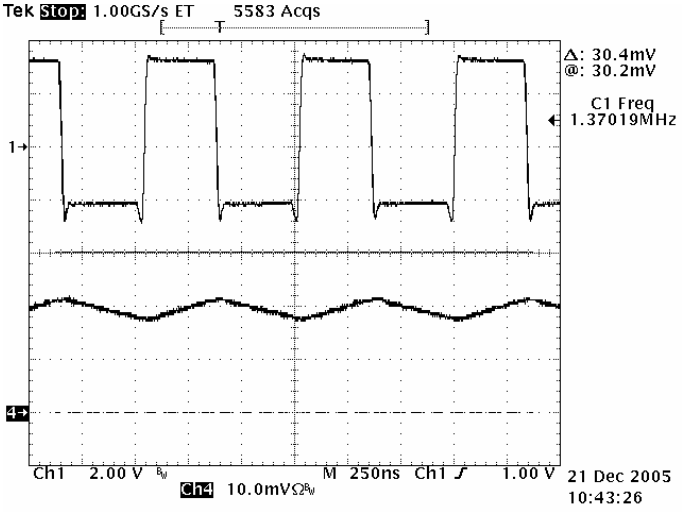
Special care needs to be taken when laying out the Printed Circuit Board for the SP6652. The input and output capacitors need to be as close as possible to the converter pins. There are also two grounds present on this IC. For the positive to negative converter, these grounds were tied together and the output capacitor was placed right at the output pins of the IC to GND to get best performance. If no special care is taken with layout noise, jitter can be present on the switch node with very little output current drawn by the load.

Test Data for above circuit design.

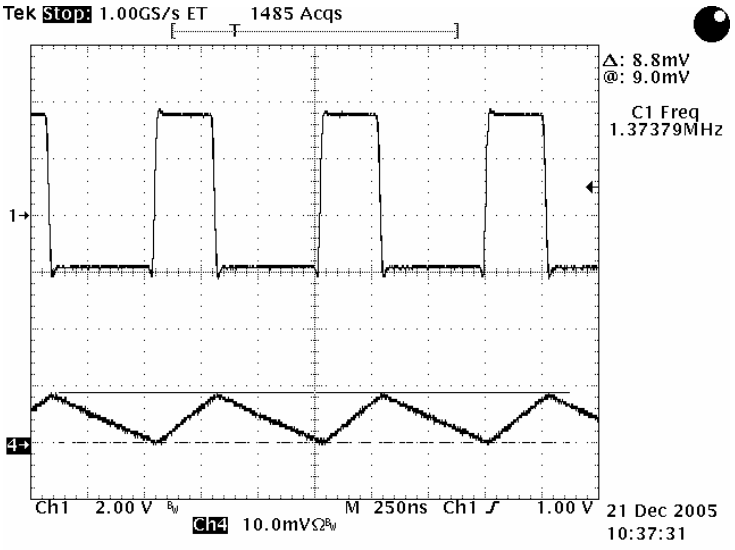
Efficiency of the Buck boost converter for 3.3V to 1.8Vout



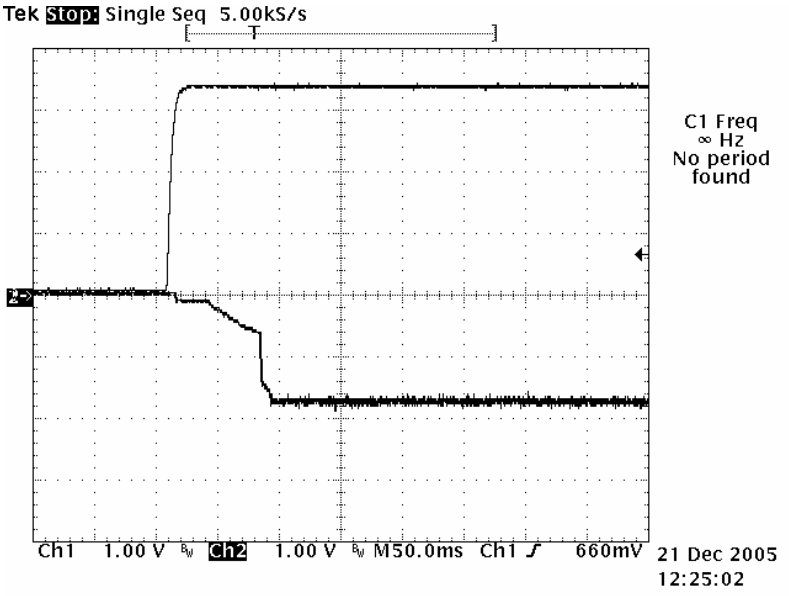
Typical wave forms for the SP6652



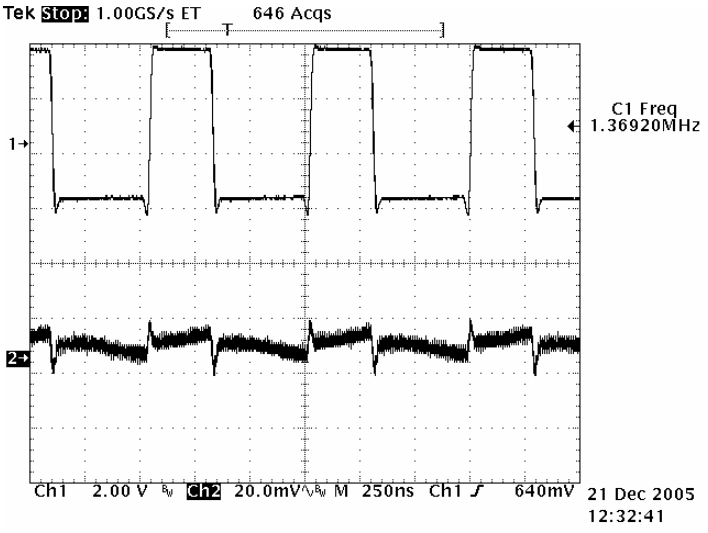
Channel 1 Switch node Channel 2 is Inductor Current I_L
I_{out} was 500mA Current setting is 500mA/Div



Channel 1 Switch node Channel 2 is Inductor Current I_L
I_{out} was 50mA Current setting is 200mA/Div



Startup characteristics of the SP6652



Channel 2 V_{out} ripple Channel 1 Switch Node
I_{out} 500mA

For further assistance:

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Live Technical Chat:	http://www.geolink-group.com/sipex/
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