Application Note ANP 16

Loop Compensation of Voltage-Mode Buck Converters

One major challenge in optimization of dc/dc power conversion solutions today is feedback loop compensation. To the laymen of dc/dc power conversion circuits, this concern can be not only difficult to understand, but a highly intimidating matter to deal with. Various effects of feedback loop stability occur with application of feedback compensation, which, if not properly calculated, can cause instability and regulation failure to occur. This application note helps to clarify the more advanced Type-III feedback loop compensation considerations in voltage-mode buck converter applications, which are viewed as inherently more stable when compared to current-mode conversion topologies.

Most designers believe the application of ceramic output capacitors is a good design decision, for both their low cost, abundance of suppliers, and the inherently low ESR. Ceramic capacitors are indeed a good choice for converter output filtering, where relatively low capacitance is required. Ceramic capacitors offer low Equivalent Series Resistance (ESR) that reduces output ripple. However, the inherently low ESR of the typical ceramic output capacitor necessitates the use of a Type-III compensation network. The Type-III compensation network, which is more complicated than Type-II, will be explained in the following text.

Buck Converter System Block Diagram

The system block diagram of a Buck-Converter is shown in figure 1 where V_{IN} and V_{OUT} are converter input and output voltage respectively. The Error Amplifier and its accompanying passive components comprise the compensation network (compensation). The focus of this application note is the proper selection of these passive components in order to meet compensation goals. Output of the compensation network is the analog control signal Vc. The Pulse-width-Modulator (Modulator) generates a duty-cycle D that is proportional to Vc. Duty-cycle control D of power switches in conjunction with the filter produce the desired voltage V_{OUT} from V_{IN}.

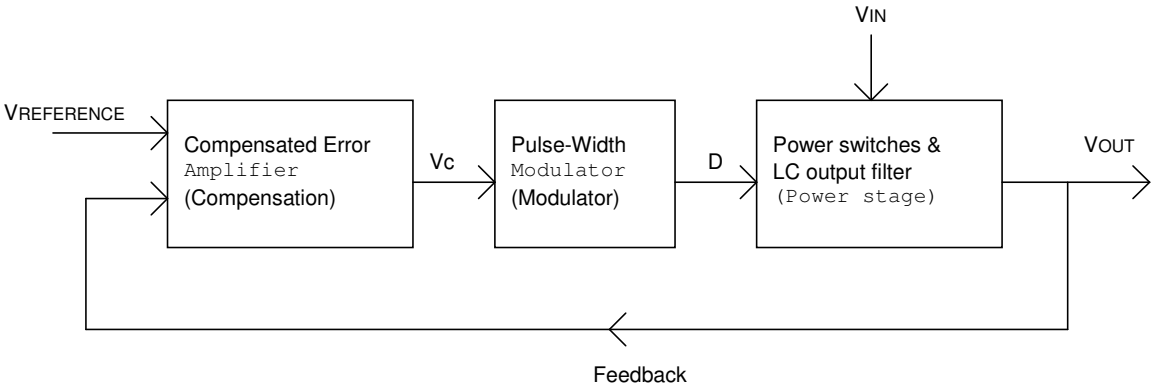

Figure 1. System Block Diagram of Buck-Converter

Open-Loop Response

System response from the input of the Modulator to the output of the power stage is called “Open-Loop Response”. It is shown in figure 2. The LC output filter gives rise to a “Double-Pole” that has a -180 degrees phase shift. Double-Pole frequency f_{LC} is given by:

$$fLC = \frac{1}{2\pi\sqrt{LC}} \quad \text{..... (1)}$$

The ESR of output capacitor C gives rise to a “ZERO” that has a +90 degree phase shift. ESR ZERO frequency f_{ESR} is given by:

$$fESR = \frac{1}{2\pi.C.ESR} \quad \text{..... (2)}$$

Figure 2 shows two plots. The top plot is representative of the Open-Loop gain and the lower plot shows the relevant phase. When the output capacitor is a small ceramic type, f_{ESR} can be significantly larger than f_{LC}. In this case, the phase of the open-loop reaches -180 degrees before the ESR Zero brings the phase to -90 degrees (see figure 2).

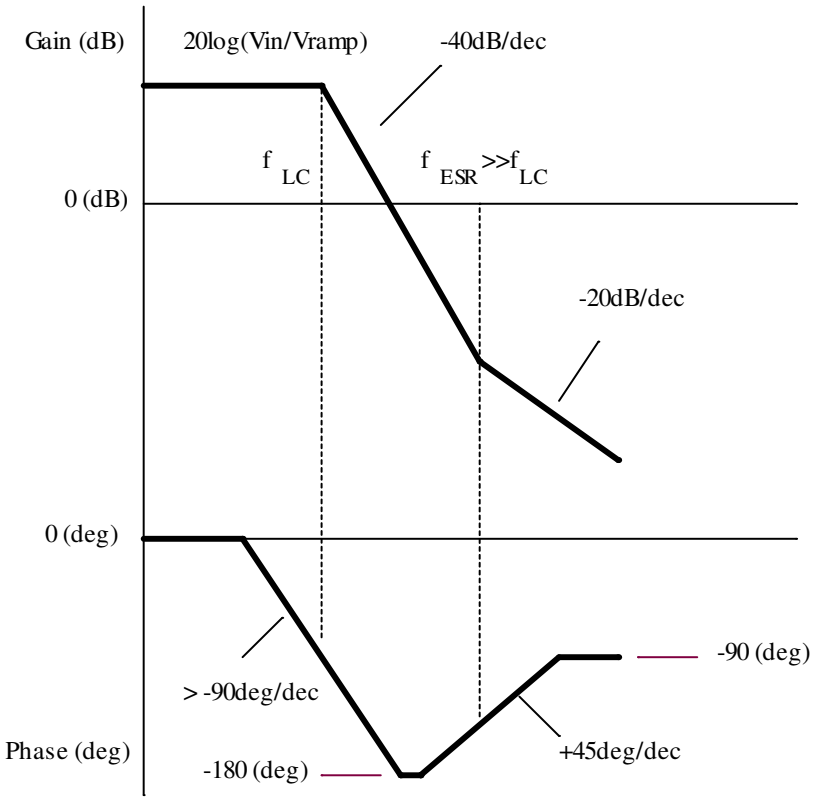

Figure 2. Gain/Phase of the Open-Loop Response with ceramic output capacitor

Goals of Compensation

The goal of compensation is to design a feedback system such that the converter will be stable and will quickly regulate the output against changes in input voltage or load conditions. Quick response requires that the Loop *0dB cross-over frequency* "fc" (also known as bandwidth) be as high as practical. In general, compensation is designed such that (fs/10)<fc<(fs/5); where fs is the switching frequency of the converter. Stability criterion requires that the **phase margin corresponding to "fc" be greater than 45 degree** where

Phase Margin = 180 degree + phase of Loop Gain

In essence we have to shape the Gain/Phase of the Error Amplifier such that when combined with Gain/Phase of the Open-Loop of figure 2 it satisfies the above requirements.

Type-III Compensation

Type-III compensation is realized by connecting resistors/capacitors to a controller's integral Error Amplifier as shown in figure 3. A nomenclature consistent with Sipex datasheet is used. Transfer function of Type-III has two "Zeros" and two "Poles" at the frequencies shown in figure 3. The combined effect of the Zeros results in a 180 degree phase boost. This phase boost is necessary to counter the 180 degree phase lag due to the output filter double-Pole shown in figure 2 and generate the required phase margin. In order to simplify the solution for the frequency of the 2nd Zero and 1st Pole, components must be chosen so that CZ2>>CP1 and R1>>RZ3. Further simplification can be made by making the frequency of the two Zeros coincide. As stated above, the goal is to locate the Poles and Zeros of the compensation such that the desired crossover frequency and corresponding phase margin is obtained.

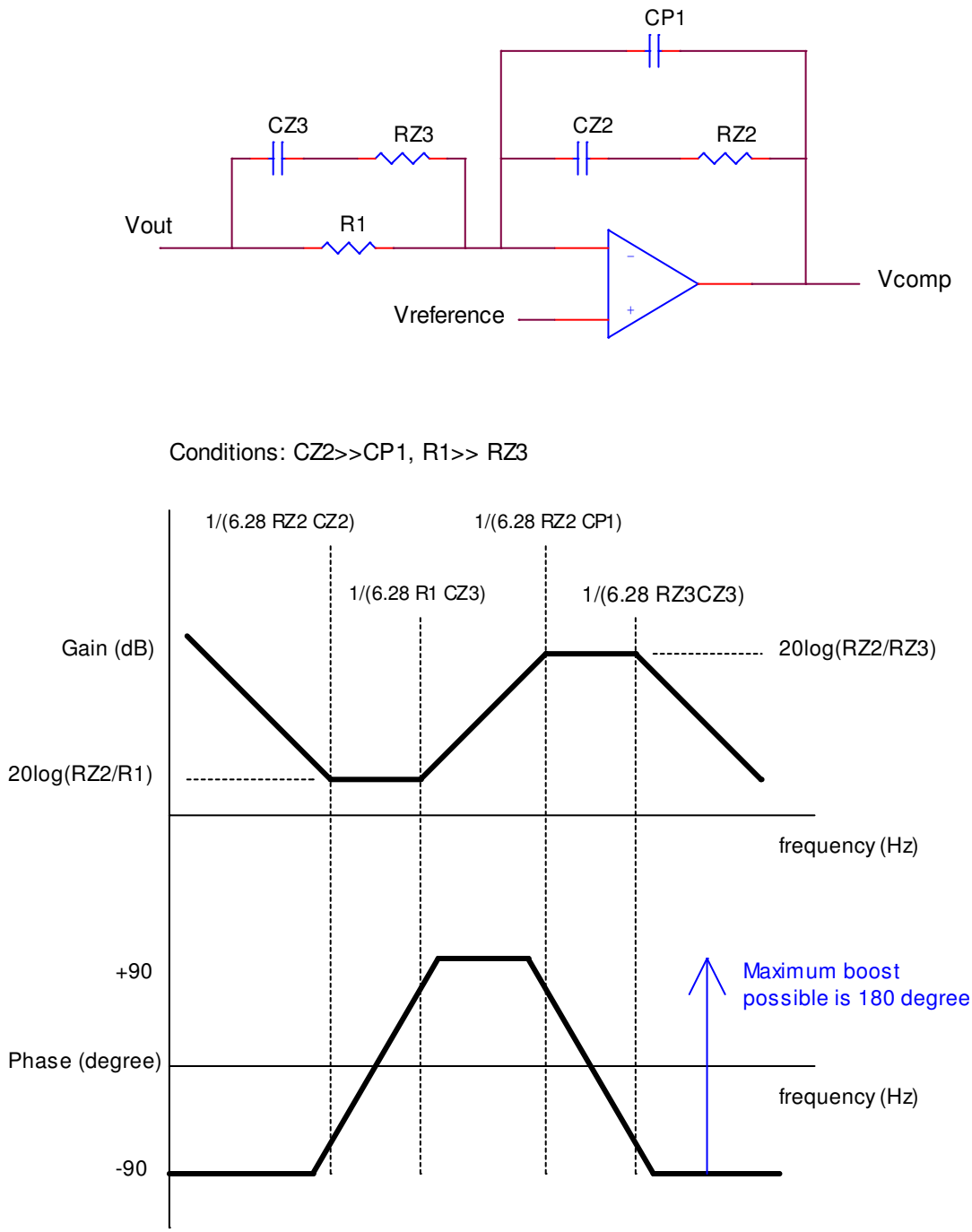

Figure 3. Type-III compensation and its associated gain/phase plots.

Six resistors and capacitors, when connected to the Error Amplifier as shown, create a type-III compensation network. Component nomenclature is the same as commonly used in Sipex datasheets. The frequency of the second “Zero” and first “Pole” are simplified solutions based on choosing CZ2>>CP1, R1>>RZ3.

Procedure for Calculating Type-III Components

As was mentioned, when a ceramic output capacitor is applied, the open loop phase usually drops to -180 degrees or close to it. In order to achieve the required phase margin of 45 degrees or greater (i.e., phase greater than -135 degrees), a type-III compensation is needed to provide sufficient phase boost. Let's assume that the phase of open-loop system gain is the lowest possible, i.e., 180 degrees. To get the minimum required closed-loop phase-margin of 45 degrees the compensation must provide a +45 degree phase margin (i.e., a boost of 95 degrees). In order to maximize the boost, Poles and Zeros must be placed as far apart as possible. We can now outline a step-by-step procedure for calculating component values, as follows:

1.) Let R1=68.1kΩ. This value generally provides a satisfactory solution and helps meet the requirement R1>>RZ3

2.) Place the second Zero at 60% of output filter's double-Pole frequency and solve for CZ3:

$$CZ3 = \frac{1}{zsf \bullet R1 \bullet \frac{1}{\sqrt{LC}}} \quad \text{..... (3)}$$

Where
L and C are output inductance and capacitance respectively
zsf is Zero scale factor = 0.6

3.) To set fc to the desired value use the following equation and calculate RZ2 from:

$$RZ2 = \frac{\left(2 \bullet \pi \bullet fc\right)^2 \bullet L \bullet C + 1}{2 \bullet \pi \bullet fc \bullet CZ3} x \frac{Vramp}{Vin} \quad \text{..... (4)}$$

Where
V_{RAMP} is the ramp amplitude and V_{IN} is converter's input voltage
f_c is typically set at 1/5 to 1/10 of switching frequency f_s

4.) Set the first Zero to coincide with the second Zero and calculate CZ2 from:

$$CZ2 = \frac{1}{zsf \bullet RZ2 \bullet \frac{1}{\sqrt{LC}}} \quad \text{..... (5)}$$

5.) Set the first Pole at switching frequency of the converter f_s and solve for CP1:

$$CP1 = \frac{1}{2 \bullet \pi \bullet RZ2 \bullet fs} \quad \text{..... (6)}$$

6.) Set the second Pole also at f_s and solve for RZ3:

$$RZ3 = \frac{1}{2 \bullet \pi \bullet CZ3 \bullet fs} \quad \text{..... (7)}$$

Example 1.) Design compensation for a Buck converter with following specification:

V_{IN} = 12V
V_{RAMP} = 1.1V
f_S = 900kHz
L = 2.2uH
C = 22uF
ESR = 3mΩ

Note: Loop Compensation component calculations discussed in this application note can be quickly iterated with the Type III Loop Compensation Calculator on the web at: www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

f_{LC} and f_{ESR} (calculated from 1 and 2 above) are 22.9kHz and 2.4MHz respectively. Since f_{ESR}/f_{LC}=105, clearly Type-III compensation has to be used.

Following the above procedure and letting fc=fs/9, we get:
R1 = 68.1kΩ
CZ3 = 170pF
RZ2 = 17.2kΩ
CZ2 = 673pF
CP1 = 10.2pF
RZ3 = 1.04kΩ

Figure 4 plots the actual SPICE simulation supporting these correct values for the Type-III compensation network.

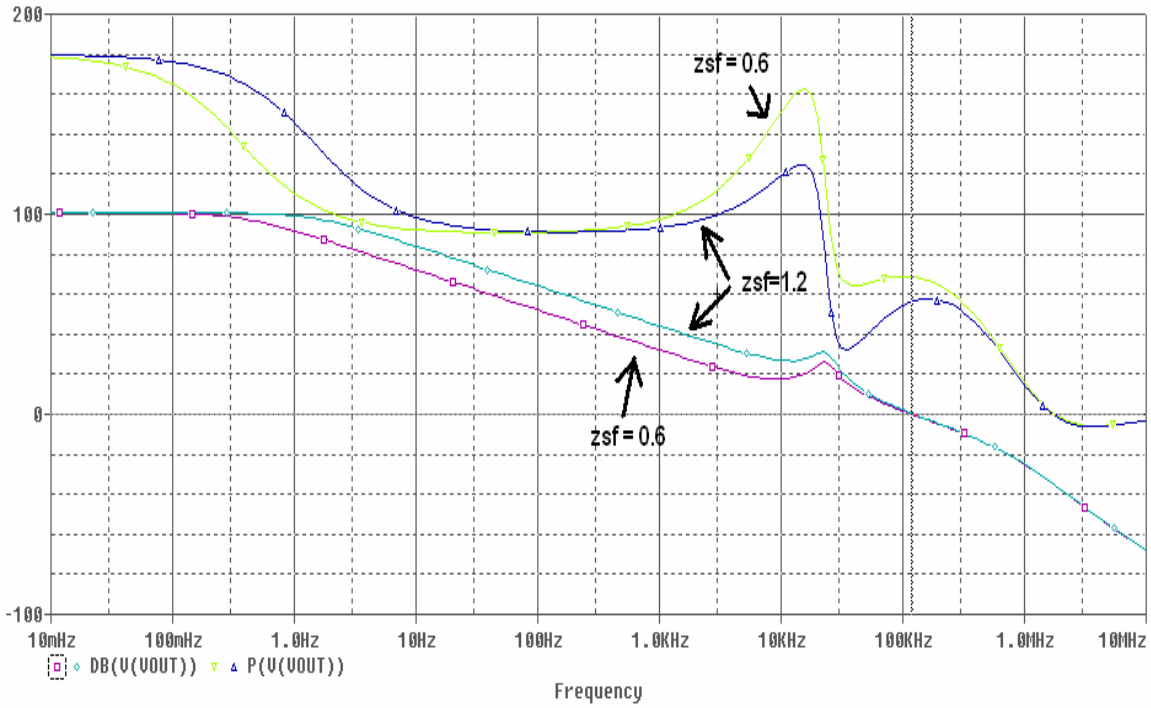

Figure 4. Spice simulation showing gain/phase for zsf=0.6, cross-over frequency *fc* is just over 100kHz and corresponding phase margin is 70 degrees

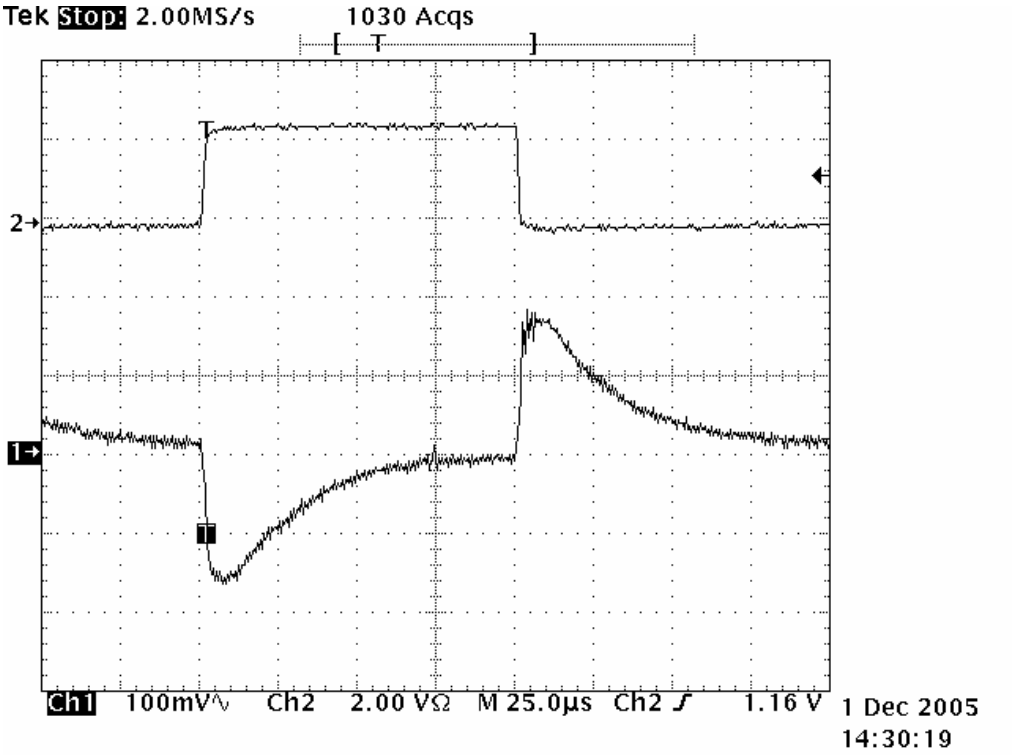

Figure 5. Step load response corresponding to conservative compensation, 0A-2.5A, transient response is 75us

Practical Considerations (adjusting system response)

A key starting point of the above procedure is locating the Zeros at 60% of f_{LC} (i.e.,zsf=0.6). This, in general, provides a conservative solution. As seen in figure 4, the phase margin of nearly 70 degrees is quite acceptable. However the tradeoff between system response and system stability apply. As seen in figure 5, the transient response is about 75us, not impressive for a 900kHz converter. For a more aggressive compensation (i.e., faster transient response) locate the Zeros closer to, or slightly above f_{LC} (i.e., zsf $\geq$ f_{LC}). For instance if it is desired to get a faster response for design example 1, let zsf=1.2. Recalculating components for Example 1 we get:

R1 = 68.1kΩ
CZ3 = 85pF
RZ2 = 34.4kΩ
CZ2 = 168pF
CP1 = 5pF
RZ3 = 2.08kΩ

Gain/phase for zsf=1.2 are shown in figure 4 and compared to the original solution. As can be seen, mid-frequency gain is increased by 10dB and phase margin has decreased 10 degrees with a minimum phase of about 30 degrees. Step load response is shown in figure 6. As seen, the response time has been reduced (improved) to a much faster 20us.

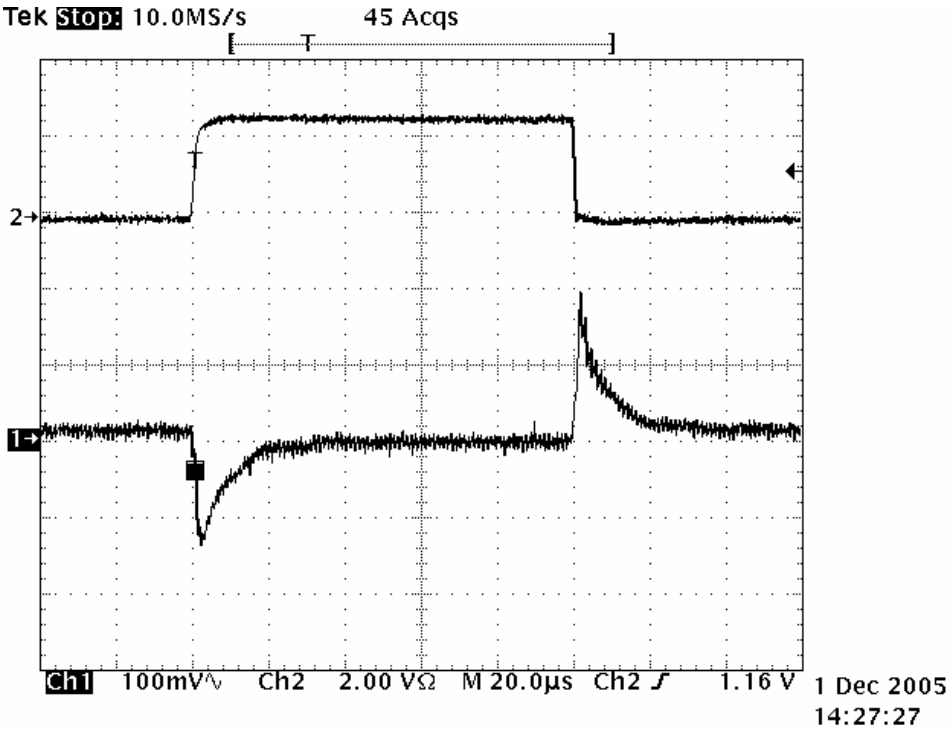

Figure 6. Step load response corresponding to aggressive compensation, transient response has been reduced (improved) to 20us

Part number	Ramp amplitude (V)
SP6132/H	1.1
SP6133	1.0
SP6134/H	1.1
SP6136	1.0
SP6137	1.1
SP6138	1.0
SP6139	1.1

Figure 7- Ramp amplitude of Sipex controllers

Conclusion

With half a dozen simple, low-cost discrete components, and some creative 'positioning', Type-III compensation can greatly improve circuit response while maintaining loop stability. The best part of this compensation case is the allowed use of low cost ceramic output capacitors for the solution.

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Live Technical Chat:	http://www.geolink-group.com/sipex/
Type III Loop Compensation Calculator:	www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

