Current Mode Compensation Techniques

April 2013 Rev. 1.0.0

APPLICATION NOTE

GENERAL DESCRIPTION

This application note shows an analysis of the XRP7664 gain blocks with specific information on selecting the frequency compensation component values. A key item of note is that the ESR of output capacitors creates a zero in the loop response that can affect stability. The application circuits shown in the datasheets (Figure 1), along with the design information given, show a typical application using ceramic capacitors. Ceramic capacitors have a very low ESR so the ESR zero with ceramics is usually at a high enough frequency that it doesn't adversely affect the stability. Other types of capacitors, such as aluminum and tantalum types, can have notably higher ESR, which, in conjunction with their higher capacitance, can result in the ESR zero being at a low enough frequency to affect the loop.

This application note also applies to the XRP7665, XRP7674, and XRP7675 specifically but can also provide understanding in compensating any current mode buck DC/DC.

FEATURES

- **This application note applies to the XRP7664, XRP7665, XRP7674 and XRP7675 products**
- **Shows the internal gain blocks of the device**
- **Analysis the total loop including external components**
- **Address the effect of using large output capacitor values with large ESR**
- **Gives a specific procedure for compensating a design using the Bode plot method**
- **Graphing templates, Figure 6 and Figure 7, for manual drawing the Bode plots.**

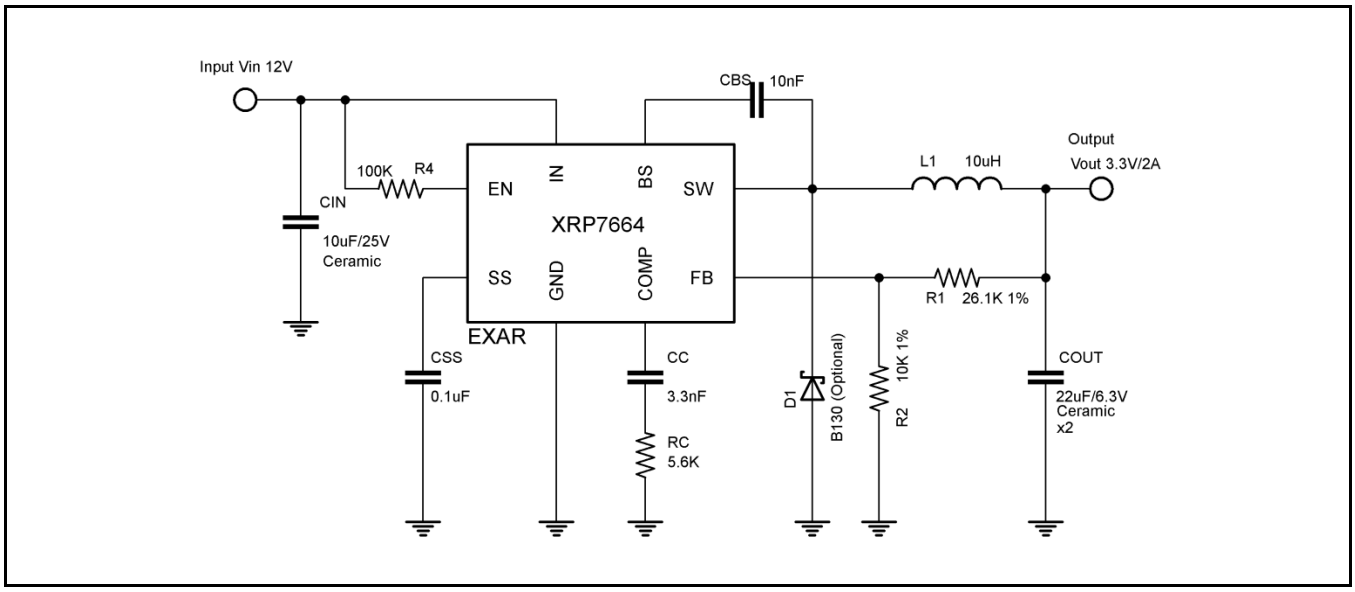

Figure 1: Datasheet Application Circuit

OVERVIEW OF THE XRP7764 FUNCTION

INTERNAL GAIN BLOCK DIAGRAM

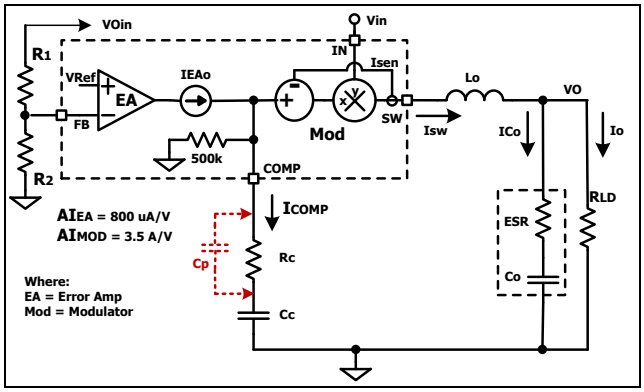

Figure 2: Internal Gain Blocks

Figure 2 shows a diagram of the XRP7664 internal gain blocks. The total loop includes the feedback divider (DIV) created by R1 and R2, Error Amp (EA), Modular (MOD), and output filter. Since the error amp is a transconductance amplifier its output voltage will be a function of IEAo and the impedance from its output to ground. Please note that this includes its internal 500kΩ (R_{LIM}) impedance.

Additionally, since the modulator is current mode control, its output current (Isw) is proportional to in input control voltage. Current mode control, under most operating conditions, effectively removes the effect of the output inductor from the filter equation and results in the output voltage (Vo) being a function of Isw times the output impedance from Vo to ground.

TERMS USED

The following terms are used in the figures and throughout this application note. The values used in this document should reflect those shown in the datasheet. In any case where they don't agree, the information in the datasheet shall be deemed correct.

- AIEA = EA Transconductance
- AIMOD = MOD Transconductance
- AV_{DIV} = Feedback Voltage Divider
- AVEA = EA Voltage Gain
- AVMOD = MOD Voltage Gain
- Cc = Compensation Capacitor
- Co = Output Capacitor
- Cp = Additional Pole Capacitor
- EA = Error Amp
- ESR = Output Capacitor ESR
- GEA = Error Amp Gain in dB
- GMOD = MOD Gain in dB
- Lo = Output Inductor
- MOD = Modulator
- Rc = Compensation Resistor
- RLD = External Load Resistance
- VCOMP = Error Amp Output
- VFB = Feedback Input Voltage
- Vo = Output Voltage
- Vref = Internal Reference Voltage

QUICK COMPENSATION PROCEDURE

The values required for the compensation will depend on the output filter and the selected cross over frequency. For most designs that use ceramic output capacitors, the addition of Cp across Rc will not be necessary, but if a high value of output capacitance, in conjunction with a high ESR, is used for Co, the additional pole created by Cp may be required for stability. In all cases bode plot drawings should be made during the design and Gain/Phase measurements should be done on the final product.

The design example used here is for a XRP7664. This procedure, however, also applies to the other devices listed in the Features section on page 1. Be sure to use the correct datasheet values for the particular device.

- Vout = 3.3V
- $I_{LD\ Max}$ = 2A
- Co = 1200µF
- ESR = 0.01Ω
- R_{LIM} = 500kΩ
- AI_{EA} = 800µA/V (From Datasheet)
- AV_{EA}= 400V/V (From Datasheet)
- AI_{MOD} = 3.5A/V (From Datasheet)
- Fco = 10kHz
- Vref = 0.925V

Unless otherwise stated: Current is in Amps, Voltage is in Volts, Resistance in Ohms, Capacitance in Farad, and Frequency in Hertz.

1. Select the crossover frequency

Select the frequency where the loop gain should cross 0dB. Typically the crossover frequency (Fco) should be around 5% to 10% of the 350kHz switching frequency. For this example we are using 10kHz.

2. Calculate the total DC gain of the loop

There are three main DC gain blocks in the loop;

AV_{DIV}, The input voltage divider made up of R1 and R2. The gain of this block is:

$$AV_{DIV} = \frac{V_{Ref}}{Vo} = 0.28$$

AV_{EA}, The Error Amp DC Gain is the gain from the datasheet or 400V/V.

$$AV_{EA} = 400$$

AV_{MOD}, The Modulator gain can be calculated from the modulator transconductance of 3.5 and the output load resistance at maximum load current.

$$R_{LD} = \frac{Vo}{I_{LD}} = \frac{3.3}{2} = 1.65$$

$$AV_{MODdc} = AI_{MOD} \cdot R_{LD}$$

$$AV_{MOD} = 3.5 \cdot 1.65 = 5.775$$

The total DC Gain of the loop is the sum of the three blocks.

$$AV_{TOTdc} := AV_{FB} \cdot AV_{EA} \cdot AV_{MOD}$$

$$AV_{TOTdc} = 0.3 \cdot 400 \cdot 5.775 = 647.5$$

The total gain in dB is.

$$G_{TOTdc} := 20 \cdot \log\left(AV_{TOTdc}\right)$$

$$G_{TOTdc} = 56.2$$

3. Determine the error amp pole frequency for the Fco chosen

Divide Fco by the total DC gain to get the pole frequency that needs to be created set Fco.

$$FP_{CO} := \frac{F_{CO}}{AV_{TOTdc}} \qquad FP_{CO} = 15.444$$

4. Find the Pole and Zero of the output filter at full load.

$$FP_o := \frac{1}{2 \cdot \pi \cdot C_o \cdot \left(R_{LD} + ESR\right)}$$

$$FP_o = 79.897$$

$$FZ_o := \frac{1}{2 \cdot \pi \cdot C_o \cdot ESR}$$

$$FZ_o = 13.263 \cdot k$$

5. Compensating the design

Set the EA poles and the EA zero at the following frequencies.

$$FP_{EA1} := FP_{CO}$$

$$FP_{EA2} := FZ_o$$

$$FZ_{EA} := FP_o$$

Now calculate the compensation component values.

$$R_C := R_{LIM} \cdot \frac{FP_{EA1}}{FZ_{EA} - FP_{EA1}}$$

$$R_C = 120k$$

$$C_c := \frac{1}{2 \cdot \pi \cdot FZ_{EA} \cdot R_C}$$

$$C_c = 16.6n$$

$$C_P := \frac{R_C + R_{LIM}}{2 \cdot \pi \cdot FP_{EA2} \cdot R_C \cdot R_{LIM}}$$

$$C_P = 124p$$

6. Creating a Bode Gain/Phase plot

Gathering together the key parameters gives.

Component Values

Cc = 16nF

Rc = 120kΩ

Cp = 100pF

Compensation Data

G_{TOTdc} = 57dB

FPo = 80Hz

FZo = 13.3kHz

FP_{EA1} = 14Hz

FP_{EA2} = 13.3kHz

FZ_{EA} = 80Hz

7. Do a Bode Gain/Phase plot to ensure stability

This can be done either manually using semi-log graph paper, or automatically using a Bode plot tool.

Figure 4 and Figure 5, show Gain and Phase plots of the example given. These were drawn manually to show the technique as shown below.

Plotting Manually the Gain, Figure 4

On the gain graph draw a horizontal line at 57 dB from 1Hz to 100kHz to represent the DC gain.

Move left to right along the 0 dB line until you reach a pole or zero frequency and put a point on the 0dB line at that frequency.

If the frequency is pole, draw a line from that point toward the right that decrease with a slope of -20dB per decade and if the frequency is a zero, draw a line from that point toward the right that increases with a slope of -20dB per decade.

Continue until all poles and zeros have been drawn.

Now put points at each pole and zero frequency that equal the sum of the DC gain and gains for each pole and zero at that frequency. Once this is done connect all the points with straight lines.

This is the gain versus frequency response for the total loop.

Plotting the Phase, Figure 5

On the phase graph, at each pole and zero frequency, put a point on the graph as follows.

If the frequency is a pole put a point at that frequency at -45 degrees.

Then draw a line that starts at 0 degrees, one decade below the pole frequency, goes through the -45 degree point, and ends at -90 degrees one decade above the pole frequency.

Now complete the plot for that pole by drawing a horizontal line from the -90 degrees point to the end of the graph on the right and from the 0 degree point to the end of the graph on the left.

If the frequency is a zero put a point at that frequency at +45 degrees.

Then draw a line that starts at 0 degrees, one decade below the pole frequency, goes through the +45 degree point, and ends at +90 degrees one decade above the pole frequency.

Now complete the plot for that zero by drawing a horizontal line from the +90 degrees point to the end of the graph on the right and from the 0 degree point to the end of the graph at the left.

Repeat the above for every pole and zero.

Once this is done identify each frequency where a pole's or zero's phase reaches 0, -90 and +90 degrees. Then at each of these frequencies add up all the phase values and put a point on the graph.

The phase margin for the full loop can now be plotted by drawing straight lines between these points.

Stability Criteria

There two main stability criteria for a stable power supply loop. One is Gain Margin and the other is Phase Margin.

The gain margin is defined as the gain of the loop at the frequency above F_{CO} that the phase crosses -180 degrees. Look at phase plot to see if the phase goes below -180 degrees. If it does look at that frequency on the gain plot to make sure that the loop has negative gain. The gain should be at least below -10 dB and preferably below -20 dB.

The phase margin is defined at the F_{CO} frequency where the gain crosses 0 dB. The phase margin is the difference between the loop phase and -180 degrees at this frequency.

For a robust design the phase margin should be at least 45 degrees. A simple way to check this is to take the loop phase value at F_{CO} and add +180 degree. For example if the phase value at F_{CO} was -120 degrees then the loop phase margin would be 180 + (-120) = 60 degrees.

Simulation Circuit

Below is a circuit that can be used to plot the Gain/Phase using a spice type simulator.

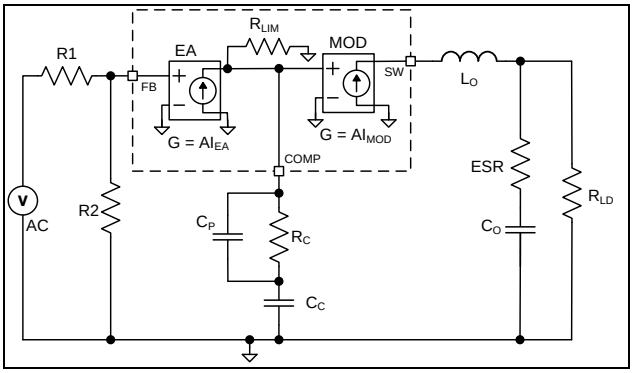

Figure 3: Simulation Model

GAIN/PHASE PLOTS OF THE EXAMPLE DESIGN

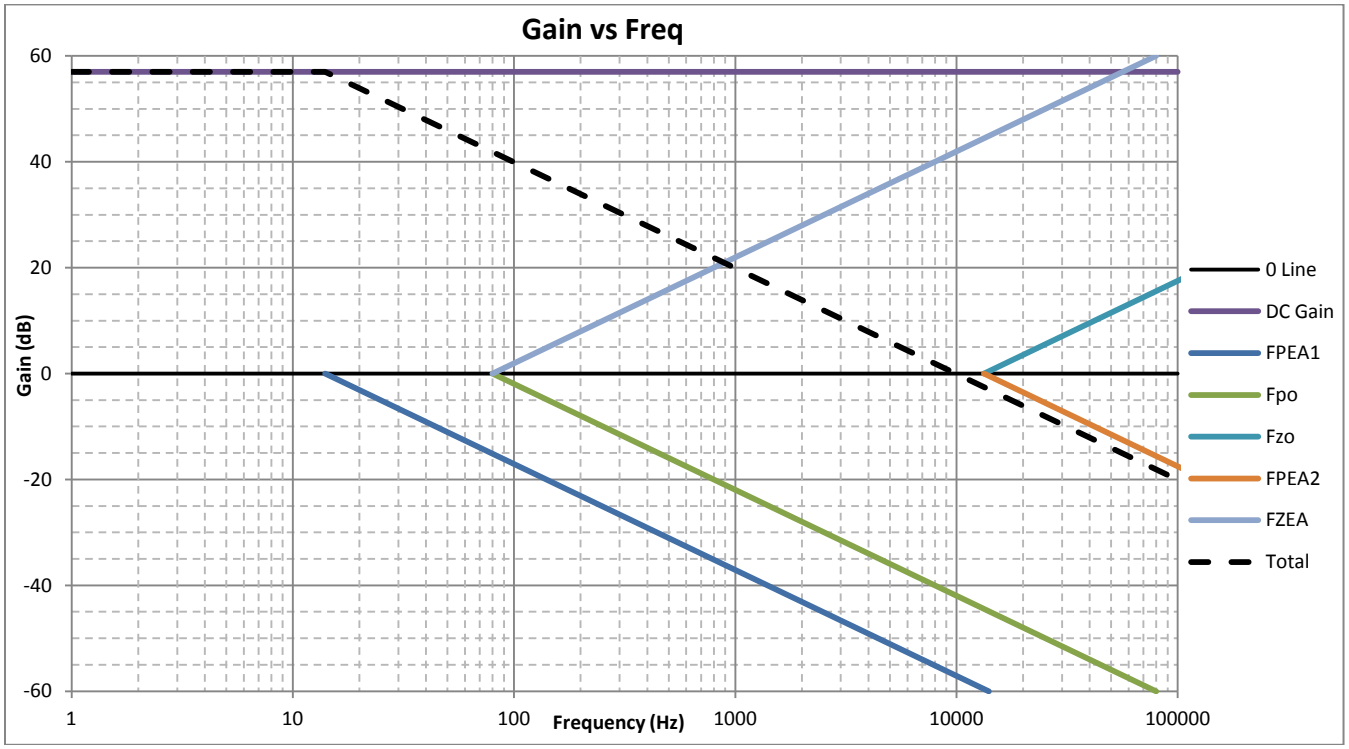

Figure 4: Gain Plots of Example

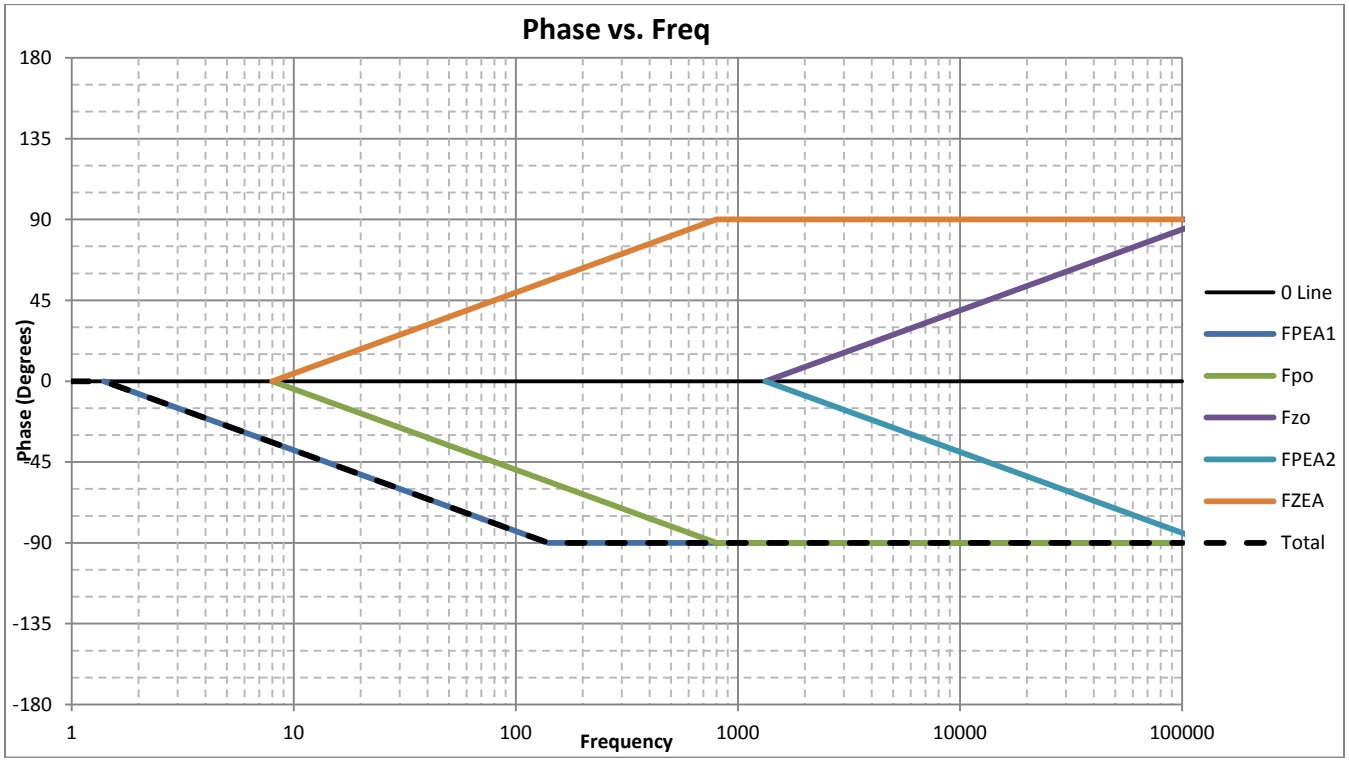

Figure 5: Phase Plots of Example

GRAPHING PAPER

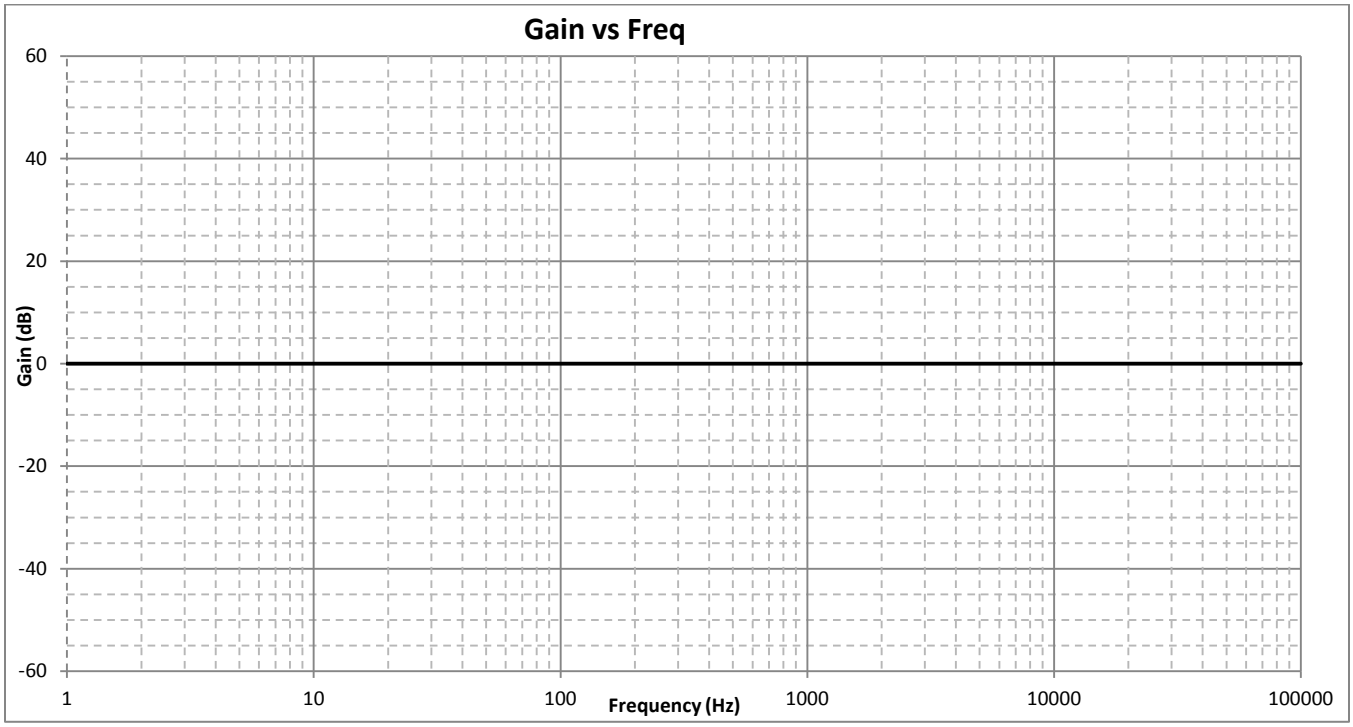

Figure 6: Gain Graphing Paper

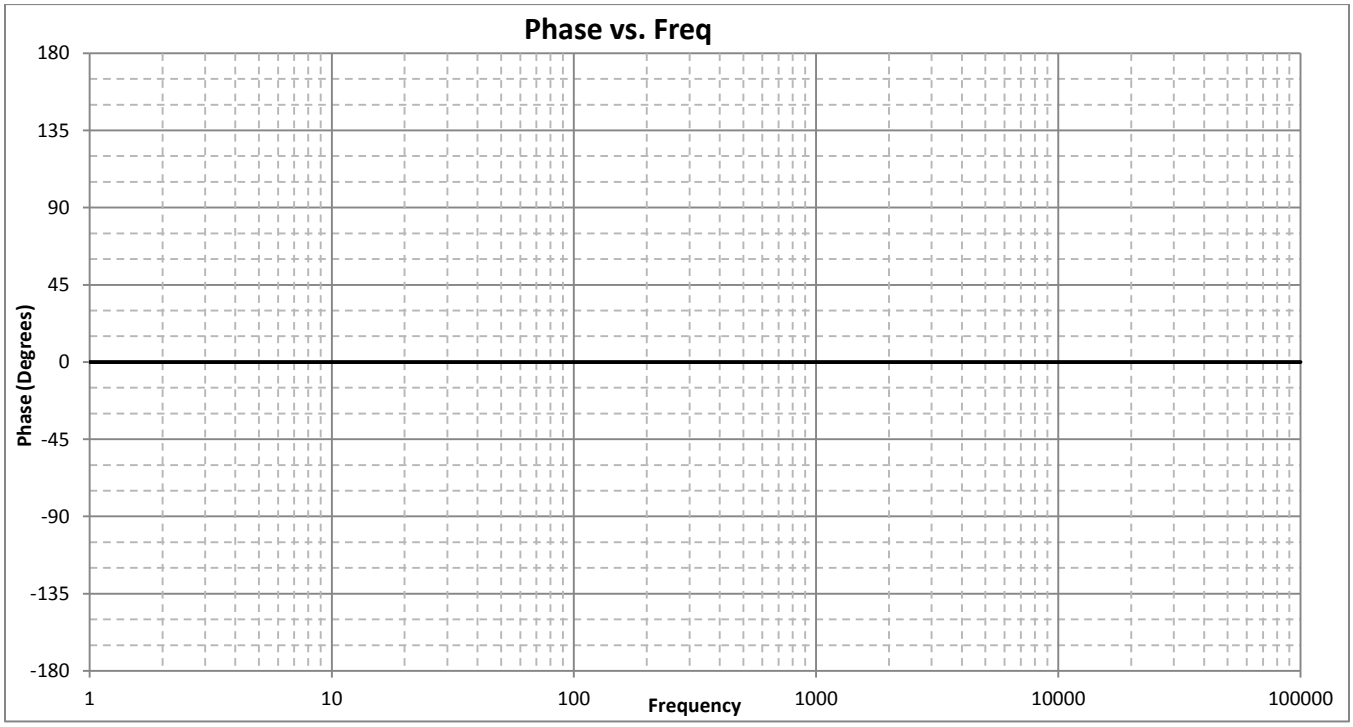

Figure 7: Phase Graphing Paper

APPENDIX

DETAILED FREQUENCY ANALYSIS

The following is a detailed analysis of the loop gain. The analysis is applicable to all the XRP devices listed in the Feature section on page 1.

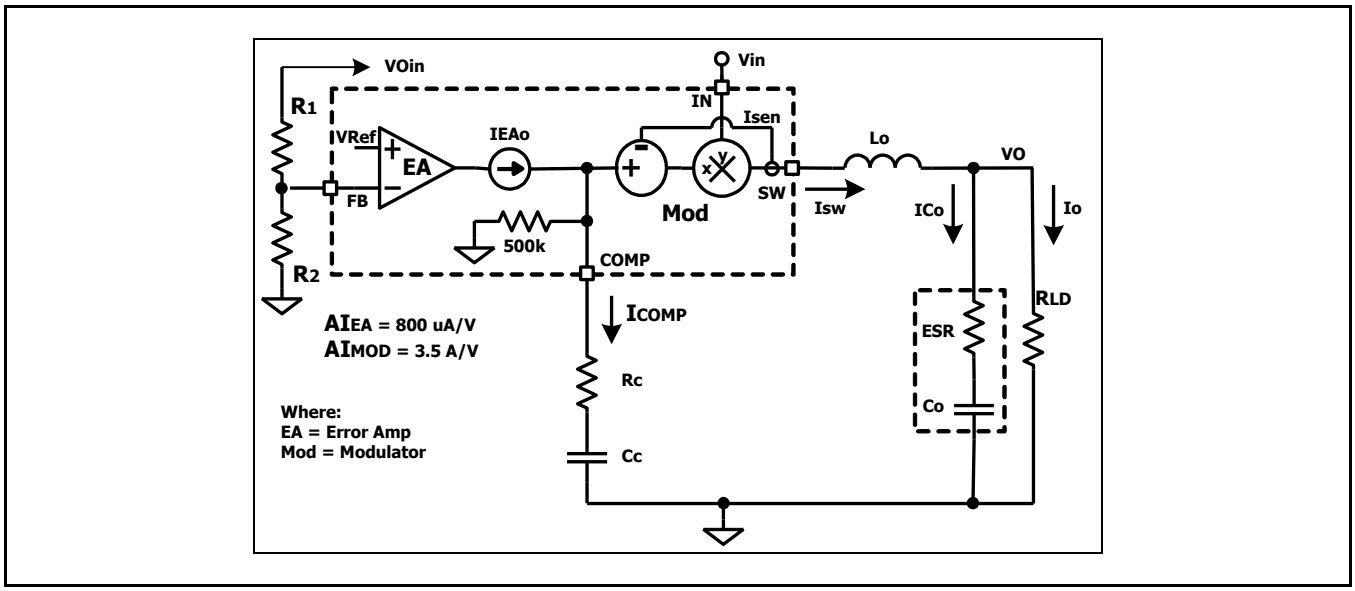

Fig. A1: Circuit Diagram

Where:

AIEA = EA Transconductance

AIMOD = MOD Transconductance

AV_{DIV} = Feedback Voltage Divider

AVEA = EA Voltage Gain

AVMOD = MOD Voltage Gain

Cc = Compensation Capacitor

Co = Output Capacitor

EA = Error Amp

ESR = Output Capacitor ESR

GEA = Error Amp Gain in dB

GMOD = MOD Gain in dB

Lo = Output Inductor

MOD = Modulator

Rc = Compensation Resistor

RLD = External Load Resistance

VCOMP = Error Amp Output

VFB = Feedback Input Voltage

Vo = Output Voltage

Vref = Internal Reference Voltage

XRP7664 Internal Gain Block Diagram

Figure A1 shows a diagram of the XRP7664 internal gain blocks. The total loop includes the feedback divider, Error Amp (EA), Modular (MOD), and Output filter. Since the error amp is a transconductance amplifier its output voltage will be a function of IEAo and the impedance from its output to ground. Please note that this includes its internal 500kΩ impedance.

Additionally, since the modulator is current mode control, its output current (Isw) is proportional to in input control voltage. Current mode control, under most operating conditions, effectively

removes the effect of the output inductor from the filter equation and results in the output voltage (Vo) being a function of Isw times the output impedance from Vo to ground.

Analysis of the open loop gain

Tracing the voltages from the output back to the input gives:

Eq. 1: $$Vo = I_{SW} \cdot Z_{VO}$$

Eq. 2: $$I_{SW} = AI_{mod} \cdot V_{comp}$$

Eq. 3: $$V_{COMP} = I_{EAo} \cdot Z_{EAo}$$

Eq. 4: $$I_{EAo} = AI_{EA} \cdot V_{FB}$$

Eq. 5: $$V_{FB} = A_{DIV} \cdot V_{Oin}$$

The Transfer Function of the total loop is:

Eq. 6: $$V_O = Z_{VO} \cdot AI_{MOD} \cdot AI_{EA} \cdot Z_{EAo} \cdot A_{DIV} \cdot V_{Oin}$$

The total loop gain is:

Eq. 7: $$AV_{LOOP} = \frac{V_O}{V_{Oin}} = Z_{VO} \cdot AI_{MOD} \cdot AI_{EA} \cdot Z_{EAo} \cdot A_{DIV}$$

Now let's explore the individual blocks.

Modulator and Output Filter Blocks

The modulator voltage gain, AVMOD, is a function of its specified transconductance and the impedance of the output filter. Since the modulator uses Current Mode Control, its output is a controlled current source. It therefore controls the current flowing in the output inductor (Lo). This effectively removes the output inductance (Lo) from loop equation.

The gain of the modulator is calculated as follows:

Eq. 8: $$AV_{MOD} = AI_{MOD} \cdot Z_{VO}$$

ZVO is the parallel combination of $R_{LD}||(Z_{Co}+ESR)$ so:

Eq. 9: $$Z_{VO} = R_{LD} \cdot \frac{(Z_{Co} + ESR)}{R_{LD} + Z_{CO} + ESR}$$

Eq. 10:
$$AV_{MOD} = AI_{MOD} \cdot R_{LD} \cdot \frac{(Z_{Co} + ESR)}{R_{LD} + Z_{CO} + ESR}$$

The modulator gain can be separated into two components; DC and AC.

Eq. 11:
$$AV_{MODdc} = AI_{MOD} \cdot R_{LD}$$

Eq. 12a:
$$AV_{MODac} = \frac{(Z_{Co} + ESR)}{R_{LD} + Z_{CO} + ESR} = \frac{s \cdot C_o \cdot ESR + 1}{s \cdot C_o \cdot (R_{LD} + ESR) + 1}$$ Eq. 12b

Error Amplifier Block

The Error Amp is also a transconductance amplifier and its voltage gain is a function of its output impedance. AV_{EA} is calculated similar to the Modulator.

Eq. 13:
$$AV_{EA} = AI_{EA} \cdot Z_{EAo}$$

The output impedance of Z_{EAo} is the parallel combination of RLIM||(ZCc+RC)

Eq. 14:
$$Z_{EAo} = R_{LIM} \cdot \frac{(Z_{Cc} + R_C)}{R_{LIM} + Z_{Cc} + R_C}$$

Eq. 15:
$$AV_{EA} = AI_{MOD} \cdot R_{LIM} \cdot \frac{(Z_{Cc} + R_C)}{R_{LIM} + Z_{Cc} + R_C}$$

The error amp gain can also be separated into DC and AC components.

Eq. 16
$$AV_{EAdc} = AI_{EA} \cdot R_{LIM}$$

Eq. 17a:
$$AV_{EAac} = \frac{(Z_{Cc} + R_C)}{R_{LIM} + Z_{Cc} + R_C} = \frac{s \cdot C_C \cdot R_c + 1}{s \cdot C_c \cdot (R_{LIM} + R_C) + 1}$$ Eq. 17b

Feedback Divider Block

The final gain block in the loop is the feedback voltage divider which sets the output voltage by dropping the output voltage down to the error amp reference voltage level. Since there are no reactive components in the divider, the gain of this block is DC with no AC component:

Eq. 18a:
$$A_{DIVdc} = \frac{R2}{R1 + R2} = \frac{V_{Ref}}{V_O}$$ Eq. 18b

Putting it all together

Rewriting the loop gain, along with separating and grouping the DC and AC gains, gives:

Eq. 19 $$AV_{LOOP} = AV_{DIV} \cdot AV_{EAdc} \cdot AV_{MODdc} \, AV_{EAac} \cdot AV_{MODac}$$

The first three terms are the loop DC gains and the last two terms are the AC gains.

DC Gains

The DC gain of the loop is:

Eq. 20 $$AV_{LOOPdc} = AV_{DIVdc} \cdot AV_{EAdc} \cdot AV_{MODdc}$$

Convert to Gain in dB:

Eq. 21: $$G_{DC} = 20 \cdot \log\left(AV_{DIVdc} \cdot AV_{EAdc} \cdot AV_{MODdc}\right)$$

AC Gains

The AC gain of the loop is:

Eq. 22: $$G_{MOD} = 20 \cdot \log\left[\frac{s \cdot C_O \cdot ESR + 1}{s \cdot C_O \cdot \left(R_{LD} + ESR\right) + 1}\right]$$

Eq. 23: $$G_{EA} = 20 \cdot \log\left[\frac{s \cdot C_C \cdot R_c + 1}{s \cdot C_c \cdot \left(R_{LIM} + R_C\right) + 1}\right]$$

Eq. 22 shows that GMOD has pole in its denominator and a zero in its numerator at the following frequencies.

Eq. 24: $$FP_{MOD} = \frac{1}{2 \cdot \pi \cdot C_O \cdot \left(R_{LD} + ESR\right)}$$

Eq. 25 $$FZ_{MOD} = \frac{1}{2 \cdot \pi \cdot C_o \cdot ESR}$$

Eq. 23 shows that the Error Amp also has pole in its denominator and a zero in its numerator at the following frequencies.

Eq. 26: $$FP_{EA} = \frac{1}{2 \cdot \pi \cdot C_c \cdot \left(R_{LIM} + R_c\right)}$$

Eq. 27:
$$FZ_{EA} = \frac{1}{2 \cdot \pi \cdot C_C \cdot R_C}$$

If required an additional error amp pole can be created by placing a capacitor (Cp) in parallel with Rc. This additional pole is may be required to cancel out the zero created by Co and its ESR if the zero frequency is low enough to affect stability.

If the value of Cp << Cc then a good approximation for the pole frequency is:

Eq. 28:
$$FP_{EA2} := \frac{R_C + R_{LIM}}{2 \cdot \pi \cdot C_P \cdot R_C \cdot R_{LIM}}$$

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	04/22/2013	Initial Release

FOR FURTHER ASSISTANCE

Email: powertechsupport@exar.com

customersupport@exar.com

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EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road

Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000

Fax: +1 (510) 668-7030

www.exar.com

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