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EXAR'S QUARTS COMPARED WITH TI'S TL16C554 AND TL16C554A

Author: PY

1.0 INTRODUCTION

This application note describes the major difference between Exar's QUARTs (ST16C554, ST16C654, and XR16C854) with TI's TL16C554 and TL16C554A. These devices are similar, with a few hardware, bus timing and firmware-related differences.

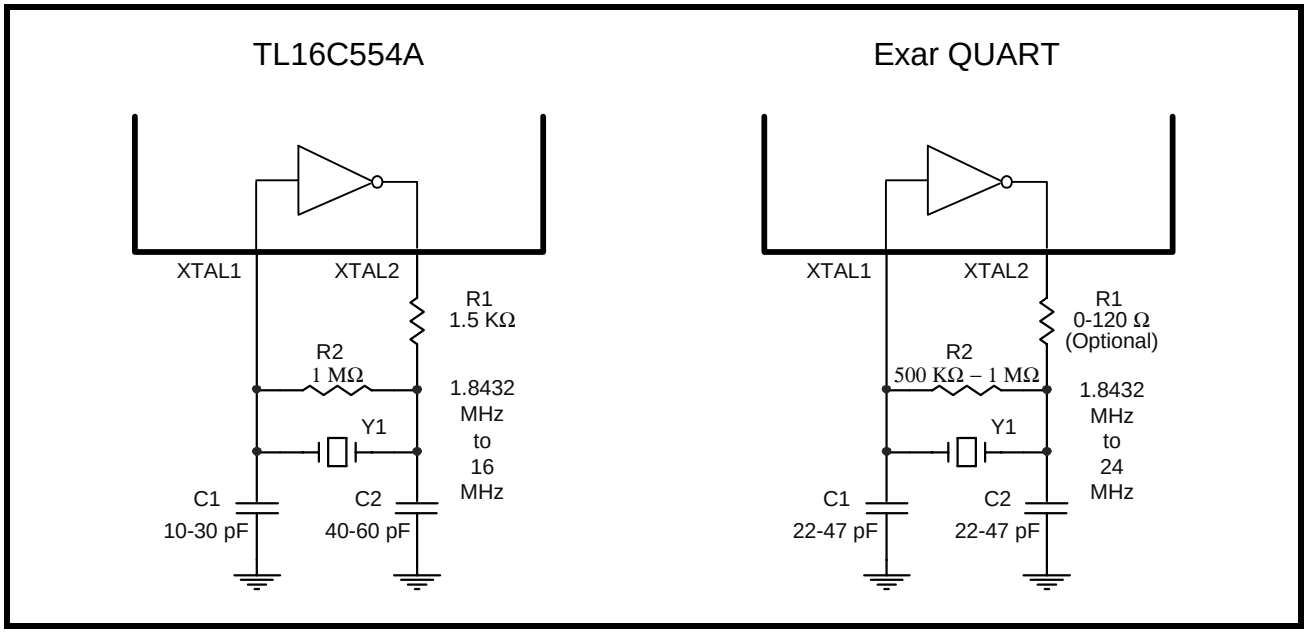
1.1 TL16C554 AND TL16C554A

The TL16C554 is listed by TI as "not recommended for new designs." In its place, they recommend the TL16C554A. The TL16C554A is an enhanced version of the TL16C554 that can operate at 5 V and 3.3 V and has Automatic RTS/CTS Flow Control.

1.2 HARDWARE DIFFERENCES

- The TI TL16C554A and Exar's ST16C554, ST16C654 and XR16C854 are all available in the 68-pin PLCC package. The Exar QUARTs are also available in the 64-pin TQFP and 100-pin QFP package while the TI QUARTs are available in a 80-pin QFP package. The Exar and TI QUARTs are pin-to-pin compatible in the 68-pin PLCC package.
- The oscillator circuitry is similar and will operate in most cases, but there are some differences when using a crystal oscillator and when using an external clock. See Figure 1below for the differences in the oscillator circuitry for a crystal oscillator. When using an external clock input for frequencies greater than 24 MHz, the Exar QUARTs will require a 2K pull-up resistor on the XTAL2 pin.

FIGURE 1. CRYSTAL OSCILLATOR CIRCUITRY DIFFERENCES



1.3 Bus Timing Differences

- The TL16C554A requires that the -CS pin is asserted first before the -IOR or -IOW pin and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted. During a read, the Exar UART can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar UART, therefore the second signal asserted will initiate the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar QUART timing can be important in DSP, ARM, and MIPS designs.

1.4 Firmware Differences

1.4.1 Firmware Differences Between the ST16C554 and TL16C554A

The internal registers in the ST16C554 and TL16C554A are similar but with one exception:

Table 1: ST16C554 and TL16C554A Register Set Differences

A2:A0	R/W	ST16C554	TL16C554A
LCR Bit-7 = 0			
100	R/W	**Modem Control Register (MCR)** • Bit-5 = Not Used	**Modem Control Register (MCR)** • Bit-5 = Auto RTS/CTS Flow Control Enable

R = Read-Only, W = Write-Only, R/W = Read/Write

1.4.2 Summary of Differences Between the ST16C554 and TL16C554A

The differences between the ST16C554 and TL16C554A are summarized in the table below.

TABLE 2: DIFFERENCES BETWEEN EXAR'S ST16C554 WITH TI'S TL16C554A

COMPARISON	ST16C554	TL16C554A
Data Bus Standard	**Intel or Motorola**	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**3 mA @ 3.3 V** **6 mA @ 5 V**	40 mA @ 3.3 V 50 mA @ 5 V
Max Frequency on XTAL1	**16 MHz @ 3.3 V** **24 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	1	1
Max Data Rate	**1 Mbps @ 3.3 V** **1.5 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	68-PLCC, 64-TQFP, 100-QFP	68-PLCC, 80-PQFP
Operating Temperature Ranges	**Commercial and Industrial**	Commercial Only
TX/RX FIFO Size	16	16
TX/RX Trigger Tables	1 Trigger Table	1 Trigger Table
TX FIFO Interrupt Trigger Levels	1	1
RX FIFO Interrupt Trigger Levels	4 Selectable	4 Selectable
Hardware Flow Control	N/A	**Auto RTS/CTS Flow Control**
Software Flow Control	N/A	N/A
Infrared Mode	N/A	N/A
Sleep Mode	N/A	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A

1.4.3 Firmware Differences Between the ST16C654 and TL16C554A

The internal registers in the ST16C654 and TL16C554A are similar but with some exceptions:

TABLE 3: ST16C654 AND TL16C554A REGISTER SET DIFFERENCES

A2:A0	R/W	ST16C654	TL16C554A
LCR Bit-7 = 0			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used
010	W	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0	**FIFO Control Register (FCR)** • Bit-5 = Not Used • Bit-4 = Not Used
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt	**Interrupt Status Register (ISR)** • Bit-5 = Not Used • Bit-4 = Not Used
100	R/W	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler • Bit-6 = IR Mode Enable • Bit-5 = XonAny	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Auto RTS/CTS Flow Control Enable
LCR = 0xBF			
010	R/W	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enhanced Functions Enable, Software Flow Control Select	N/A
100	R/W	**XON1**	N/A
101	R/W	**XON2**	N/A
110	R/W	**XOFF1**	N/A
111	R/W	**XOFF2**	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.4.3.1 Summary of Differences Between the ST16C654 and TL16C554A

The differences between the ST16C654 offers more features than the TL16C554A with these differences:

TABLE 4: DIFFERENCES BETWEEN EXAR'S ST16C654 WITH TI'S TL16C554A

COMPARISON	ST16C654	TL16C554A
Data Bus Standard	**Intel or Motorola**	Intel
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**3 mA @ 3.3 V** **6 mA @ 5 V**	40 mA @ 3.3 V 50 mA @ 5 V
Max Frequency on XTAL1	**16 MHz @ 3.3 V** **24 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	**1 or 4**	1
Max Data Rate	**1 Mbps @ 3.3 V** **1.5 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	68-PLCC, 64-TQFP, 100-QFP	68-PLCC, 80-PQFP
Operating Temperature Ranges	**Commercial and Industrial**	Commercial Only
TX/RX FIFO Size	**64**	16
TX/RX Trigger Tables	1 Trigger Table	1 Trigger Table
TX FIFO Interrupt Trigger Levels	**4 Selectable**	1
RX FIFO Interrupt Trigger Levels	4 Selectable	4 Selectable
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	**Auto Xon/Xoff Flow Control**	N/A
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	**Sleep Mode with Auto Wake-up**	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	N/A	N/A

1.4.4 Firmware Differences Between the TL16C554A and XR16C854

The internal registers in the XR16C854 offers more features than the TL16C554A with these differences:

TABLE 5: XR16C854 AND TL16C554A REGISTER SET DIFFERENCES

A2:A0	R/W	XR16C854	TL16C554A
LCR Bit-7 = 0			
001	R/W	**Interrupt Enable Register (IER)** • Bit-7 = Auto CTS# Interrupt Enable • Bit-6 = Auto RTS# Interrupt Enable • Bit-5 = Xoff Interrupt Enable	**Interrupt Enable Register (IER)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Not Used
010	W	**FIFO Control Register (FCR)** • Bit-5 = TX FIFO Trigger Level Select Bit-1 • Bit-4 = TX FIFO Trigger Level Select Bit-0	**FIFO Control Register (FCR)** • Bit-5 = Not Used • Bit-4 = Not Used
010	R	**Interrupt Status Register (ISR)** • Bit-5 = Auto RTS/CTS Interrupt • Bit-4 = Xoff or Special Character Interrupt	**Interrupt Status Register (ISR)** • Bit-5 = Not Used • Bit-4 = Not Used
100	R/W	**Modem Control Register (MCR)** • Bit-7 = BRG Prescaler • Bit-6 = IR Mode Enable • Bit-5 = XonAny • Bit-2 = OP1 Control/Auto RS485 Enable	**Modem Control Register (MCR)** • Bit-7 = Not Used • Bit-6 = Not Used • Bit-5 = Auto RTS/CTS Flow Control Enable • Bit-2 = OP1 Control
LCR Bit-7 = 0, FCTR Bit-6 = 1			
111	W	**Enhanced Mode Select Register (EMSR)** • RX/TX DMA Select, FLVL select - TX or RX FIFO	N/A
111	R	**FIFO Level Register (FLVL)** • Current Level of the TX or RX FIFO	N/A
LCR Bit-7 = 0, DLL = 0x00, DLM = 0x00			
000	R	**Device Revision (DREV)**	N/A
001	R	**Device ID (DVID)**	N/A
LCR = 0xBF			
000	R	**FIFO Data Count Register (FC)**	N/A
000	W	**Trigger Level Register (TRG)** • Programmable Trigger Levels 1-64 for TX and RX FIFO	N/A
001	R/W	**Feature Control Register (FCTR)** • RX/TX Programmable Trigger Level Select, Scratchpad Swap, Trigger Table Select, Auto RS485 Enable, RX IR Input Inversion, Auto RTS Hysteresis Select (LSB)	N/A
010	R/W	**Enhanced Feature Register (EFR)** • Auto RTS/CTS Enable, Enhanced Functions Enable, Software Flow Control Select	N/A
100	R/W	**XON1**	N/A
101	R/W	**XON2**	N/A
110	R/W	**XOFF1**	N/A
111	R/W	**XOFF2**	N/A

R = Read-Only, W = Write-Only, R/W = Read/Write

1.4.4.1 Summary of Differences Between the XR16C854 and TL16C554A

The differences between the XR16C854 and TL16C554A are summarized in the table below.

TABLE 6: DIFFERENCES BETWEEN EXAR'S XR16C854 WITH TI'S TL16C554A

COMPARISON	XR16C854	TL16C554A
Data Bus Standard	**Intel and PC Mode**	Intel
Device ID and Revision	**Device ID and Revision**	N/A
Power Supply Operation	3.3 and 5 V	3.3 and 5 V
Max Operating Current	**2.7 mA @ 3.3 V** **4 mA @ 5 V**	40 mA @ 3.3 V 50 mA @ 5 V
Max Frequency on XTAL1	**22 MHz @ 3.3 V** **33 MHz @ 5 V**	14 MHz @ 3.3 V 16 MHz @ 5 V
Data Sampling Rates	16X	16X
BRG Prescaler	**1 or 4**	1
Max Data Rate	**1.375 Mbps @ 3.3 V** **2 Mbps @ 5 V**	875 Kbps @ 3.3 V 1 Mbps @ 5V
Package	68-PLCC, 64-TQFP, 100-QFP	68-PLCC, 80-PQFP
Operating Temperature Ranges	**Commercial and Industrial**	Commercial Only
TX/RX FIFO Size	**128**	16
TX/RX Trigger Tables	**4 Trigger Tables**	1 Trigger Table
TX FIFO Interrupt Trigger Levels	**Programmable (Table D)** **4 Selectable (Tables A-C)**	1
RX FIFO Interrupt Trigger Levels	**Programmable (Table D)** **4 Selectable (Tables A-C)**	4 Selectable
TX/RX FIFO Counters	**TX/RX FIFO Counters**	N/A
Hardware Flow Control	Auto RTS/CTS Flow Control	Auto RTS/CTS Flow Control
Software Flow Control	**Auto Xon/Xoff Flow Control**	N/A
Auto Hysteresis Level	**16 Selectable Levels**	N/A
Infrared Mode	**IrDA encoder/decoder (ver 1.0)**	N/A
Sleep Mode	**Sleep Mode with Auto Wake-up**	N/A
Diagnostic Modes	Local loopback	Local Loopback
RS485 Mode	**Auto RS485 Mode**	N/A

1.5 REPLACING THE TL16C554A WITH THE ST16C554, ST16C654 OR XR16C854

You can directly replace TI's TL16C554A with Exar's ST16C554, ST16C654 or XR16C854 with minimal hardware changes if using the 68-PLCC package. The crystal oscillator circuitry should work in most cases, but it may be necessary to modify the oscillator circuitry as shown in Figure 1. If replacing with the 64-TQFP or 100-QFP packages, hardware changes will be required since the TL16C554A is not available in those packages.

Replacing the TL16C554A with the ST16C554 is simple when the system is not using Automatic RTS/CTS Hardware Flow Control.

If replacing the TL16C554A with the ST16C654 or XR16C854, minor software updates will be necessary since Automatic RTS/CTS Hardware Flow Control is enabled differently for each QUART. Alos, it would need to be updated in order to take advantage of the enhanced features of the ST16C654 and XR16C854 that are not available in the TL16C554A.

There should not be any timing problems replacing the TL16C554A with the ST16C554, ST16C654 or XR16C854 because they are more flexible than the TL16C554A as described in the bus timing section.