August 2002

EXAR'S XR16C854 COMPARED WITH OXFORD'S OX16C954

Author: PY

1.0 INTRODUCTION

This application note describes the major difference between Exar's XR16C854 with Oxford's OX16C954. These devices have a few hardware, bus timing and firmware-related differences.

1.1 HARDWARE DIFFERENCES

The Oxford OX16C954 and Exar XR16C854 are available in the 68-pin PLCC package. Additionally, the XR16C854 is available in the 64-pin TQFP and 100-pin QFP packages (for compatibility to early families). The OX16C954 is availabe in the 80-pin TQFP. In the 68-pin PLCC package, the Exar and Oxford UARTs are pin-to-pin compatible. A

nother alternative to the OX16C954 is the XR16L784. Please see DAN144 for complete details.

1.2 BUS TIMING DIFFERENCES

The OX16C954 requires that the -CS pin is asserted before the -IOR or -IOW pin at the beginning of the read/write cycle and the -IOR or -IOW pin must be de-asserted before the -CS pin is de-asserted at the end of the cycle. During a read, the Exar UART can have either the -CS or the -IOR signal asserted first and have either signal be de-asserted first. The signals are wire-ORed in the Exar UART, therefore the second signal asserted initiates the read cycle and the first signal de-asserted terminates the read cycle. The same is true during a write for -CS and -IOW. The flexibility of the Exar UARTs timing can be important in designs using DSP, ARM, and MIPS processors.

1.3 FIRMWARE DIFFERENCES

- The internal registers of the XR16C854 are much simpler than the internal registers of the OX16C954. The XR16C854 only has one level of shadow registers while the OX16C954 has 3 levels. The XR16C854 has the 16C550 Standard Register Set and the Enhanced Register Set. The Enhanced Register Set can be accessed by writing 0xBF to the LCR register. Note that the XR16C854 has more registers in the Enhanced Register Set than the OX16C954 has in their Enhanced Register Set. The OX16C954 has a Standard Register Set, Enhanced Register Set, Indexed Control Register Set and Additional Status Register Set. As long as the last value written to LCR was not 0xBF, the Index Control Register (ICR) is accessed by writing the desired address offset for the ICR to the Scratchpad register and then writing to the Index Control Register. Note that this is for writing to the Index Control Register only. To read from the Index Control Register, you must write to a bit in one of the Indexed Control Registers to enable reading from the Index Control Register. The Additional Status Registers can only be read when another bit in the Indexed Control Registers is set.
- The XR16C854 has Automatic 2 character Xon/Xoff Software Flow Control. In Automatic 2 character Xon/Xoff Software Flow Control, two flow control characters (Xoff1, Xoff2, Xon1, Xon2) are sent at the appropriate times instead of just a single character. This is to ensure that the first character is not accidentally interpreted as a software flow control character if it was not meant to be. More importantly, it will allow the software routine to be able to use the entire character set including the Xon and Xoff characters as part of the data stream since they will not necessarily be interpreted as software flow control characters unless they are received one after another. The OX16C954 only has the Automatic 1 character Xon/Xoff Software Flow Control.
- The XR16C854 has 16 selectable levels of RTS Hysteresis ranging from ±4 to ±52 when using programmable trigger levels (Table-D) are used. For example if the RX Trigger Level was programmed for 68 bytes and the RTS Hysteresis was selected at ±52, the RTS# pin will not be forced to a logic 1 (RTS off) until the

receive FIFO reaches 120 bytes. The RTS# pin will return to a logic 0 (RTS on) after the RX FIFO is unloaded to 16 bytes. The OX16C954 has a similar feature. For the OX16C954, the software driver has to manually select the upper level to halt transmission and the lower level to resume transmission independent of the RX Trigger Level. It is also up to the software driver to ensure that the upper level is greater than the lower level since the device does not perform that check.

- The OX16C954 can be programmed to operate in a wake-up mode for Multidrop applications. This feature is not available in the XR16C854.
- The OX16C954 can disable and enable the TX or RX output. This feature is not available in the XR16C854.
- The XR16C854 has a BRG prescaler of 1 or 4. The OX16C954 has a Baud Rate Generator Prescaler of 1 to 31.875.
- The XR16C854 has a Data Sampling Rate of 16X. The OX16C954 has a Data Sampling Rate of 4X to 16X.

1.4 REPLACING THE OX16C954 WITH THE XR16C854

You can directly replace Oxford's OX16C954 with Exar's XR16C854 in the 68-PLCC package. If using the XR16C854 in the other packages, hardware changes will be required since the OX16C954 is not available in those packages.

There should not be any timing problems replacing the OX16C954 with the XR16C854 because it is more flexible than the OX16C954 as described in the bus timing section.

The software will need to be updated to take advantage of the enhanced features of the XR16C854 that are not available in or different from the OX16C954.

In a nutshell, the XR16C854 and OX16C954 have similar features but the XR16C854 has a much simpler internal register set for faster and easier software development.