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UPGRADING FROM XR68C681 TO XR68C92/192

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1.0 INTRODUCTION

This application note describes the hardware and firmware differences between the XR68C681 and the XR68C92/192 as well as the steps involved in upgrading the XR68C681 to the newer XR68C92/192. In this note, the XR68C681 will be referred to as the C681 device and the XR68C92, XR68C192 family of devices will be referred to as C92/192. Also, this application note must be used along with the datasheets of these devices for a complete understanding of the differences.

2.0 HARDWARE DIFFERENCES

2.1 PACKAGE

The C681 and the C92/192 are fully pin-to-pin compatible in the 44-PLCC package footprint only. The C681 is also available in the 40-PDIP and 40-CDIP packages. The C92/192 is also available in the 44-TQFP package. The C92 (only) is also available in the 40-PDIP package, but is not recommended for new designs in this package and therefore is not covered in this application note.

2.2 OPERATING VOLTAGE

The C681 is a 5V device only. The C92/192 can operate from 2.97 to 5.5V and it also has 5V tolerant inputs.

2.3 CRYSTAL OSCILLATOR

The max frequency of the input clock is only 7.372MHz for the C681, whereas it is 24MHz for the C92/192 at 5V VCC.

2.4 FIFO DEPTH

The C681 has 3-byte RX and TX FIFOs whereas the C92 has 8-byte FIFOs and the C192 has 16-byte FIFOs.

3.0 FIRMWARE DIFFERENCES

In the following discussion, the firmware differences are briefly explained. Please refer to the datasheets of the XR68C681 and the XR68C92/192 for more details. The internal registers are very similar in the C681 and the C92/192. Table 1 below shows the differences:

TABLE 1: INTERNAL REGISTERS OF XR68C681 VS. XR68C92/192

ADDRESS A3:A0	MODE	XR68C681 REGISTER	XR68C92/192 REGISTER	COMMENTS
0000	R/W	Mode Registers A (MR1, MR2)	Mode Registers A (**MR0**, MR1, MR2)	Extra register in C92/192
0010	R	Masked Interrupt Status Reg (MISR)	Reserved	
1000	R/W	Mode Registers B (MR1, MR2)	Mode Registers B (**MR0**, MR1, MR2)	Extra register in C92/192
1100	R/W	Interrupt Vector Register (IVR)	General Purpose Register (GPR)	

3.1 MODE REGISTERS MR0A, MR0B:

The MR0 registers add the following functionality to the C92/192:
Bit-7: Watchdog Timer (See datasheet for details)
Bit-6: RX Trigger Level (Go to page 2 for details)
Bits 5,4: TX Trigger Level (Go to page 2 for details)
Bit 3,1: Reserved (Bit-1 is used for factory test mode)
Bits 2,1 of MR0A: Extended baud rate tables (See datasheet for details); bits 2,1 of MR0B are reserved

3.2 MASKED INTERRUPT STATUS REGISTER MISR:

This register ANDs the values of the write-only Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR) together.

*MISR value = [ISR value] * [IMR value]*

In the C92/192, the user needs to store the value written into the IMR and do the ANDing operation in software.

3.3 COMMAND REGISTER (CRA, CRB) DIFFERENCES:

The upper nibble of the Command Register in both the C681 and the C92/192 is used to issue various commands. While many of the commands are the same, some are different as shown in Table 2 below:

TABLE 2: COMMANDS DESCRIPTION AND DIFFERENCES BETWEEN THE XR68C681 AND XR68C92/192

COMMAND REGISTER BITS 7:4	XR68C681	XR68C92/192
1000	Set RX BRG Select Extend Bit	Set -RTS output to LOW (Assertion)
1001	Clear RX BRG Select Extend Bit	Set -RTS output to HIGH (Negation)
1010	Set TX BRG Select Extend Bit	Enable Time-out Mode
1011	Clear TX BRG Select Extend Bit	Set Mode Register Pointer to MR0
1100	Set Standby Mode (Channel A only)	Disable Time-out Mode
1101	Set Active Mode (Channel A only)	Not used
1110	Not used	Enable Power Down Mode (Channel A only)
1111	Not used	Disable Power Down Mode (Channel A only)

3.4 RECEIVE TRIGGER LEVELS:

The C681 provides a choice of generating a Receive Ready interrupt either for each character received or when the RX FIFO is full (via MR1 bit-6). The C92/192 combines this bit and the new MR0 bit-6 to provide four RX trigger levels as follows:

MR0 BIT-6	MR1 BIT-6	RX TRIGGER LEVELS IN	
		XR68C92 (8-BYTE FIFO)	XR68C192 (16-BYTE FIFO)
0	0	1 byte in FIFO	1 byte in FIFO
0	1	3 bytes in FIFO	6 bytes in FIFO
1	0	6 bytes in FIFO	12 bytes in FIFO
1	1	8 bytes in FIFO	16 bytes in FIFO

3.5 TRANSMIT TRIGGER LEVELS:

The C681 generates a Transmit Ready interrupt only when the transmit FIFO is empty. The C92/192 via the MR0 register bits 4 and 5 provides four TX trigger levels as shown in the table below:

MR0 BIT-5	MR0 BIT-4	TX TRIGGER LEVELS IN	
		XR68C92 (8-BYTE FIFO)	XR68C192 (16-BYTE FIFO)
0	0	FIFO Fully Empty	FIFO Fully Empty
0	1	4 FIFO locations empty	6 FIFO locations empty
1	0	6 FIFO locations empty	12 FIFO locations empty
1	1	1 FIFO location empty	1 FIFO location empty

3.6 BAUD RATE TABLES

There are four baud rate tables available in the C681 and six baud rate tables available in the C92/192.
The parameters that select the baud rate table and decide the baud rate in the C681 are:

1. ***CSR bits 7:4 for RX clock and CSR bits 3:0 for TX clock***
2. ***ACR bit-7***
3. ***Set RX BRG Select Extend bit for RX clock***
4. ***Set TX BRG Select Extend bit for TX clock***

The parameters that select the baud rate table and decide the baud rate in the C92/192 are:

1. ***CSR bits 7:4 for RX clock and CSR bits 3:0 for TX clock***
2. ***ACR bit-7***
3. ***MR0A bit-0 for Extended Baud Rate Table 1***
4. ***MR0A bit-2 for Extended Baud Rate Table 2***

The first two parameters are identical for the C681 and the C92/192. The remaining parameters result in different baud rates. Please refer to the datasheets for a complete listing of baud rates.

4.0 SUMMARY

For direct drop-in replacement of the XR68C681 by the XR68C92 or the XR68C192, the following conditions must be satisfied:

- 44-PLCC package is used
- 5V VCC is used
- MISR is not used
- Extended baud rate selection is not used
- Stand-by mode is not used

Otherwise, hardware and/or software changes are required.

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