A Comparison between Exar's XR-68C681 and Signetics' SCC68692 DUART Devices

1. Introduction

The purpose of this document is to try to list differences between the XR-68C681 and the Signetics SCC68692 DUART Devices. In general the devices are pretty much the same. They both have the same pin out, and appear to somewhat electrically similarly. However, there are some firmware-related differences that the user should be aware of. These differences are listed below:

1A. Register Addressing (Read Mode Registers)

This table compares the Register Addressing, for the Read Mode Registers (e.g, those DUART Registers that one accesses when performing a read to the DUART), between the two devices. Any differences between the two devices are in italics.

A Comparison between Exar's XR-68C681 and Signetics' SCC68692 DUART Devices

Table 1, Addressing of "Read Mode" Registers within the XR-68C681 and the Signetics SCC68692 Devices

A3	A2	A1	A0	XR-68C681	SCC68692
0	0	0	0	Mode Register, Channel A (MR1A, MR2A)	Mode Register, Channel A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Status Register A (SRA)
0	***0***	***1***	***0***	***Masked Interrupt Status Register (MISR)***	***BRG Test***
0	0	1	1	Receiver Holding Register A (RHRA)	Receiver Holding Register A (RHRA)
0	1	0	0	Input Port Change Register (IPCR)	Input Port Change Register (IPCR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
0	1	1	0	Counter/Timer Upper Byte Register (CTUR)	Counter/Timer Upper Byte Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte Register (CTLR)	Counter/Timer Lower Byte Register (CTLR)
1	0	0	0	Mode Registers, Channel B (MR1B, MR2B)	Mode Registers, Channel B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Status Register B (SRB)
1	***0***	***1***	***0***	***RESERVED***	***1X/16X Test***
1	0	1	1	Receiver Holding Register B (RHRB)	Receiver Holding Register B (RHRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port Register (IPR)	Input Port Register (IPR)
1	1	1	0	Start Counter Command	Start Counter Command
1	1	1	1	Stop Counter Command	Stop Counter Command

Note: shaded blocks are Address-Triggered Commands

1B. Register Address (Write Mode Registers)

Table 2, Register Addressing for the Write Mode Registers

A3	A2	A1	A0	XR-68C681	SCC68692
0	0	0	0	Mode Registers, Channel A (MR1A, MR2A)	Mode Registers, Channel A (MR1A, MR2A)
0	0	0	1	Clock Select Register A (CSRA)	Clock Select Register A (CSRA)
0	0	1	0	Command Register A (CRA)	Command Register A (CRA)
0	0	1	1	Transmitter Holding Register A (THRA)	Transmitter Holding Register A (THRA)
0	1	0	0	Auxillary Control Register (ACR)	Auxillary Control Register (ACR)
0	1	0	1	Interrupt Mask Register (IMR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper Byte Register (CTUR)	Counter/Timer Upper Byte Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte Register (CTLR)	Counter/Timer Lower Byte Register (CTLR)
1	0	0	0	Mode Registers, Channel B (MR1B, MR2B)	Mode Registers, Channel B (MR1B, MR2B)
1	0	0	1	Clock Select Register B (CSRB)	Clock Select Register B (CSRB)
1	0	1	0	Command Register B (CRB)	Command Register B (CRB)
1	0	1	1	Transmitter Holding Register B (THRB)	Transmitter Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Output Port Configuration Register (OPCR)	Output Port Configuration Register (OPCR)
1	1	1	0	Set Output Port Bits Command	Set Output Port Bits Command
1	1	1	1	Clear Output Port Bits Command	Clear Output Port Bits Command

Note: There were no differences in the Addressing of the Write Only Registers.
Shaded blocks denote "Address-Triggered" command

2. Upper Nibble Commands in the Command Register

The bit format of the Command Register for each Channel is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Miscellaneous Commands				**Enable/Disable Tx**		**Enable/Disable Rx**	
See Text				00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = (Do not use)		00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = (Do not use)	

The bit format and function of the lower nibble of the Command Register are identical between the two devices. However, there are some differences in the Miscellaneous Commands associated with the Upper Nibble of the Command Register. Table 3 presents the Commands for all bit combinations of the Upper Nibble of the Command Registers. Unless specified, these commands can be assumed to apply to both Channels A and B. Please note that any differences between the two devices are in italics.

Table 3, Upper Nibble of Command Register (Miscellaneous Commands)

Bit 7	Bit 6	Bit 5	Bit 4	XR-68C681	SCC68692
0	0	0	0	Null Command	Null Command
0	0	0	1	Reset MR Pointer	Reset MR Pointer
0	0	1	0	Reset Receiver	Reset Receiver
0	0	1	1	Reset Transmitter	Reset Transmitter
0	1	0	0	Reset Error Status	Reset Error Status
0	1	0	1	Reset Break Change Interrupt	Reset Break Change Interrupt
0	1	1	0	Start Break	Start Break
0	1	1	1	Stop Break	Stop Break
1	***0***	***0***	***0***	***Set Receiver BRG Select Extend Bit***	***Assert RTSN***
1	***0***	***0***	***1***	***Clear Receiver BRG Select Extend Bit***	***Negate RTSN***
1	***0***	***1***	***0***	***Set Transmitter BRG Select Extend Bit***	***Set Timeout Mode On***
1	***0***	***1***	***1***	***Clear Transmitter BRG Select Extend Bit***	***Not Used***
1	***1***	***0***	***0***	***Channel A: Set Standby (Low Power) Mode***	***Disable Timeout Mode***
1	***1***	***0***	***1***	***Channel A: Set Active (Normal Power) Mode***	***Not Used***
1	***1***	***1***	***0***	***Reserved***	***Channel A: Set Standby (Low Power) Mode Channel B: Not Used***
1	***1***	***1***	***1***	***Reserved***	***Channel A: Set Active (Normal Power) Mode Channel B: Not Used***

3. BRG Test, 1X/16X Test - SCC68692

A read to DUART Address 02h and/or 0Ah (where the h suffix denotes a hexadecimal expression) will place the Signetics device into a certain test mode. Please see Signetics' Literature for a description of these modes.

4. Receiver Time-out Mode - SCC68692

When the Receiver Time-out Mode is enabled, the received data stream will control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches the "zero" count, the counter ready bit is set and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message end before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

Note: The Receiver Time-out mode can be Enabled and Disabled by writing the appropriate commands to the Channel Command Register (see Table 3).

5. Commands to Assert/Negate RTS* - SCC68692

The upper nibble of the Channel Command Register (Miscellaneous Commands), has provision to allow the user to *directly* Assert and Negate the Active-low RTS (Request to Send) output pin. This feature is somewhat available within the XR-68C681, via two of the Output Port pins (one for each channel). However, in the case of the XR-68C681 device, the user must first configure one of the Output Port pins to be the RTS* signal. Afterwards, assertion and negation is generally accomplished by applying the Address-Triggered "Set Output Port Bit" and/or "Clear Output Port Bit" commands or via the Rx/Tx RTS Control features. Hence, the XR-68C681's approach is not as direct as that of the SCC68692 device.