A Comparison between Exar's XR-88C681 with Signetics' SCC2692 DUART Devices

Introduction

Although the XR-88C681 and the Signetic SCC2692 devices have exactly the same pin outs, they are not drop-in compatible devices. The incompatibility between these two devices is mainly software. The Register Addressing is slightly different between these two devices. As well as the meaning of commands written to the Command Register. The specifics of these differences are ennumerated in this write up in Tables 1 through 3. There are numerous differences in features as well, and each of these are presented below.

1. I/Z Modes - XR-88C681

The XR-88C681 allows the user to Command the DUART into the Z-Mode (sometimes referred to as the "Zilog" Mode). This mode can be useful if the user wishes to daisy chain a series of DUART's together, as shown in Figure 1.

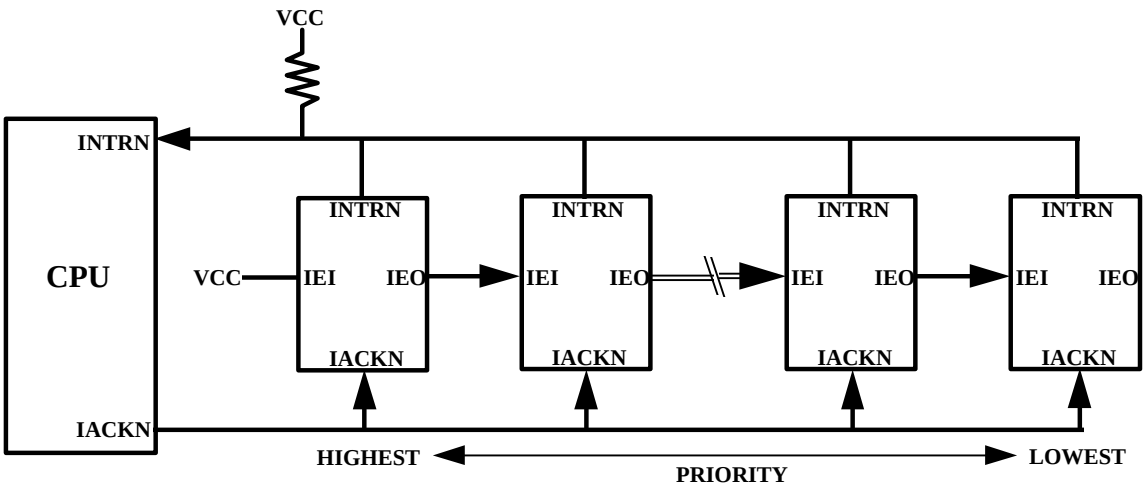

Figure 1, An Illustration of XR-88C681 devices operating in a Daisy Chain, when commanded into the Z-Mode.

A more detailed discussion of the XR-88C681's Z Mode operation can be found in the Data Sheet. However, for the sake of this report, let's just say that the Z-Mode is a manner which allows several DUARTs to be configured in a Daisy Chain, as presented in Figure 1, and allows the CPU to perform Vectored Interrupt Processing and Interrupt Prioritization for all of the DUART devices.

The SCC2692 device does not offer the Z-Mode of operation.

2. BRG Test and 1X/16X Test - SCC2692

A read to DUART Address 02h and/or 0Ah (where the h suffix denotes a hexadecimal expression) will place the Signetics device into a certain test mode. Please see Signetics' Literature for a description of these modes.

3. Receiver Time-out Mode

When the Receiver Time-out Mode is enabled, the received data stream will control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches the "zero" count, the counter ready bit is set and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message end before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

Note: The Receiver Time-out mode can be Enabled and Disabled by writing the appropriate commands to the Channel Command Register (see Table 3).

4. Register Addressing differences between the two devices

Each of these devices consists of Read Only and Write Only registers. There are numerous cases where, for a given DUART address (A3 - A0), the register that is accessed during a read operation is not the same as that accessed during a write operation. Hence, I have divided the DUART registers into two groups: Read Mode and Write Mode registers.

Tables 1 and 2 presents the Register Addressing (of both devices) for the Read Mode and Write Mode Registers, respectively.

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Table 1, Read Register Addressing

A3	A2	A1	A0	SCC2692	XR-88C681
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Status Register A (SRA)
0	***0***	***1***	***0***	***BRG Test***	***Interrupt Status Register, Masked, ISR_M***
0	0	1	1	Rx Holding Register A (RHRA)	Rx Holding Register A (RHRA)
0	1	0	0	Input Port Change Register (IPCR)	Input Port Change Control Register (IPCR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Status Register (ISR)
0	1	1	0	Counter/Timer Upper Byte (CTUR)	Counter/Timer Upper Byte (CTUR)
0	1	1	1	Counter/Timer Lower Byte (CTLR)	Counter/Timer Lower Byte (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Status Register B (SRB)
1	***0***	***1***	***0***	***1x/16x Test***	***Reserved***
1	0	1	1	Rx Holding Register B (RHRB)	Rx Holding Register B (RHRB)
1	***1***	***0***	***0***	***Reserved***	***Interrupt Vector Register (IVR)***
1	1	0	1	Input Port (PR)	Input Port (PR)
1	1	1	0	Start Counter Command	Start Counter Command
1	1	1	1	Stop Counter Command	Stop Counter Command

Note: Differences between the two devices are written in Bold-Italics
Shaded boxes denoted "Address Triggered" commands

Table 2, Write Register Addressing

A3	A2	A1	A0	SCC2692	XR-88C681
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Clock Select Register A (CSRA)	Clock Select Register A (CSRA)
0	0	1	0	Command Register A (CRA)	Command Register A (CRA)
0	0	1	1	Tx Holding Register A (THRA)	Tx Holding Register A (THRA)
0	1	0	0	Aux. Control Register (ACR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Mask Register (IMR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper Byte Register (CTUR)	Counter/Timer Upper Byte Register (CTUR)
0	1	1	1	Counter/Timer Lower Byte Register (CTLR)	Counter/Timer Lower Byte Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Clock Select Register B (CSRB)	Clock Select Register B (CSRB)
1	0	1	0	Command Register B	Command Register B (CRB)
1	0	1	1	Tx Holding Register B (THRB)	Tx Holding Register B (THRB)
1	***1***	***0***	***0***	***Reserved***	***Interrupt Vector Register (IVR)***
1	1	0	1	Output Port Configuration Register (OPCR)	Output Port Configuration Register (OPCR)
1	1	1	0	Set Output Port Bits Command	Set Output Port Bits Commands
1	1	1	1	Reset Output Port Bits Command	Reset Output Port Bits Command

Note: Differences between the two devices are written in Bold Italics
Shaded boxes denote "Address-Triggered" Commands

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5. Differences in Commands being issued to the Command Register, between the XR-88C681 and the SCC2692 devices.

The Command Register Format for both the XR-88C681 and the SC26C92 devices is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Miscellaneous Commands				**Tx Enable/Disable**		**Rx Enable/Disable**	
See Table 3				00 = No Change 01 = Enable Tx 10 = Disable Tx 11 = Undefined, Do Not Use		00 = No Change 01 = Enable Rx 10 = Disable Rx 11 = Undefined, Do Not Use	

The Lower Nibble of the Channel Command Register is for Enabling/Disabling the Transmitter and Receiver. The Upper Nibble of the Channel Command Register is for Miscellaneous Commands. There are some differences in the sets of these Miscellaneous Commands, between these two devices. These differences are listed in Table 3.

Table 3, Comparison of Commands to the Command Register between the Two Devices

First 4 bits of Command Word to CR	SCC2692	XR-88C681
0 0 0 0	NULL Command	NULL Command
0 0 0 1	Reset MR Pointer	Reset MR Pointer
0 0 1 0	Reset Rx	Reset Rx
0 0 1 1	Reset Tx	Reset Tx
0 1 0 0	Reset Error Status	Reset Error Status
0 1 0 1	Reset Break Change Interrupt	Reset Break Change Interrupt
0 1 1 0	Start Break	Start Break
0 1 1 1	Stop Break	Stop Break
1 0 0 0	***Assert RTSN***	***Set Rx BRG Select Extend Bit***
1 0 0 1	***Negate RTSN***	***Clear Rx BRG Select Extend Bit***
1 0 1 0	***Set Timeout Mode ON***	***Set Tx BRG Select Extend Bit***
1 0 1 1	***Not Used***	***Clear Tx BRG Select Extend Bit***
1 1 0 0	***Disable Timeout Mode***	***Set Standby Mode(A)/ Reset IUS Latch (B)***
1 1 0 1	***Not Used***	***Set Active Mode (A)/Set Z Mode (B)***
1 1 1 0	***Power Down Mode On(A)/Reserved (B)***	***Reserved***
1 1 1 1	***Disable Power Down Mode (A)/Reserved (B)***	***Reserved***