Application Note

Line Card Redundancy Design With the XRT83SL38 T1/E1 SH/LH LIU ICs

REDUNDANCY APPLICATIONS

INTRODUCTION

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with EXAR's Line Interface Units (LIU). EXAR offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs.

TYPICAL REDUNDANCY SCHEMES

- 1:1 One backup card for every primary card (Facility Protection)
- 1+1 One backup card for every primary card (Line Protection)
- N+1 One backup card for N primary cards

XRT83L38S (Short Haul) and XRT83L38 (Long Haul) T1/E1/J1 Line Interface Unit

The XRT83L38S/L38 short haul and long haul LIUs are fully integrated octal transceivers. They have key design features allowing system designers to implement redundancy applications that ensure reliability. The "internal" impedance mode eliminates the need for external relays when using the 1:1 and 1+1 redundancy schemes.

EXAR's XRT83L38S/L38 FEATURES

- Individual Channel Control for all Features
- Internal Impedance Mode for Transmit and Receive
  - T1 (Twisted Pair 100 ohm)
  - J1 (Twisted Pair 110 ohm)
  - E1 (Co-axial Cable 75 ohm)
  - E1 (Twisted Pair 120 ohm)
- One Bill of Materials for T1/E1/J1
- Transmitters with Multiple Options for Tri-State
  - Power Down
  - Programmable Through the Microprocessor Interface
  - Hardware Pins for Fastest Switching Time Available
  - Missing TxCLK
  - Individual Channel Control
- Hardware Pins for Termination Impedance Selections (Host Mode and Hardware Mode)
- Requires "No" Relays for 1:1 and 1+1 Redundancy Applications
- Hitless Protection Switching (HPS)
- Fast Switching Time

PROGRAMMING CONSIDERATIONS

The XRT83L38S/L38 has two modes of operation, Host Mode and Hardware Mode. In Host Mode, there are two bits in register 130 (82h) that control the transmitter outputs and the Rx line impedance select, TxONCNTL (Bit 7) and TERCNTL (Bit 6). When TxONCNTL is programmed to "1", tri-stating the transmitter outputs is switched to the hardware pins:

Hardware Pins

TxON0 → Pin 169
TxON1 → Pin 170
TxON2 → Pin 171
TxON3 → Pin 172
TxON4 → Pin 90
TxON5 → Pin 91
TxON6 → Pin 92
TxON7 → Pin 93

When TERCNTL is programmed to "1", control of the Rx line impedance select (RxTSEL) is switched to the hardware pin:

Hardware Pin

RxTSEL → Pin 83 (Low=External, Hi=Internal)

Either mode works well with redundancy applications. The user can determine which mode has the fastest switching time for a unique application. In many cases, the switching time will be faster when using the hardware pins to control the line impedance interface.

REFERENCE DESIGN

1:1 REDUNDANCY

A 1:1 facility protection redundancy scheme has one backup card for every primary card. When using 1:1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

TRANSMIT 1:1 REDUNDANCY

For 1:1 redundancy, the transmitters on the primary and backup card should be programmed for "internal" impedance mode. The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 1. for a simplified block diagram of the transmit section for a 1:1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

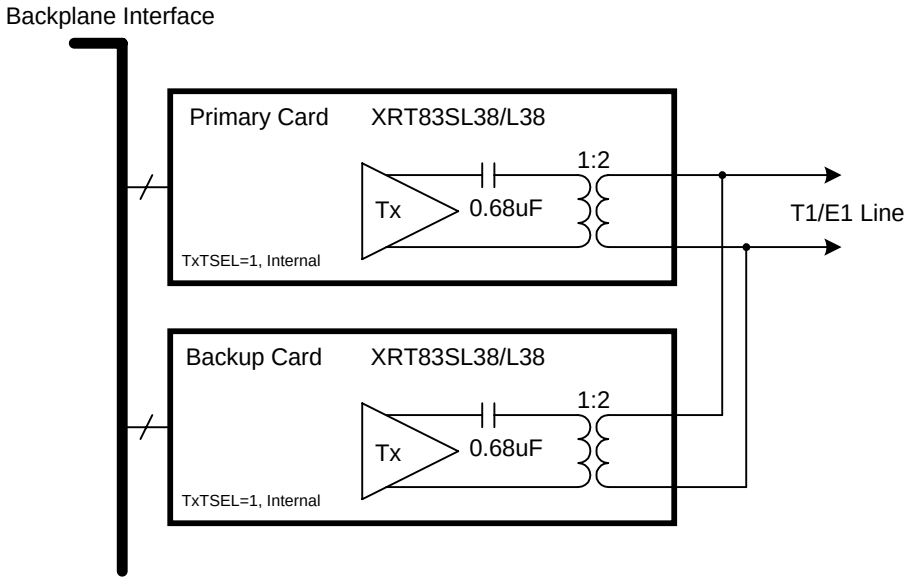

Figure 1a. Simplified Block Diagram of the Transmit Section for a 1:1 Redundancy Scheme Using Two Transformers

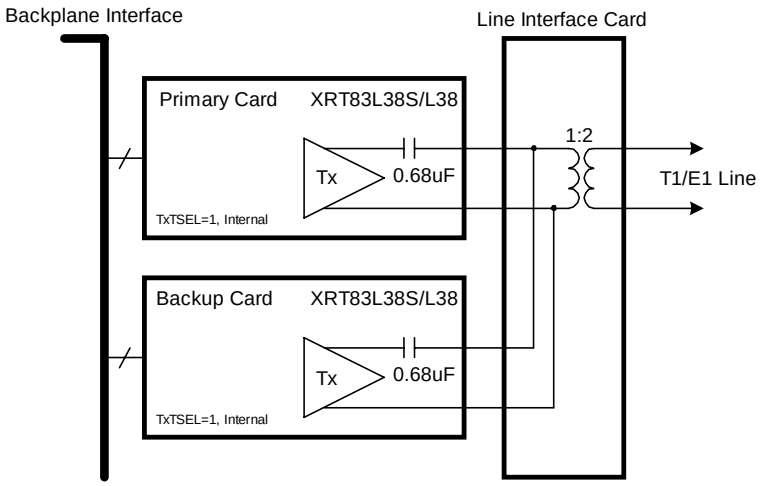

Figure 1b. Simplified Block Diagram of the Transmit Section for a 1:1 Redundancy Scheme Using One Common Transformer

RECEIVE (1:1 REDUNDANCY)

For 1:1 redundancy, the receivers on the primary card should be programmed for “internal” impedance mode. The receivers on the backup card should be programmed for “external” impedance mode. Since there is no external resistor in the circuit, the receivers on the backup card will be high impedance. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to “internal” impedance mode, then the primary card to “external” impedance mode. See Figure 2. for a simplified block diagram of the receive section for a 1:1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

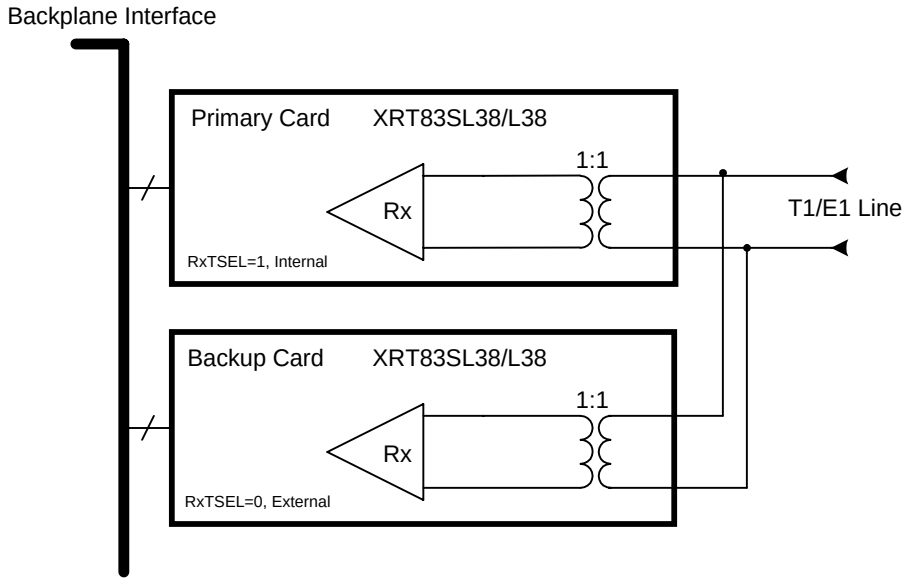

Figure 2a. Simplified Block Diagram of the Receive Section for a 1:1 Redundancy Scheme Using Two Transformers

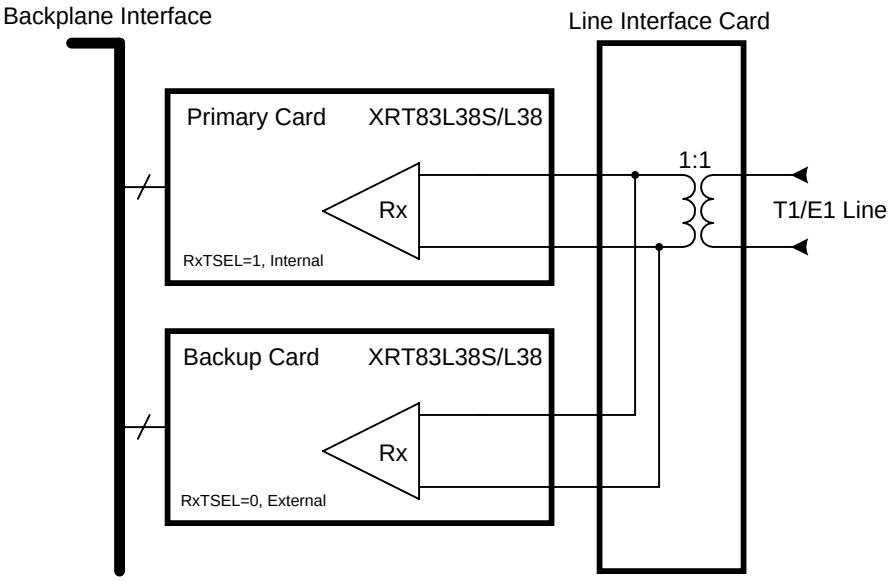

Figure 2b. Simplified Block Diagram of the Receive Section for a 1:1 Redundancy Scheme Using One Common Transformer

1+1 REDUNDANCY

A 1+1 line protection redundancy scheme has one backup card for every primary card. When using 1+1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. The receiver inputs on the backup card have the ability to monitor the line for bit errors in high impedance mode. The transmit and receive sections of the LIU device are described separately.

TRANSMIT 1+1 REDUNDANCY

For 1+1 redundancy, the transmitters on the primary and backup cards should be programmed for “internal” impedance mode. The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 3. for a simplified block diagram of the transmit section for a 1+1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

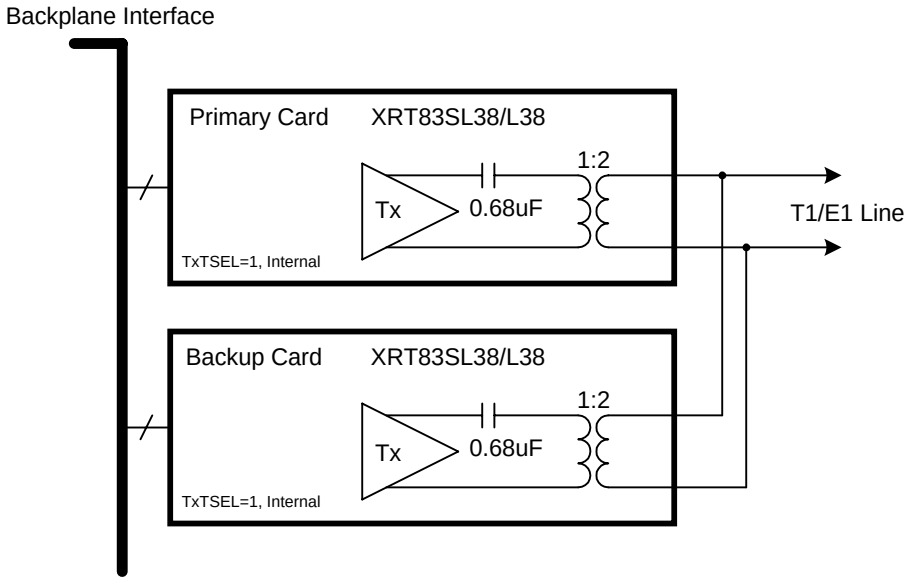

Figure 3a. Simplified Block Diagram of the Transmit Section for a 1+1 Redundancy Scheme Using Two Transformers

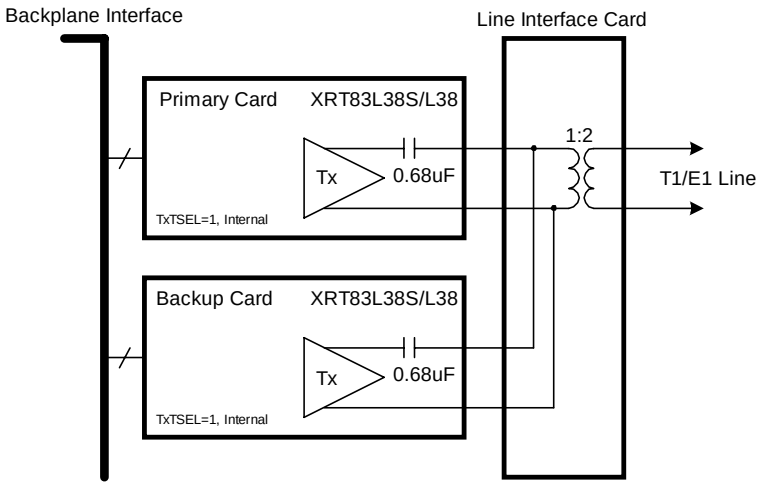

Figure 3b. Simplified Block Diagram of the Transmit Section for a 1+1 Redundancy Scheme Using One Common Transformer

RECEIVE (1+1 REDUNDANCY)

For 1+1 redundancy, the receivers on the primary card should be programmed for “internal” impedance mode. The receivers on the backup card should be programmed for “external” impedance mode. Since there is no external resistor in the circuit, the receivers on the backup card will be high impedance. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. In high impedance mode, the receivers have the ability to monitor the line for bit errors. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to “internal” impedance mode, then the primary card to “external” impedance mode. See Figure 4. for a simplified block diagram of the receive section for a 1+1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

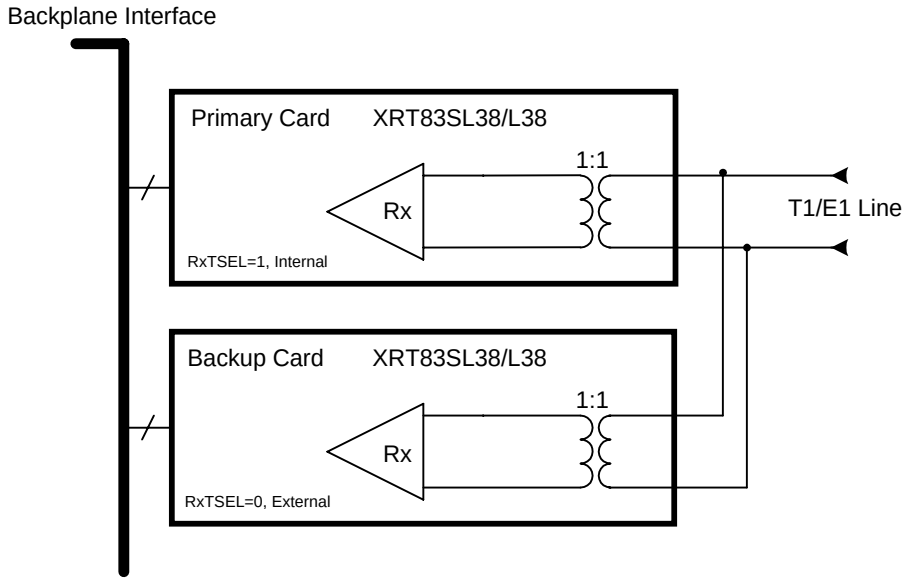

Figure 4a. Simplified Block Diagram of the Receive Section for a 1+1 Redundancy Scheme Using Two Transformers

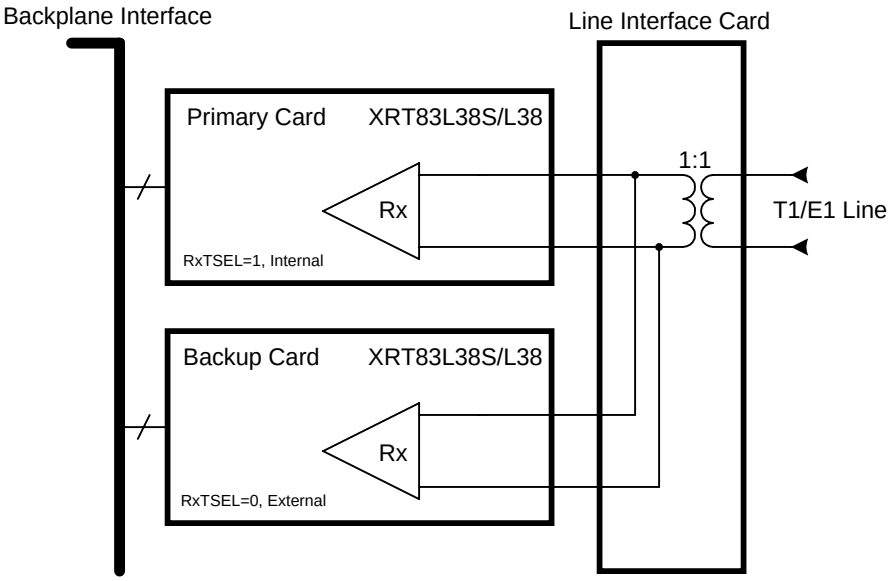

Figure 4b. Simplified Block Diagram of the Receive Section for a 1+1 Redundancy Scheme Using One Common Transformer

N+1 REDUNDANCY

N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. However, the relays create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in "internal" impedance mode, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

TRANSMIT

For N+1 redundancy, the transmitters on all cards should be programmed for “internal” impedance mode providing one bill of materials for T1/E1/J1. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 5. for a simplified block diagram of the transmit section for an N+1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

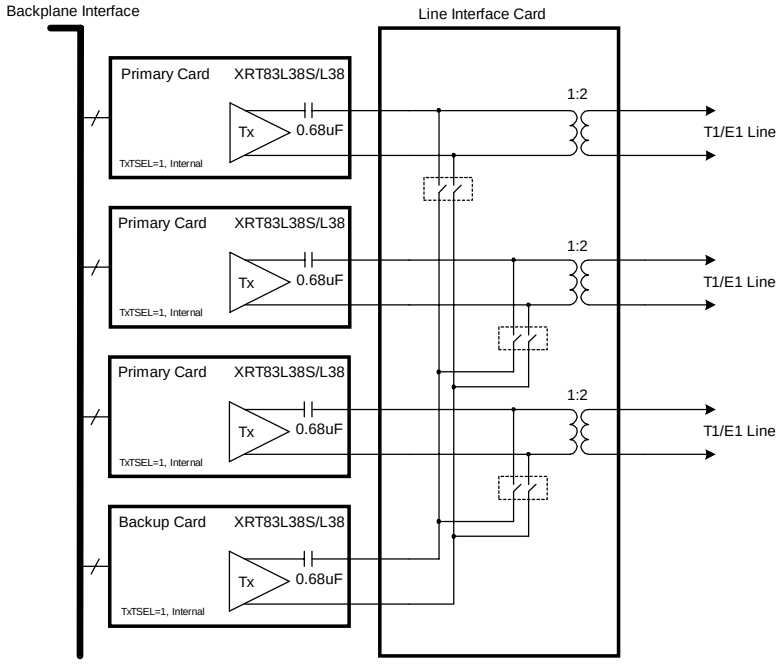

Figure 5. Simplified Block Diagram of the Transmit Section for an N+1 Redundancy Scheme

RECEIVE

For N+1 redundancy, the receivers on the primary cards should be programmed for “internal” impedance mode. The receivers on the backup card should be programmed for “external” impedance mode. Since there is no external resistor in the circuit, the receivers on the backup card will be high impedance. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to “internal” impedance mode, then the primary card to “external” impedance mode. See Figure 6. for a simplified block diagram of the receive section for a N+1 redundancy scheme. (For simplification, the overvoltage protection circuitry was omitted. For a reference design in overvoltage protection, please see the Overvoltage Protection Application Note)

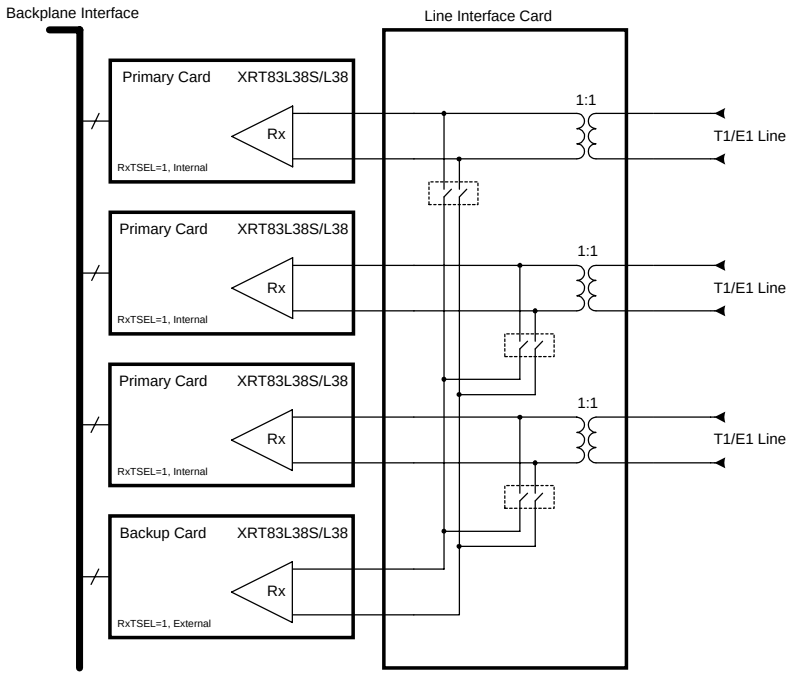

Figure 6. Simplified Block Diagram of the Receive Section for an N+1 Redundancy Scheme

TEST DATA and LABORATORY SETUP

When connecting a back up card to the primary card in redundancy applications, the LIU must meet T1/E1 physical layer requirements. The most critical physical layer requirements are pulse template, receive sensitivity, and jitter tolerance.

PULSE TEMPLATE

As with most physical layer requirements, T1 and E1 have different specifications to meet. However, the lab setup is very similar. Figure 7 is a simplified block diagram of the lab setup used to measure the pulse template of EXAR's XRT83SL38. The cable length simulator can be configured to test either T1 or E1 according to the value set from the control panel. For T1, the maximum cable loss specification is 655ft. For E1, the cable length is usually within 6ft. Figure 8 is a plot of the pulse template taken from the T1 setup. Figure 9 is a plot of the pulse template taken from the E1 setup.

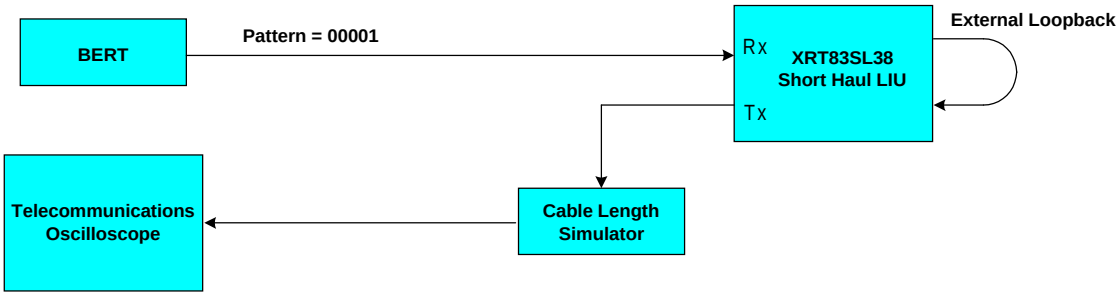

Figure 7 Simplified Lab Setup for Pulse Template Measurements

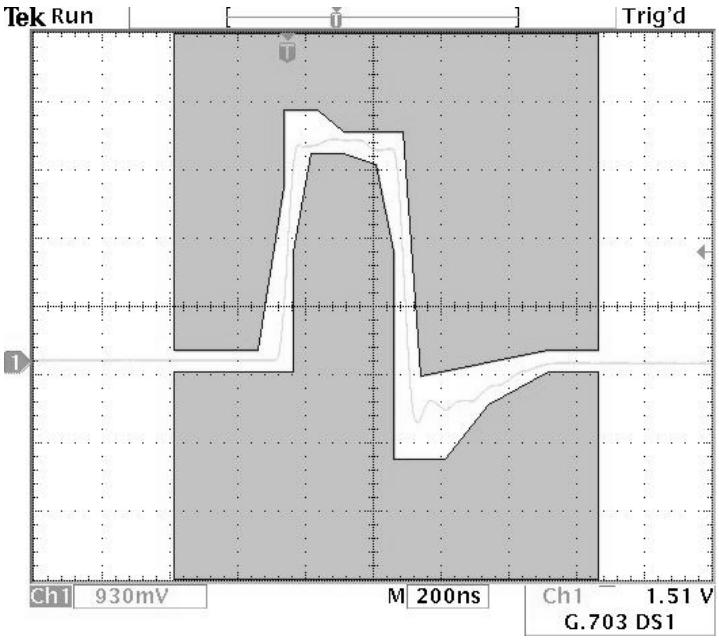

Figure 8 Pulse Template for T1 100ohm Impedance

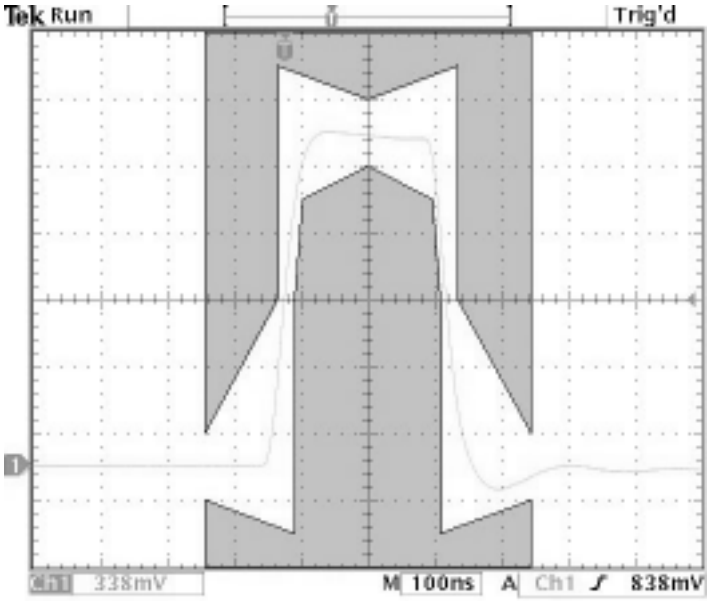

Figure 9 Pulse Template for E1 75ohm Impedance

RECEIVE SENSITIVITY

Receive sensitivity is measured by attenuating the receive inputs until an alarm status occurs such as LOS, LOF, Bit Errors, etc. Figure 10 is a simplified block diagram of the lab setup used to measure the receive sensitivity of EXAR's XRT83SL38. For short haul T1 applications, the maximum cable loss specification is 655ft of cable loss and 6dB of flat loss. For E1, the maximum cable loss is 6dB and a flat loss of 12dB. For both T1 and E1, the XRT83SL38 was able to receive signals attenuated up to 3,096ft of cable loss or 19dB of flat loss in the short haul mode.

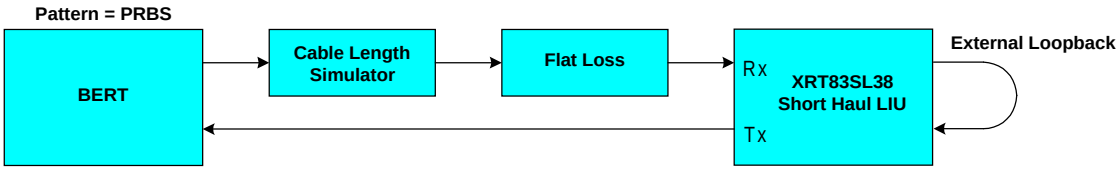

Figure 10 Simplified Lab Setup for Receive Sensitivity Measurements

JITTER TOLERANCE

The jitter tolerance is measured by adding jitter to the receiver inputs until there is a specified number of bit errors within a given time interval (known as Gate Time). For T1, the frequency (rate of deviation) added to the receiver inputs is from 10Hz to 40kHz. For E1, the frequency is from 10Hz to 100kHz. Figure 11 is a plot of the jitter tolerance with the jitter attenuator (JA) disabled. For optimum performance, the JA should be configured in the receive path of the XRT83SL38 (see the XRT83SL38 datasheet for more information).

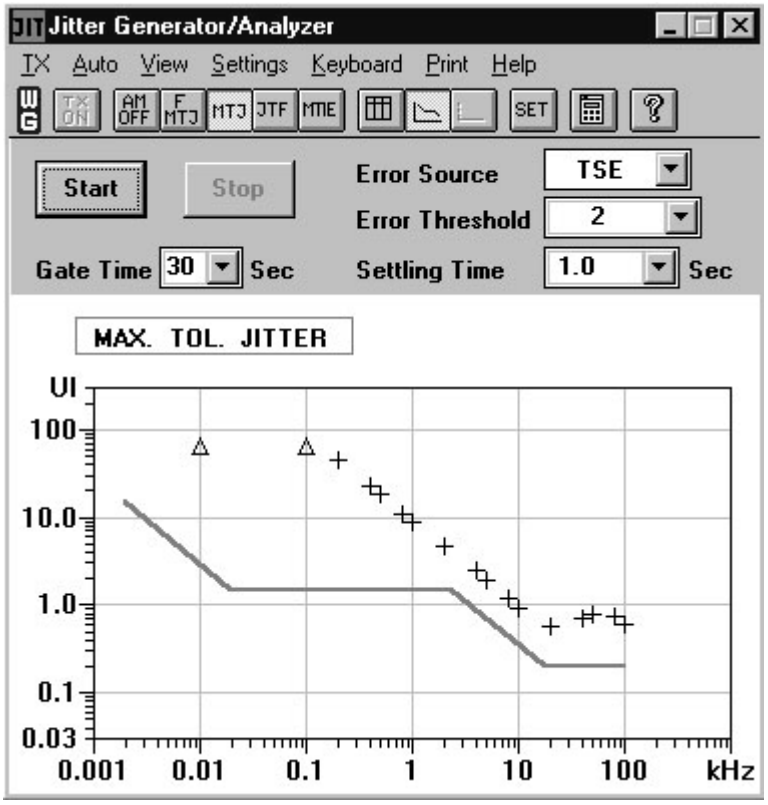

Figure 11 Jitter Tolerance for E1 75ohm