TAN-059

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Experience Our Connectivity

DS-1/E1 Line Recovered Clock PLL Timing

INTRODUCTION

The analog interface of Exar LIU devices contains a CDR (Clock and Data Recovery) block that recovers a clock signal from the incoming data. This clock signal derives its timing and phase from the received input data. In the event that data is disconnected from Rtip and Rring or an RLOS condition occurs, the Recovered Clock (RCLK) will switch over to an internal master clock derived from the MCLK input pin to the PLL. The Recovered Clock will remain in phase with MCLK until the Loss of Data condition is cleared. Once RLOS is cleared, RCLK will switch back to the Recovered Clock signal derived from the CDR block. The timing diagram and specifications are listed below in Figure 1 and Table 1.

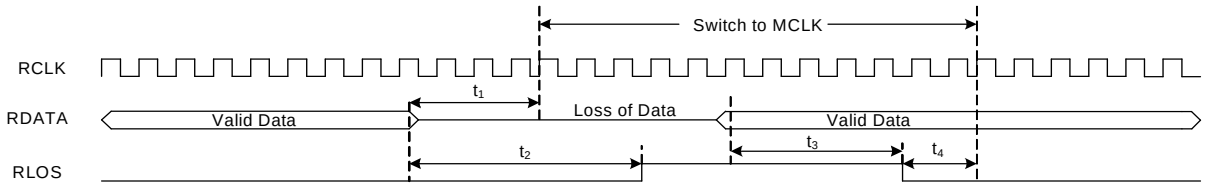

Figure 1. PLL Recovered Clock Timing

PLL Recovered Clock Timing Specifications					
Symbol	**Parameter**	**Min**	**Typical**	**Max DS1**	**Max E1**
t_1	Switch from RCLK to MCLK	-	-	19.4µS	14.6µS
t_2	RLOS pin declares loss of data	-	see Note 3	-	-
t_3	RLOS pin clears loss condition	-	see Note 3	-	-
t_4	Switch back to RCLK	-	-	23.9µS	18.1µS

Table 1. PLL Recovered Clock Timing Specifications

Notes:

1. *The Phase Shift from RCLK to MCLK or from MCLK back to RCLK will be equal to the phase difference between the external oscillator provided to the MCLK input pin and the incoming data.*
2. *There will be NO gaps on the RCLK pin during any timing events unless the external oscillator is faulty.*
3. *RLOS declaration and clearance depends on the LIU and which mode it's configured in. The LIU supports both G.775 and ETSI-300-233. Refer to the product Datasheet for more details.*