XRT86VL3X

Applications Note

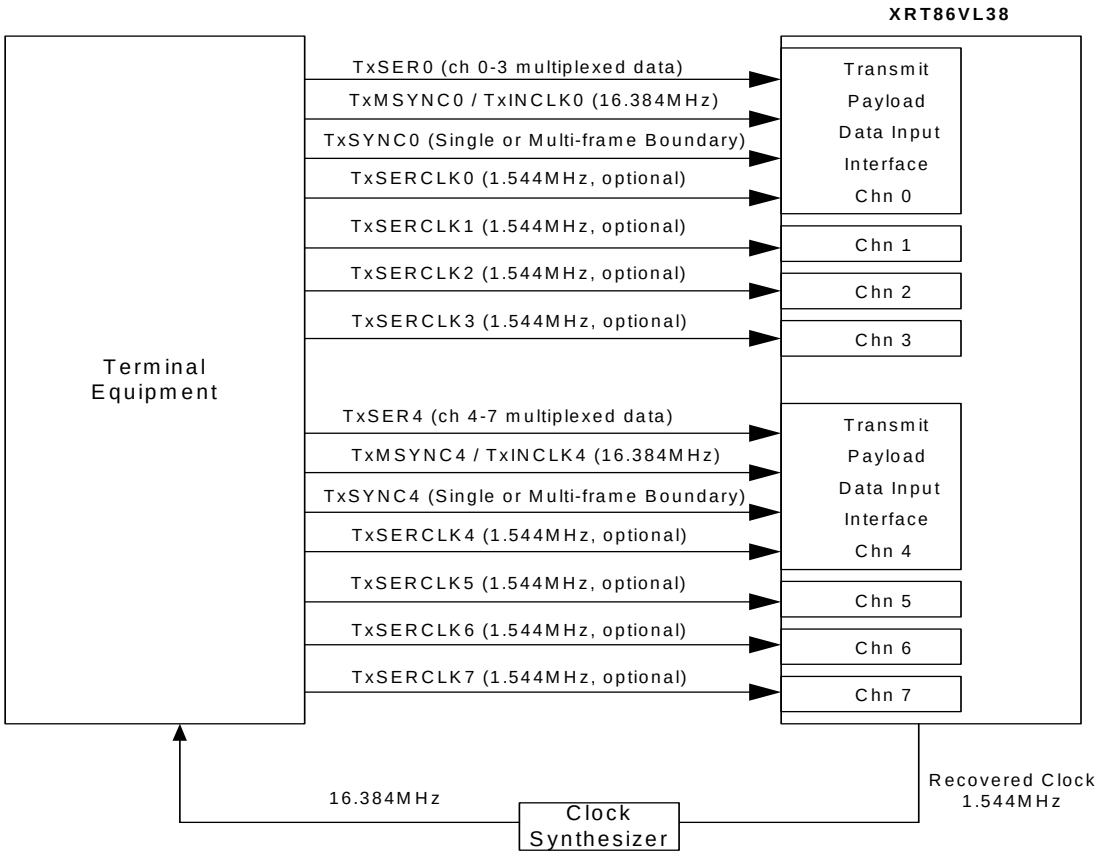
HMVIP High Speed Backplane Interface Operation and Timing

T1 Transmit HMVIP Backplane Interface

T1 Transmit HMVIP Interface Signals

When the T1 transmit framer block is configured in the HMVIP backplane mode, all signals are configured as inputs to the Transmit Payload Data Input Interface block. The Transmit Payload Data Input Interface will consist of the following signals shown in Figure 1 below.

Figure 1: Interface Signals to the Transmit Payload Data Input Interface Block in T1 HMVIP Backplane Mode



Terminal Equipment will need to supply a 16.384MHz clock to the TxMSYNC/TxINCLK pin on Channel 0 and Channel 4 as the high-speed bus input clock. (In high-speed mode, TxMSYNC is referred to as the TxINCLK signal from here on). In addition, Terminal Equipment should supply a multi-frame or single-frame boundary pulse on the TxSYNC pin for the framer to locate the beginning of the multiplexed frame. Single-frame or multi-frame pulse is selected in the Synchronization Mux Register (address: 0xn109).

Multiplexed data on channels 0 –3 should be provided on the TxSER pin of channel 0 at 16.384MHz and multiplexed data on channels 4-7 should be provided on the TxSER pin of channel 4 at 16.384MHz. Terminal Equipment can optionally supply a 1.544MHz clock to the TxSERCLK pins for each channel. The framer will use the TxSERCLK as the timing reference for the transmit line interface of the device. If the device is configured in loop-timing, or internal timing mode, Terminal Equipment will not need to provide the TxSERCLK as inputs to the device.

It is the responsibility of the Terminal Equipment to phase-lock the TxSERCLK and TxINCLK to the Recovered Clock of the XRT86VL38 in order to prevent any transmit slip events from occurring. In HMVIP mode, the recovered clock of each channel within the device is output to a hardware pin - RxCHNn_4/RxSCLKn when the fractional/signaling interface is enabled. *

* Receive fractional/signaling interface is enabled by programming RxFr1544 (bit 4 in register 0xn122) to '1'.

Multiplexing Scheme

Terminal Equipment multiplexes payload data of every four channels into one serial data stream at 16.384MHz, and provides multiplexed payload data at the rising edge of TxINCLK. The Transmit Payload Data Input Interface then latches the data on TxSER at falling edge of the TxINCLK.

Terminal Equipment multiplexes four channels of 1.544MHz into one serial stream at 16.384MHz as described below:

1) The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet of the 16.384MHz-multiplexed stream.

First Octet of the 16.384Mbit/s Data Stream

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

where Fn = F-bit of Channel N

2) After the first octet of data is sent, Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.

3) After framing bits of all 4 channels are sent, Terminal Equipment will start sending the payload bits of all 4 channels. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0. After all 8 bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1, 2, and 3. After all 8 bits of Timeslot 0 of all four channels are sent, it will start sending the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how the 9^{th} to 16^{th} octets of the 4 channels multiplexed data should be provided on the TxSER pin at 16.384MHz.

9th to 16th Octets of the 16.384Mbit/s Data Stream

Octet	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
9	1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0
10	5_0	5_0	6_0	6_0	7_0	7_0	8_0	8_0
11	1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1
12	5_1	5_1	6_1	6_1	7_1	7_1	8_1	8_1
13	1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2
14	5_2	5_2	6_2	6_2	7_2	7_2	8_2	8_2
15	1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3
16	5_3	5_3	6_3	6_3	7_3	7_3	8_3	8_3

where Xn = The Xth payload bit of Channel N

4) After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream. Terminal Equipment should continue to stuff “don’t care” bits every time after 3 time-slot of payload data of all four channels are sent in order to create the 16.384MHz data stream, as described in the table below.

Table below shows how T1 data can be mapped into 16.384MHz data in the byte-multiplexed mode

Mapping of T1 Data into a 16.384Mbit/s Serial Data Stream

F_0 F_0 F_1 F_1 F_2 F_2 F_3 F_3	56 cycles	TS0	TS1	TS2	64 cycles	TS3	TS4	TS5
	Don't' Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
	64 cycles	TS6	TS7	TS8	64 cycles	TS9	TS10	TS11
	Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
	64 cycles	TS12	TS13	TS14	64 cycles	TS15	TS16	TS17
	Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
	64 cycles	TS18	TS19	TS20	64 cycles	TS21	TS22	TS23
	Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles

For HMVIP mode, the Transmit Single-frame Synchronization signal (TxSYNC) should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The XRT86VL38 device supports either positive or negative polarity on the TxSYNC signal, therefore, Terminal Equipment can provide TxSYNC to be active high or active low.

TxSYNC of Channel 0 pulses HIGH or LOW to identify the start of multiplexed data stream of Channel 0-3. TxSYNC of Channel 4 pulses HIGH or LOW to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH or LOW pulse on the TxSYNC signal, the framer can locate the position of the beginning of a multiplexed T1 frame. It is the responsibility of the Terminal Equipment to align the multiplexed serial data with the TxSYNC pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT86L38 and send to the LIU interface.

Signaling Insertion

Signaling information can be embedded on the transmit serial input (TxSER), or it can be inserted from the TxSIG/TxCHN[0] pin or from the TSCR registers (0xn340-n357) as shown in Figure 2. When inserting signaling from TxSIG pin, signaling bit A of the corresponding time slot is repeated and sent via the TxSIG pin when the Terminal Equipment is sending the 5th payload bit of that time slot.

Similarly, signaling bit B, C, and D of the corresponding time slot is repeated and sent via the TxSIG pin when the Terminal Equipment is providing the 6th, 7th, and 8th payload bit of that time slot. Every time slot has its own signaling data on the TxSIG pin. Figure 3 shows the timing diagram of the signals on TxSIG and TxSER when signaling is inserted from the TxSIG pin.

Figure 2: Signaling Insertion on the Transmit side

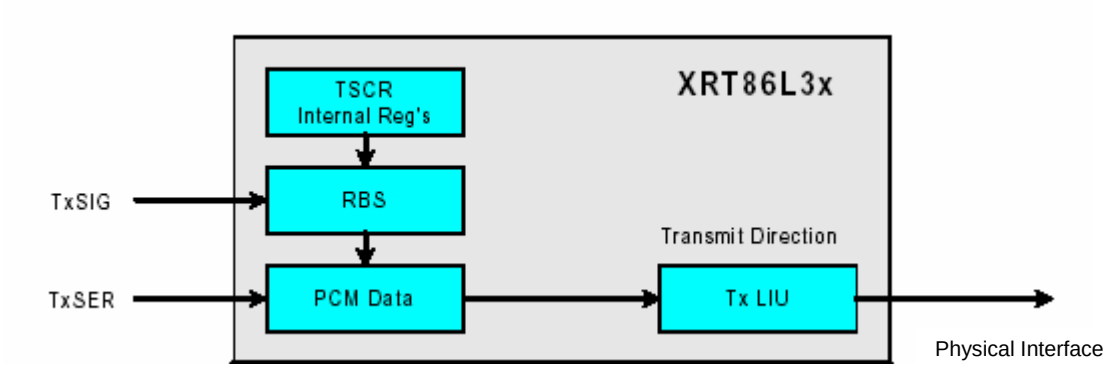
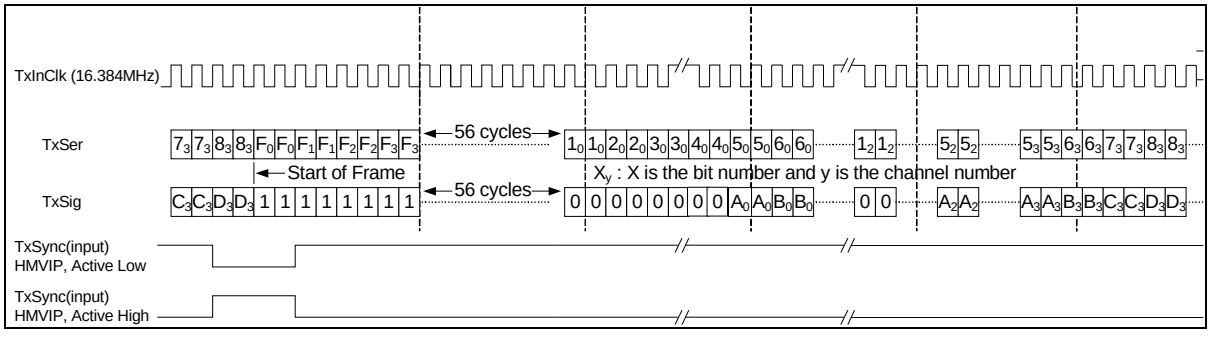


Figure 3: Timing signals when the T1 transmit framer is running at HMVIP 16.384MHz Mode

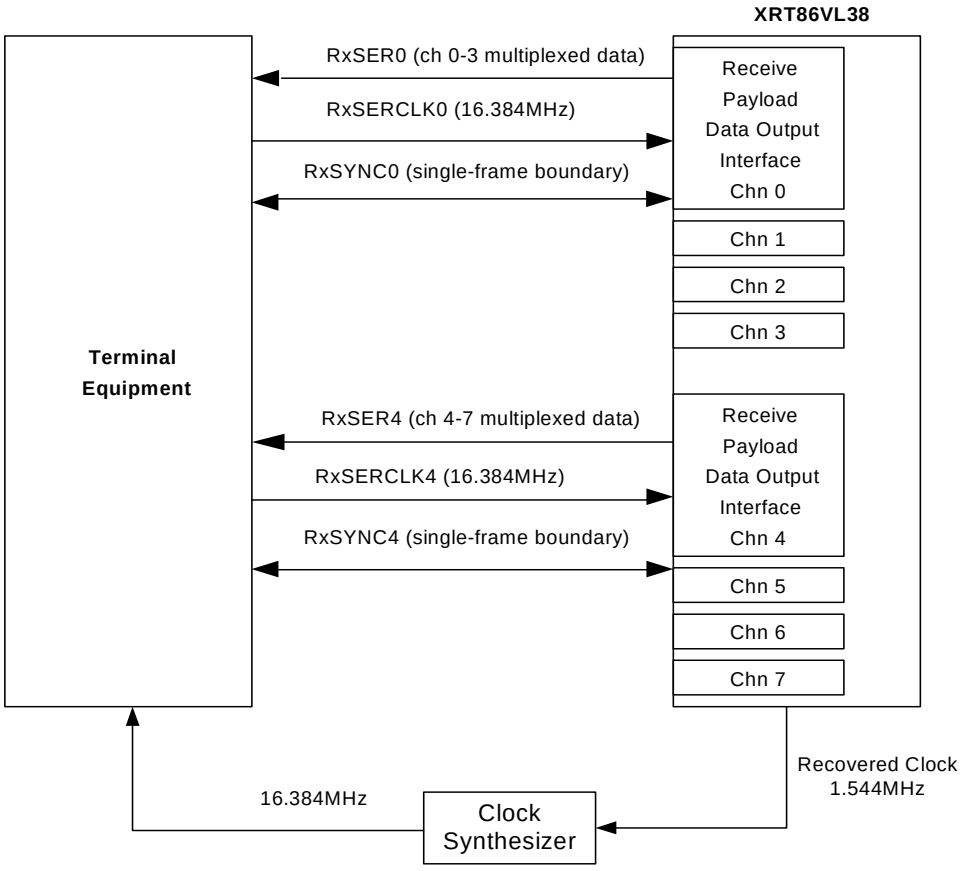


T1 Receive HMVIP Backplane Interface

T1 Receive HMVIP Interface Signals

When the T1 receive framer block is configured in the HMVIP backplane mode, RxSERCLK is configured as a clock input, RxSYNC can be configured as either input or output, and RxSER is always an output to the Receive Payload Data Output Interface block, as shown in Figure 4 below.

Figure 4: Interface Signals to the Receive Payload Data Output Interface Block in T1 HMVIP Backplane Mode



Terminal Equipment will need to supply a 16.384MHz high-speed clock to the RxSERCLK pin on Channel 0 and Channel 4 as the timing reference for the backplane interface. If the receive slip buffer is enabled, Terminal Equipment should also supply a single-frame boundary pulse on the RxSYNC pin for the framer to output the beginning of a multiplexed frame.

If the receive slip buffer is bypassed, then the single-frame boundary pulse will be output on the RxSYNC pin.

It is the responsibility of the Terminal Equipment to phase-lock the RxSERCLK to the Recovered Clock of the XRT86VL38 to prevent any receive slip events from occurring.

In HMVIP mode, the recovered clock of each channel within the device is output to a hardware pin - RxCHNn_4/RxSCLKn when the fractional/signaling interface is enabled.*

* Receive fractional/signaling interface is enabled by programming RxFr1544 (bit 4 in register 0xn122) to '1'.

Multiplexing Scheme

The receive framer multiplexes payload data of four channels from the line side and output one serial data stream at 16.384MHz to the backplane interface. The Receive Back-plane Interface then outputs multiplexed data of channels 0-3 on RxSER0 and multiplexed data of channels 4-7 on RxSER4 pins at 16.384Mbit/s.

Following the same multiplexing scheme as in the transmit side, the receive framer will repeat each framing bit and payload bits for all 4 channels and group them together in a byte-interleaved way, stuff in "Don't Care Bits" (56 cycles after the F-bits, and 64 cycles after every 3 time slots as indicated below.

Mapping of T1 Data into 16.384Mbit/s Data Stream

F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3	56 cycles	TS0	TS1	TS2	64 cycles	TS3	TS4	TS5
								Don't' Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
								64 cycles	TS6	TS7	TS8	64 cycles	TS9	TS10	TS11
								Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
								64 cycles	TS12	TS13	TS14	64 cycles	TS15	TS16	TS17
								Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles
								64 cycles	TS18	TS19	TS20	64 cycles	TS21	TS22	TS23
								Don't Care	64 Cycles	64 Cycles	64 Cycles	Don't Care	64 Cycles	64 Cycles	64 Cycles

The multiplexing scheme on the receive side is the same as the multiplexing scheme on the transmit side. Please refer to the Transmit Section for the detailed description of the multiplexing scheme.

Signaling Extraction

Signaling data can be passed through and output on the receive serial output (RxSER), or it can be extracted to the Receive Signaling Output (RxSIG), as well as the Receive Signaling Array Registers (RSAR) as shown in Figure 5. When signaling substitution is enabled, signaling data on RxSER will be replaced by the signaling data contained in the Receive Signaling Substitution Register (address: 0xn3C0-0xn3DF). However, signaling data extracted to RxSIG and RSAR remain unchanged when signaling substitution is enabled.

When extracting signaling information to the RxSIG pin, signaling bit A of the corresponding channel will be repeated and output to the RxSIG pin when the receive framer is outputting the 5th bit of that channel. Following the same pattern, signaling bits B, C, and D will be repeated and output to RxSIG pin when the receive framer is outputting the 6th, 7th, 8th bit of that channel as shown in Figure6.

Figure 5: Signaling Extraction and Substitution on the receive side

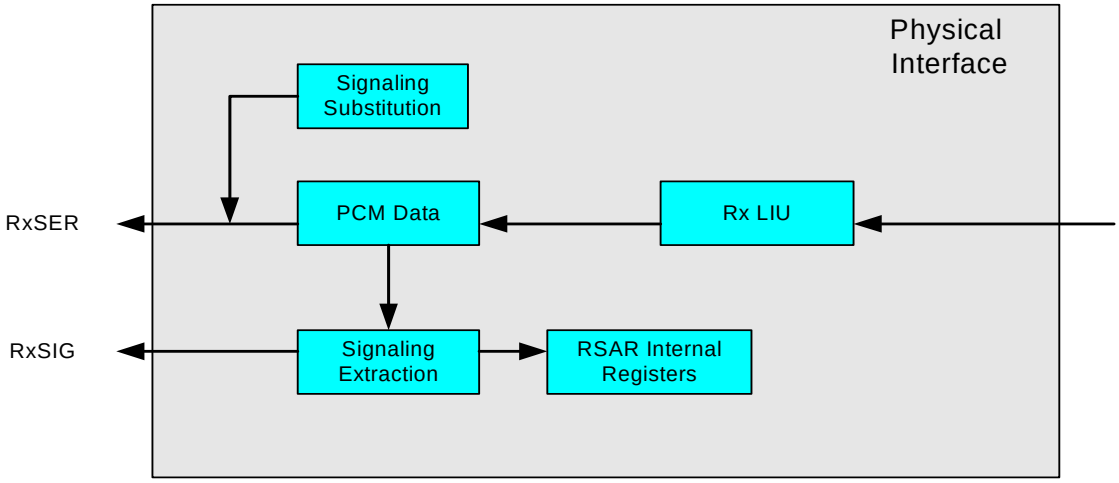
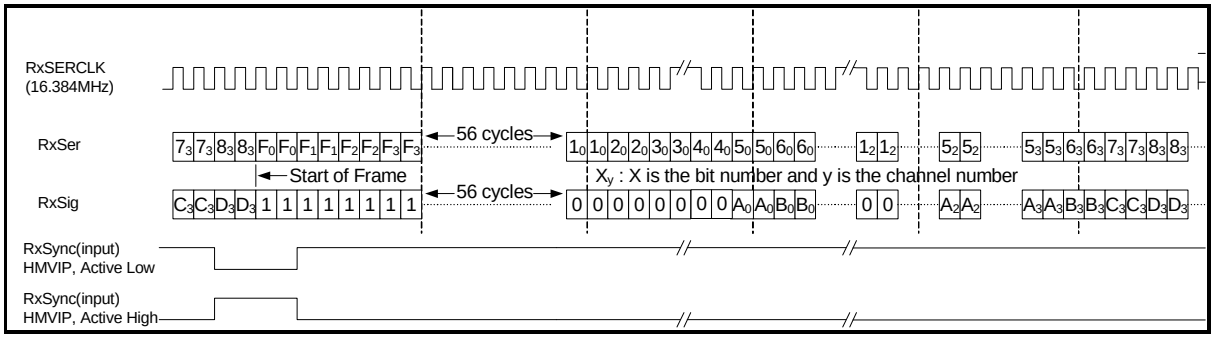


Figure 6: Timing signals when the T1 receive framer is running at HMVIP 16.384MHz Mode

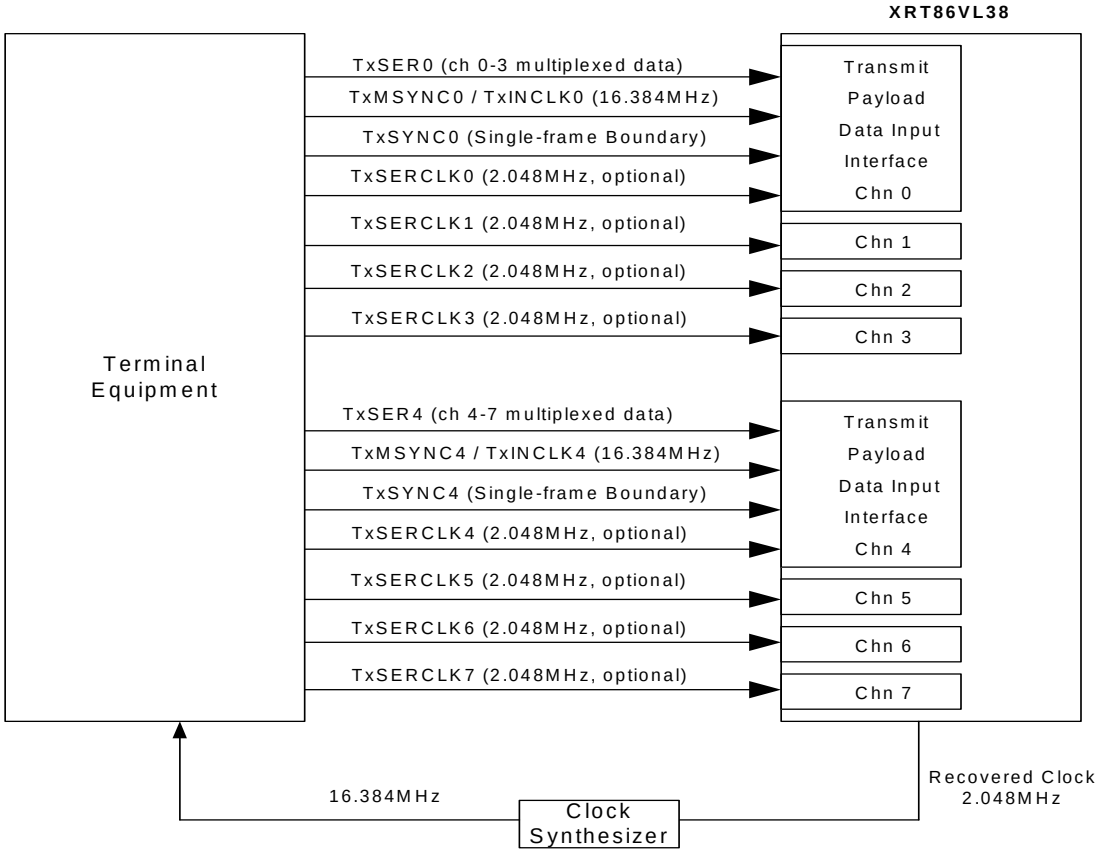


E1 Transmit HMVIP Backplane Interface

E1 Transmit HMVIP Interface Signals

In E1 HMVIP mode, the backplane interface signals are similar to that of the T1 mode. The main differences between T1 and E1 modes are the reference line clock rate (TxSERCLK), handling of the framing bits and frame boundary pulse, and the addition of "Don't Care" bits for T1 mode. All backplane interface signals on the transmit side are configured as inputs to the Transmit Payload Data Input Interface block as shown in Figure 5 below.

Figure 7: Interface Signals to the Transmit Payload Data Input Interface Block in E1 HMVIP Backplane Mode



Terminal Equipment will need to supply a 16.384MHz clock to the TxMSYNC/TxINCLK pin on Channel 0 and Channel 4 as the high-speed bus input clock. (In high-speed mode, TxMSYNC is referred to as the TxINCLK signal from here on). In addition, Terminal Equipment should supply a single-frame boundary pulse on the TxSYNC pin for the framer to locate the beginning of the multiplexed frame.

Multiplexed data on channels 0 –3 should be provided on the TxSER pin of channel 0 at 16.384MHz and multiplexed data on channels 4-7 should be provided on the TxSER pin of channel 4 at 16.384MHz. Terminal Equipment can optionally supply a 2.048MHz clock to the TxSERCLK pins for each channel. The framer will use the TxSERCLK as the timing reference for the transmit line interface of the device. If the device is configured in loop-timing, or internal timing mode, Terminal Equipment will not need to provide the TxSERCLK as inputs to the device.

It is the responsibility of the Terminal Equipment to phase-lock the TxSERCLK and TxINCLK to the Recovered Clock of the XRT86VL38 in order to prevent any transmit slip events from occurring. In HMVIP mode, the recovered clock of each channel within the device is output to a hardware pin - RxCHNn_4/RxSCLKn when the fractional/signaling interface is enabled. *

* Receive fractional/signaling interface is enabled by programming RxFr2048 (bit 4 in register 0xn122) to ‘1’.

Multiplexing Scheme

Terminal Equipment multiplexes payload data of every four channels into one serial data stream at 16.384MHz, and provides multiplexed payload data at the rising edge of TxINCLK. The Transmit Payload Data Input Interface then latches the data on TxSER at falling edge of the TxINCLK.

Terminal Equipment multiplexes four channels of 2.048MHz into one serial stream at 16.384MHz as described below:

1) The FAS bits of Channel 0 are repeated and grouped together to form the first octet of the multiplexed data stream. The FAS bit of Channel 0 is sent first, followed by FAS bit of Channel 1 and 2. The FAS bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet of the 16.384MHz-multiplexed stream.

First Octet of the 16.384Mbit/s Data Stream

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
F_0	F_0	F_0	F_0	F_0	F_0	F_0	F_0

where Fn = F-bit of Channel N

2) After the FAS/NON-FAS bits of Channel 0-3 are sent in the first 8 octets, Terminal Equipment starts sending the payload bits of each channel. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0. After all 8 bits of Timeslot 0 within Channel 0 are sent, Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1, 2, and 3. After the payload bits of Timeslot 0 of all four channels are sent, it will start sending the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how the 9^{th} to 16^{th} octets of the 4 channels multiplexed data should be provide on the TxSER pin at 16.384MHz.

9th to 16th Octets of the 16.384Mbit/s Data Stream

Octet	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
9	1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0
10	5_0	5_0	6_0	6_0	7_0	7_0	8_0	8_0
11	1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1
12	5_1	5_1	6_1	6_1	7_1	7_1	8_1	8_1
13	1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2
14	5_2	5_2	6_2	6_2	7_2	7_2	8_2	8_2
15	1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3
16	5_3	5_3	6_3	6_3	7_3	7_3	8_3	8_3

where Xn = The Xth payload bit of Channel N

Unlike in T1 mode, Terminal Equipment need not stuff in “Don’t Care” bits every 3 time slots to create a 16.384MHz data stream. E1 data is mapped into 16.384MHz data in the byte-multiplexed mode as shown in the table below.

Mapping of E1 Data into a 16.384Mbit/s Serial Data Stream

FAS/NON-FAS	TS0	TS1	TS2	TS3	TS4	TS5
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles
TS6	TS7	TS8	TS9	TS10	TS11	TS12
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles
TS13	TS14	TS15	TS16	TS17	TS18	TS19
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles
TS20	TS21	TS22	TS23	TS24	TS25	TS26
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles
TS27	TS28	TS29	TS30	TS31		
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles		

For HMVIP mode, the Transmit Single-frame Synchronization signal (TxSYNC) should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The XRT86VL38 device supports either positive or negative polarity on the TxSYNC signal, therefore, Terminal Equipment can provide TxSYNC to be active high or active low.

TxSYNC of Channel 0 pulses HIGH or LOW to identify the start of multiplexed data stream of Channel 0-3. TxSYNC of Channel 4 pulses HIGH or LOW to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH or LOW pulse on the TxSYNC signal, the framer can position the beginning of the multiplexed T1 frame. It is the responsibility of the Terminal Equipment to align the multiplexed serial data with the TxSYNC pulse.

The framing bits, signaling, and payload data are de-multiplexed inside the XRT86VL38 and send to the LIU interface.

Signaling Insertion

Signaling information can be embedded on the transmit serial input (TxSER) or it can be inserted from the TxSIG/TxCHN[0] pin or from the TSCR registers (0xn340-0xn357) as shown in Figure 8. When inserting signaling from TxSIG pin, signaling bit A of the corresponding time slot is repeated and sent via the TxSIG pin when the Terminal Equipment is sending the 5th payload bit of that time slot.

Similarly, signaling bit B, C, and D of the corresponding time slot is repeated and sent via the TxSIG pin when the Terminal Equipment is providing the 6th, 7th, and 8th payload bit of that time slot. Every time slot has its own signaling data on the TxSIG pin. Figure 9 shows the timing diagram of the signals on TxSIG and TxSER when signaling is inserted from the TxSIG pin.

Figure 8: Signaling Insertion on the Transmit side

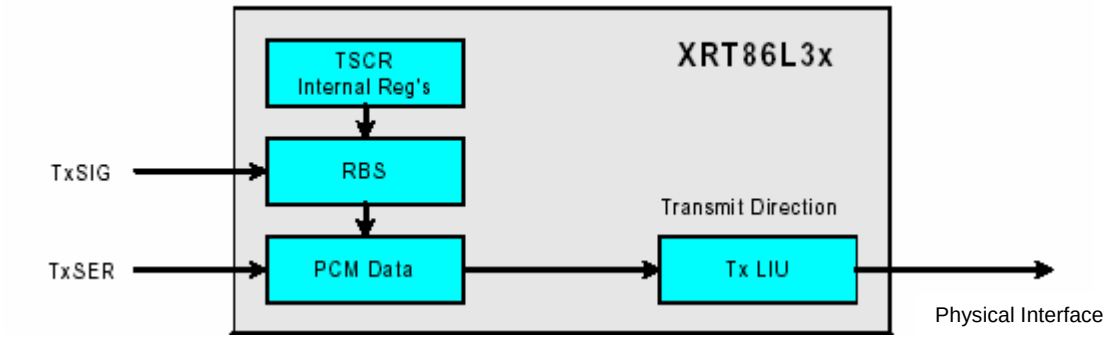
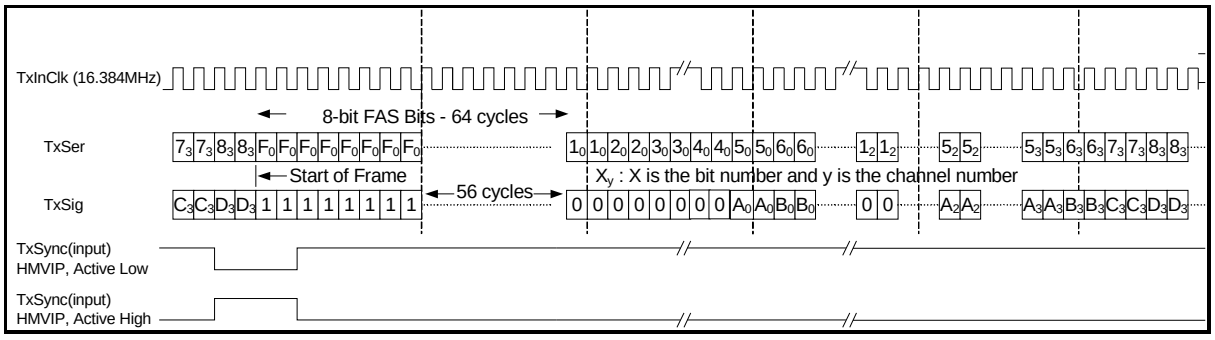


FIGURE 9: TIMING SIGNALS WHEN THE E1 TRANSMIT FRAMER IS RUNNING AT HMVIP 16.384MHZ MODE

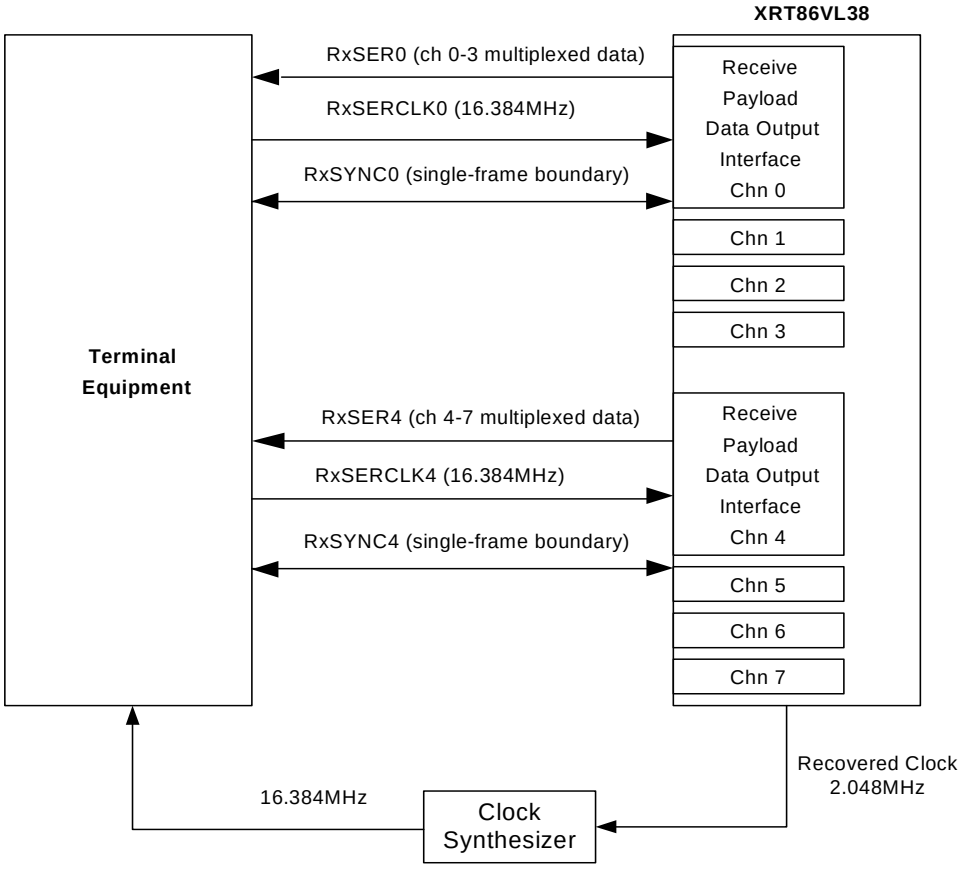


E1 Receive HMVIP Backplane Interface

E1 Receive HMVIP Interface Signals

When the E1 receive framer block is configured in the HMVIP backplane mode, RxSERCLK is configured as a clock input, RxSYNC can be configured as either input or output, and RxSER is always an output to the Receive Payload Data Output Interface block, as shown in Figure 10 below.

FIGURE 10: INTERFACE SIGNALS TO THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK IN E1 HMVIP BACKPLANE MODE



Terminal Equipment will need to supply a 16.384MHz high-speed clock to the RxSERCLK pin on Channel 0 and Channel as the timing reference for the backplane interface. If the receive slip buffer is enabled, Terminal Equipment should also supply a single-frame

boundary pulse on the RxSYNC pin for the framer to output the beginning of a multiplexed frame.

If the receive slip buffer is bypassed, then the single-frame boundary pulse will be output on the RxSYNC pin.

It is the responsibility of the Terminal Equipment to phase-lock the RxSERCLK to the Recovered Clock of the XRT86VL38 to prevent any receive slip events from occurring.

In HMVIP mode, the recovered clock of each channel within the device is output to a hardware pin - RxCHNn_4/RxSCLKn when the fractional/signaling interface is enabled.*

* Receive fractional/signaling interface is enabled by programming RxFr2048 (bit 4 in register 0xn122) to '1'.

Multiplexing Scheme

The receive framer multiplexes payload data of four channels from the line side and output one serial data stream at 16.384MHz to the backplane interface. The Receive Back-plane Interface then outputs multiplexed data of channels 0-3 on RxSER0 and multiplexed data of channels 4-7 on RxSER4 pin at 16.384Mbit/s.

Following the same multiplexing scheme as in the transmit side, the receive framer will repeat each FAS/NON-FAS and payload bits for all 4 channels and group them together in a byte-interleaved way as described in the figure below.

Mapping of E1 Data into 16.384Mbit/s Data Stream

FAS/NON-FAS	TS0	TS1	TS2	TS3	TS4	TS5
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles

TS6	TS7	TS8	TS9	TS10	TS11	TS12
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles

TS13	TS14	TS15	TS16	TS17	TS18	TS19
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles

TS20	TS21	TS22	TS23	TS24	TS25	TS26
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles

TS27	TS28	TS29	TS30	TS31
64 Cycles	64 Cycles	64 Cycles	64 Cycles	64 Cycles

Signaling Extraction

Signaling data can be passed through and output on the receive serial output (RxSER), or it can be extracted to the Receive Signaling Output (RxSIG), as well as the Receive Signaling Array Registers (RSAR) as shown in Figure 11. When signaling substitution is enabled, signaling data on RxSER will be replaced by the signaling data contained in the Receive Signaling Substitution Register (address: 0xn3C0-0xn3DF). However, signaling data extracted to RxSIG and RSAR remain unchanged when signaling substitution is enabled.

When extracting signaling information to the RxSIG pin, signaling bit A of the corresponding channel will be repeated and output to the RxSIG pin when the receive framer is outputting the 5th bit of that channel. Following the same pattern, signaling bits B, C, and D will be repeated and output to RxSIG pin when the receive framer is outputting the 6th, 7th, 8th bit of that channel as shown in Figure 12.

Figure 11: Signaling Extraction and Substitution on the receive side

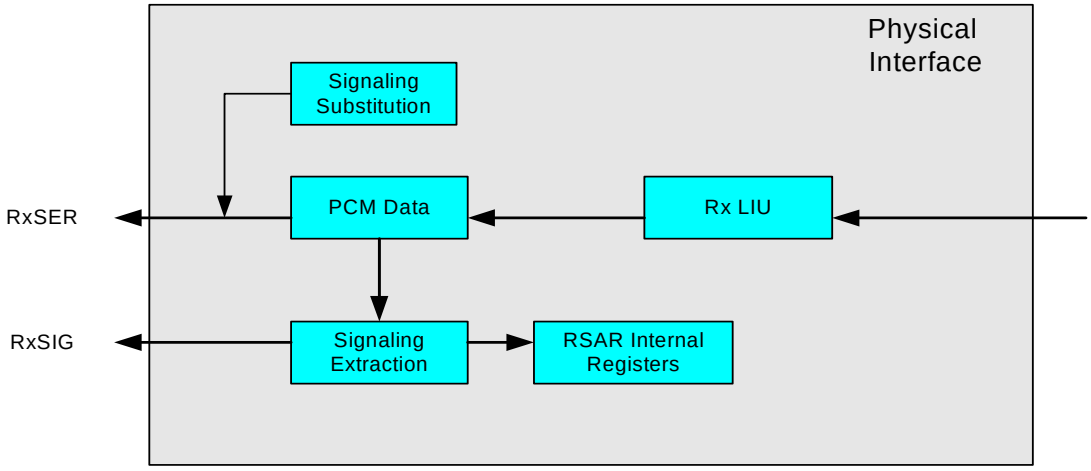
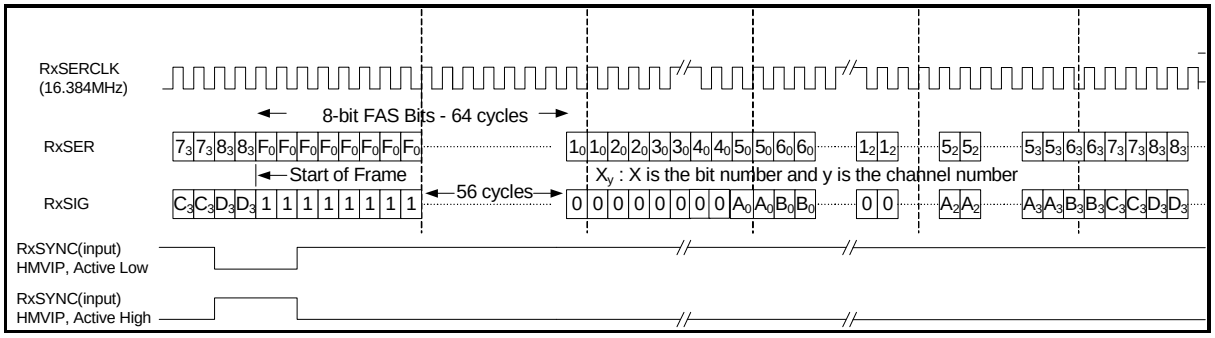


FIGURE 12: TIMING SIGNALS WHEN THE E1 RECEIVE FRAMER IS RUNNING AT HMVIP 16.384MHZ MODE



Configuring the Transmit T1/E1 Framer in HMVIP High-Speed Backplane Interface mode:

The following steps provide the necessary steps to configure the device in HMVIP mode after the basic configuration for T1 or E1 mode has been loaded.

1. Select loop-timing, internal-timing, or external timing modes.

Using loop-timing or internal timing modes, Terminal Equipment need not provide a clock to the TxSERCLK pin. The transmit framer will use the recovered clock or internal clock derived from MCLKIN input as the timing reference for the transmit section of the device. If external timing is used, Terminal Equipment will need to provide a 1.544MHz (for T1) and a 2.048MHz (for E1) clock to the TxSERCLK pin on each channel as clock inputs to the Transmit Payload Data Input Interface Block.

Register 0xn100 – CLOCK SELECT REGISTER (CSR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3-2	Bit 1	Bit 0
BPVI	IST1	8kHZ	CLDET	Reserved	CSS[1]	CSS[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

Select loop-timing mode (i.e. Select recovered clock as transmit timing reference):

Set CSS[1:0] to ‘00’ or ‘11’ to select loop-timing mode.

Select internal-timing mode (i.e. Select internal clock derived from MCLKIN input as transmit timing reference):

Set CSS[1:0] to ‘10’ to select internal-timing mode.

Select external-timing mode (i.e. Select TxSERCLK as transmit timing reference):

Set CSS[1:0] to ‘01’ to select external-timing mode.

2. Enable the high-speed backplane multiplexed bus.

Set TxMUXEN, Bit 2 in the Transmit Interface Control Register (TICR) to '1'.

Register 0xn120 – TRANSMIT INTERFACE CONTROL REGISTER (TICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
TxSYNC FRD	Reserved	TxSYNC Is LOW	TxFR1544/ TxFR2048	TxICLKINV	TxMUXEN	TxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

3. Enable the HMVIP high-speed backplane multiplexed mode at 16.384MHz.

Set TxIMODE, Bit 1-0 in the Transmit Interface Control Register (TICR) to '10'.

Register 0xn120 – TRANSMIT INTERFACE CONTROL REGISTER (TICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
TxSYNC FRD	Reserved	TxSYNC Is LOW	TxFR1544/ TxFR2048	TxICLKINV	TxMUXEN	TxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

By default, the XRT86VL38 device is configured in the 12.352MHz bit multiplexed high-speed mode once the TxMUXEN is set to '1' in T1 mode.

4. The 86VL38 device has the ability to support either positive or negative polarity on the transmit framer boundary signal (TxSYNC).

Select TxSYNC to be Active 'HIGH' or Active 'LOW'. Set TxSYNCIsLOW, Bit 5 in the Transmit Interface Control Register (TICR) to '0' to select TxSYNC to be active 'HIGH'. Setting this bit to '1' will select TxSYNC to be active 'LOW'.

Register 0xn120 – TRANSMIT INTERFACE CONTROL REGISTER (TICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
TxSYNC FRD	Reserved	TxSYNC Is LOW	TxFR1544/ TxFR2048	TxICLKINV	TxMUXEN	TxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

5. **(T1 Mode ONLY)** Select TxSYNC to be Single-frame boundary or Multi-frame boundary.

Set MSYNC, Bit 5 in the Synchronization Mux Register (SMR) to '1' to select TxSYNC to be multi-frame boundary. Setting this bit to '0' will select TxSYNC to be single-frame boundary.

Register 0xn109 – SYNCHRONIZATION MUX REGISTER (SMR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3-2	Bit 1	Bit 0
Reserved	MFRAME ALIGN	MSYNC	SYNCINV	Reserved	CRCSRC	FSRC
R/W	R/W	R/W	R/W	R/W	R/W	R/W

6) **(T1 Mode ONLY)** Select Transmit Frame Sync Alignment Enforcement.

Set MFRAMEALIGN, Bit 6 in the Synchronization Mux Register (SMR) to '1' to force the transmit framer to align with the multi-frame boundary on the TxSYNC pin if MSYNC (Bit 5) is set to '1'. Setting this bit to '0' will not enforce the transmit framer to align with the multi-frame boundary.

Register 0xn109 – SYNCHRONIZATION MUX REGISTER (SMR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3-2	Bit 1	Bit 0
Reserved	MFRAME ALIGN	MSYNC	SYNCINV	Reserved	CRCSRC	FSRC
R/W	R/W	R/W	R/W	R/W	R/W	R/W

Configuring the Receive T1/E1 Framer in HMVIP High-Speed Backplane Interface mode:

1) Enable the receive high-speed backplane multiplexed bus.

Set RxMUXEN, Bit 2 in the Receive Interface Control Register (RICR) to '1'.

Register 0xn122 – RECEIVE INTERFACE CONTROL REGISTER (RICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
RxSYNC FRD	Reserved	RxSYNC Is LOW	RxFR1544/ RxFR2048	RxICLKINV	RxMUXEN	RxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

2) Enable the receive HMVIP high-speed backplane multiplexed mode at 16.384MHz.

Set RxIMODE, Bit 1-0 in the Receive Interface Control Register (RICR) to '10'.

Register 0xn122 – RECEIVE INTERFACE CONTROL REGISTER (RICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
RxSYNC FRD	Reserved	RxSYNC Is LOW	RxFR1544/ RxFR2048	RxICLKINV	RxMUXEN	RxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

By default, the receive framer is configured in the 12.352MHz bit multiplexed high-speed mode once the RxMUXEN is set to '1' in T1 mode.

3) The 86VL38 device has the ability to support either positive or negative polarity on the receive framer boundary signal (RxSYNC).

Select RxSYNC to be Active 'HIGH' or Active 'LOW'.

Set RxSYNCIsLOW, Bit 5 in the Receive Interface Control Register (RICR) to '0' to select RxSYNC to be active 'HIGH'. Setting this bit to '1' will select RxSYNC to be active 'LOW'.

Register 0xn122 – RECEIVE INTERFACE CONTROL REGISTER (RICR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
RxSYNC FRD	Reserved	RxSYNC Is LOW	RxFR1544/ RxFR2048	RxICLKINV	RxMUXEN	RxIMODE [1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

4) Users have the ability to select RxSYNC to be input or output from the device in HMVIP mode. If RxSYNC is selected to be an input, Terminal Equipment must provide a single-frame boundary on the RxSYNC pin for the framer to locate the beginning of the single-frame. If RxSYNC is selected to be an output, single-frame boundary is output on the RxSYNC pin.

Register 0xn116 – SLIP BUFFER CONTROL REGISTER (SBCR)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1-0
TxSB_ ISFIFO	Reserved	Reserved	SB_FORCE SF	SB_SF ENB	SB_SDIR	SB_ENB[1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W

To Select RxSYNC as Input:

Set SB_ENB[1:0], Bit 1-0 in the Slip Buffer Control Register (SBCR) to '01' or '10'.

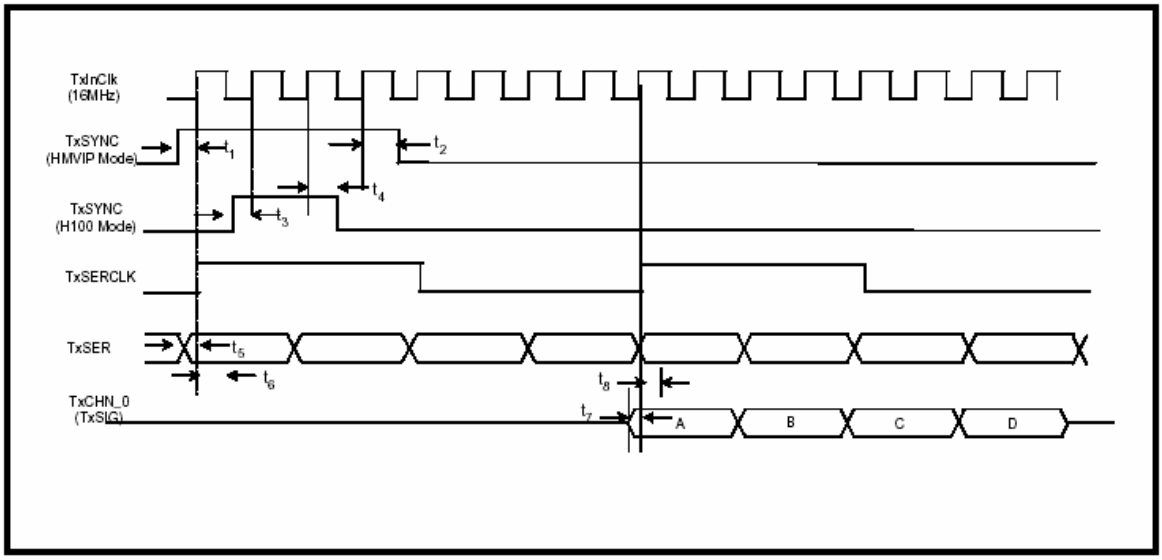
To Select RxSYNC as Output:

Set SB_ENB[1:0], Bit 1-0 in the Slip Buffer Control Register (SBCR) to '00' or '11'.

AC ELECTRICAL CHARACTERISTICS TRANSMIT FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	TxSYNC Setup Time - HMVIP Mode	6			nS	
t_2	TxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	TxSYNC Setup Time - H100 Mode	6			nS	
t_4	TxSYNC Hold Time - H100 Mode	3			nS	
t_5	TxSER Setup Time - HMVIP and H100 Mode	6			nS	
t_6	TxSER Hold Time - HMVIP and H100 Mode	3			nS	
t_7	TxSIG Setup Time - HMVIP and H100 Mode	6			nS	
t_8	TxSIG Hold Time - HMVIP and H100 Mode	3			nS	

FIGURE 117. FRAMER SYSTEM TRANSMIT TIMING DIAGRAM (HMVIP AND H100 MODE)



NOTE: Setup and Hold time is not valid from TxInClk to TxSERCLK as TxInClk is used as the timing source for the back plane interface and TxSERCLK is used as the timing source on the line side.

AC ELECTRICAL CHARACTERISTICS RECEIVE FRAMER (HMVIP/H100 MODE)

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_1	RxSYNC Setup Time - HMVIP Mode	6			nS	
t_2	RxSYNC Hold Time - HMVIP Mode	3			nS	
t_3	RxSYNC Setup Time - H100 Mode	6			nS	
t_4	RxSYNC Hold Time - H100 Mode	3			nS	
t_5	Rising Edge of RxSERCLK to Rising Edge of RxSER delay			11	nS	

NOTE: NOTE: Both RxSERCLK and RxSYNC are inputs

FIGURE 118. FRAMER SYSTEM RECEIVE TIMING DIAGRAM (HMVIP/H100 MODE)