E1 Software Customization for RLOS Compliance

INTRODUCTION

The International Telecommunications Union specifies RLOS for E1 with two components; (a) analog LOS, and (b) digital LOS (ITU-G.775). To provide flexibility, a range is given for both components. To summarize, the analog portion is specified between 9dB and 35dB, while the digital portion is specified between 10 UI and 255 UI. For most E1 devices, EXAR chooses 15dB and 32UI within the specified ranges. However, EXAR has incorporated a software feature that allows the user to customize the threshold of the analog portion of the RLOS. The purpose of this application note is to describe how this process works.

EXAR DEVICES

- XRT86VL30 (single channel DS-1/E1 Framer+LIU Combo)
- XRT86VX38 (eight channel DS-1/E1 Framer+LIU Combo)
- XRT83VL38 (eight channel DS-1/E1 Long Haul LIU)

PROCEDURE

The idea behind the software implementation is to customize the analog threshold to any value between 9dB and 35dB by using the Cable Loss Indicator Bits (referred to as CLOS) within the registers of the LIU portion. *Note: The specification states that RLOS must be declared for a signal that is less than 35dB and RLOS must be cleared for a signal that is greater than 9dB.* This register is in address location 0xn7 within the LIU section of all E1 devices. The value of the CLOS register bits is equal to the amount of gain needed to normalize the input to the receiver block within the LIU. Therefore, this value is equal to the amount of attenuation present on RTIP/RRING. CLOS can be used to create a time stamp = 0 seconds within a software routine whenever it is less than the desired amount of attenuation (see Figure 1 – we have chosen 20dB to be the monitored value for this example).

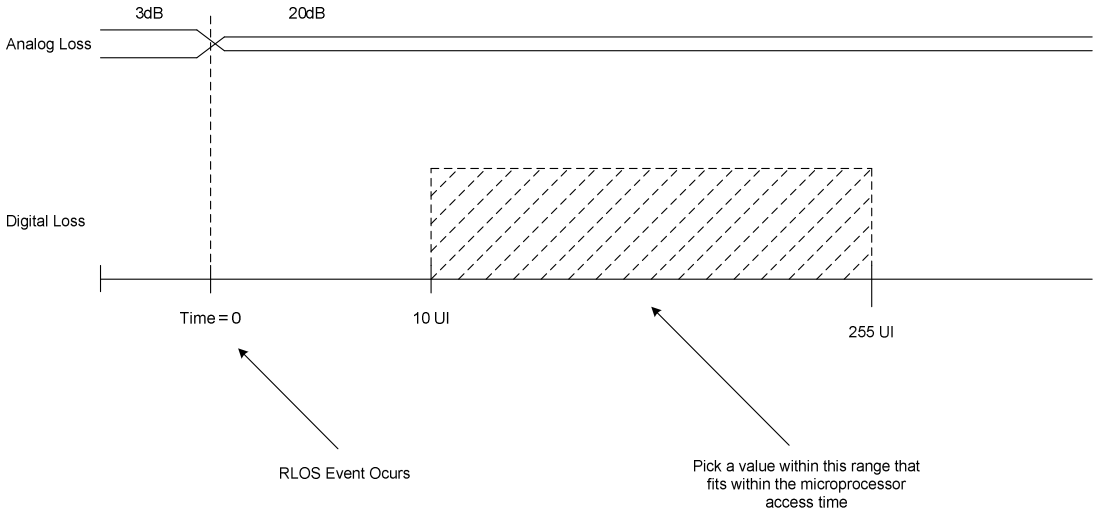

Figure 1. Analog and Digital Components of RLOS

Once the value of the cable loss has hit the threshold, it is then up to the microprocessor to validate the RLOS by reading the CLOS bits at X amount of seconds before the software can declare RLOS, where X is the following:

10 UI < X > 255 UI

Example:

Microprocessor Speed: 33MHz
Microprocessor Access Time: 13.6 uS (assuming 4.5 clock cycles per access)

One Time Stamp: 13.6 uS

10 UI for E1 = 4.88 uS
255 UI for E1 = 12.45 mS

In this case, the software can validate the RLOS at the very next access time, because it fits within the 10 UI to 255 UI interval allowed in G.775. For optimum compliance, software can choose a value that is in the middle of the range. However, it is only necessary to be within the range. Any value can be chosen. Figure 2 is a simplified diagram showing the software routine.

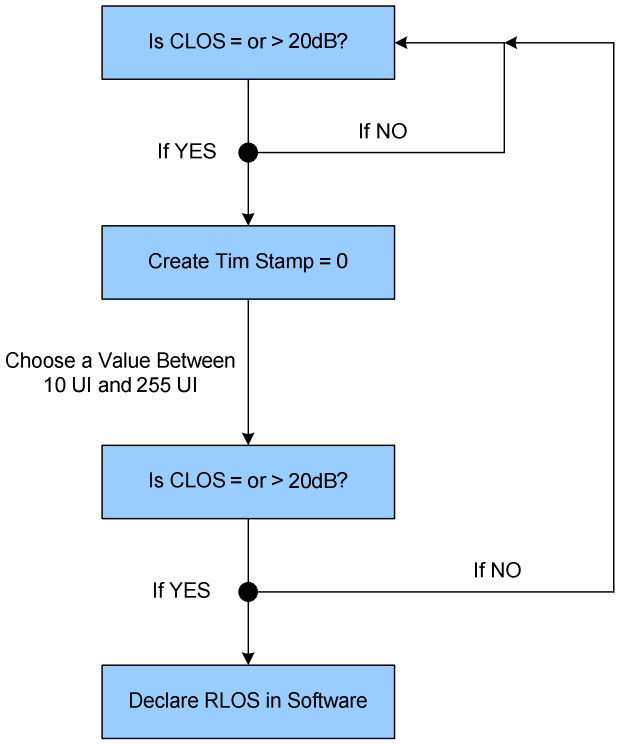

Figure 2. Flow Chart of a Typical Software Routine for RLOS

Note: This Procedure Can be Customized for RLOS Clearance Using the Same Methodology