Solving the Power-Up Challenge for SmartFusion2 SoC FPGAs

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A ready-made, compact and flexible circuit for powering a SmartFusion2 FPGA

Field-programmable gate arrays (FPGAs) continue to grow in popularity because they offer a dynamic, fast time-to-market solution that allows for design flexibility and IP reuse. FPGAs, such as those in the SmartFusion2 SoC FPGA family, allow end system designers to better react to last minute product definition changes and reduce development times. FPGAs require multiple dedicated rails to supply core, I/O, memory, and other precision voltages and so need carefully designed power management solutions. Improper start-up/shut-down sequencing, uncontrolled rise times or non-monotonic ramp-up of sensitive multi-rail systems can cause reliability issues and system faults. This paper will discuss an ideal power management solution which not only provides easy control of these vital parameters but is also compact, flexible and easy to implement.

Introduction

The SmartFusion2 SoC FPGAs are a family of flash FPGA devices which may be used for implementing a wide range of general purpose or dedicated functions in the communications, industrial, medical, defense, and aviation markets. The SmartFusion2 SoC requires four dedicated rails to supply core, I/O, memory and auxiliary voltages. These rails require unique start-up and shut-down sequencing for reliable operation.

Options for Designing a SmartFusion2 FPGA Power-Up System

Designers essentially can take one of two basic approaches to designing a power-up system for SmartFusion2 SoC FPGAs. The first is a traditional analog solution. Traditional analog power solutions are static solutions, designed for a particular application. If a power rail requires modifications to voltage, ramp rate or sequencing, the power design must also change. Component values must be recalculated and changed to meet the new system requirements. If this modification comes late in the design cycle, it could even require a board change resulting in time-to-market delays. Analog power solutions tend to be fixed, less flexible solutions that typically require more board real-estate than a programmable power solution. A typical 4-channel analog power solution can utilize nearly 150 components – more if soft-start, margining, or sequencing functions are implemented discretely.

Exar's SmartFusion2 Power Solution

The second approach is a programmable solution such as that provided by the Exar XRP7714, a quad channel universal PMIC that features programmable power technology. The reference design supplies all four power rails:

- 1.2V for the main supply rail
- 1.5V for general purpose I/Os
- 2.5V for auxiliary voltage
- 1.8V for the internal memory

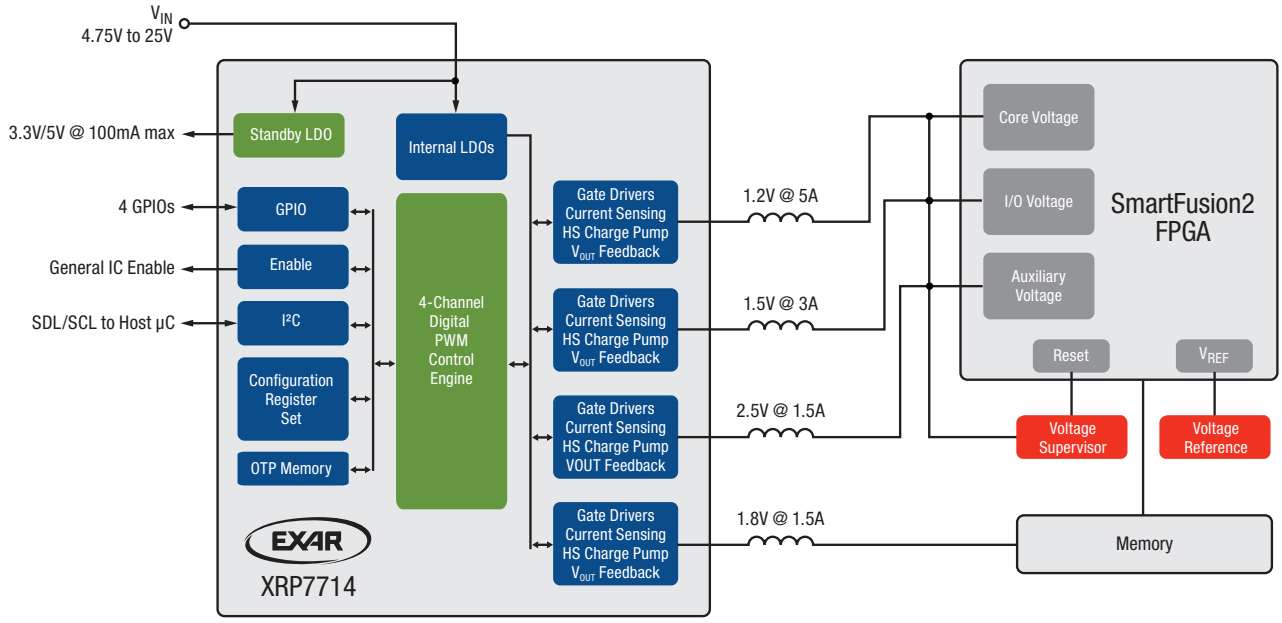

Figure 1: Exar FPGA Power Solution using the XRP7714

This programmable power solution is flexible and allows dynamic changes to output voltage levels, sequencing, timing, switching frequency, and other functions. Modifications to power rails can occur at any time without board level changes, even after a product is in the field. Faults, output voltages and currents can also be monitored. Four GPIO signals are available and can be programmed to provide the status of power good signals, enables, and faults.

Comparison to Traditional Analog Solutions

The XRP7714 SmartFusion2 power reference design supplies 4 power rails in a compact 1.5" x 1.5" footprint, uses less than 35 components and includes many features not available in a basic analog solution. These include:

- Soft-start
- Margining
- Sequencing and tracking
- Dynamic voltage control
- Conditional fault management

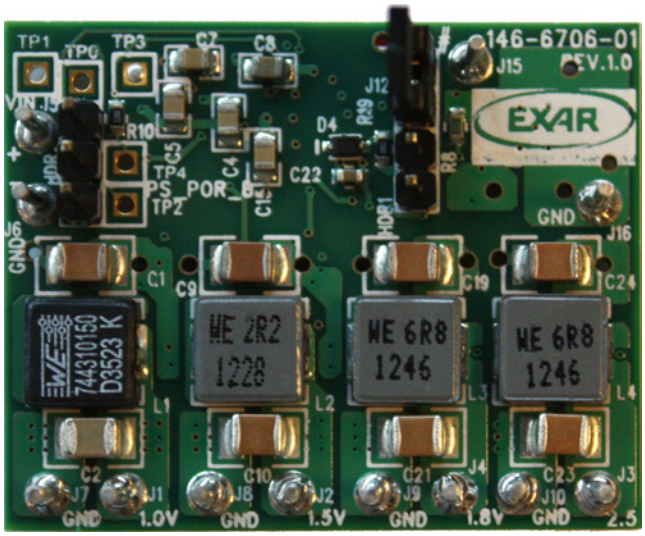

Figure 2: Exar FPGA Power Reference Design provides 1.2V, 1.5V, 1.8V, and 2.5V in a compact 1.5" x 1.5" solution

Software-Based Flexibility

The power solution is easily customized using Exar's design and configuration software, PowerArchitect™. It offers fast prototyping and time-to-market while accommodating last minute production changes without significant delays. Output voltage, switching frequency, sequencing and fault management are programmable via I²C.

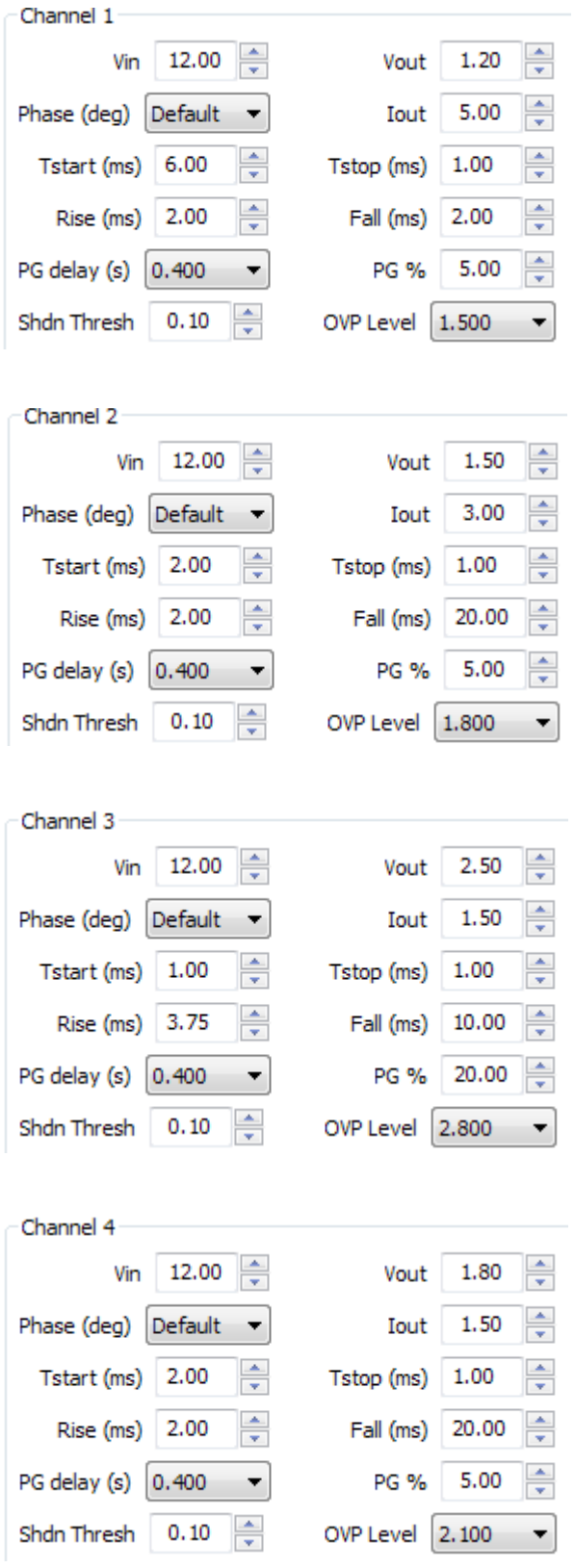

Figure 3: Configuration Settings in PowerArchitect

Each channel of the XRP7714 has been independently configured to meet the SmartFusion2 sequencing requirements. Table 1 indicates the power-on and power-down ramp rates for each rail.

Supply (V)	Power-On Rate (V/ms)	Power-Down Rate (V/ms)
1.2	0.6	0.6
1.5	0.75	0.0075
2.5	0.67	0.25
1.8	0.9	0.09

Table 1: Power-on and Power-down Supply Sequencing

Figure 3 illustrates the power-on and power-down supply sequencing.

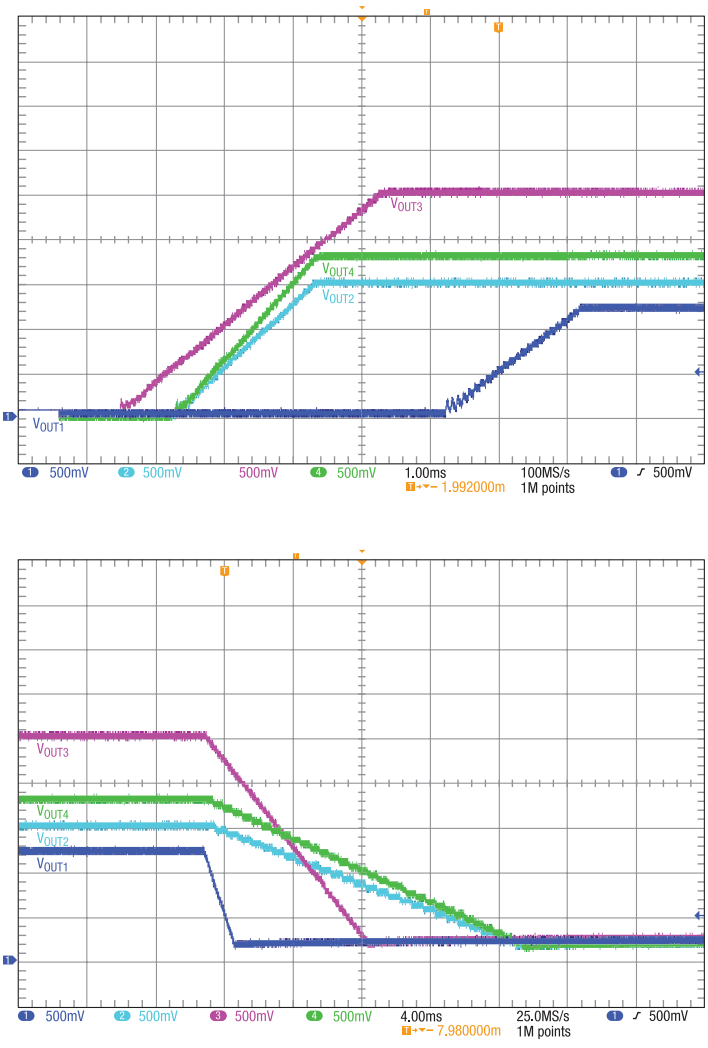

Figure 3: Power-on and Power-off Sequencing

The reference design, which is supported by PowerArchitect™ 4.x, includes configuration files, and connects to the Exar Communications Module (XRP77XXEVB-XCM-V80). The communication module provides an interface to PowerArchitect and allows programming of the board.

Conclusion

The SmartFusion2 power reference design is a complete four-output power system designed to power a SmartFusion2 SoC FPGA. The order and ramp rates for each supply are programmed to accommodate SmartFusion2 sequencing requirements. All power supply operations can be controlled over an I²C interface. The reference design is an ideal power management solution for powering FPGAs like the SmartFusion2. It is compact, flexible, and easy to implement.

For More Information

- Download this product's data sheet: XRP7714
- Review the Evaluation Board Manual for: Exar Communications Module
- Download this Software Tool: PowerArchitect™ 4.x
- Download the SmartFusion2 configuration files

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