November 2017

1.0 INTRODUCTION

This document describes an errata for the XR28V38x LPC UART family, customers who will be affected, the root cause of the errata, the severity of the errata and suggested work-around(s) for the errata.

2.0 BACKGROUND

The XR28V382 and XR28V384 are Exar's two channel and four channel LPC UARTs respectively. Under specific conditions, both devices exhibit incorrect interrupt behavior. Interrupts are reported by the device, in each channel's respective IRQ frame on the SERIRQ pin. By hardware default, channels A and B of the XR28V382 use IRQ frames 3 and 4 respectively, and channels A, B, C and D of the XR28V384 use IRQ frames 3, 4, 5 and 9 respectively. IRQ frames, however may be modified by BIOS settings. The XR28V38x devices may operate in either Continuous Mode, in which IRQ frames are initiated by the host continuously, or in Quiet Mode in which IRQ frames are initiated by the XR28V38x device only upon a change of interrupt states.

2.1 Interrupts not reported on SERIRQ pin when IRQ Channel Select Register bits [6:4] = '000'

The XR28V382 and XR28V384 exhibit incorrect behavior when all 3 of the following conditions are met:

1) Both UART channels of the XR28V382 OR two or more UART channels of the XR28V384 are open. Typically, when a UART channel is opened, interrupt generation is enabled (IER = 0x0F) and the SERIRQ output is enabled (MCR[3] = '1'). When the UART channel is closed all interrupts are disabled (IER = 0x00) and the SERIRQ output is disabled (MCR[3] = '0').

2) IRQ Channel Select Register bit [6:4] is set to '000' (default hardware setting of the device).

3) Not all opened UART channels have pending interrupts, i.e. only 1 out of 2 channels in the XR28V382 and a maximum of 3 out of 4 opened channels in the XR28V384 have pending interrupts.

When all 3 of the above conditions are met, the SERIRQ pin does not generate interrupts as depicted in Figure 1 on page 2. Figure 1 uses 2 channels as an example and the definitions of open and closed UART channels.

2.1.1 Customers who will be affected

Any customer who is using the SERIRQ pin for reporting interrupts and meet all 3 of the above conditions in section 2.1.

2.1.2 Root cause

Error when IRQ Channel Select Register bit [6:4] = 000 is the root cause of this issue.

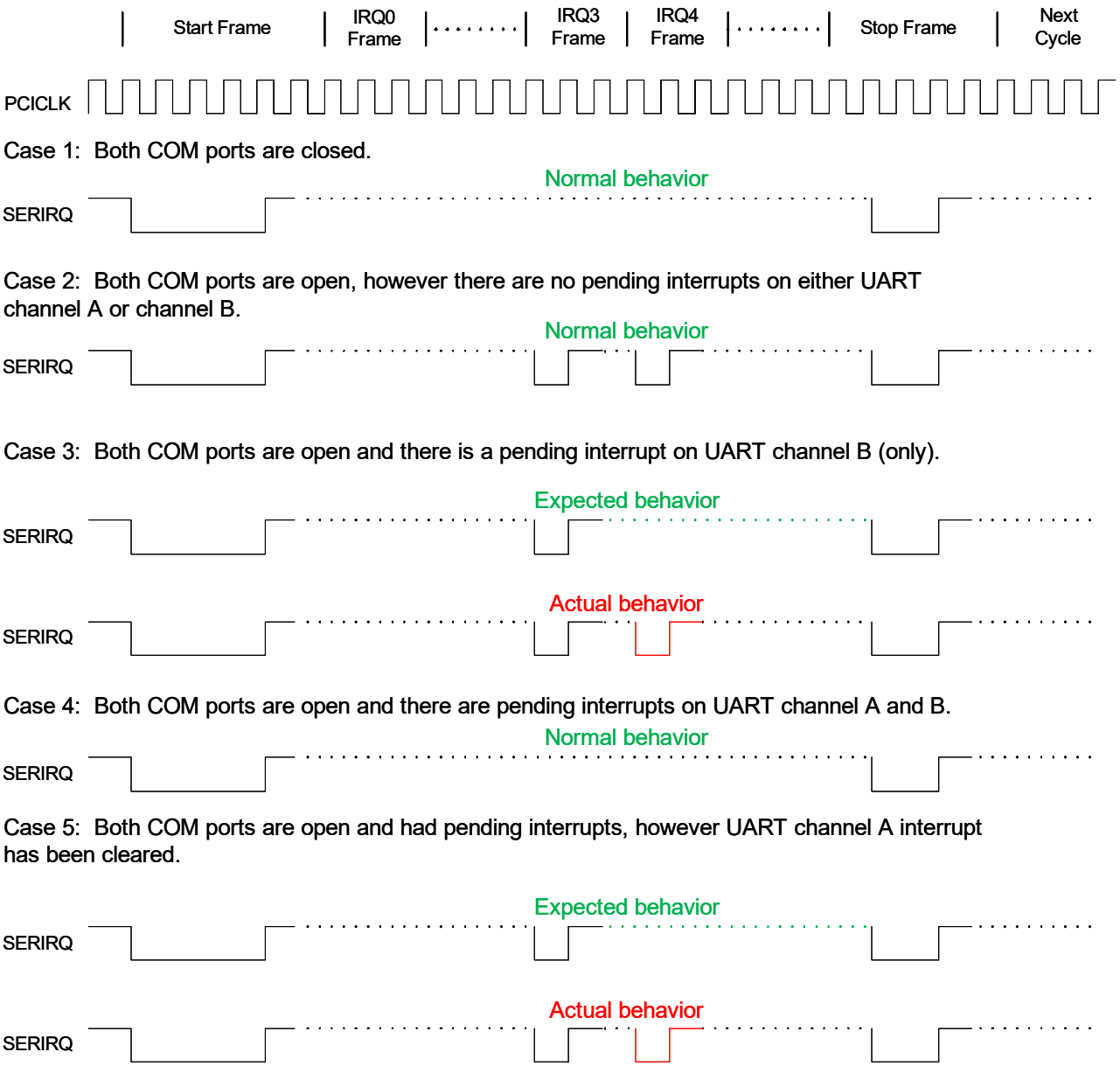
2.1.3 Severity - Low

The severity of this issue is low as there is an alternate setting which correctly generates interrupts with the same polarity.

2.1.4 Suggested Work-Around

The work-around for this mode is to program the IRQ Channel register bits [6:4] to '101. In this mode, all incorrect behavior is eliminated.

Figure 1


Start Frame
IRQ0 Frame
IRQ3 Frame
IRQ4 Frame
Stop Frame
Next Cycle
PCICLK
Case 1: Both COM ports are closed.
Normal behavior
SERIRQ
Case 2: Both COM ports are open, however there are no pending interrupts on either UART channel A or channel B.
Normal behavior
SERIRQ
Case 3: Both COM ports are open and there is a pending interrupt on UART channel B (only).
Expected behavior
SERIRQ
Actual behavior
SERIRQ
Case 4: Both COM ports are open and there are pending interrupts on UART channel A and B.
Normal behavior
SERIRQ
Case 5: Both COM ports are open and had pending interrupts, however UART channel A interrupt has been cleared.
Expected behavior
SERIRQ
Actual behavior
SERIRQ

2.2 A change of interrupt state may not be reported on the SERIRQ pin in Quiet Mode

The XR28V38x may exhibit incorrect behavior when operating in quiet mode. A change of state may not be reported on the SERIRQ pin if the change of interrupt state occurs during an ongoing SERIRQ cycle.

2.2.1 Customers who will be affected

Any customer who is using the SERIRQ pin for reporting interrupts in quiet mode.

2.2.2 Root cause

If there is an interrupt status change during the SERIRQ cycle (between the SERIRQ start frame and stop frame), then the interrupt status change is ignored, and no subsequent SERIRQ start frame is initiated.

2.2.3 Severity - High

The severity of this issue is high as the quiet mode may be unstable when the interrupt handler is not informed of some interrupt change of states.

2.2.4 Suggested Work-Around

The suggested work-around is to use the XR28V38x in Continuous mode. In the Continuous mode, the SERIRQ start frame is initiated by the host and therefore avoids this condition where the XR28V38x does not correctly initiate the SERIRQ start frame.

3.0 TECHNICAL SUPPORT

Send any questions about this document or any other technical questions to **uarttechsupport@exar.com**.

4.0 REVISION HISTORY

Revision	Date	Description
1.0.0	07/08/2015	Preliminary document
1A	11/14/2017	Added MaxLinear logo.

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