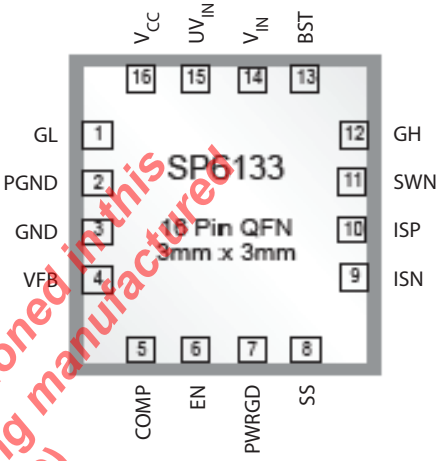
SP6133

Synchronous Buck Controller

FEATURES

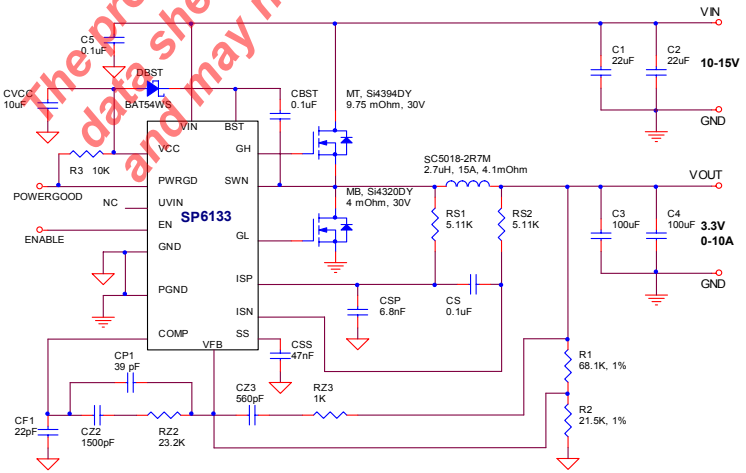
- 5V to 24V Input step down converter
- Up to 30A output capability
- Highly integrated design, minimal components
- UVLO Detects Both V_{CC} and V_{IN}
- Overcurrent circuit protection with auto-restart
- Power Good Output, ENABLE Input
- Maximum Controllable Duty Cycle Ratio up to 92%
- Wide BW amp allows Type II or III compensation
- Programmable Soft Start
- Fast Transient Response
- High Efficiency: Greater than 95% possible
- Available in Lead Free, RoHS Compliant 16-Pin QFN package
- External Driver Enable/Disable
- U.S. Patent #6,922,041



DESCRIPTION

The SP6133 is a synchronous step-down switching regulator controller optimized for high efficiency. The part is designed to be especially attractive for single supply step down conversion from 5V to 24V. The SP6133 is designed to drive a pair of external NFETs using a fixed 300 kHz frequency, PWM voltage mode architecture. Protection features include UVLO, thermal shutdown, output short circuit protection, and overcurrent protection with auto restart. The device also features a PWRGD output and an enable input. The SP6133 is available in a space saving 16-pin QFN and offers excellent thermal performance.

TYPICAL APPLICATION CIRCUIT



Note: Die attach paddle is internally connected to GND.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 6V
V_{IN} 24.5V
BST..... 30V
BST-SWN 7V
SWN .....-2V to 24.5V
GH .....-0.3V to BST+0.3V
GH-SWN..... 6V

All other pins.....-0.3V to V_{CC}+0.3V

Peak Output Current < 10µs
GH,GL 2A

Storage Temperature..... -65°C to 150°C
Power Dissipation..... 1W
ESD Rating..... 2kV HBM
Thermal Resistance..... 41.9°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: -40°C < T_{AMB} < 85°C, 4.5V < V_{CC} < 5.5V, BST=V_{CC}, SWN = GND = PGND = 0.0V, UV_{IN} = 3.0V, CV_{CC} = 10µF, C_{COMP} = 0.1µF, CGH = CGL = 3.3nF, C_{SS} = 50nF, R_{PWRGD} = 10KΩ.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
QUIESCENT CURRENT					
VIN Supply Current		1.5	3.0	mA	VFB = 1V (no switching)
VCC Supply Current		1.5	3.0	mA	VFB = 1V (no switching)
BST Supply Current		0.2	0.4	mA	VFB = 1V (no switching)
PROTECTION: UVLO					
VCC UVLO Start Threshold	4.00	4.25	4.5	V	
VCC UVLO Hysteresis	150	200	250	mV	
UVIN Start Threshold	2.35	2.50	2.65	V	Apply voltage to UVIN pin
UVIN Hysteresis	200	300	400	mV	Apply voltage to UVIN pin
VIN Start Threshold	9.0	9.5	10.0	V	UVIN Floating
VIN Hysteresis		300		mV	UVIN Floating
Enable Pullup Current		0.4		µA	Apply voltage to EN pin
ERROR AMPLIFIER REFERENCE					
Error Amplifier Reference	0.792	0.800	0.808	V	2x Gain Config.
Error Amplifier Reference Over Line & Temperature	0.788	0.800	0.812	V	
COMP Sink Current	70	150	230	µA	
COMP Source Current	-230	-150	-70	µA	
VFB Input Bias Current	1	50	100	nA	
COMP Common Mode Output Range	1.9	3.0	3.2	V	
COMP Pin Clamp Voltage	3.2	3.5	3.8	V	VFB = 0.7V

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: -40°C < T_{AMB} < +85°C, 4.5V < V_{CC} < 5.5V, BST=V_{CC},SWN = GND = PGND = 0.0 V, UV_{IN} = 3.0V, CV_{CC} = 0.1µF, C_{COMP} = 0.1µF, CGH = CGL = 3.3nF, C_{SS} = 50nF.

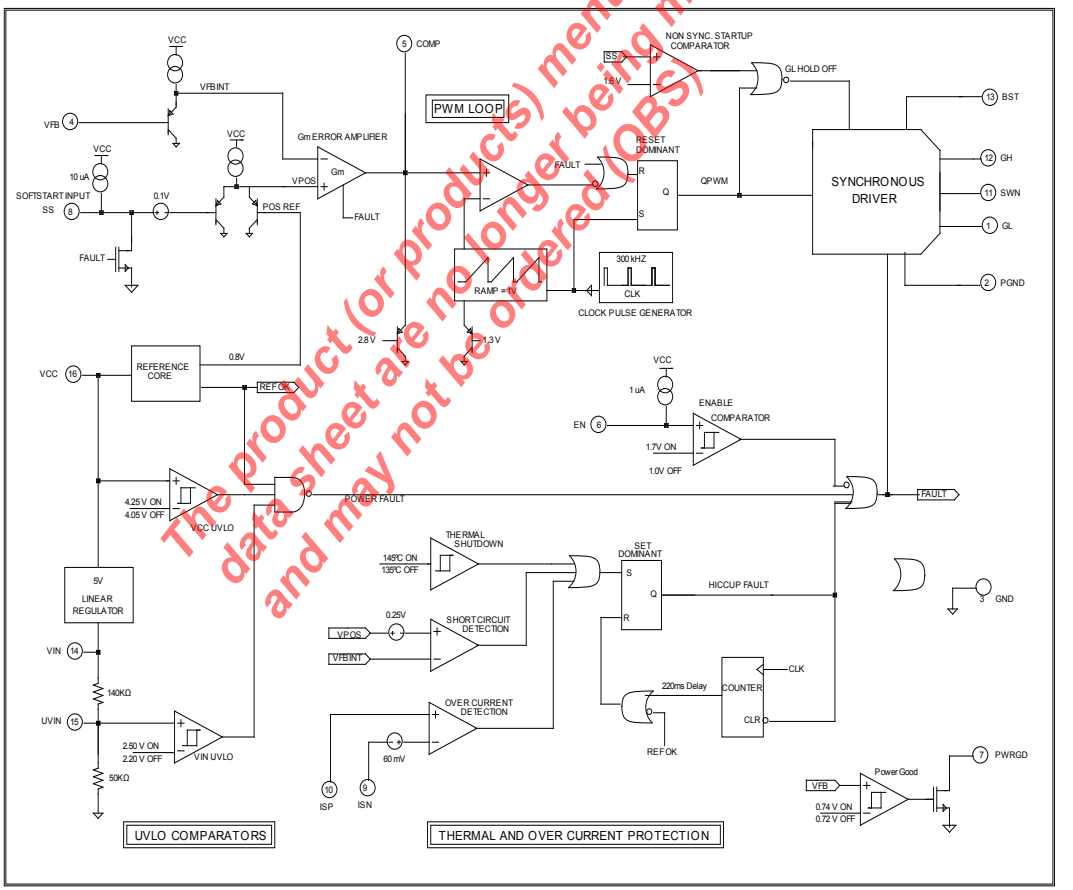
PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
CONTROL LOOP: PWM COMPARATOR, RAMP & LOOP DELAY PATH					
Ramp Offset	1.7	2.0	2.3	V	TA = 25˚C
Ramp Amplitude	0.80	1.0	1.20	V	
GH Minimum Pulse Width		50	100	ns	
Maximum Controllable Duty Ratio	92			%	
Maximum Duty Ratio	100			%	Guaranteed by design
Internal Oscillator Frequency	255	300	345	kHz	
TIMERS: SOFTSTART					
SS Charge Current:	-16	-10	-4	µA	
SS Discharge Current:	1.0	2.0	3.0	mA	Fault Present
VCC LINEAR REGULATOR					
VCC Output Voltage	4.6	5.0	5.4	V	VIN = 6 to 23V, ILOAD = 0mA to 30mA
Dropout Voltage	250	500	750	mV	IVCC = 30mA
POWER GOOD OUTPUT					
Power Good Threshold	-10	-7.5	-5	%	
Power Good Hysteresis		2.0	4.0	%	
Power Good Sink Current	1.0		10	mA	VFB = 0.7V, VPWRGD = 0.2V
PROTECTION: SHORT CIRCUIT & THERMAL					
Short Circuit Threshold Voltage	0.2	0.25	0.3	V	Measured VREF (0.8V) - VFB
Overcurrent Threshold Voltage	54	60	66	mV	Measured ISP - ISN
ISP, ISN Common Mode Range	0		3.3	V	
Hiccup Timeout	185	220	270	ms	
Thermal Shutdown Temperature	135	145	155	˚C	Guaranteed by design
Thermal Hysteresis		10		˚C	

ELECTRICAL SPECIFICATIONS

Unless otherwise specified: -40°C < T_{AMB} < +85°C, 4.5V < V_{CC} < 5.5V, BST=V_{CC},SWN = PGND = GND = 0.0V, U_{VIN} = 3.0V, CV_{CC} = 0.1µF, C_{COMP} = 0.1µF, CGH = CGL = 3.3nF, C_{SS} = 50nF.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
OUTPUT: NFET GATE DRIVERS					
GH & GL Rise Times		35	50	ns	Measured 10% to 90%
GH & GL Fall Times		30	40	ns	Measured 90% to 10%
GL to GH Non Overlap Time		45	70	ns	GH & GL Measured at 2.0V
SWN to GL Non Overlap Time		25	40	ns	Measured SWN = 100mV to GL = 2.0V
GH & GL Pull Down Resistance	15	50	85	KΩ	
Driver Pull Down Resistance		1.5	1.9	Ω	
Driver Pull Up Resistance		2.5	3.9	Ω	

BLOCK DIAGRAM



PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	GL	High current driver output for the low side NFET switch. It is always low if GH is high or during a fault. Resistor pull down ensures low state at low voltage.
2	PGND	Ground Pin. The power circuitry is referenced to this pin. Return separately from other ground traces to the (-) terminal of Cout.
3	GND	Ground pin. The control circuitry of the IC is referenced to this pin.
4	VFB	Feedback Voltage and Short Circuit Detection pin. It is the inverting input of the Error Amplifier and serves as the output voltage feedback point for the Buck Converter. The output voltage is sensed and can be adjusted through an external resistor divider. Whenever VFB drops 0.25V below the positive reference, a short circuit fault is detected and the IC enters hiccup mode.
5	COMP	Output of the Error Amplifier. It is internally connected to the non-inverting input of the PWM comparator. An optimal filter combination is chosen and connected to this pin and either ground or VFB to stabilize the voltage mode loop.
6	EN	Enable Pin. Pulling this pin below 0.4V will place the IC into sleep mode. This pin is internally pulled to VCC with a 1µA current source.
7	PWRGD	Power Good Output. This open drain output is pulled low when VOUT is outside of the regulation. Connect an external resistor to pull high.
8	SS	Soft Start/Fault Flag. Connect an external capacitor between SS and GND to set the soft start rate based on the 10µA source current. The SS pin is held low via a 1mA (min) current during all fault conditions.
9	ISN	Negative Input for the Sense Comparator. There should be a 60mV offset between PSENSE and NSENSE. Offset accuracy +10%.
10	ISP	Positive Input for the Inductor Current Sense.
11	SWN	Lower supply rail for the GH high-side gate driver. Connect this pin to the switching node at the junction between the two external power MOSFET transistors.
12	GH	High current driver output for the high side NFET switch. It is always low if GL is high or during a fault.
13	BST	High side driver supply pin. Connect BST to the external boost diode and capacitor as shown in the Application Schematic of page 1. High side driver is connected between BST pin and SWN pin.
14	VIN	Supply Input -- supplies power to the internal LDO.
15	UVIN	Under Voltage lock-out for VIN voltage. Internally has a resistor divider from VIN to ground. Can be overridden with external resistors.
16	VCC	Output of the Internal LDO. If VIN is less than 5V then Vcc should be powered from an external 5V supply.

Note: Die attach paddle is internally connected to GND.

THEORY OF OPERATION

General Overview

The SP6133 is a fixed frequency, voltage mode, synchronous PWM controller optimized for high efficiency. The part has been designed to be especially attractive for single supply input voltages ranging between 5V and 24V.

The heart of the SP6133 is a wide bandwidth transconductance amplifier designed to accommodate Type II and Type III compensation schemes. A precision 0.8V reference present on the positive terminal of the error amplifier permits the programming of the output voltage down to 0.8V via the V_{FB} pin. The output of the error amplifier, COMP, compared to a 1V peak-to-peak ramp is responsible for trailing edge PWM control. This voltage ramp and PWM control logic are governed by the internal oscillator that accurately sets the PWM frequency to 300 kHz.

The SP6133 contains two unique control features that are very powerful in distributed applications. First, non-synchronous driver control is enabled during start up to prohibit the low side NFET from pulling down the output until the high side NFET has attempted to turn on. Second, a 100% duty cycle timeout ensures that the low side NFET is periodically enhanced during extended periods at 100% duty cycle. This guarantees the synchronized refreshing of the BST capacitor during very large duty ratios.

The SP6133 also contains a number of valuable protection features. A programmable input UVLO allows a user to set the exact value at which the conversion voltage is at a safe point to begin down conversion, and an internal V_{CC} UVLO ensures that the controller itself has enough voltage to properly operate. Other protection features include thermal shutdown and short-circuit detection. In the event that either a

thermal, short-circuit, or UVLO fault is detected, the SP6133 is forced into an idle state where the output drivers are held off for a finite period before a re-start is attempted.

Soft Start

"Soft Start" is achieved when a power converter ramps up the output voltage while controlling the magnitude of the input supply source current. In a modern step down converter, ramping up the non-inverting input of the error amplifier controls soft start. As a result, excess source current can be defined as the current required to charge the output capacitor

$$IV_{IN,\,x} = \frac{C_{OUT} \bullet \Delta V_{OUT}}{\Delta T_{Soft\text{-}start}}$$

The SP6133 provides the user with the option to program the soft start rate by tying a capacitor from the SS pin to GND. The selection of this capacitor is based on the 10µA pull up current present at the SS pin and the 0.8V reference voltage. Therefore, the excess current source can be redefined as:

$$IV_{IN,\,x} = C_{OUT} \bullet \Delta V_{OUT} \bullet \frac{10\mu A}{(C_{SS} \bullet 0.8V)}$$

Hiccup

Upon the detection of a power, thermal, or short-circuit fault, the SP6133 is forced into an idle state for a minimum of 200ms. The SS and COMP pins are immediately pulled low, and the gate drivers are held off for the duration of the timeout period. Power and thermal faults have to be removed before a restart may be attempted, whereas, a short-circuit fault is internally cleared shortly after the fault latch is set. Therefore, a restart attempt is guaranteed every 200ms (typical) as long as the short-circuit condition persists.

A short-circuit detection comparator has also been included in the SP6133 to protect against the accidental short or severe build up of current at the output of the power converter. This comparator constantly monitors the inputs to the error amplifier, and if the V_{FB} pin ever falls more than 250mV (typical) below the voltage reference, a short-circuit fault is set. Because the SS pin overrides the internal 0.8V reference during soft start, the SP6133 is capable of detecting short-circuit faults throughout the duration of soft start as well as in regular operation.

Error Amplifier & Voltage Loop

As stated before, the heart of the SP6133 voltage error loop is a high performance, wide bandwidth transconductance amplifier. Because of the amplifier's current limited (±100µA) transconductance, there are many ways to compensate the voltage loop or to control the COMP pin externally. If a simple, single pole, single zero response is required, then compensation can be as simple as an RC circuit to ground. If a more complex compensation is required, then the amplifier has enough bandwidth (45°C at 4 MHz) and enough gain (60 dB) to run Type III

compensation schemes with adequate gain and phase margins at crossover frequencies greater than 200 kHz.

The common mode output of the error amplifier (COMP) is 0.9V to 2.2V. Therefore, the PWM voltage ramp has been set between 1.0V and 2.0V to ensure proper 0% to 100% duty cycle capability. The voltage loop also includes two other very important features. One is a non-synchronous start up mode. Basically, the GL driver cannot turn on unless the GH driver has attempted to turn on or the SS pin has exceeded 1.7V. This feature prevents the controller from "dragging down" the output voltage during startup or in fault modes. The second feature is a 100% duty cycle timeout that ensures synchronized refreshing of the BST capacitor at very high duty ratios. In the event that the GH driver is on for 20 continuous clock cycles, a reset is given to the PWM flip flop half way through the 20th cycle. This forces GL to rise for the remainder of the cycle, in turn refreshing the BST capacitor.

Gate Drivers

The SP6133 contains a pair of powerful 2Ω Pull-up and 1.5Ω Pull-down drivers. These state-of-the-art drivers are designed to drive an external NFET capable of handling up to 30A. Rise, fall, and non-overlap times have all been minimized to achieve maximum efficiency. All drive pins GH, GL, & SWN are monitored continuously to ensure that only one external NFET is ever on at any given time.

Thermal & Short-Circuit Protection

Because the SP6133 is designed to drive large NFETs running at high current, there is a chance that either the controller or power converter will become too hot. Therefore, an internal thermal shutdown (145°C) has been included to prevent the IC from malfunctioning at extreme temperatures.

Over-Current Protection

Over-current is detected by monitoring a differential voltage across the output inductor as shown in figure 1. Inputs to an over-current detection comparator, set to trigger at 60 mV nominal, are connected to the inductor as shown.

Since the average voltage sensed by the comparator is equal to the product of inductor current and inductor DC resistance (DCR) then I_{MAX} = 60mV / DCR. Solving this equation for the specific inductor in circuit 1, I_{MAX} = 14.6A. When I_{MAX} is reached, a 220 ms time-out is initiated, during which top and bottom drivers are turned off. Following the time-out, a restart is attempted. If the fault condition persists, then the time-out is repeated (referred to as hiccup).

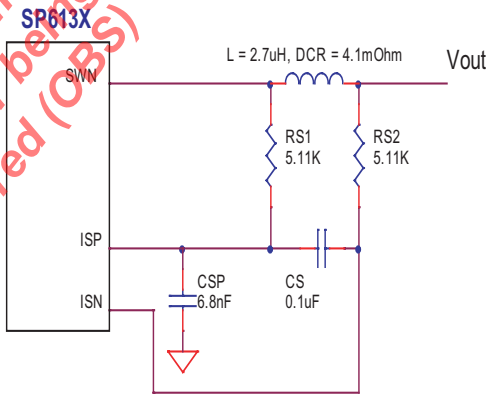


Figure 1: Over-current detection circuit

Increasing the Current Limit

If it is desired to set Imax > {60mV / DCR} (in this case larger than 14.6A), then a resistor R_{S3} should be added as shown in figure 2. R_{S3} forms a resistor divider and reduces the voltage seen by the comparator.

$$\text{Since: } \frac{60mV}{R_{S3}} = \frac{I_{MAX} \bullet DCR}{\{R_{S1} + R_{S2} + R_{S3}\}}$$

Solving for RS3 we get:

$$R_{S3} = \frac{[60mV \bullet (R_{S1} + R_{S2})]}{[(Imax \bullet DCR) - 60mV]} \quad .....(1)$$

As an example: if desired I_{MAX} is 17A, then R_{S3} = 63.4KΩ.

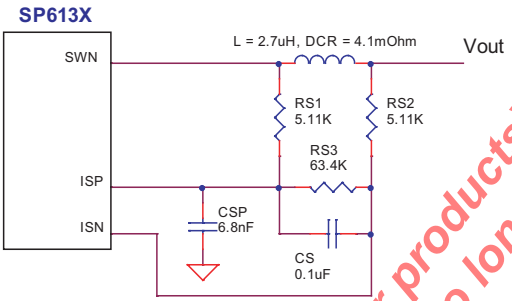


Figure 2- Over-current detection circuit for Imax > 60mV / DCR

Decreasing the Current Limit

If it is required to set Imax < {60mV / DCR}, a resistor is added as shown in figure 3. RS3 increases the net voltage detected by the current-sense comparator. Voltage at the positive and negative terminal of comparator is given by:

$$VSP = V_{OUT} + (I_{MAX} \bullet DCR)$$

$$VSN = V_{OUT} \bullet \{R_{S3} / (R_{S2} + R_{S3})\}$$

Since the comparator is triggered at 60mV:
VSP-VSN = 60 mV

Combining the above equations and solving for R_{S3}:

$$R_{S3} = R_{S2} \bullet \frac{[V_{OUT} - 60mV + (I_{MAX} \bullet DCR)]}{60mV - (I_{MAX} \bullet DCR)} \quad .....(2)$$

As an example: for I_{MAX} of 12A and V_{OUT} of 3.3V, calculated R_{S3} is 1.5MΩ.

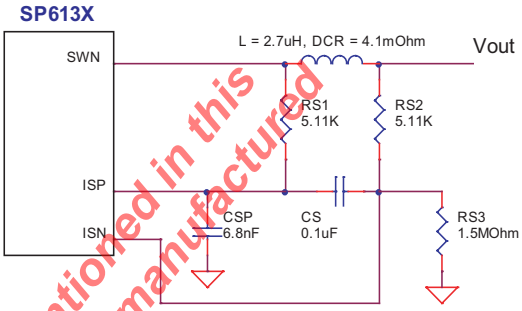


Figure 3- Over-current detection circuit for I_{MAX} < {60mV / DCR}

Power MOSFET Selection

There are four main criterion in selecting Power MOSFETs for buck conversion:

- Voltage rating BV_{DSS}
- On resistance $R_{DS(ON)}$
- Gate-to-drain charge Q_{GD}
- Package type

In order to better illustrate the MOSFET selection process, the following buck converter design example will be used: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 10A, f = 300KHz, DCR = 4.5mΩ (inductor DC resistance), efficiency = 94% and T_A = 40˚C.

Select the voltage rating based on maximum input voltage of the converter. A commonly used practice is to specify BV_{DSS} at least twice the maximum converter input voltage. This is done to safeguard against switching transients that may break down the MOSFET. For converters with V_{IN} of less than 10V, a 20V rated MOSFET is sufficient. For convert-

ers with 10-15V_{IN}, as in the above example, select a 30V MOSFET.
The calculation of $R_{DS(ON)}$ for Top and Bottom MOSFETs is interrelated and can be done using the following procedure:

1) Calculate the maximum permissible power dissipation $P_{(DISSIPATION)}$ based on required efficiency. The converter in the above example should deliver an output power P_{OUT} = 3.3Vx10A = 33W. For a target efficiency of 94%, input power P_{IN} is given by $P_{IN} = P_{OUT}/0.94 = 35.1W$. Maximum allowable power dissipation is then:

$$P_{(DISSIPATION)} = P_{IN} - P_{OUT} = 2.1\ W$$

2) Calculate the total power dissipation in top and bottom MOSFETs $P_{(MOSFET)}$ by subtracting inductor losses from $P_{(DISSIPATION)}$ calculated in step 1. To simplify, disregard core losses; then $P_L = I^2_{RMS} \cdot DCR \cdot 1.4$, where 1.4 accounts for the increase in DCR at operating temperature. For the above example P_L = 0.63W. Then:
$P_{(MOSFET)} = 2.1W - 0.63W = 1.47W$.

3) Calculate $R_{DS(ON)}$ of the bottom MOSFET by allocating 40% of calculated losses to it. 40% dissipation allocation reflects the fact that the the top MOSFET has essentially no switching loss. Then $P_{(BOTTOM)} = 0.4x1.47W = 0.59W$. $R_{DS(ON)} = P/(I^2_{RMS} \cdot 1.5)$ where $I_{RMS} = I_{OUT} \cdot \{1-(V_{OUT}/V_{IN})\}^{0.5}$ and 1.5 accounts for the increase in $R_{DS(ON)}$ at the operating temperature. Then:

$$R_{DS(ON)} = \frac{P}{[\{I^2_{OUT} \cdot (1-V_{OUT}/V_{IN})\} \cdot 1.5]}$$

$= 5.4\ m\Omega$.

4) Allocate 60% of the calculated losses to the top MOSFET, $P_{(TOP)} = 0.6x1.47 = 0.88W$. Assume conduction losses equal to switching losses, then P = 0.5x0.88W = 0.44W. Since it operates at the duty cycle of $D = V_{IN}/V_{OUT}$; then:

$$R_{DS(ON)} = \frac{P}{[I^2_{OUT} \cdot (V_{OUT}/V_{IN}) \cdot 1.5]}$$

$= 10.7\ m\Omega$.

Gate-to-drain charge Q_{GD} for the top MOSFET needs to be specified. A simplified expression for switching losses is:

$$P_S = I_{OUT} \cdot V_{IN} \cdot f \cdot \left\{\frac{V_{IN}}{dv/dt} + \frac{I_{OUT}}{di/dt}\right\} \quad \text{.....(3)}$$

where dv/dt and di/dt are the rates at which voltage and current transition across the top MOSFET respectively, and f is the switching frequency. Voltage switching time $\left(V_{IN}/_{dv/dt}\right)$ is related to Q_{GD}:

$$\left(V_{IN}/_{dv/dt}\right) = Q_{GD}/I_G \quad \text{..... (4)}$$

where I_G is Current charging the gate-to-drain capacitance. It can be calculated from:

$I_G = (V_{DRIVE}-V_{GATE})/R_{DRIVE}$.....(5)
where V_{DRIVE} is the drive voltage of the SP6133 top driver minus the drop across the boost diode (approximately 4.5V); V_{GATE} is the top MOSFET's gate voltage corresponding to I_{OUT} (assume 2.5V) and R_{DRIVE} is the internal resistance of the SP6133 top driver (assume 2Ω average for turn-on and turn-off). Substituting these values in equation (5) we get I_G = 1A. Substituting for I_G in equation (4), we get $\left(V_{IN}/_{dv/dt}\right) = Q_{GD}$. Substituting for $\left(V_{IN}/_{dv/dt}\right)$ in equation (3) we have:

$$P_S = I_{OUT} \cdot V_{IN} \cdot f \cdot \left\{Q_{GD} + (I_{OUT}/di/dt)\right\}$$

Solving for Q_{GD} we get:

$$Q_{GD} = \left\{\frac{P_S}{I_{OUT} \cdot V_{IN} \cdot f} - \frac{I_{OUT}}{di/dt}\right\} \quad \text{..... (6)}$$

Di/dt is usually limited by parasitic DC-Loop Inductance (Lp) according to $di/dt = V_{IN}/Lp$. Lp is due to wiring and PCB traces connecting input capacitors and switching MOSFETs.

For typical Lp of 12nH and V_{IN} of 12V, di/dt is 1A/ns. Substituting for di/dt in equation (6) we get Q_{GD} = 2 nC.

In selecting a package type, the main considerations are cost, power/current handling capability and space constraints. A larger package in general offers higher power and current handling at increased cost. Package selection can be narrowed down by calculating the required junction-to-ambient thermal resistance θ_{JA}:

$$\theta_{JA} = \{T_{J(MAX)} - T_{A(MAX)}\} / P_{(MAX)} \quad \text{..... (7)}$$

Where: $T_{J(MAX)}$ is the die maximum temperature rating, $T_{A(MAX)}$ is maximum ambient temperature, and $P_{(MAX)}$ is maximum power dissipated in the die.

It is common practice to add a guard-band of 25˚C to the junction temperature rating. Following this convention, a 150˚C rated MOSFET will be designed to operate at 125˚C (i.e., $T_{J(MAX)}$ = 125˚C). $P_{(MAX)}$ = 0.88W (from section 4) and $T_{A(MAX)}$ = 40˚C as specified in the design example. Substituting in equation (7) we get θ_{JA} = 96.6 ˚C/W.

For the top MOSFET, we now have determined the following requirements: BV_{DSS} = 30V, $R_{DS(ON)}$ = 10.7mΩ, Q_{GD} = 2 nC and $\theta_{JA} \leq$ 96.6˚C/W. An SO-8 MOSFET that meets the requirements is Vishay-Siliconix's Si4394DY; BV_{DSS} = 30V, $R_{DS(ON)}$ = 9.75mΩ @ V_{GS} = 4.5V, Q_{GD} = 2.1nC and θ_{JA} = 90˚C/W.

The bottom MOSFET has the requirements of BV_{DSS} = 30V and $R_{DS(ON)}$ = 5.4mΩ. Vishay-Siliconix's Si4320DY meets the requirements; BVdss = 30V, $R_{DS(ON)}$ = 4mΩ @ Vgs = 4.5V.

Power Good

Power Good (PWRGD) is an open drain output that is pulled low when V_{OUT} is outside regulation. The PWRGD pin can be connected to VCC with an external 10KΩ resistor. During startup, output regulates when Soft Start (SS) reaches 0.8V (the reference voltage). PWRGD is enabled when SS reaches 1.6V. PWRGD output can be used as a "Power on Reset". The simplest way to adjust delay of the "Power on Reset" signal with respect to V_{OUT} in regulation is with the Soft Start Capacitor (C_{SS}) and is given by: C_{SS} = (Iss • Tdelay)/0.8 where Iss is the Soft Start charge current (10µA nominal).

Under Voltage Lock Out (UVLO)

The SP6133 has two separate UVLO comparators to monitor the bias (Vcc) and Input (V_{IN}) voltages independently. The Vcc UVLO is internally set to 4.25V. The V_{IN} UVLO is programmable through UVIN pin. When UVIN pin is greater than 2.5V the SP6133 is permitted to start up pending the removal of all other faults. A pair of internal resistors is connected to UVIN as shown in figure 4. Therefore without external biasing the V_{IN} start threshold is 9.5V. A small capacitor may be required between UVIN and GND to filter out noise. For applications with V_{IN} of 5V or 3.3V, connect UVIN directly to V_{IN}.

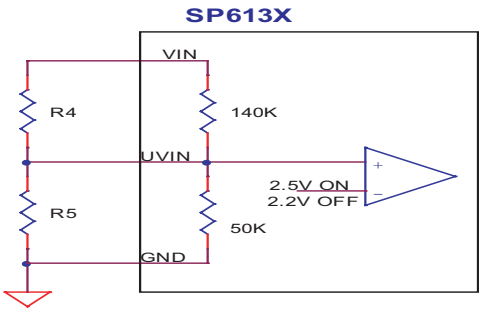


Figure 4- Internal and external bias of UVIN

To program the V_{IN} start threshold, use a pair of external resistors as shown. If external resistors are an order of magnitude smaller than internal resistors, then the V_{IN} start threshold is given by:

$$V_{IN}(start) = 2.5 \bullet (R4+R5)/R5 \quad \text{..... (8)}$$

For example, if it is required to have a V_{IN} start threshold of 7V, then let R5 = 5KΩ and using equation (8) we get R4 = 9.09KΩ.

Inductor Selection

There are many factors to consider in selecting the inductor including cost, efficiency, size and EMI. In a typical SP6133 circuit, the inductor is chosen primarily for value, saturation current and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response. Low inductor values provide the smallest size, but cause large ripple currents, poor efficiency and need more output capacitance to smooth out the larger ripple current. The inductor must also be able to handle the peak current at the switching frequency without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. A good compromise between size, loss and cost is to set the inductor ripple current to be within 20% to 40% of the maximum output current.

The switching frequency and the inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \bullet Fs \bullet K_R \bullet I_{OUT(MAX)}}$$

where:

Fs = switching frequency

K_R = ratio of the ac inductor ripple current to the maximum output current

The peak to peak inductor ripple current is:

$$I_{PP} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \bullet Fs \bullet L}$$

Once the required inductor value is selected, the proper selection of core material is based on peak inductor current and efficiency requirements. The core must be large enough not to saturate at the peak inductor current

$$I_{PEAK} = I_{OUT(MAX)} + I_{PP}/2$$

and provide low core loss at the high switching frequency. Low cost powdered iron cores have a gradual saturation characteristic but can introduce considerable AC core loss, especially when the inductor value is relatively low and the ripple current is high. Ferrite materials, on the other hand, are more expensive and have an abrupt saturation characteristic with the inductance dropping sharply when the peak design current is exceeded. Nevertheless, they are preferred at high switching frequencies because they present very low core loss and the design only needs to prevent saturation. In general, ferrite or molypermalloy materials are the better choice for all but the most cost sensitive applications.

The power dissipated in the inductor is equal to the sum of the core and copper losses. To minimize copper losses, the winding resistance needs to be minimized, but this usually comes at the expense of a larger inductor. Core losses have a more significant contribution at low output current where the copper losses are at a minimum, and can typically be neglected at higher output currents where the copper losses dominate. Core loss information is usually available from the magnetic vendor.

The copper loss in the inductor can be calculated using the following equation:

$$P_{L(C_U)} = I^2_{L(RMS)} \bullet R_{WINDING}$$

where $I_{L(RMS)}$ is the RMS inductor current that can be calculated as follows:

$$I_{L(RMS)} = I_{OUT(MAX)} \bullet \sqrt{1 + \frac{1}{3} \bullet \left\{ \frac{I_{PP}}{I_{OUT(MAX)}} \right\}^2}$$

Output Capacitor Selection

The required ESR (Equivalent Series Resistance) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough that both the resistive voltage deviation due to a step change in the load current and the output ripple voltage do not exceed the tolerance limits expected on the output voltage. During an output load transient, the output capacitor must supply all the additional current demanded by the load until the SP6133 adjusts the inductor current to the new value.

Therefore, the capacitance must be large enough so that the output voltage is held up while the inductor current ramps up or down to the value corresponding to the new load current. Additionally, the ESR in the output capacitor causes a step in the output voltage equal to the current. Because of the fast transient response and inherent 100% and 0% duty cycle capability provided by the SP6133 when exposed to output load transients, the output capacitor is typically chosen for ESR, not for capacitance value.

The output capacitor's ESR, combined with the inductor ripple current, is typically the main contributor to output voltage ripple. The maximum allowable ESR required to maintain a specified output voltage ripple can be calculated by:

$$R_{ESR} \leq \frac{\Delta V_{OUT}}{I_{PK-PK}}$$

where:

ΔV_{OUT} = Peak to Peak Output Voltage Ripple

I_{PK-PK} = Peak to Peak Inductor Ripple Current

The total output ripple is a combination of the ESR and the output capacitance value and can be calculated as follows:

$$\Delta V_{OUT} = \sqrt{(I_{PP} R_{ESR})^2 + \left\{\frac{I_{PP} \cdot (1-D)}{C_{OUT} \cdot F_S}\right\}^2}$$

where:

Fs = Switching Frequency

D = Duty Cycle

C_{OUT} = Output Capacitance Value

Input Capacitor Selection

The input capacitor should be selected for ripple current rating, capacitance and voltage rating. The input capacitor must meet the ripple current requirement imposed by the switching current. In continuous conduction mode, the source current of the high-side MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. Most of this current is supplied by the input bypass capacitors. The RMS value of input capacitor current is determined at the maximum output current and under the assumption that the peak to peak inductor ripple current is low, it is given by:

$$I_{CIN(RMS)} = I_{OUT(MAX)} \cdot \sqrt{D \cdot (1-D)}$$

Schottky Diode Selection

When paralleled with the bottom MOSFET, an optional Schottky diode can improve efficiency and reduce noise. Without this Schottky diode, the body diode of the bottom MOSFET conducts the current during the non-overlap time when both MOSFETs are turned off. Unfortunately, the body diode has high forward voltage and reverse recovery problems. The reverse recovery of the body diode causes additional switching noise when the diode turns off. The Schottky diode alleviates these sources of noise and additionally improves efficiency thanks to its low forward voltage. The reverse voltage across the diode is equal to input voltage, and the diode must be able to handle the peak current equal to the maximum load current.

The power dissipation of the Schottky diode is determined by:

$$P_{DIODE} = 2 \cdot V_F \cdot I_{OUT} \cdot T_{NOL} \cdot F_S$$

where:
T_{NOL} = non-overlap time between GH and GL.
VF = forward voltage of the Schottky diode.

Loop Compensation Design

The open loop gain of the whole system can be divided into the gain of the error amplifier, PWM modulator, buck converter output stage, and feedback resistor divider. In order to cross over at the selected frequency FCO, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency.

The goal of loop compensation is to manipulate loop frequency response such that its gain crosses over 0db at a slope of -20db/dec. The first step of compensation design is to pick the loop crossover frequency. High crossover frequency is desirable for fast transient response, but often jeopardizes the system stability. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The ESR zero is contributed by the ESR associated with the output capacitors and can be determined by:

$$f_{Z(ESR)} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{ESR}}$$

The next step is to calculate the complex conjugate poles contributed by the LC output filter.

$$f_{P(LC)} = \frac{1}{2\pi \cdot \sqrt{L \cdot C_{OUT}}}$$

When the output capacitors are of a Ceramic Type, the SP6133 Evaluation Board requires a Type III compensation circuit to give a phase boost of 180° in order to counteract the effects of an under damped resonance of the output filter at the double pole frequency.

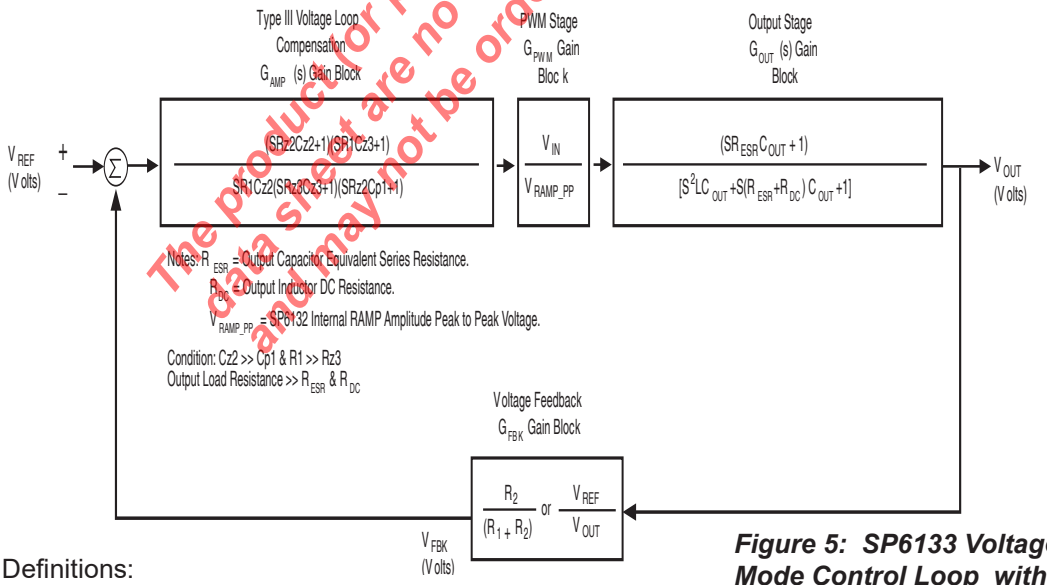


Figure 5: SP6133 Voltage Mode Control Loop with Loop Dynamic

Definitions:
RESR = Output Capacitor Equivalent Series Resistance
RDC = Output Inductor DC Resistance
VRAMP_PP = SP6133 internal RAMP Amplitude Peak to Peak Voltage

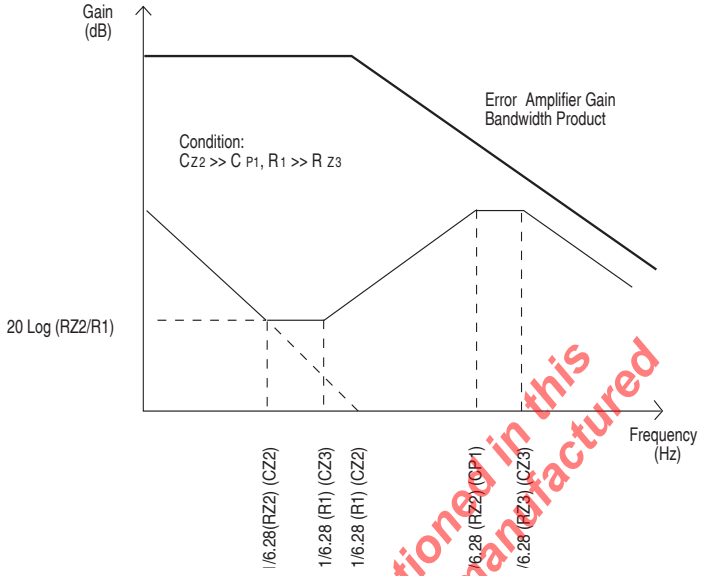


Figure 6: Bode Plot of Type III Error Amplifier Compensation

Note: Loop Compensation component calculations discussed in this Datasheet can be quickly iterated with the Type III Loop Compensation Calculator on the web at:
www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

INDUCTORS - SURFACE MOUNT							
Manufacturer/Part No.	Inductance (uH)	Inductor Specification					Manufacturer Website
		Series R mOhms	Isat (A)	Size LxW(mm)	Ht.(mm)	Inductor Type	
Inter-Technical SC5018-2R7M	**2.7**	**4.10**	**15.0**	**12.6x12.6**	**4.5**	**Shielded Ferrite Core**	www.inter-technical.com

CAPACITORS - SURFACE MOUNT								
Manufacturer/Part No.	Capacitance (uF)	Capacitor Specification						Manufacturer Website
		ESR ohms (max)	Ripple Current (A) @ 45C	Size LxW(mm)	Ht.(mm)	Voltage (V)	Capacitor Type	
TDK C3225X7R1C226M	**22**	**0.005**	**4.00**	**3.2x2.5**	**2.0**	**16.0**	**X7R Ceramic**	www.tdk.com
TDK C3225X5R0J107M	**100**	**0.005**	**4.00**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic**	www.tdk.com

MOSFETS - SURFACE MOUNT								
Manufacturer/Part No.	MOSFET	MOSFET Specification						Manufacturer Website
		RDS(on) mΩ (max)	ID Current (A)	Qg nC (Typ)	nC (Max)	Voltage (V)	Foot Print	
Vishay Si4394DY	**N-Channel**	**9.75**	**14**	**12.5**	**-**	**30**	**SO-8**	www.vishay.com
Vishay Si4320DY	**N-Channel**	**4**	**22**	**45**	**70**	**30**	**SO-8**	www.vishay.com

Note: Components highlighted in **bold** are those used on the SP6133 Evaluation Board.

Table 1. Input and Output Stage Components Selection Charts

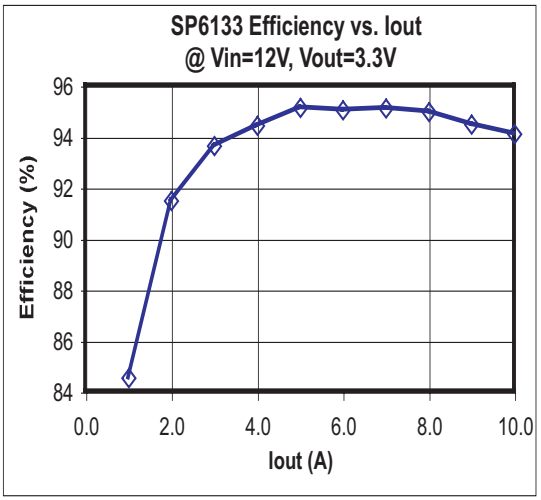


Figure 7: Efficiency vs. IOUT, VIN = 12V

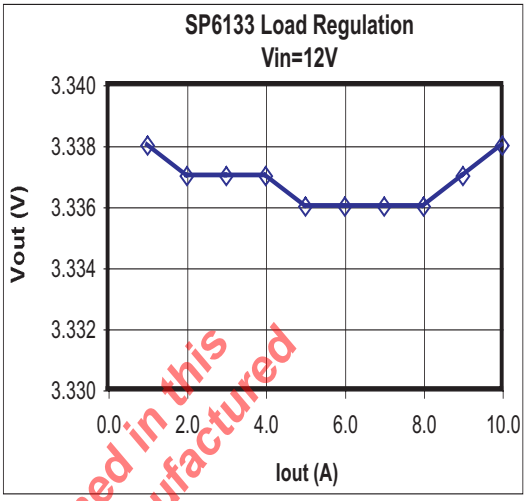


Figure 8: Load Regulation, 12V

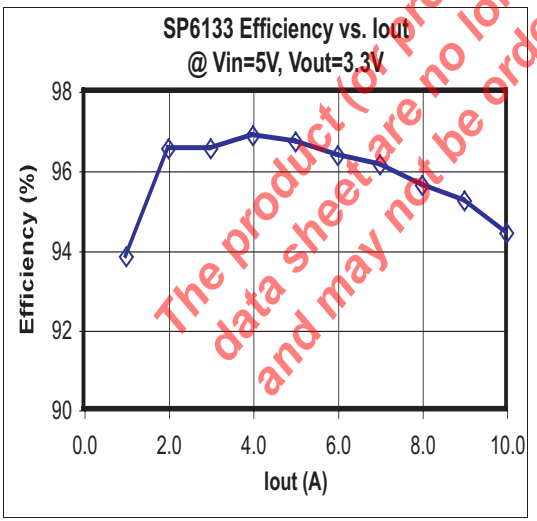


Figure 9: Efficiency vs. IOUT, VIN = 5V

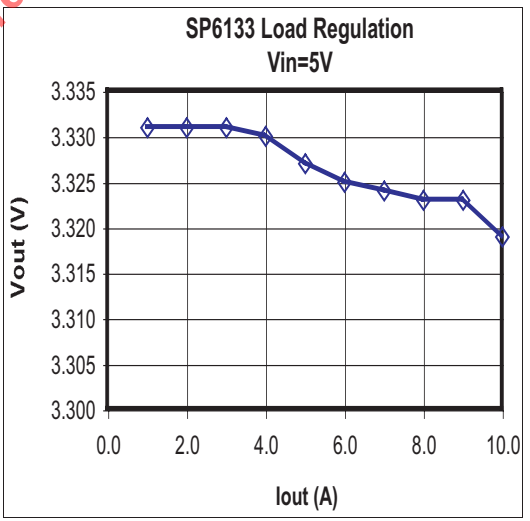


Figure 10: Load Regulation, 5V

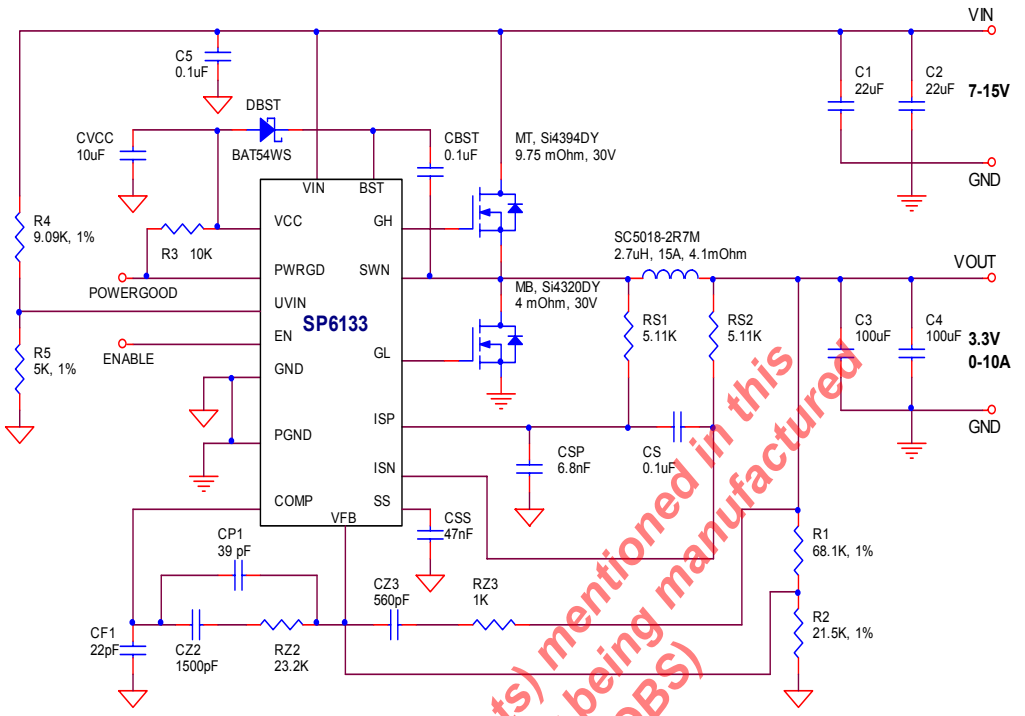


Figure 11: SP6133 circuit showing wide input range

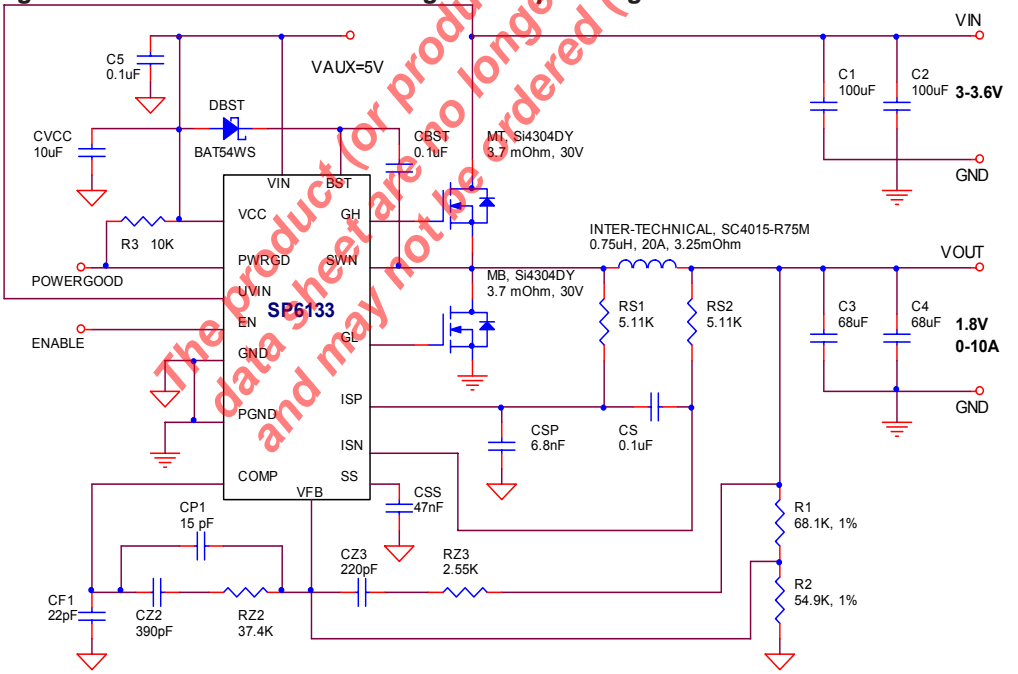


Figure 12. SP6133: 3.3V Input Buck Regulator with auxiliary 5V bias

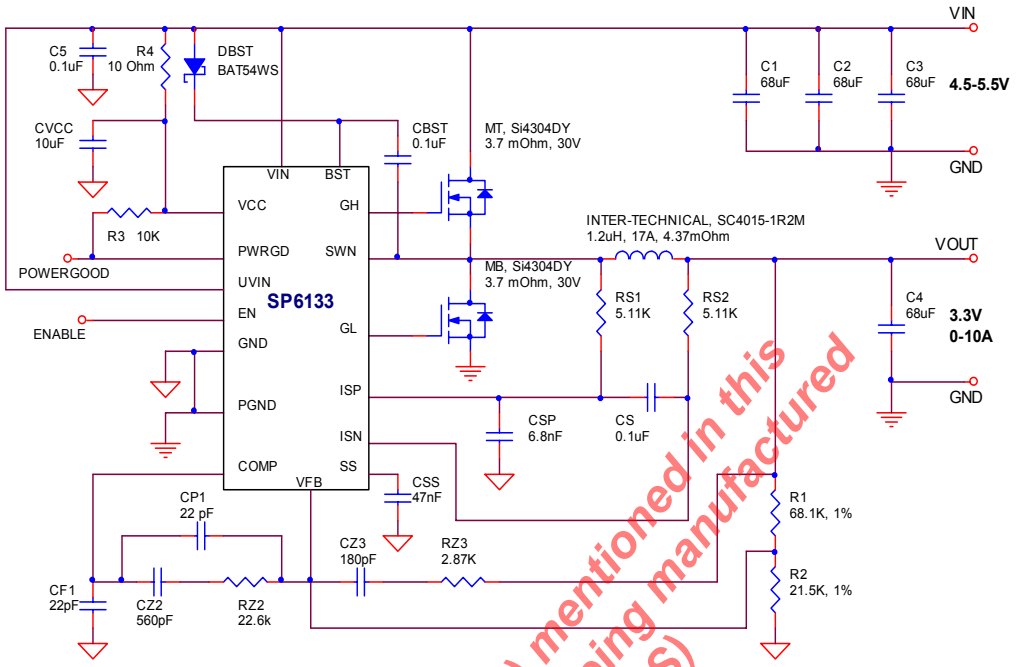


Figure 13. SP6133: 5V Input Buck Regulator

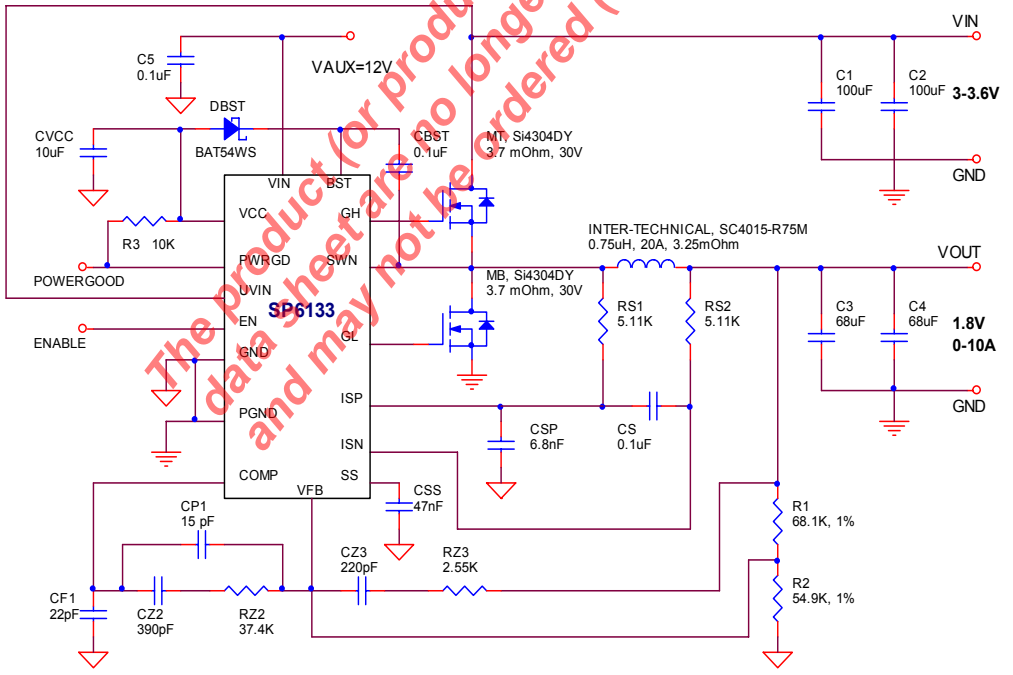


Figure 14. SP6133: 3.3V Input Buck Regulator with auxiliary 12V bias

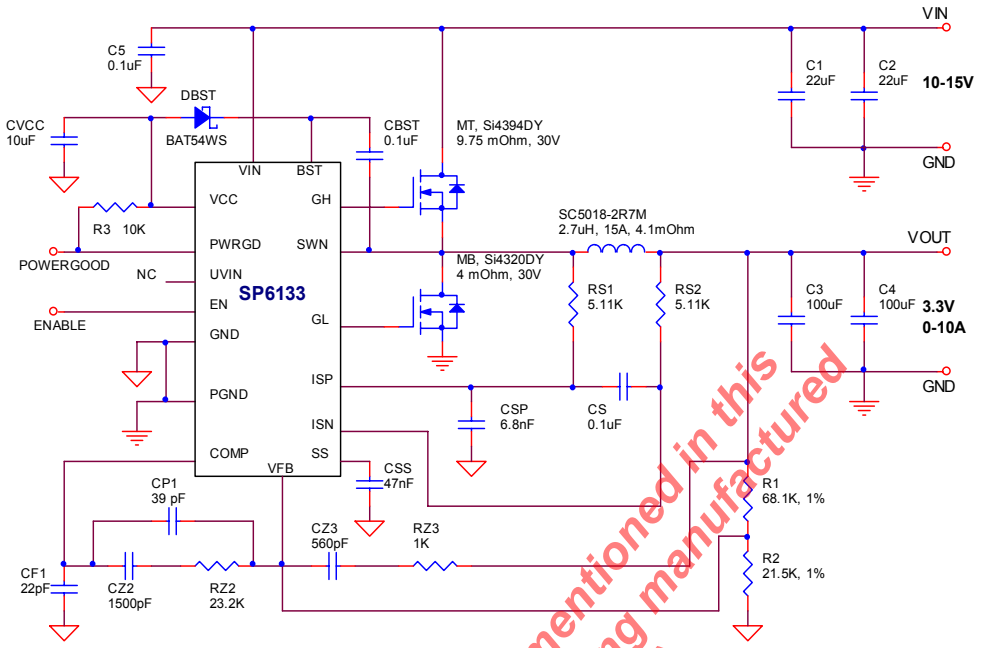
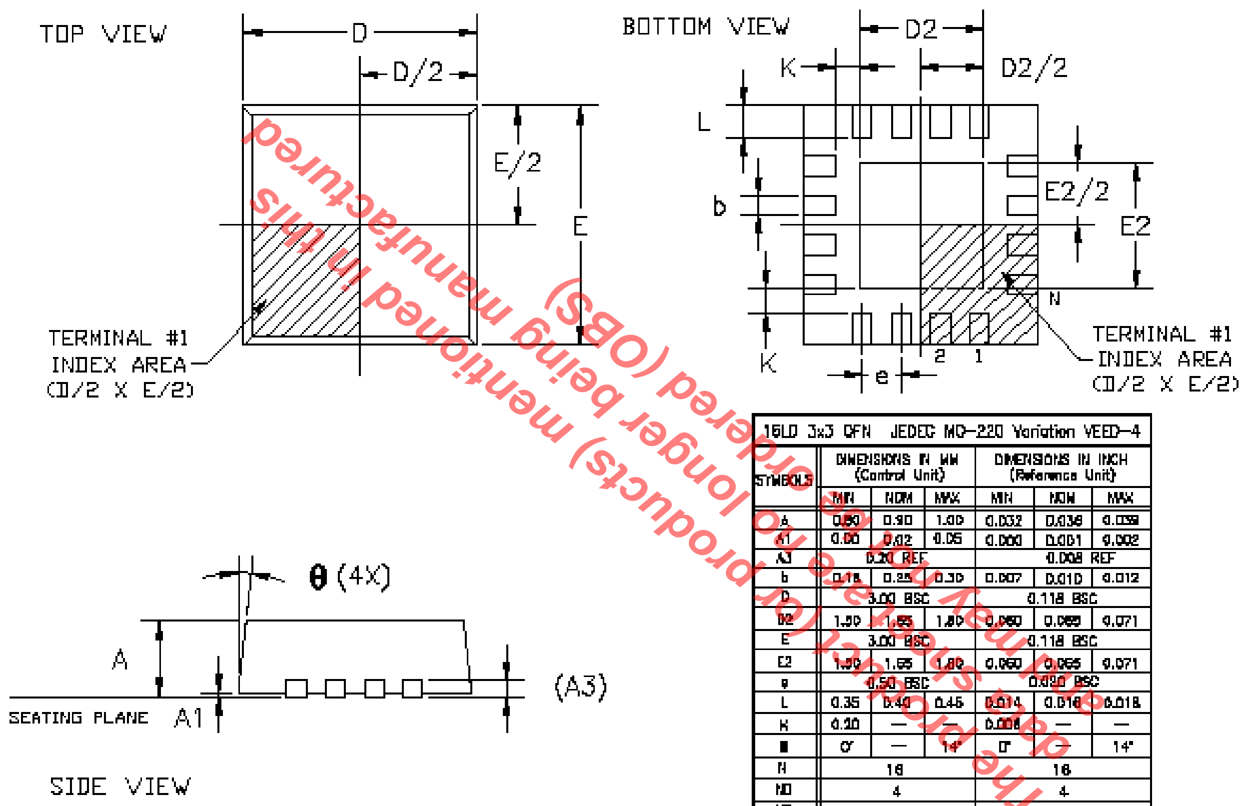


Figure 15. SP6133: 10-15V Input Buck Regulator

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/12/05	JL
B	MODIFY DRAWING FORMAT	07/20/06	JL



16LD 3x3 QFN JEDEC MO-220 Variation VEED-4						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	3.00 BSC			0.118 BSC		
D2	1.50	1.65	1.80	0.060	0.065	0.071
E	3.00 BSC			0.118 BSC		
E2	1.50	1.65	1.80	0.060	0.065	0.071
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	—	—	0.008	—	—
θ	0°	—	14°	0°	—	14°
N	16			16		
ND	4			4		
NE	4			4		

SIPEX CORPORATION

16 PIN 3x3 QFN PACKAGE OUTLINE

Packaging Approval:		Drawing No:	16-PIN 3x3 QFN
By: JL	Date: 07/20/06	Revision: B	Sheet: 1 OF 1

ORDERING INFORMATION

Part Number	Temperature Range	Package	Package Method	Lead Free(2)
SP6133ER1-L/TR	-40°C to +85°C	QFN16 3x3	Tape and Reel	Yes
SP6133EB	SP6133 Evaluation Board			

Notes:

1. Refer to www.maxlinear.com/SP6133 for most up-to-date Ordering Information.

2. Visit maxlinear.com for additional information on Environmental Rating.

REVISION HISTORY

Revision	Date	Desription
L	10/24/06	Legacy Sipex datasheet
M	01/22/20	Updated to MaxLinear logo. Updated Ordering Information. Added Revision History.

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DATE	Rev	Changes Implemented	Input Source
Oct 26-05		SP613x family has the same “GH Minimum Pulse Width” max spec is 100ns.	Khanh Thai
Oct 27-05		File Size Reduction from 5MB to <1 MB.	Field
Nov 1-05		Dropout voltage typo on pg3: mV, not V.	Field
Nov 3-05		Die attach paddle internally connected to GND..	Field
Nov 11-05		Multiple corrections to examples, Figures 1,2 &3; affecting layout	Shahin Maloyan
Nov 17-05		Ed Lam authorized the creation of a Preliminary data-sheet to be sent to Partnernet in the interim time where we are trying to get the FINAL datasheet approved.	Field
Nov 21-05		Page 8 remove"232kohm standard".	Shahin Maloyan
Jan 11-06		Post-approval additions of diagrams: Vin10-15, Vin3.3-Vaux12v, Vin3.3-Vaux5v, vin5V, Vin7-15V. Proposed simplifi-cation of equation 2 accepted.	Shahin Maloyan
Jan 13-06		Post-approval changes, affecting layout: 1- page 1, Use the schematic of figure 15 as main schematic. 2- page 14, inductors, change “TDK RLF12560T-2R7N110” and its description to “Inter-Technical SC5018-2R7M, 2.7uH, 4.1mOhm, 15A, 12.6x12.6mm, 4.5mm, Shielded Ferrite core, www.inter-technical.com” 3- page 14, remove all the other inductors.	Shahin Maloyan
Feb 16-06		Added “Solved by Sipex tm” @ end and LOGO. Grey scale on tables.	Kevin O'Malley,
		Changing links and metatags for more suitable search engine results.	Brad Hudon
		Ordering information can’t have dots, must have dashes.	Mark Levi
		Added U.S. Patent; #6,922,041. (affecting layout)	Stuart Schneck
		Changed Header to single box Fill grey 30% edge wt 4/40% grey .	Sally Pena
Oct 20-06	K	Updated Block Diagram	Shahin Maloyan
Oct23-06	K	Brought into PC inDesign. fixed some resulting format is-sues. changed x to • Added TypeIII calculator note.	Kevin O'Malley
Oct24-06	L	Block diagram file used was incorrect...Hand drawn cor-rections such as non-synchronous.	Shahin M
		This information is not to be given out to customers.	