XRT75VL00D

E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET

SEPTEMBER 2008 *REV. 1.0.4*

GENERAL DESCRIPTION

The XRT75VL00D is a single-channel fully integrated Line Interface Unit (LIU) with Sonet Desynchronizer for E3/DS3/STS-1 applications. It incorporates an independent Receiver, Transmitter and Jitter Attenuator in a single 52 pin TQFP package.

The XRT75VL00D can be configured to operate in either E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) modes. The transmitter can be turned off (tri-stated) for redundancy support and for conserving power.

The XRT75VL00D's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75VL00D incorporates an advanced crystal-less jitter attenuator that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications. Also, the jitter attenuator can be used for clock smoothing in SONET STS-1 to DS3 de-mapping.

The XRT75VL00D provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75VL00D supports local, remote and digital loop-backs. The XRT75VL00D also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements.
- Detects and Clears LOS as per G.775.
- Meets Bellcore GR-499 CORE Jitter Transfer Requirements.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards.
- Meets ETSI TBR 24 Jitter Transfer Requirements.
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled.
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock.
- Provides low jitter output clock.

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitter can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuator can be selected in Receive or Transmit paths.
- 16, 32 or 128 bits selectable FIFO size.
- Meets the Jitter and Wander specifications described in T1.105.03b,ETSI TBR-24, Bellcore GR-253 and GR-499 standards.
- Jitter Attenuator can be disabled.
- De-Synchronizer for SONET STS-1 to DS-3 demapping.

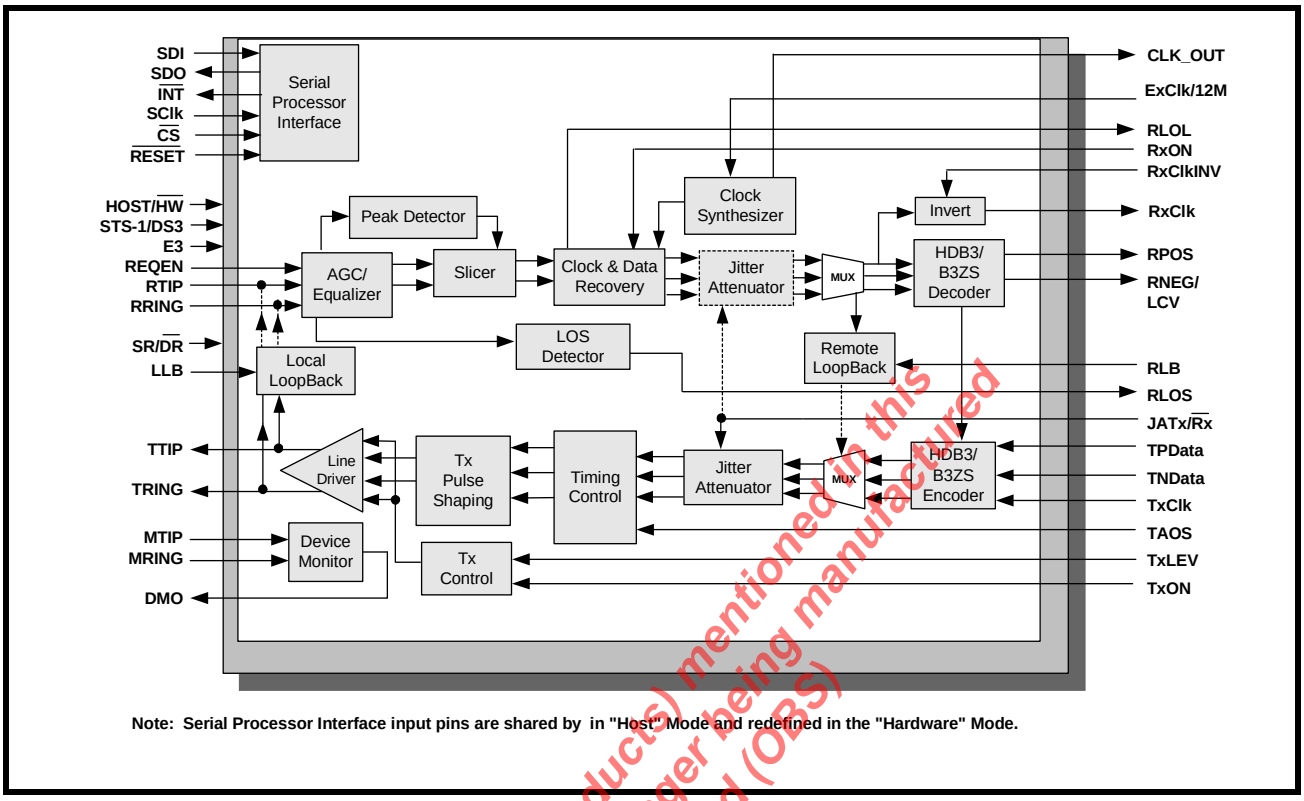
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Hardware Mode for control and configuration.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Available in 52 pin TQFP.
- -40℃ to 85℃ Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.
- Fiber Optic Terminals.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75VL00D



Note: Serial Processor Interface input pins are shared by in "Host" Mode and redefined in the "Hardware" Mode.

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE.
- Transmitter can be turned off in order to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

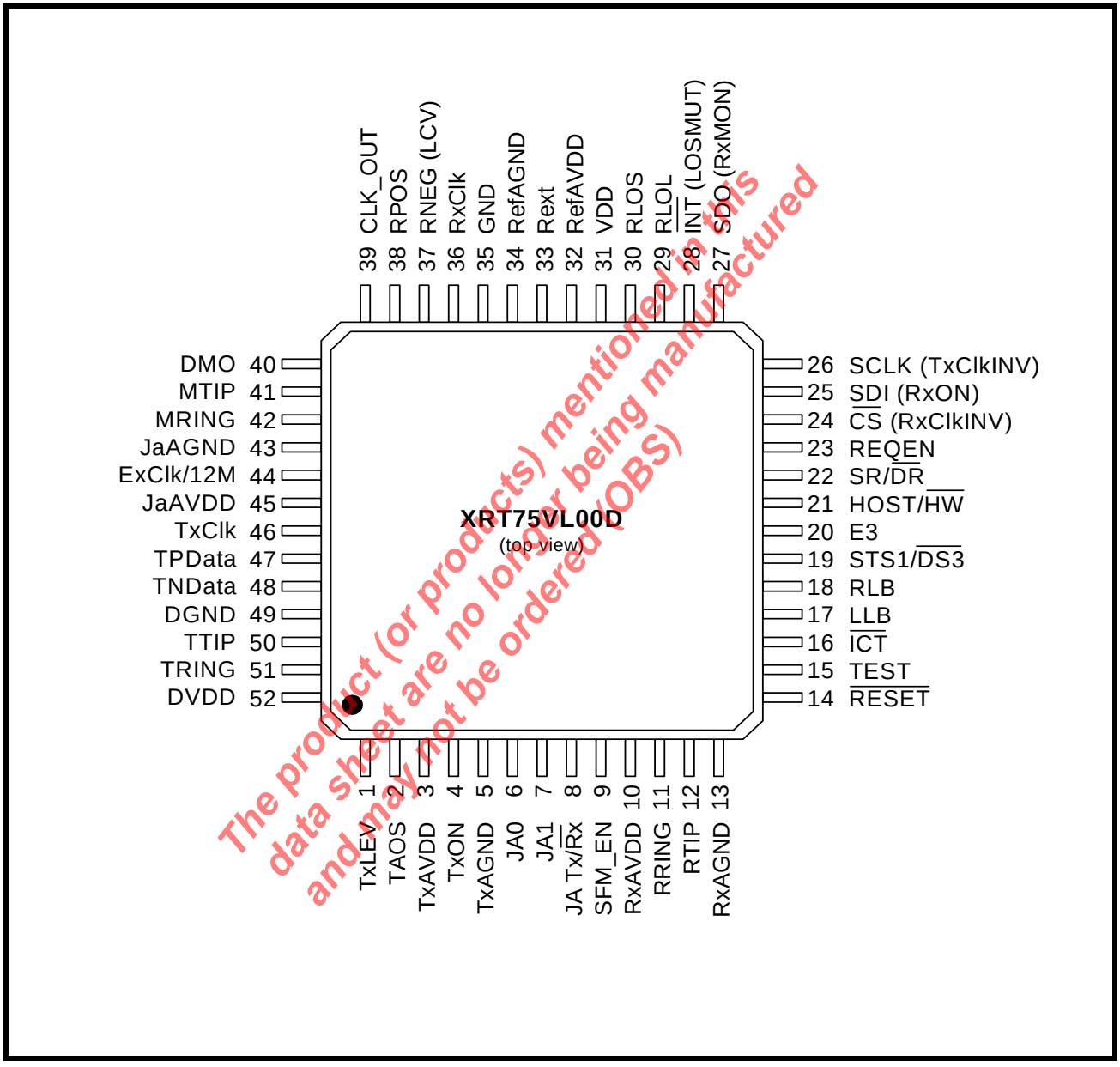
- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).
- Recovered Data can be muted while the LOS Condition is declared.

- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

JITTER ATTENUATORS

The XRT75VL00D includes a Jitter Attenuator that meets the Jitter requirements specified in the ETSI TBR-24, Bellcore GR-499 and GR-253 standards. In addition, the jitter attenuator also meets the Jitter and Wander specifications described in the ANSI T1.105.03b 1997, Bellcore GR-253 and GR-499 standards.

FIGURE 2. PIN OUT OF THE XRT75VL00D



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75VL00DIV	52 Pin TQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
4	TxON	I	**Transmitter ON Input** Setting this input pin "High" turns on the Transmitter. ***NOTES:*** 1. *Even when the XRT75VL00D is configured in HOST mode, this pin still controls the TTIP and TRING outputs* 2. *When the Transmitter is turned off either in Host or Hardware mode,the TTIP and TRING outputs are Tri-stated.* 3. *This pin is internally pulled down*
46	TxClk	I	**Transmit Clock Input for TPData and TNData** The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%. The XRT75VL00D samples the TPData and TNData pins on the falling or rising edge of TxClk signal based on the status of TxClkINV pin (in Hardware mode) or the status of the bit in the Channel Register (in HOST mode).
26	TxClkINV/ SClk	I	**Transmit Clock Invert or Serial Clock Input:** Function of this depends on whether the XRT75VL00D is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin “High” configures the Transmitter to sample the TPData and TNData data on the rising edge of the TxClk. ***NOTE:*** *If the XRT75VL00D is configured in HOST mode, this pin functions as SClk input pin (please refer to the pin description for Microprocessor interface).*
48	TNData	I	**Transmit Negative Data Input** If the XRT75VL00D is configured in Dual-rail mode, this pin is sampled on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode). ***NOTES:*** 1. *This input pin is ignored and should be tied to GND if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.*
47	TPData	I	**Transmit Positive Data Input** The XRT75VL00D samples this pin on the falling or rising edge of TxClk based on the status of the TClkINV pin (in Hardware mode) or the status of the control bit in the Channel Register (in HOST mode).
50	TTIP	O	**Transmit TTIP Output** The XRT75VL00D uses this pin along with TRING to transmit a bipolar signal to the line using a 1:1 transformer.

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
51	TRING	O	**Transmit Ring Output** The XRT75VL00D uses this pin along with TTIP to transmit a bipolar signal to the line using a 1:1 transformer.
1	TxLEV	I	**Transmit Line Build-Out Enable/Disable Select** This input pin is used to enable or disable the Transmit Line Build-Out circuit. Setting this pin to "High" disables the Line Build-Out circuit. In this mode, partially-shaped pulses are output onto the line via the TTIP and TRING output pins. Setting this pin to "Low" enables the Line Build-Out circuit. In this mode, shaped pulses are output onto the line via the TTIPand TRING output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this pin to "1" if the cable length between the Cross-Connect and the transmit output is greater than 225 feet. 2. Set this pin to "0" if the cable length between the Cross-Connect and the transmit output is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT75VL00D is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT75VL00D is configured to operate in the Hardware Mode. ***NOTES:*** *1. This pin is internally pulled down.* *2. If the XRT75VL00D is configured in HOST mode, this pin may be tied to GND.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
25	RxON/ SDI	I	**Receiver Turn ON Input or Serial Data Input:** Function of this pin depends on whether the XRT75VL00D is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" turns on and enables the Receiver.. ***NOTES:*** 1. *If the XRT75VL00D is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface)* 2. *This pin is internally pulled down.*
23	REQEN	I	**Receive Equalization Enable Input** Setting this input pin "High" enables the Internal Receive Equalizer. Setting this pin "Low" disables the Internal Receive Equalizer. ***NOTES:*** 1. *This input pin is ignored and may be connected to GND if the XRT75VL00D is operating in the HOST Mode* 2. *This pin is internally pulled down.*
36	RxClk	O	**Receive Clock Output** The Recovered Clock signal from the incoming line signal is output through this pin.By default, the Receiver Section outputs data via RPOS and RNEG pins on the rising edge of this clock signal. Configure the Receiver Section to update data on the RPOS and RNEG pins on the falling edge of RxClk by doing the following: a) **Operating in Hardware mode**, pull the RxClkINV pin to "High". b) **Operating in Host mode**, write a "1" to RxClkINV bit field within the Receive Control Register.
24	RxClkINV/ $\overline{CS}$	I	**RxClk INVERT or Chip Select**: Function of this pin depends on whether the XRT75VL00D is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures the Receiver Section to invert the RxClk output signals and outputs the recovered data via RPOS and RNEG on the falling edge of RxClk. ***NOTE:*** *If the XRT75VL00D is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).*
38	RPOS	O	**Receive Positive Data Output** This output pin pulses "High" whenever the XRT75VL00D has received a Positive Polarity pulse in the incoming line signal at the RTIP/RRing inputs.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
37	RNEG/LCV	O	**Receive Negative Data Output/Line Code Violation Indicator** **Function of these pins depends on whether the XRT75VL00D is configured in Single Rail or Dual Rail mode.** If the XRT75VL00D is configured in Dual Rail mode, a negative pulse is output through RNEG. **In Hardware mode:** Tie the pin SR/$\overline{DR}$ (pin 22) "High" to configure the XRT75VL00D in Single Rail mode and tie "Low" to configure in Dual Rail mode. **In HOST mode:** XRT75VL00D can be configured in Single Rail or Dual Rail by setting or clearing the bit in the block control register. **Line Code Violation Indicator** If the XRT75VL00D is configured in Single Rail mode then: Whenever the Receiver Section detects a Line Code violation, it pulses this output pin "High". This output pin remains "Low" at all other times. It is advisable to sample this output pin using the RxClk output signal.
11	RRING	I	**Receive Ring Input** This input pin along with RTIP is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
12	RTIP	I	**Receive TIP Input** This input pin along with RRNG is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
27	RxMON/ SDO	I	**Receive Monitoring Mode or Serial Data Output:** In Hardware mode, when this pin is tied "High" XRT75VL00D configures into monitoring channel. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows to monitor very weak signal before declaring LOS. In HOST Mode, XRT75VL00D can be configured to be a monitoring channel by setting the bits in the receive control register. ***NOTE:*** *If the XRT75VL00D is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).*

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
44	ExClk/12M	I	**Clock Input (34.368 MHz or 44.736 MHz or 51.84 MHz ± 20 ppm):** Based on the mode selected, provide the appropriate reference clock signal. If the XRT75VL00D is configured for Single Frequency Mode with the SFM_EN tied "High", then provide a 12.288 MHz ± 20 ppm clock and depending on the mode, the correct frequency is generated internally by the clock synthesizer..
9	SFM_EN	I	**Single Frequency Enable:** Tie this pin "High" to select the single frequency mode. When enabled, a single frequency clock, 12.288 MHz is input through the ExClk input pin and the internal clock synthesizer generates the appropriate clock frequency. ***NOTE:*** *This pin is internally pulled down.*
39	CLK_OUT	O	**Clock out put:** When the Single Frequency Mode is selected, a low jitter clock will be out put. The frequency of this clock depends on whether the XRT75VL00D is configured in E3 or DS3 or STS-1 mode.

OPERATING MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
21	HOST/($\overline{HW}$)	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure the XRT75VL00D in HOST mode. Tie this "Low" to configure in Hardware mode. When the XRT75VL00D is configured in HOST mode, the states of many discrete input pins are ignored. ***NOTE:*** *This pin is internally pulled up.*
20	E3	I	**E3 Mode Select Input** A "High" on this pin configures to operate in the E3 mode. A "Low" on this pin configures to operate in either STS-1 or DS3 mode depending on the setting on pin 19. ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00D is configured to operate in HOST mode.*
19	STS-1/$\overline{DS3}$	I	**STS-1/DS3 Select Input** A "High" on this pin configures to operate in STS-1 mode. A "Low" on this pin configures to operate in DS3 mode. This pin is ignored if the E3 pin is set to "High". ***NOTES:*** 1. *This pin is internally pulled down* 2. *This pin is ignored and may be tied to GND if the XRT75VL00D is configured to operate in HOST mode.*
22	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select:** Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, Transmit input at TNData should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. ***NOTE:*** *This pin is internally pulled down.*

CONTROL AND ALARM INTERFACE

42	MRING	I	**Monitor Ring Input** The bipolar line output signal from TRING is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
41	MTIP	I	**Monitor Tip Input** The bipolar line output signal from TTIP is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled down.*
40	DMO	O	**Drive Monitor Output** If MTIP and MRING has no transition pulse for 128 ± 32 TxClk cycles, DMO goes "High" to indictae the driver failure. DMO output stays "High" until the next AMI signal is detected.

CONTROL AND ALARM INTERFACE

30	RLOS	O	**Receive Loss of Signal Output Indicator** This output pin toggles "High" if Receiver has detected a Loss of Signal Condition in the incoming line signal. The criteria for declaring/clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode and is described in Section 2.04.
29	RLOL	O	**Receive Loss of Lock Output Indicator:** This output pin toggles "High" if the XRT75VL00D has detected a Loss of Lock Condition. LOL (Loss of Lock) condition is declared if the recovered clock frequency deviates from the Reference Clock frequency (available at ExClk input pin) by more than 0.5%.
33	Rext	****	**External Bias control Resistor of 3.3 KΩ ±1%.** Should be connected to RefAGND via 3.3 KΩ resistor.
15	TEST	I	**Test Mode:** Connect this pin “High” to configure the XRT75VL00D in test mode. ***NOTE:*** *This pin is internally pulled Down.*
16	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled “High".*
2	TAOS	I	**Transmit All Ones Select** A “High" on this pin causes the Transmitter Section to generate and transmit a continuous AMI all “1’s” pattern onto the line. The frequency of this “1’s” pattern is determined by TxClk. ***NOTES:*** *1. This input pin is ignored if the XRT75VL00D is operating in the HOST Mode and should be tied to GND.* *2. Analog Loopback and Remote Loopback have priority over request.* *3. This pin is internally pulled down.*
28	LOSMUT/ $\overline{\text{INT}}$	I/O	**MUTE-upon-LOS Enable Input or Interrupt Ouput:** In Hardware Mode, setting this pin “High” configures the XRT75VL00D to Mute the recovered data on the RPOS and RNEG whenever an LOS condition is declared. RPOS and RNEG outputs are pulled “Low”. ***NOTE:*** *If the XRT75VL00D is configured in HOST mode, this pin functions as $\overline{\text{INT}}$ pin (please refer to the pin description for the Microprocessor Interface).*

CONTROL AND ALARM INTERFACE

17	LLB	I	**Local Loop-back** This input pin along with RLB configures different Loop-Back modes. **NOTE:** *This input pin is ignored and may be connected to GND if the XRT75VL00D is operating in the HOST Mode.*
18	RLB	I	**Remote Loop-back** This input pin along with LLB configures different Loop-Back modes. **NOTE:** *This input pin is ignored and should be connected to GND if the XRT75VL00D is operating in the HOST Mode.*

RLB	LLB	Loopback Mode
0	0	Normal Operation
0	1	Analog Local
1	0	Remote
1	1	Digital

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
24	$\overline{CS}$/RxClkINV	I	**Microprocessor Serial Interface - Chip Select** Tie this "Low" to enable the communication with Serial Microprocessor Interface. **NOTE:** *If the XRT75VL00D is configured in Hardware Mode,this pin functions as RxClkINV.*
26	SCLK/TxClkINV	I	**Serial Interface Clock Input** The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **NOTE:** *If the XRT75VL00D is configured in Hardware Mode, this pin functions as TxClkINV.*
25	SDI/RxON	I	**Serial Data Input:** Data is serially input through this pin. The input data is sampled on the rising edge of the SCLK pin (pin 26). **NOTES:** 1. *This pin is internally pulled down* 2. *If the XRT75VL00D is configured in Hardware Mode, this pin functions as RxON.*
27	SDO/RxMON	O	**Serial Data Output:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SCLK and this pin is tri-stated upon completion of data transfer. **NOTE:** *If the XRT75VL00D is configured in Hardware Mode, this pin functions as RxMON.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
14	$\overline{\text{RESET}}$	I	**Register Reset:** Setting this input pin "Low" causes the XRT75VL00D to reset the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*
28	$\overline{\text{INT}}$/LOSMUT	I/O	**INTERRUPT Output:** This pin functions as Interrupt Output for Serial Interface. A transition to “Low” indicates that an interrupt has been generated by the Serial Interface. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register. ***NOTE:*** *If the XRT75VL00D is in Hardware mode, this pin functions as LOSMUT.*

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
6	JA0	I	**Disable Jitter Attenuator/FIFO Size Select::** In Hardware Mode, this pin along with JA1 pin provides the following functions in the table below. **JA0 / JA1 / Operation** **0 / 0 / 16 bit FIFO** **0 / 1 / 32 bit FIFO** **1 / 0 / 128 bit FIFO** **1 / 1 / Disable Jitter Attenuator** ***NOTE:*** *This pin is internally pulled down.*
7	JA1	I	**Disable Jitter Attenuator/FIFO Size Select:** In Hardware Mode, this pin along with JA0 pin provides the functions in the table above. ***NOTE:*** *This pin is internally pulled down.*
8	JA Tx/$\overline{\text{Rx}}$	I	**Jitter Attenuator Select:** In Hardware Mode setting this pin "High" selects the Jitter Attenuator in the Transmit path and setting "Low" selects in Receive path. ***NOTE:*** *This pin is internally pulled down.*

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
3	TxAVDD	****	**Transmitter Analog VDD 3.3 V ± 5%**
10	RxAVDD	****	**Receiver Analog VDD 3.3 V ± 5%**
32	RefAVDD	****	**Reference Analog VDD 3.3 V ± 5%**
5	TxAGND	****	**Transmitter Analog GND**
13	RxAGND	****	**Receiver Analog GND**
34	RefAGND	****	**Reference Analog GND**
45	JaAVDD	****	**Jitter Attenuator Analog VDD 3.3 V ± 5%**
43	JaAGND	****	**Jitter Attenuator Analog GND**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
31	DVDD	****	**VDD 3.3 V ± 5% Receiver Digital**
35	DGND	****	**GND**
52	DVDD	****	**VDD 3.3 V ± 5% Transmitter Digital**
49	DGND	****	**GND**

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		20	$^0C/W$	linear air flow 0ft/min
ThetaJC			6	$^0C/W$	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current (Measured while transmitting and receiving all 1's)	65	120	175	mA
P_{DD}	Power Dissipation	210	385	610	mW
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, I_{OUT} = -4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75VL00D (DUAL-RAIL DATA)

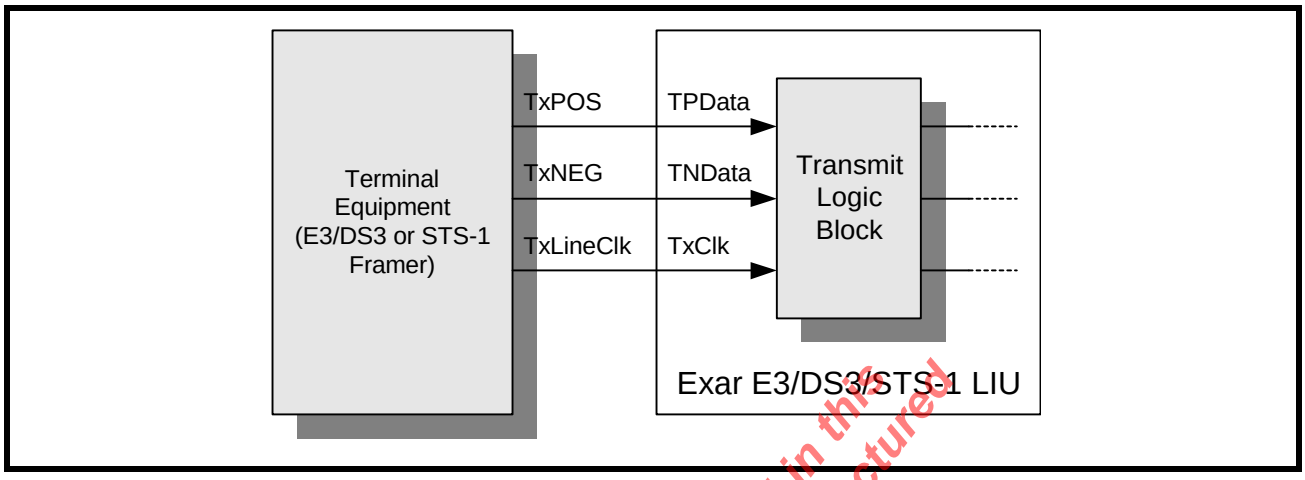
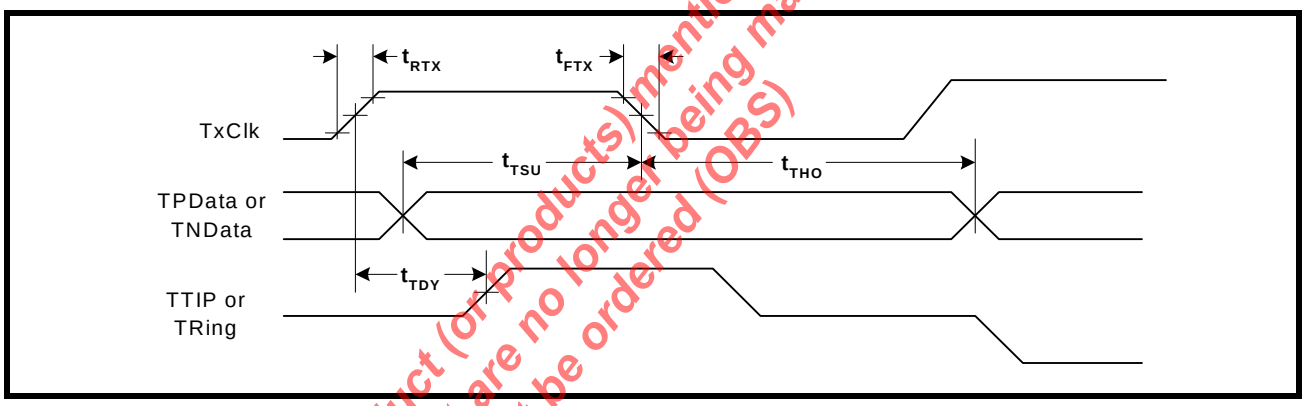
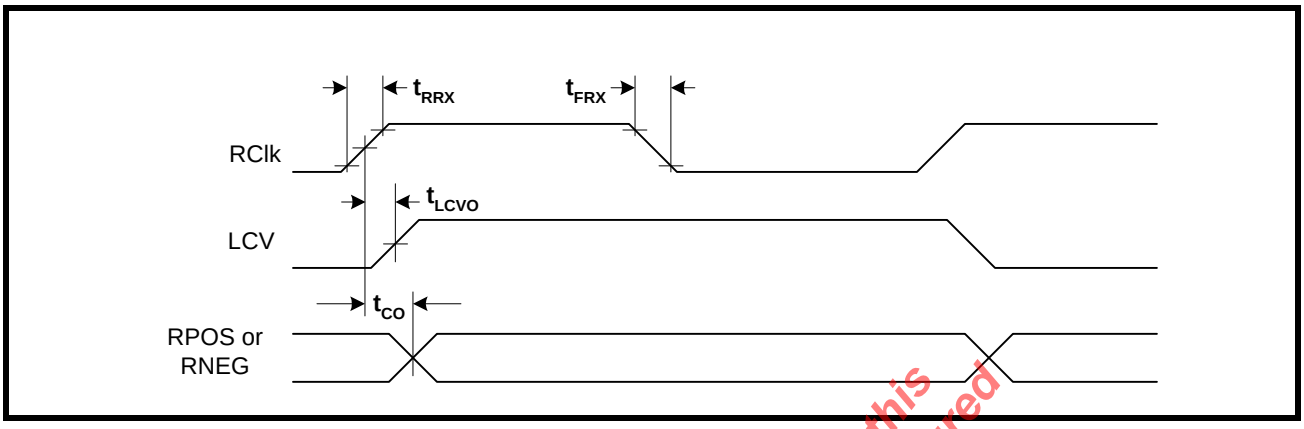


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



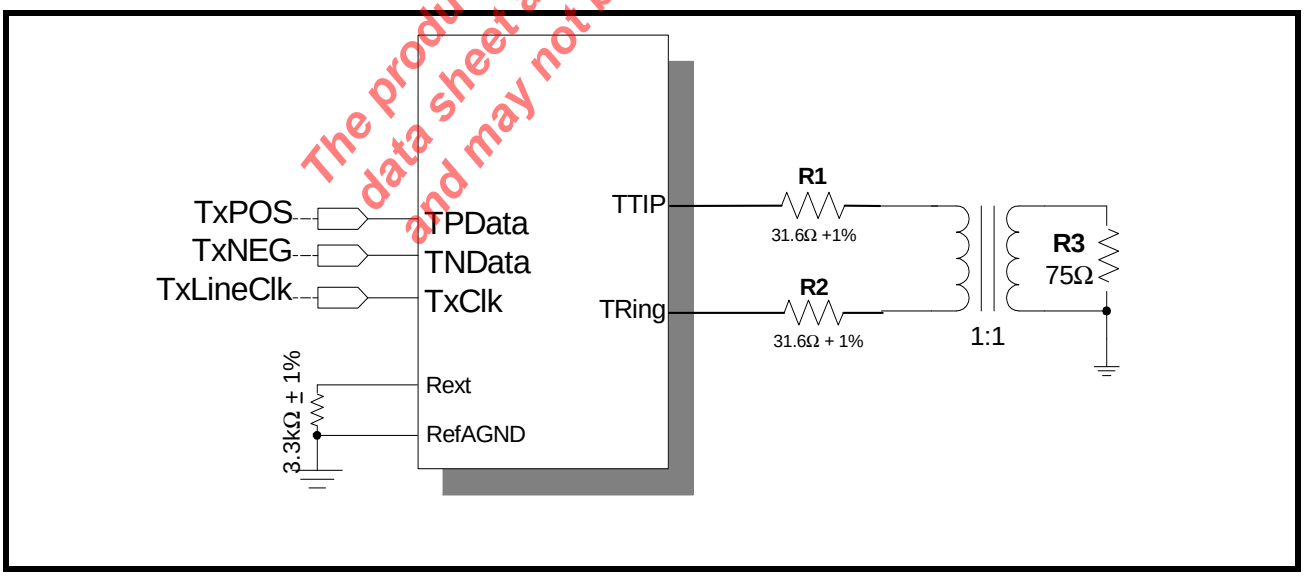
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns
t_{TDY}	TTIP/TRing to TxClk rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle E3 DS3 STS-1	45	50 34.368 44.736 51.84	55	% MHz MHz MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75VL00D meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation at the secondary of the transformer. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

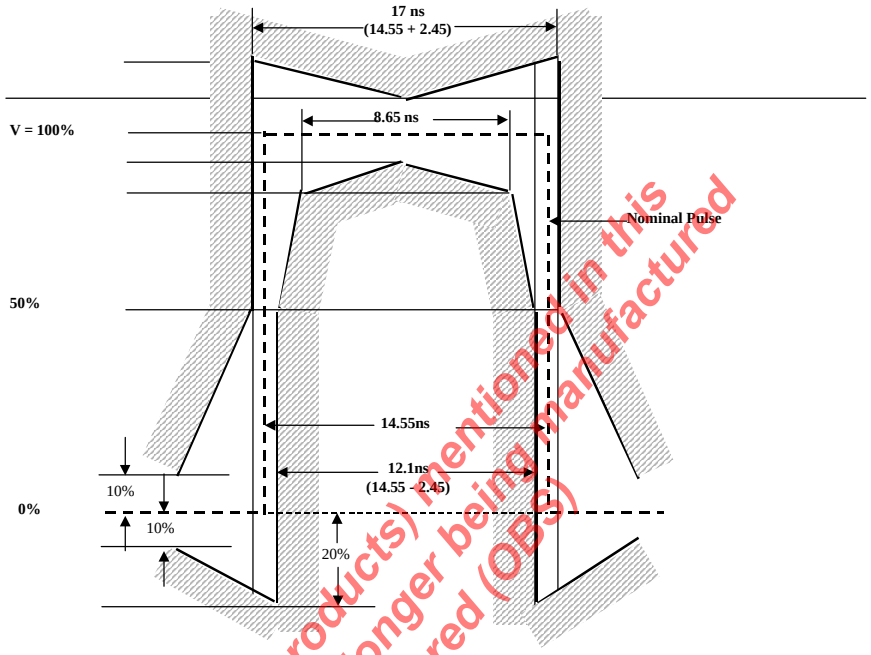


TABLE 3: E3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (T_A = 25^{0}C AND VDD = 3.3 V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Intrinsic Jitter		0.02	0.05	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-15		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

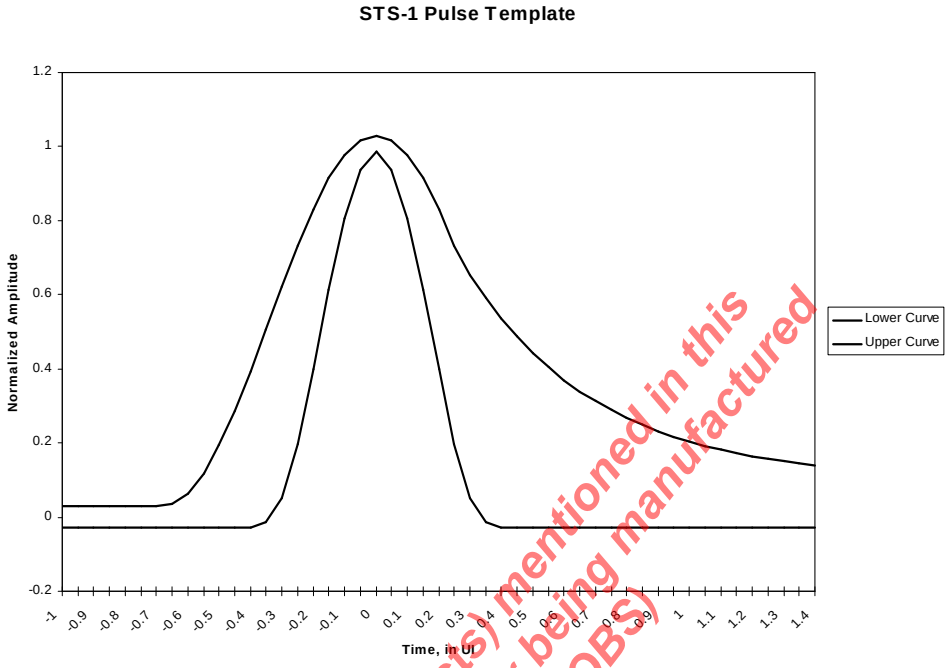


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS (TA = 25^{0}C AND VDD =3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal		Refer to Table 10		
Signal Level to Clear Loss of Signal		Refer to Table 10		

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

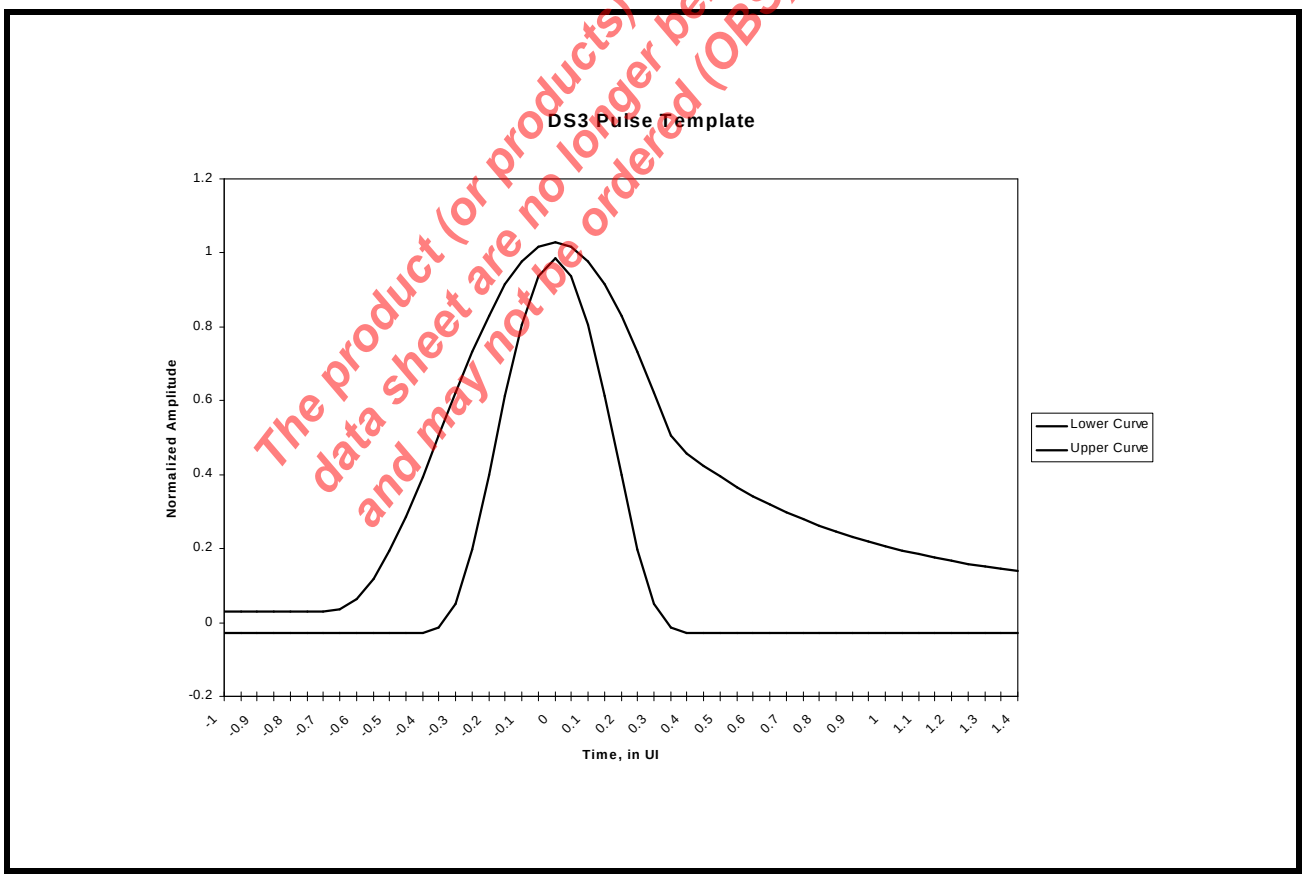


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER AND RECEIVER LINE SIDE SPECIFICATIONS ($T_A = 25^0C$ AND VDD = 3.3V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
Intrinsic Jitter		0.02	0.05	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15	0.60		UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE

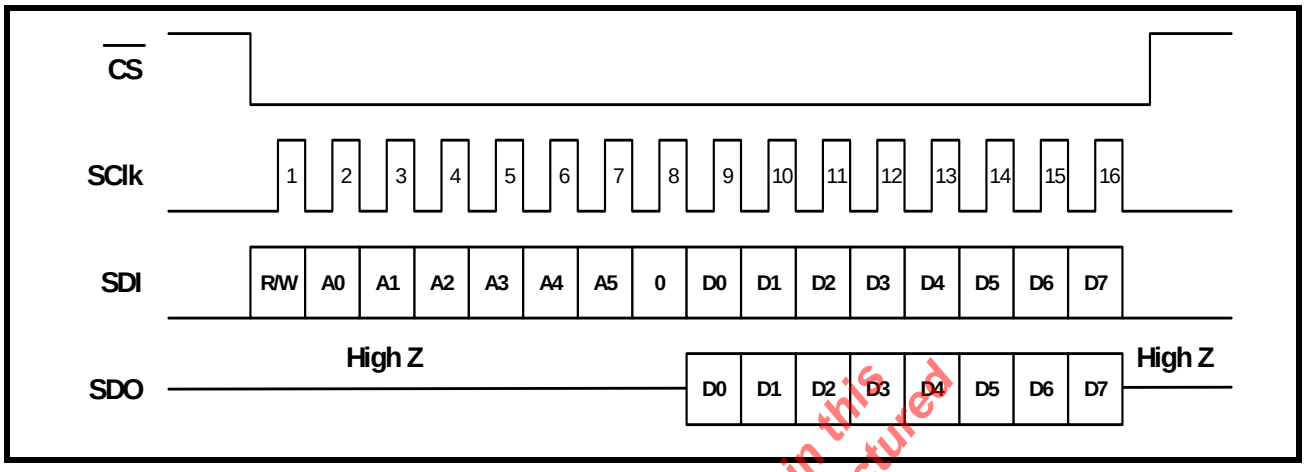


FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

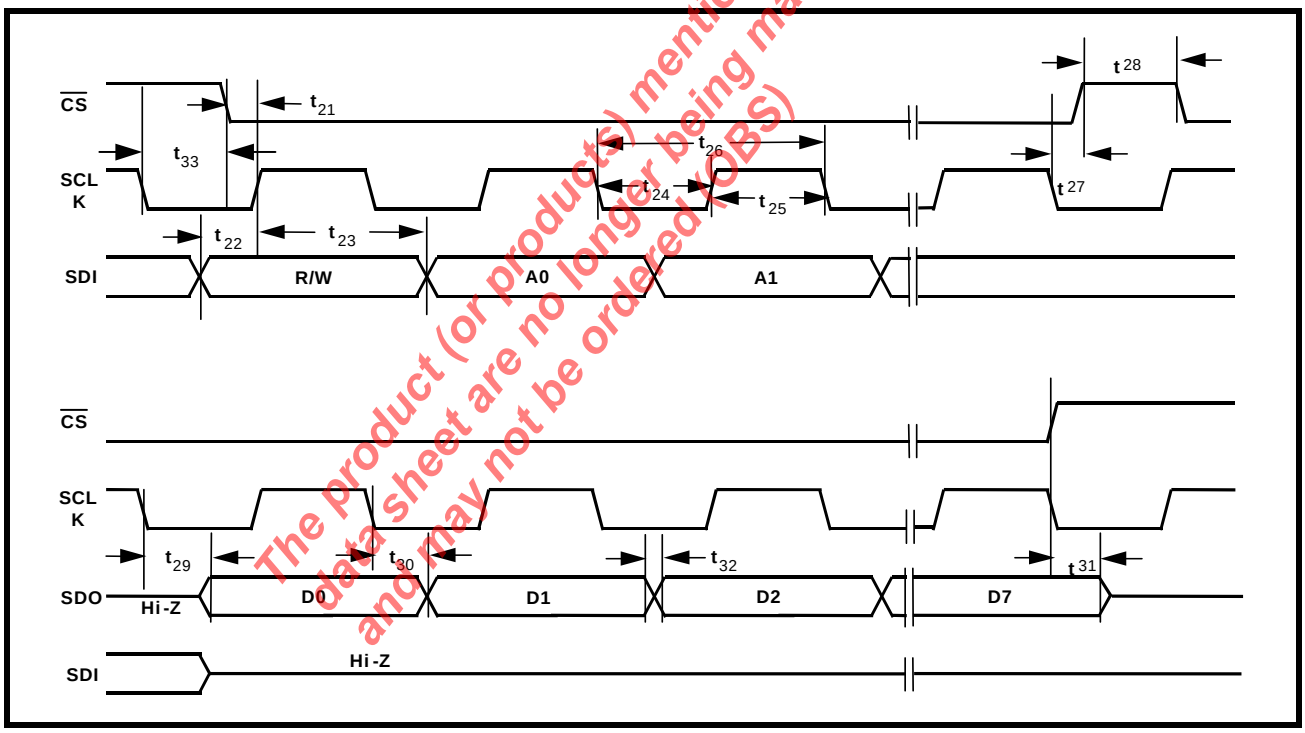


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

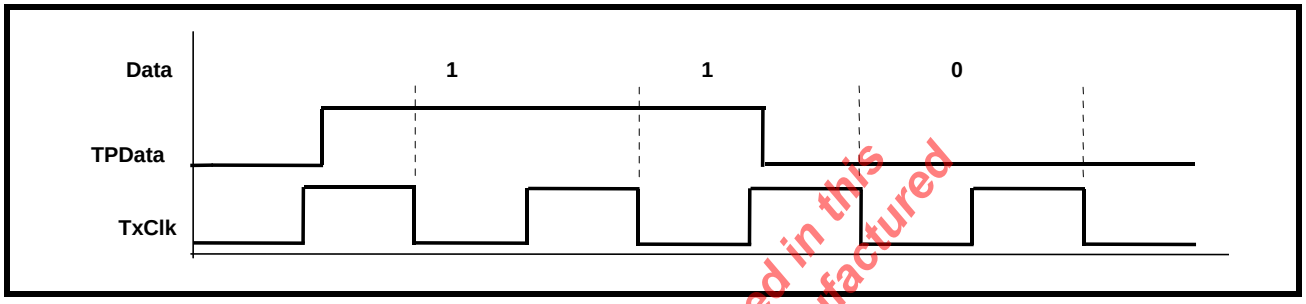
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time		25		ns
t_{25}	SClk "High" Time		25		ns
t_{26}	SClk Period		50		ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ "Inactive" Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z		10		ns
t_{32}	Rise/Fall time of SDO Output			5	ns
t_{33}	SCLK Falling Edge to $\overline{CS}$ Low Assertion Time	5			ns

4.0 THE TRANSMITTER SECTION:

The Transmitter Section accepts TTL/CMOS level signals from the Terminal Equipment in the selectable data formats.

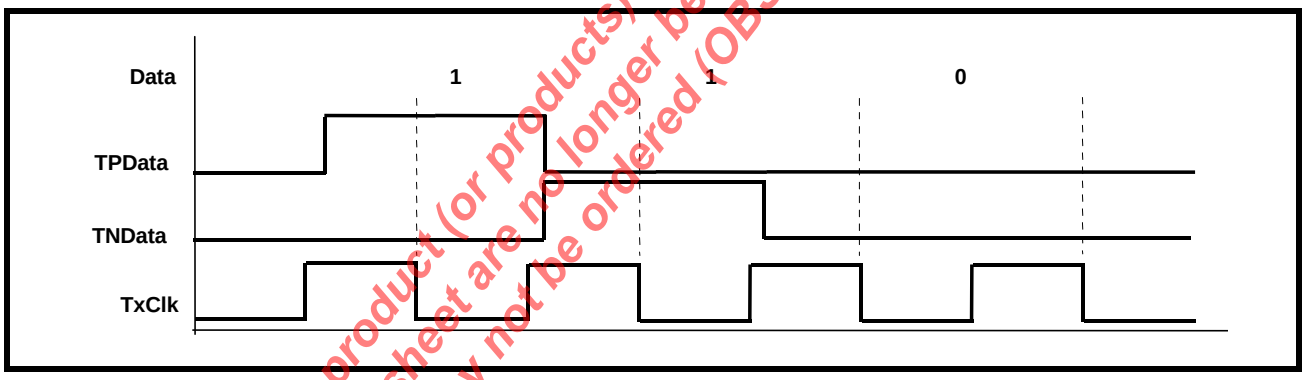
- In Single-Rail or un-encoded Non-Return-to-Zero (NRZ) input data via TPData pin while the TNData pin must be grounded. The NRZ or Single-Rail mode is selected when the SR/$\overline{DR}$ input pin is “High” (in Hardware Mode) or bit 0 of the control register is “1” (in Host Mode). Figure 12 illustrates the Single-Rail or NRZ format.

FIGURE 12. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)



- In Dual-Rail mode, data is input via TPData and TNData pins. TPData contains positive data and TNData contains negative data. The SR/$\overline{DR}$ input pin = “Low” (in Hardware Mode) or bit 0 of the control register = “0” (in Host Mode) enables the Dual-Rail mode. Figure 13 illustrates the Dual-Rail data format.

FIGURE 13. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements. Figure 7, Figure 8 and Figure 9 illustrate the pulse template requirements.
- Encode the un-encoded NRZ data into either B3ZS format (for DS3 or STS-1) or HDB3 format (for E3) and convert to pulses with shapes and width that are compliant with industry standard pulse template requirements. Figure 7,Figure 8 and Figure 9 illustrate the pulse template requirements.

4.1 TRANSMIT CLOCK:

The Transmit Clock applied via TxClk pin, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock be supplied and thus eliminates the need to use an expensive oscillator.

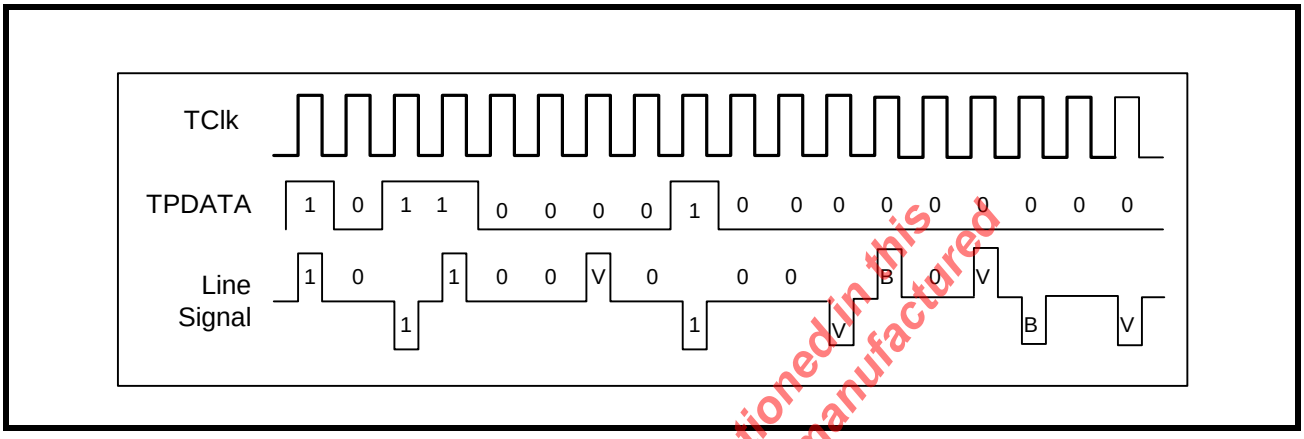
4.2 B3ZS/HDB3 ENCODER:

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.2.1 B3ZS Encoding:

An example of B3ZS encoding is shown in Figure 14. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of DC component into the line signal.

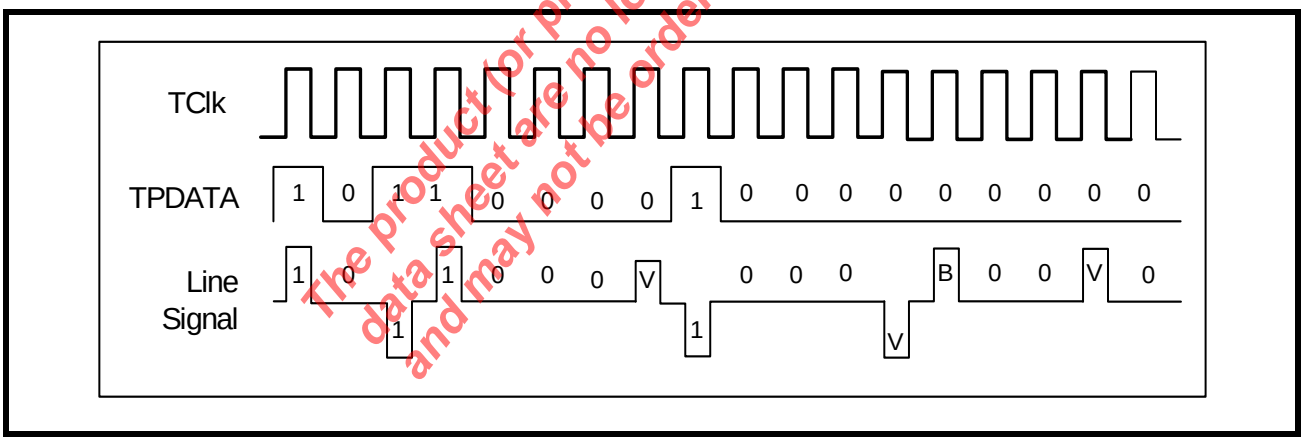
FIGURE 14. B3ZS ENCODING FORMAT



4.2.2 HDB3 Encoding:

An example of the HDB3 encoding is shown in Figure 15. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of bipolar (B) pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

FIGURE 15. HDB3 ENCODING FORMAT



NOTES:

1. *When Dual-Rail data format is selected, the B3ZS/HDB3 Encoder is automatically disabled.*
2. *In Dual-Rail format, the Bipolar Violations in the incoming data stream is converted to valid data pulses.*
3. *Encoder and Decoder is enabled only in Single-Rail mode.*

4.3 TRANSMIT PULSE SHAPER:

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meet the industry standard mask template requirements for STS-1 and DS3. See Figure 8 and Figure 9.

For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. This is illustrated in Figure 7.

The Pulse Shaper Block also consists of a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV input pin “High” or “Low” (in Hardware Mode) or setting the TxLEV bit to “1” or “0” in the control register (in Host Mode).

For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet.

For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled.

4.3.1 Guidelines for using Transmit Build Out Circuit:

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV input pin “Low” (in Hardware Mode) or setting the TxLEV control bit to “0” (in Host Mode).

If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.3.2 Interfacing to the line:

The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 6.

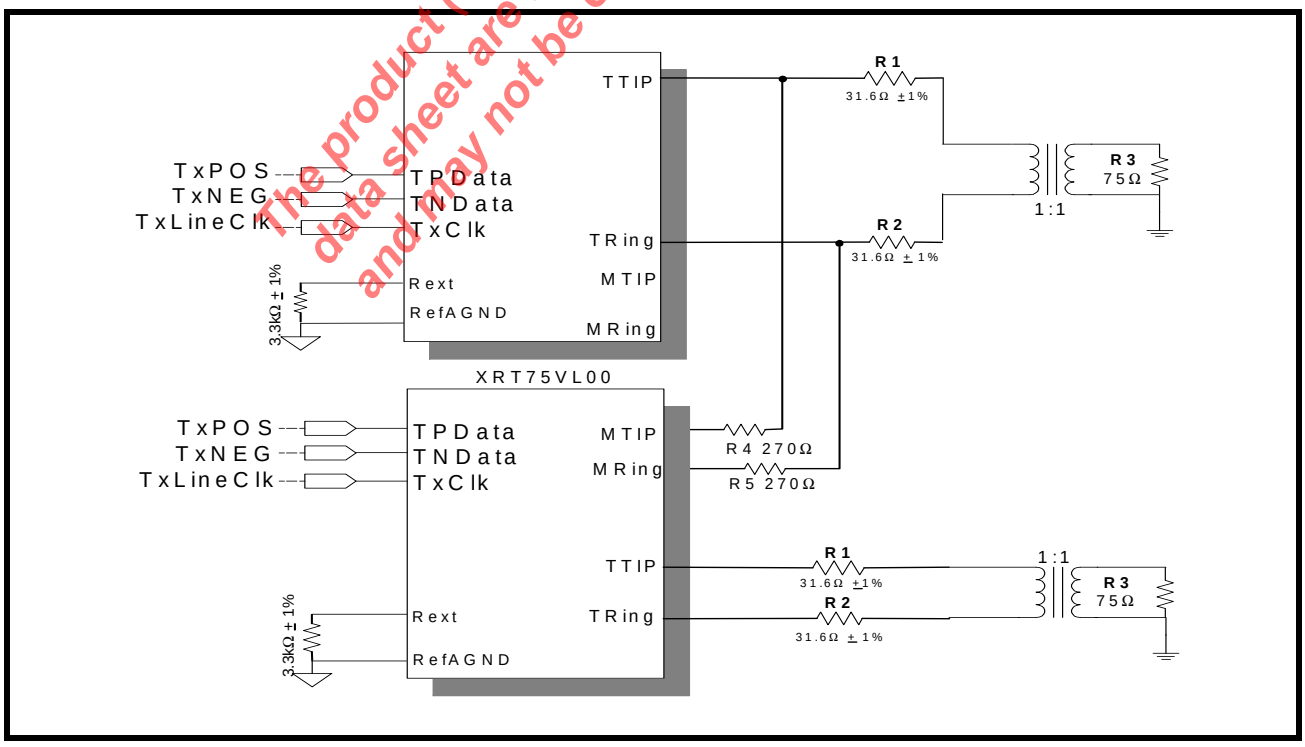
4.4 Transmit Drive Monitor:

This feature is used for monitoring the transmit line for occurrence of fault conditions such as short circuit on the line or defective line driver.The device can also be configured for internal tranmit driver monitoring.

To monitor the transmitter output of another chip, connect MTIP pin to the TTIP line via a 270 Ω resistor and MRing pins to TRing line via 270 Ω resistor as shown in Figure 16

In order to configure the device for internal transmit driver monitoring, set the TxMON bit to “1” in the transmit control register.

FIGURE 16. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP and MRing are connected to the TTIP and TRing lines, the drive monitor circuit monitors the line for transitions. The DMO (Drive Monitor Output) will be asserted “Low” as long as the transitions on the line are detected via MTIP and MRing.

If no transitions on the line are detected for 128 ± 32 TxClk periods, the DMO output toggles “High” and when the transitions are detected again, DMO toggles “Low”.

NOTE: *The Drive Monitor Circuit is only for diagnostic purposes and does not have to be used to operate the transmitter.*

4.5 Transmitter Section On/Off:

The transmitter section can be turned on or off. To turn on the transmitter in the Hardware mode, pull TxON pin “High”. In the Host mode, write a “1” to the TxON control bit AND pull the TxON pin “High” to turn on the transmitter.

When the transmitter is turned off, the TTIP and TRing are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *If the XRT75VL00D is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a “1” to the TxON control bit transfers the control to TxON pin.*

5.0 THE RECEIVER SECTION:

This section describes the detailed operation of the various blocks in the receiver. The receiver recovers the TTL/CMOS level data from the incoming bipolar B3ZS or HDB3 encoded input pulses.

5.1 AGC/Equalizer:

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB.

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce the Inter-Symbol Interference (ISI) so that, the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data.

The Equalizer can either be “IN” or “OUT” by setting the REQEN pin “High” or “Low” (in Hardware Mode) or setting the REQEN control bit to “1” or “0” (in Host Mode).

RECOMMENDATIONS FOR EQUALIZER SETTINGS:

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be left “IN” by setting the REQEN pin to “High” (in Hardware Mode) or setting the REQEN control bit to “1” (in Host Mode).

However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be left “OUT” for cable length less than 300 feet by setting the REQEN pin “Low” (in Hardware Mode) or by setting the REQEN control bit to “0” (in Host Mode).This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics.

NOTE: *The results of extensive testing indicates that even when the Equalizer was left “IN” (REQEN = “HIGH”), regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.*

The Equalizer also contain an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. This capability can be turned on by writing a “1” to the RxMON bits in the control register or by setting the RxMON pin (pin 27) “High”.

5.1.1 Interference Tolerance:

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error-free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same

recommendation is being used. Figure 17 shows the configuration to test the interference margin for DS3/ STS1. Figure 18 shows the set up for E3.

FIGURE 17. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

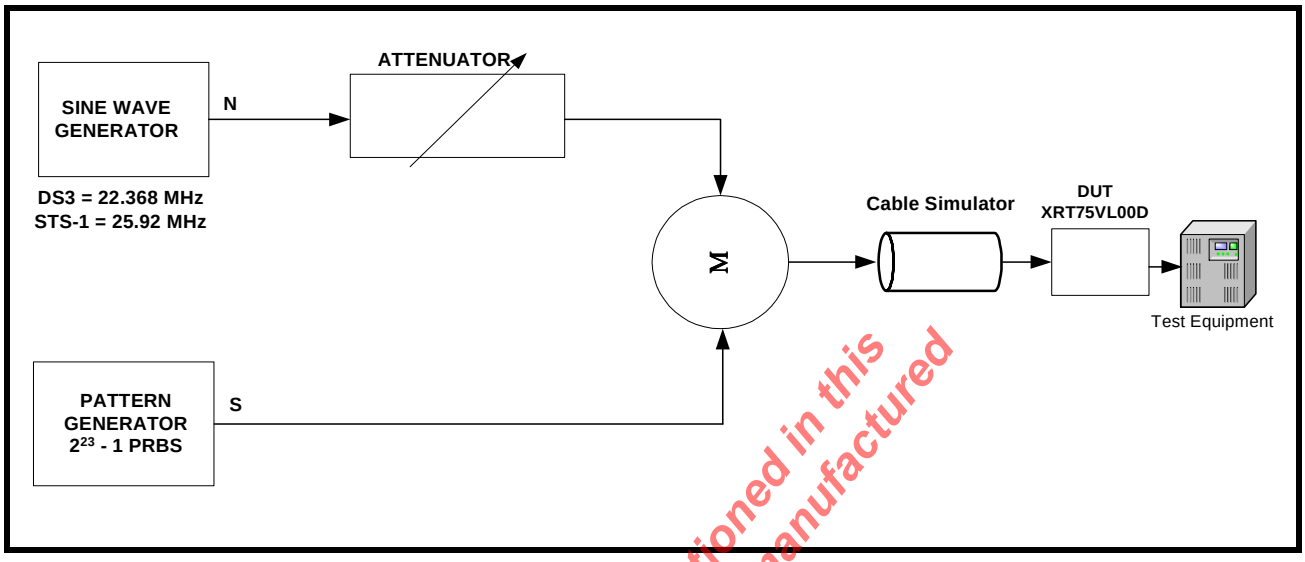


FIGURE 18. INTERFERENCE MARGIN TEST SET UP FOR E3.

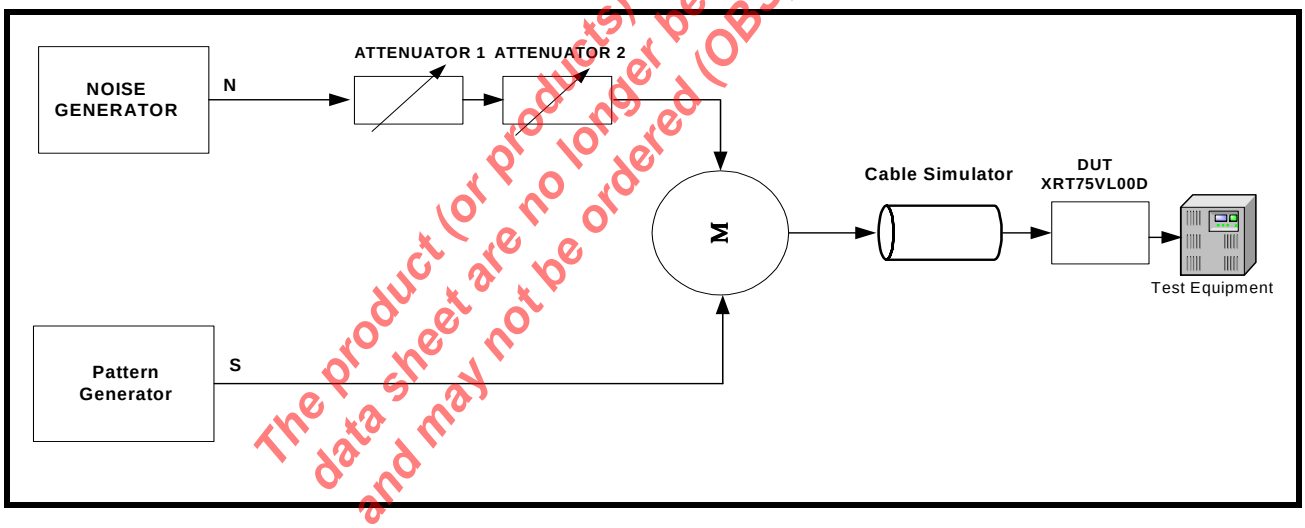


TABLE 9: INTERFERENCE MARGIN TEST RESULTS

MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	-14 dB
	12 dB	-18 dB
DS3	0 feet	-17 dB
	225 feet	-16 dB
	450 feet	-16 dB
STS-1	0 feet	-16 dB
	225 feet	-15 dB
	450 feet	-15 dB

5.2 Clock and Data Recovery:

The Clock and Data Recovery Circuit extracts the embedded clock, from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder.

The Clock Recovery PLL can be in one of the following two modes:

TRAINING MODE:

In the absence of input signals at RTIP and RRing pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk input pin exceed 0.5%, the clock recovery unit enters into Training Mode and a Loss of Lock condition is declared by toggling RLOL output pin “High” (in Hardware Mode) or setting the RLOL bit to “1” in the control registers (in Host Mode). Also, the clock output on the RxClk pin is the same as the reference clock applied on ExClk pin.

DATA/CLOCK RECOVERY MODE:

In the presence of input line signals on the RTIP and RRing input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk out pin is the Recovered Clock signal.

5.3 B3ZS/HDB3 Decoder:

The decoder block takes the output from clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream.

Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV output pins to indicate line code violation.

NOTE: *In Single- Rail (NRZ) mode, the decoder is bypassed.*

5.4 LOS (Loss of Signal) Detector:

5.4.1 DS3/STS-1 LOS Condition:

A Digital Loss of Signal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses.

Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 10.The status of the ALOS condition is reflected in the ALOS status control register.

RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS output pin is toggled “High” and the RLOS bit is set to “1” in the status control register.

TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
DS3	1	≤20mV	≥90mV
STS-1	1	≤25mV	≥115mV

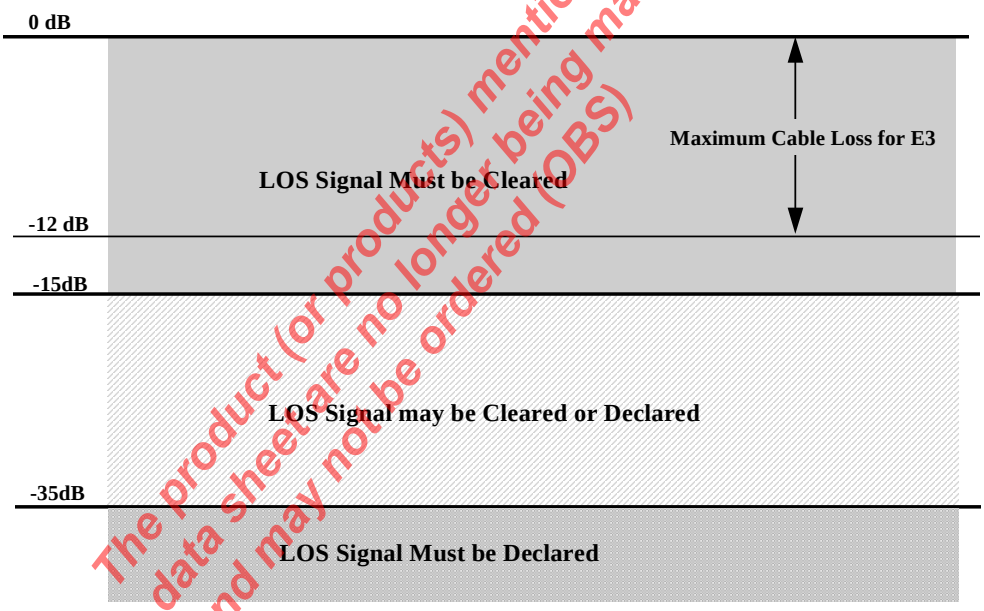
DISABLING ALOS/DLOS DETECTOR:

For debugging purposes it is useful to disable the ALOS/DLOS detector. Writing a "1" to the ALOS and DLOS bits disables the LOS detector on a per channel basis.

5.4.2 E3 LOS Condition:

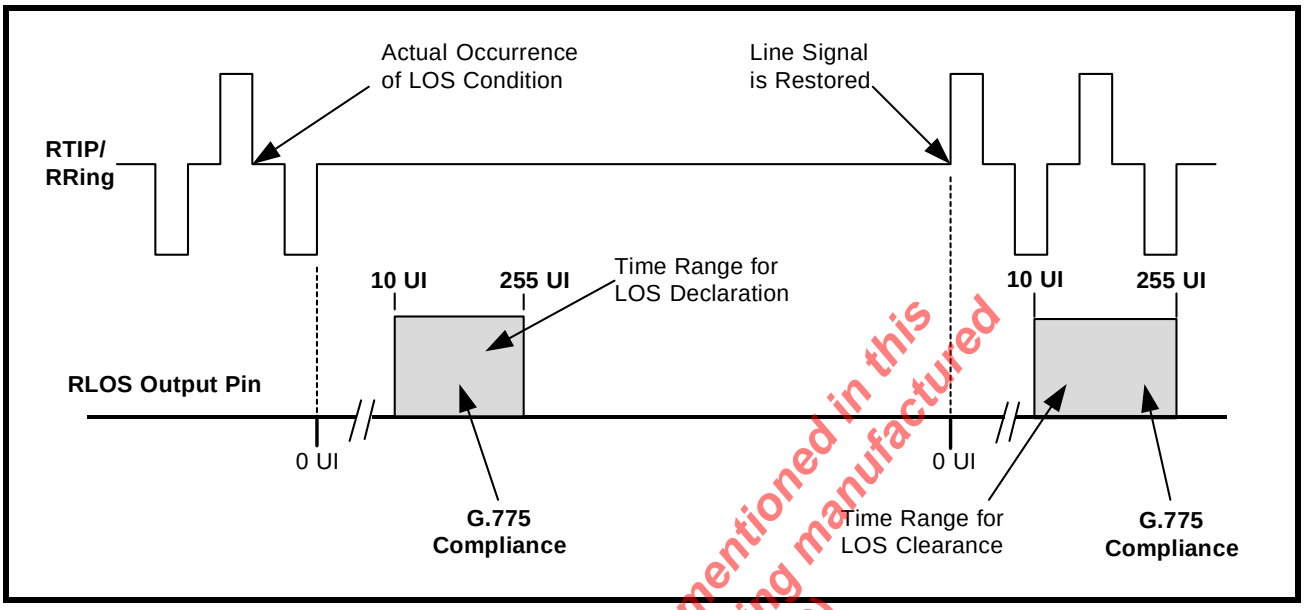
If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal level is defined to be between 15 and 35 dB below the normal level. If the signal drops below 35 dB for 175 ± 75 consecutive pulse periods, LOS condition is declared. This is illustrated in Figure 19.

FIGURE 19. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775



As defined in ITU-T G.775, an LOS condition is also declared between 10 and 255 UI (or E3 bit periods) after the actual time the LOS condition has occurred. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 20 shows the LOS declaration and clearance conditions.

FIGURE 20. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



5.4.3 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the ExClk pin and output this clock on the RxClk output. The data on the RPOS and RNEG pins can be forced to zero by pulling the LOSMUT pin “High” (in Hardware Mode) or by setting the LOSMUT bits in the individual channel control register to “1” (in Host Mode).

NOTE: *When the LOS condition is cleared, the recovered data is output on RPOS and RNEG pins.*

6.0 JITTER:

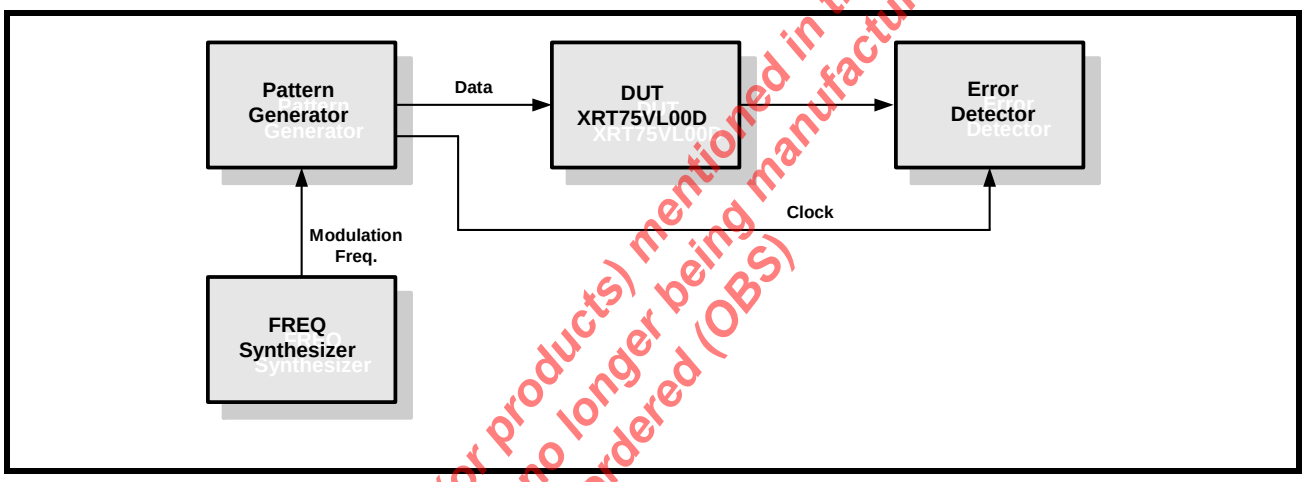
There are three fundamental parameters that describe circuit performance relative to jitter:

- **Jitter Tolerance (Receiver)**
- **Jitter Transfer (Receiver/Transmitter)**
- **Jitter Generation**

6.1 JITTER TOLERANCE - RECEIVER:

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 21, jitter is introduced by the sinusoidal modulation of the serial data bit sequence.

FIGURE 21. JITTER TOLERANCE MEASUREMENTS

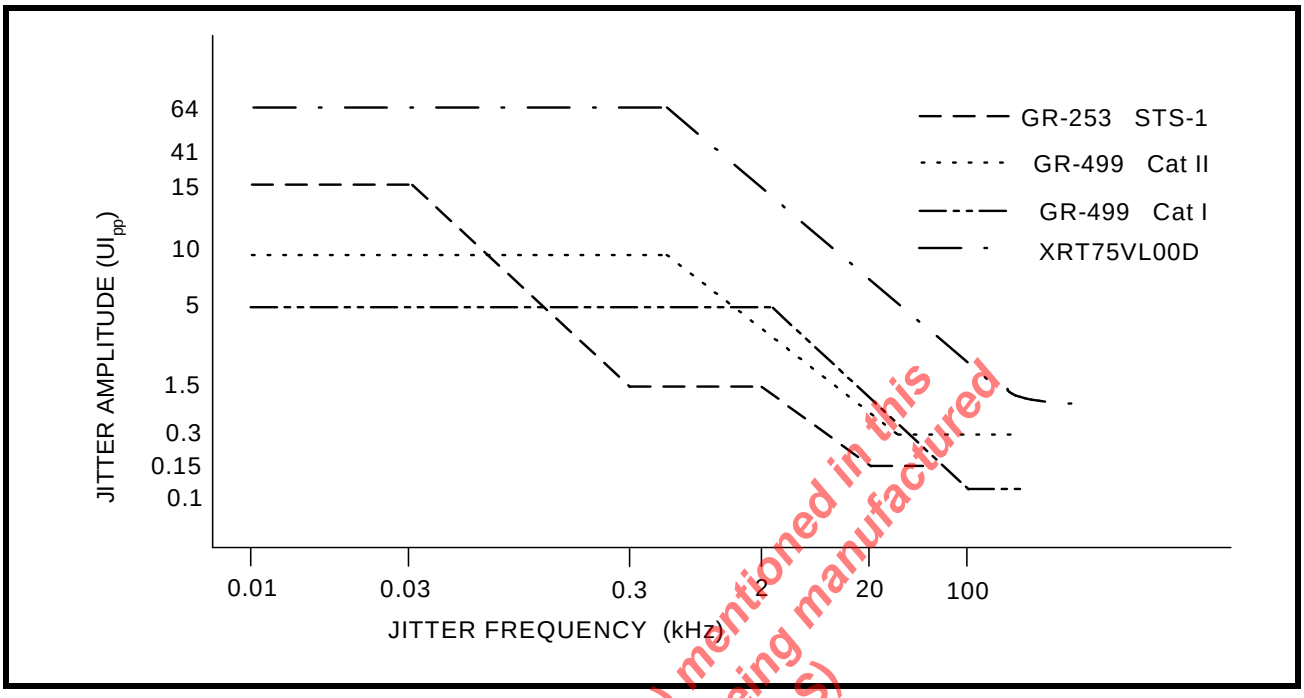


Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points.Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

6.1.1 DS3/STS-1 Jitter Tolerance Requirements:

Bellcore GR-499 CORE, Issue 1, December 1995 specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 22 shows the jitter tolerance curve as per GR-499 specification along with the measured performance for the device.

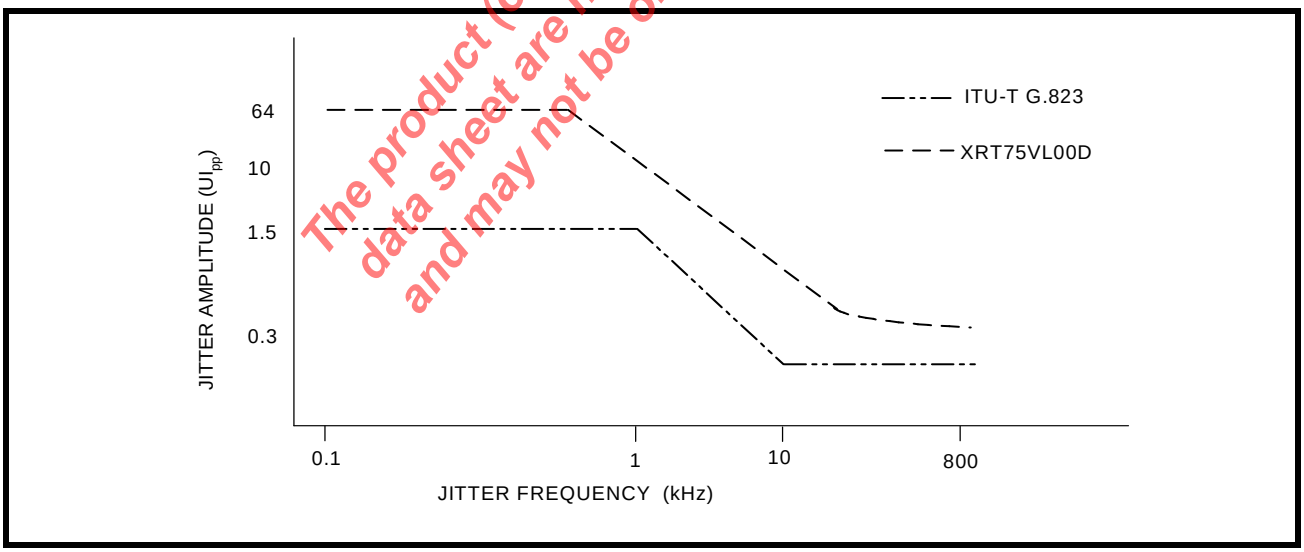
FIGURE 22. INPUT JITTER TOLERANCE FOR DS3/STS-1



6.1.2 E3 Jitter Tolerance Requirements:

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to accommodate and tolerate jitter up to certain specified limits. Figure 23 shows the tolerance curve and the actual measured data for the device.

FIGURE 23. INPUT JITTER TOLERANCE FOR E3



The Figure 11 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI P-P)			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

6.2 JITTER TRANSFER - RECEIVER/TRANSMITTER:

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency.

There are two distinct characteristics in jitter transfer: jitter gain (jitter peaking) defined as the highest ratio above 0 dB; and jitter transfer bandwidth.The overall jitter transfer bandwidth is controller by a low bandwidth loop,which is part of the XRT75VL00D.

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter.A zero dB jitter transfer indicates the element had no effect on jitter.

Table 12 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 12: JITTER TRANSFER SPECIFICATIONS

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

The XRT75VL00D meets the above Jitter Specifications.

6.3 JITTER GENERATION:

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.4 Jitter Attenuator:

An advanced crystal-less jitter attenuator is included in the XRT75VL00D. The jitter attenuator uses the internal reference clock.

In Host mode, by clearing or setting the JATx/$\overline{Rx}$ bit in the control register selects the jitter attenuator either in the Receive or Transmit path. In Hardware mode, JATx/$\overline{Rx}$ pin selects the jitter attenuator in Receive or Transmit path.

The FIFO is either a 16-bit, 32-bit or 128-bit register. In Host mode, the bits JA0 and JA1can be set to appropriate combination to select the different FIFO sizes or to disable the jitter attenuator. In Hardware mode, appropriate setting of the pins JA0 and JA1 selects the different FIFO sizes or disable the jitter attenuator. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the

dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter.*

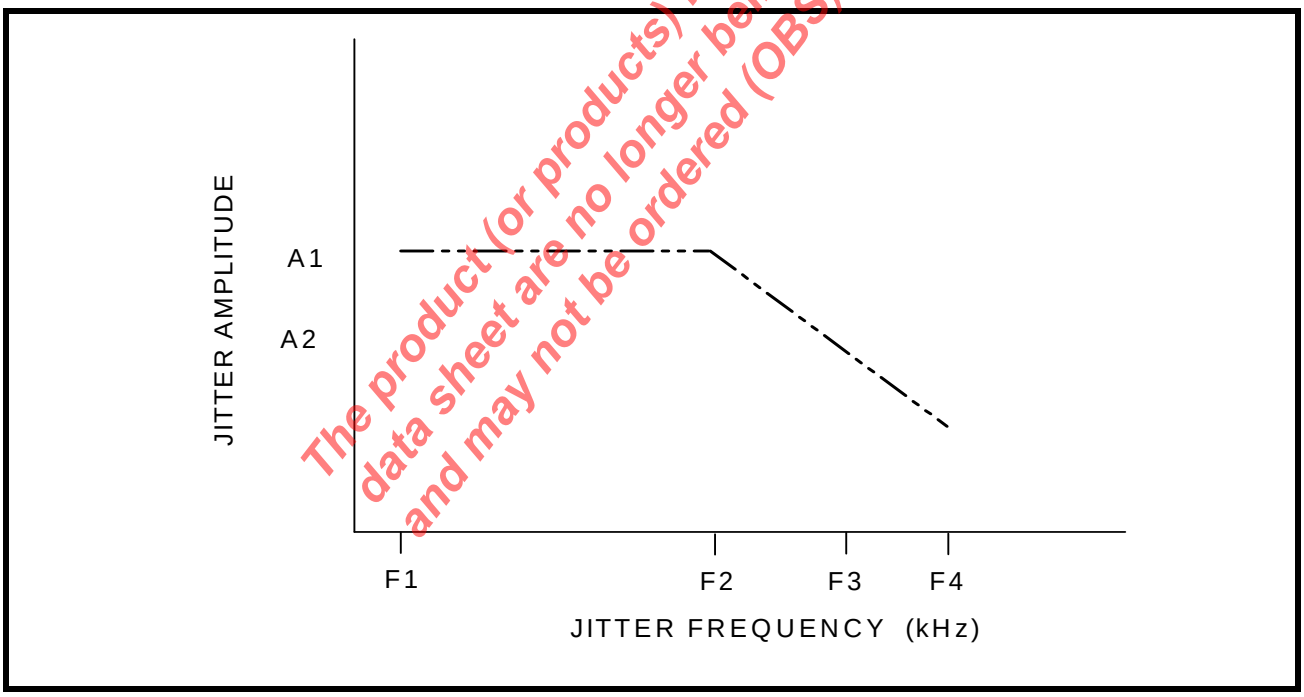
Table 13 specifies the jitter transfer mask requirements for various data rates:

TABLE 13: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75VL00D meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 24.

FIGURE 24. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



7.0 SERIAL HOST INTERFACE:

A flexible serial microprocessor interface is incorporated in the XRT75VL00D. The interface is generic and is designed to support the common microprocessors/microcontrollers. The XRT75VL00D operates in Host mode when the HOST/$\overline{HW}$ pin is tied “High”. The serial interface includes a serial clock (SClk), serial data input (SDI), serial data output (SDO), chip select (CS) and interrupt output (INT). The serial interface timing is shown in Figure 11.

The active low interrupt output signal ($\overline{INT}$ pin) indicates alarm conditions like LOS, DMO and FL to the processor.

When the XRT75VL00D is configured in Host mode, the following input pins,TxLEV, TAOS, RLB, LLB, E3, STS-1/DS3, REQEN, JATx/Rx, JA0 and JA1 are disabled and must be connected to ground.

Table 14 below illustrates the functions of the shared pins in either Host mode or in Hardware mode.

TABLE 14: FUNCTIONS OF SHARED PINS

PIN NUMBER	IN HOST MODE	IN HARDWARE MODE
24	$\overline{CS}$	RxClkINV
26	SClk	TxClkINV
25	SDI	RxON
27	SDO	RxMON
28	$\overline{INT}$	LOSMUT

NOTE: *While configured in Host mode, the TxON input pin will be active if the TxON bit in the control register is set to "1", and can be used to turn on and off the transmit output drivers. This permits a system designed for redundancy to quickly switch out a defective line card and switch-in the backup line card.*

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x00	APS/Redundancy (read/write)	Reserved	Reserved	Reserved	RxON	Reserved	Reserved	Reserved	TxON
0x01	Interrupt Enable (read/write)	Reserved		CNT_SATIE	PRBSIE	FLIE	RLOLIE	RLOSIE	DMOIE
0x02	Interrupt Status (reset on read)	Reserved		CNT_SATIS	PRBSIS	FLIS	RLOLIS	RLOSIS	DMOIS
0x03	Alarm Status (read only)	Reserved	PRBSLS	DLOS	ALOS	FL	RLOL	RLOS	DMO
0x04	Transmit Control (read/write)	Reserved		TxMON	INSPRBS	Reserved	TAOS	TxClkINV	TxLEV
0x05	Receive Control (read/write)	Reserved		DLOSDIS	ALOSDIS	RxClkINV	LOSMUT	RxMON	REQEN
0x06	Block Control (read/write)	Reserved		PRBSEN	RLB	LLB	E3	STS1/$\overline{DS3}$	SR/$\overline{DR}$
0x07	Jitter Attenuator (read/write)	Reserved			DFLCK	PNTRST	JA1	JATx/$\overline{Rx}$	JA0
0x08-0x1F	Reserved								
0x20	Interrupt Enable-Global (read/write)	Reserved					Reserved	Reserved	INTEN
0x21	Interrupt Status (read only)	Reserved					Reserved	Reserved	INTST

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x22-0x2F	Reserved	Reserved							
0x30	PRBS Error Count (MSB)	MSB							LSB
0x31	PRBS Error Count (LSB)	MSB							LSB
0x32-0x37	Reserved								
0x38	PRBS Holding	MSB							LSB
0x39-0x3D	Reserved								
0x3E	Chip_id (read only)	Device part number (7:0)							
0x3F	Chip_version (read only)	Chip revision number (7:0)							

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x00	R/W	D0	RxON	Bit 4 = RxON, Receiver Turn On. Writing a “1” to the bit field turns on the Receiver and a “0” turn off the Receiver.	0
		D4	TxON	Bit 0 = TxON, Transmitter Turn On. Writing a “1” to the bit field turn on the Transmitter. Writing a “0” turns off the transmitter and tri-state the transmitter output (TTIP/TRing).	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x01	R/W	D0	DMOIE	Writing a "1" to this bit field enables the DMO interrupt and triggers an interrupt when the transmitter driver fails. Writing a "0" disables the interrupt.	0
		D1	RLOSIE	Writing a "1" to this bit field enables the RLOS interrupt and triggers an interrupt when the RLOS condition occurs. Writing a "0" disables the interrupt.	0
		D2	RLOLIE	Writing a "1" to this bit field enables the RLOL interrupt and triggers an interrupt when RLOL condition occurs. Writing a "0" disables the interrupt.	0
		D3	FLIE	Writing a "1" to this bit field enables the FL interrupt and triggers an interrupt when the FIFO Limit of the Jitter Attenuator is within 2 bits of overflow/underflow condition. Writing a "0" disables the interrupt. ***NOTE:*** *This bit field is ignored when the Jitter Attenuator is disabled.*	0
		D4	PRBSIE	Writing a "1" to this bit enables the PRBS bit error interrupt.	0
		D5	CNT_SATIE	Writing a "1" to this bit enables the PRBS error-counter saturation interrupt. When the PRBS error counter reaches 0xFFFF, an interrupt will be generated.	0
0x02	Reset Upon Read	D0	DMOIS	This bit is set to "1" every time a DMO status change has occurred since the last cleared interrupt.This bit is cleared when read.	0
		D1	RLOSIS	This bit is set to "1" every time a RLOS status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D2	RLOLIS	This bit is set to "1" every time a RLOL status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D3	FLIS	This bit is set to "1" every time a FIFO Limit status change has occurred since the last cleared interrupt. This bit is cleared when read.	0
		D4	PRBSIS	This bit is set to "1" when a PRBS bit error is detected. This bit is cleared when read.	0
		D5	CNT_SATIS	This bit is set to "1" when the PRBS error counter has saturated (0xFFFF). This bit is cleared when read.	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x03	Read Only	D0	DMO	This bit is set to “1” every time the MTIP/MRing input pins have not detected any bipolar pulses for 128 consecutive bit periods.	0
		D1	RLOS	This bit is set to “1” every time the receiver declares an LOS condition.	0
		D2	RLOL	This bit is set to “1” every time when the receiver declares a Loss of Lock condition.	0
		D3	FL	This bit is set to “1” every time the FIFO in the Jitter Attenuator is within 2 bit of underflow/overflow condition.	0
		D4	ALOS	This bit is set to “1” every time the receiver declares Analog LOS condition.	0
		D5	DLOS	This bit is set to “1” every time the receiver declares Digital LOS condition.	0
		D6	PRBSLS	This bit is set to “1” every time the PRBS detects a bit error.	0
0x04	R/W	D0	TxLEV	Writing a “1” to this bit disables the Transmit Build-out circuit and writing a “0” enables the Transmit Build-out circuit. ***NOTE:*** *See section 4.03 for detailed description.*	0
		D1	TxClkINV	Writing a “1” to this bit configures the transmitter to sample the data on TPData/TNData input pins on the rising edge of TxClk.	0
		D2	TAOS	Setting this bit to “1” causes a continuous stream of marks to be sent out at the TTIP and TRing pins.	0
		D3	Reserved	This Bit Location is Not Used.	
		D4	INSPRBS	Writing a “1” to this bit causes the PRBS generator to insert a single-bit error onto the transmit PRBS data stream. ***NOTE:*** *PRBS Generator/Detector must be enabled for this bit to have any effect.*	0
		D5	TxMON	When this bit is set to “1”, the driver monitor is connected to its own transmit channel and monitors the transmit driver. When a transmit failure is detected, the DMO output will go high. When this bit is “0”, MTIP and MRing can be connected to other transmit channel for monitoring.	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x05	R/W	D0	REQEN	Setting this bit to "1" enables the Receive Equalizer . ***NOTE:*** *See section 2.01 for detailed description.*	0
		D1	RxMON	Writing a "1" to this bit configures the Receiver into monitoring mode. In this mode, the Receiver can monitor a signal at the RTIP/RRing pins that be attenuated up to 20dB flat loss.	0
		D2	LOSMUT	Writing a "1" to this bit causes the RPOS/RNEG outputs to be grounded while the LOS condition is declared. ***NOTE:*** *If this bit has ben set, it will remain set evan after LOS condition is cleared.*	0
		D3	RxClkINV	Writing a "1" to this bit configures the Receiver to output RPOS/RNEG data on the falling edge of RxClk.	0
		D4	ALOSDIS	Writing a "1" to this bit disables the ALOS detector.	0
		D5	DLOSDIS	Writing a "1" to this bit disables the DLOS detector.	0
0x06	R/W	D0	SR/$\overline{DR}$	Writing a "1" to this bit configures the Receiver and Transmitter into Single-Rail (NRZ) mode.	0
		D1	STS-1/$\overline{DS3}$	Writing a "1" to this bit configures the channel 0 into STS-1 mode. ***NOTE:*** *This bit field is ignored if the chip is configured to operate in E3 mode.*	0
		D2	E3	Writing a "1" to this bit configures the chip in E3 mode.	0
		D3	LLB	Writing a "1" to this bit configures the chip in Local Loopback mode.	0
		D4	RLB	Writing a "1" to this bit configures the chip in Remote Loopback mode. **RLB / LLB / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital**	0
		D5	PRBSEN	Writing a "1" to this bit enables the PRBS generator/detector.PRBS generator generate and detect either 2^{15}-1 (DS3 or STS-1) or 2^{23}-1 (for E3). The pattern generated and detected are unframed pattern.	0

TABLE 16: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x07	R/W	D0	JA0	This bit along with JA1 bit configures the Jitter Attenuator as shown in the table below. JA0 / JA1 / Mode 0 / 0 / 16 bit FIFO 0 / 1 / 32 bit FIFO 1 / 0 / 128 bit FIFO 1 / 1 / Disable Jitter Attenuator	0
		D1	JATx/$\overline{Rx}$	Writing a “1” to this bit selects the Jitter Attenuator in the Transmit Path. A “0” selects in the Receive Path.	0
		D2	JA1	This bit along with the JA0 configures the Jitter Attenuator as shown in the table.	0
		D3	PNTRST	Setting this bit to “1” resets the Read and Write pointers of the jitter attenuator FIFO.	0
		D4	DFLCK	Set this bit to "1" to disable the SONET APS Recovery Time of the PLL. When this bit is "0", the APS Recovery Time is enabled. This helps to reduce the time for the PLL to lock to the incoming frequency when the Jitter Attenuator switches to narrow band. This is required for SONET to DS-3 Mapping/Demapping De-Synchronization applications.	0
0x08	Reserved				

TABLE 17: REGISTER MAP DESCRIPTION - GLOBAL

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x20	R/W	D0	INTEN	Bit 0 = INTEN Writing a “1” to this bit enables the interrupts.	0
0x21	Read Only	D0	INTST	Bit 0 = INTST bit is set to “1” if an interrupt service is required. The source level interrupt status register is read to determine the cause of interrupt.	0
0x22 - 0x2F	Reserved				
0x30	Reset Upon Read	D[7:0]	PRBSmsb	PRBS error counter MSB [15:8]	

ADDRESS (HEX)	TYPE	BIT LOCATION	SYMBOL	DESCRIPTION	DEFAULT VALUE(BIN)
0x31	Reset Upon Read	D[7:0]	PRBSlsb	PRBS error counter LSB [7:0]	
0x32-0x37	Reserved				
0x38	Read Only	D[7:0]	PRBShold	PRBS Holding Register	
0x39-0x3D	Reserved				
0x3E	Read Only	D[7:0]	Chip_id	This read only register contains device id.	01010001
0x3F	Read Only	D[7:0]	Chip_version	This read only register contains chip version number	00000001

8.0 DIAGNOSTIC FEATURES:

8.1 PRBS Generator and Detector:

The XRT75VL00D contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. This feature is only available in Host mode. With the PRBSEN bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for half RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

When PRBS mode is enabled, the PRBS counter starts counting each single bit error. The PRBS counter is 16 bits wide. The current value in the counter can be read via two readback operations of the Serial I/O registers.

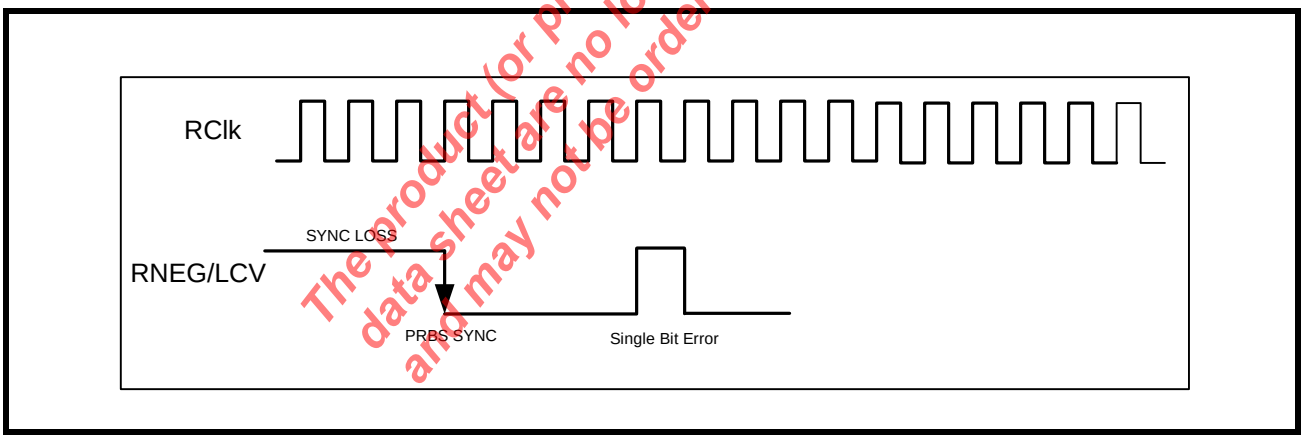
1) Either the Least Significant Byte (LSB, address 0x30) or the Most Significant Byte (MSB, address 0x31) can be read first. The value of the un-read register will be copied into the Holding register (address 0x38) and both the LSB and MSB registers will be reset to zero.

2) Read the Holding register and concatenate the result with the value from the first read operation to get the full 16 bit counter value.

When the PRBS mode is first enabled, errors will be counted while the receiver logic is synchronizing to the PRBS pattern. When RNEG/LCV goes "Low" indicating PRBS synchronization, reset the counter by reading either the LSB or the MSB register.

Figure 25 shows the status of RNEG/LCV pin when the XRT75VL00D is configured in PRBS mode.

FIGURE 25. PRBS MODE



8.2 LOOPBACKS:

The XRT75VL00D offers three loopback modes for diagnostic purposes. In Hardware mode, the loopback modes are selected via the RLB and LLB pins. In Host mode, the RLB and LLB bits in the control registers select the loopback modes.

8.2.1 ANALOG LOOPBACK:

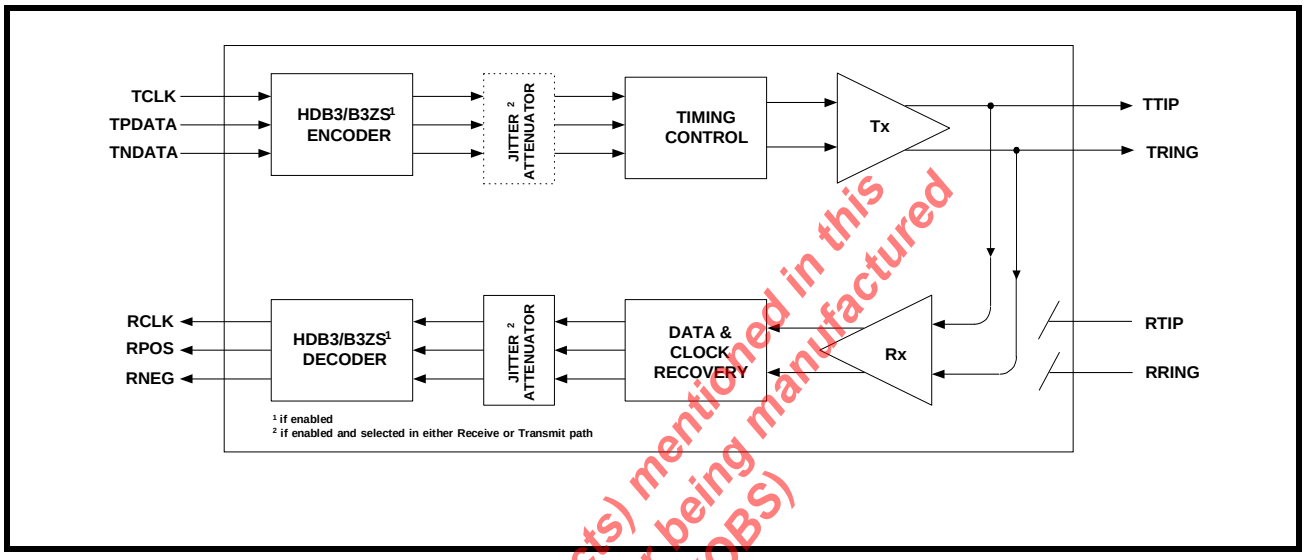
In this mode, the transmitter outputs (TTIP and TRING) are connected internally to the receiver inputs (RTIP and RRING) as shown in Figure 26. Data and clock are output at RCLK, RPOS and RNEG pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

XRT75VL00D can be configured in Analog Loopback either in Hardware mode via the LLB and RLB pins or in Host mode via LLB and RLB bits in the channel control registers.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP and TRING pins.*
2. *Signals on the RTIP and RRING pins are ignored during analog loopback.*

FIGURE 26. ANALOG LOOPBACK

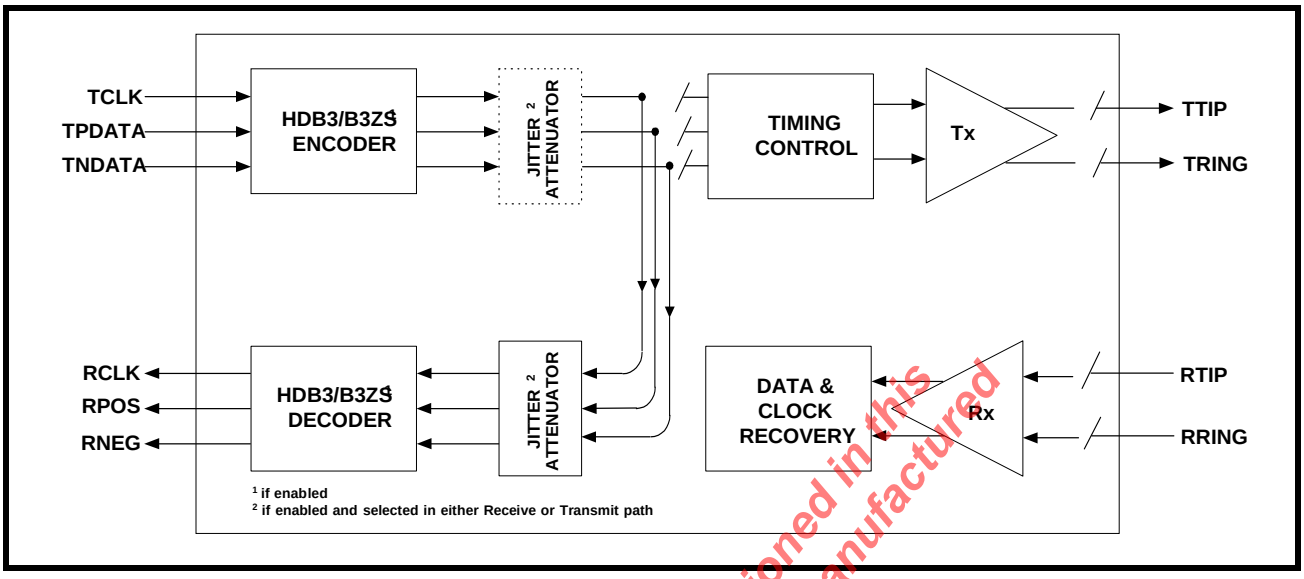


8.2.2 DIGITAL LOOPBACK:

The Digital Loopback function is available either in Hardware mode or Host mode. When the Digital Loopback is selected, the transmit clock (TxClk) and transmit data inputs (TPDATA & TNDATA) are looped back and output onto the RxClk, RPOS and RNEG pins as shown in Figure 27. The data presented on TxClk, TPDATA and TNDATA are not output on the TTIP and TRING pins.This provides the capability to configure the protection card (in redundancy applications) in Digital Loopback mode without affecting the traffic on the primary card.

NOTE: *Signals on the RTIP and RRING pins are ignored during digital loopback.*

FIGURE 27. DIGITAL LOOPBACK



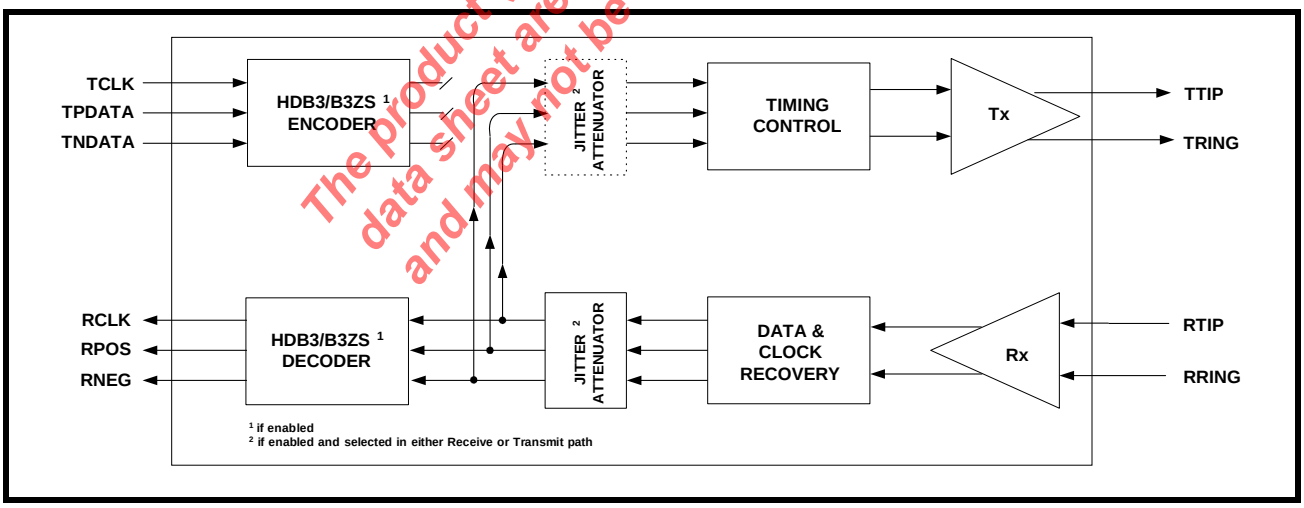
8.2.3 REMOTE LOOPBACK:

With Remote loopback activated as shown in Figure 28,the receive data on RTIP and RRING is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RPOS and RNEG pins.

During the remote loopback mode, if the jitter attenuator is selected in the transmit path, the receive data after the Clock and Data Recovery Block is looped back to the transmit path and pass through the jitter attenuator using RxClk as the transmit timing.

NOTE: Input signals on TxClk, TPDATA and TNDATA are ignored during Remote loopback.

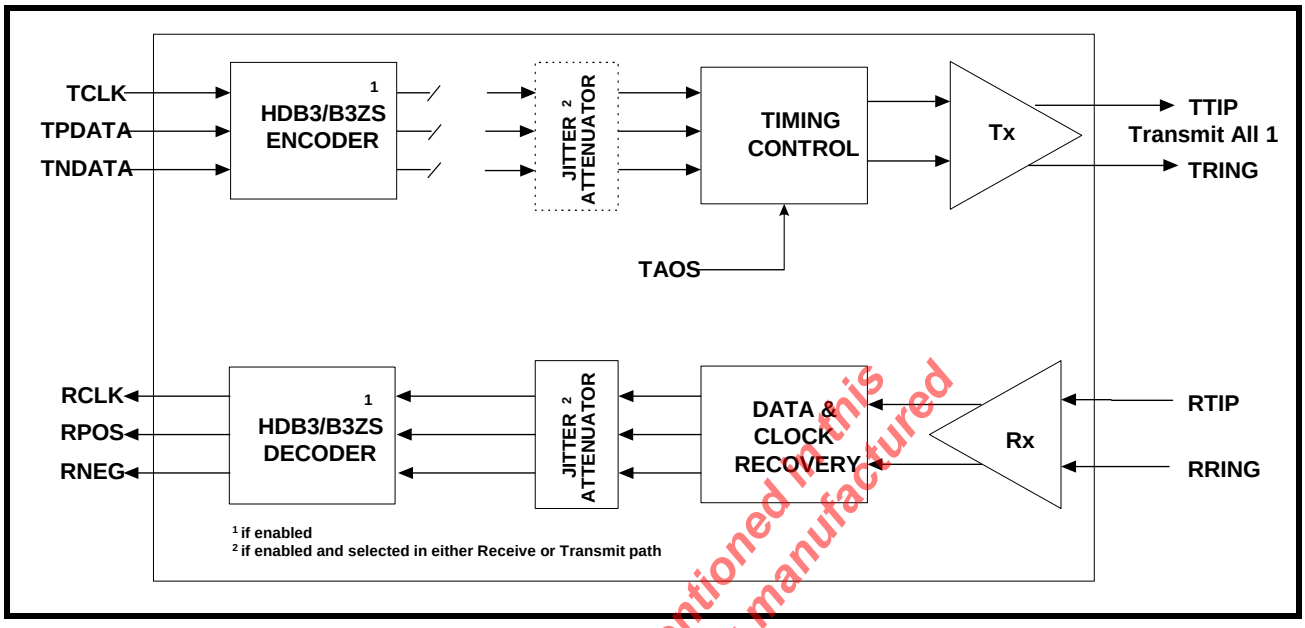
FIGURE 28. REMOTE LOOPBACK



8.3 TRANSMIT ALL ONES (TAOS):

Transmit All Ones (TAOS) can be set either in Hardware mode by pulling the TAOS pins “High” or in Host mode by setting the TAOS control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP and TRING pins. The frequency of this “1’s” pattern is determined by TClk.TAOS data path is shown in Figure 29.

FIGURE 29. TRANSMIT ALL ONES (TAOS)



9.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE LIU

The LIU with D-SYNC is very similar to the non D-SYNC LIU in that they both contain Jitter Attenuator blocks within each channel. They are also pin to pin compatible with each other. However, the Jitter Attenuators within the D-SYNC have some enhancements over and above those within the non D-SYNC device. The Jitter Attenuator blocks will support all of the modes and features that exist in the non D-SYNC device and in addition they also support a SONET/SDH De-Sync Mode.

NOTE: *The "D" suffix within the part number stands for "De-Sync".*

The SONET/SDH De-Sync feature of the Jitter Attenuator blocks permits the user to design a SONET/SDH PTE (Path Terminating Equipment) that will comply with all of the following Intrinsic Jitter and Wander requirements.

- **For SONET Applications**
  - Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 Applications)
  - ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement
- **For SDH Applications**
  - Jitter and Wander Generation Requirements per ITU-T G.783 (for DS3 and E3 Applications)

Specifically, if the user designs in the LIU along with a SONET/SDH Mapper IC (which can be realized as either a standard product or as a custom logic solution, in an ASIC or FPGA), then the following can be accomplished.

- The Mapper can receive an STS-N or an STM-M signal (which is carrying asynchronously-mapped DS3 and/or E3 signals) and byte de-interleave this data into N STS-1 or 3*M VC-3 signals
- The Mapper will then terminate these STS-1 or VC-3 signals and will de-map out this DS3 or E3 data from the incoming STS-1 SPEs or VC-3s, and output this DS3 or E3 to the DS3/E3 Facility-side towards the LIU
- This DS3 or E3 signal (as it is output from these Mapper devices) will contain a large amount of intrinsic jitter and wander due to (1) the process of asynchronously mapping a DS3 or E3 signal into a SONET or SDH signal, (2) the occurrence of Pointer Adjustments within the SONET or SDH signal (transporting these DS3 or E3 signals) as it traverses the SONET/SDH network, and (3) clock gapping.
- When the LIU has been configured to operate in the "SONET/SDH De-Sync" Mode, then it will (1) accept this jittery DS3 or E3 clock and data signal from the Mapper device (via the Transmit System-side interface) and (2) through the Jitter Attenuator, the LIU will reduce the Jitter and Wander amplitude within these DS3 or E3 signals such that they (when output onto the line) will comply with the above-mentioned intrinsic jitter and wander specifications.

9.1 BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS

This section provides an in-depth discussion on the mechanisms that will cause Jitter and Wander within a DS3 or E3 signal that is being transported across a SONET or SDH Network. A lot of this material is introductory, and can be skipped by the engineer that is already experienced in SONET/SDH designs.

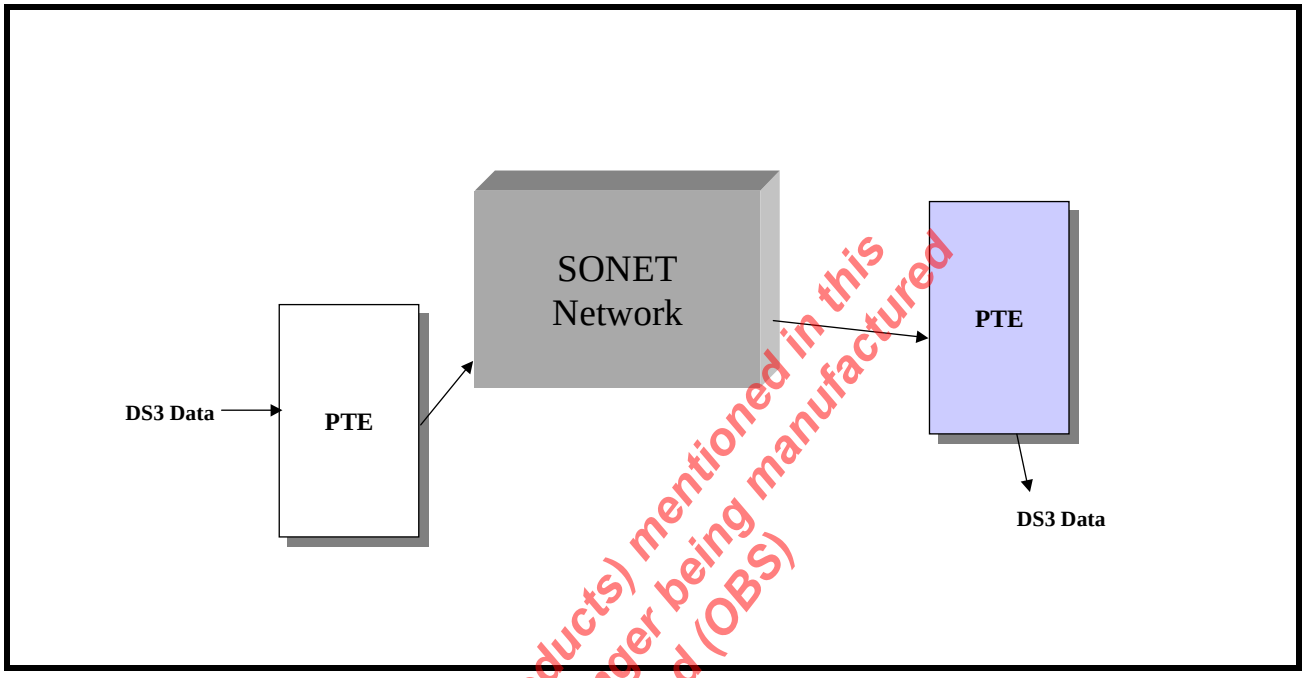
In the wide-area network (WAN) in North America it is often necessary to transport a DS3 signal over a long distance (perhaps over a thousand miles) in order to support a particular service. Now rather than realizing this transport of DS3 data, by using over a thousand miles of coaxial cable (interspaced by a large number of DS3 repeaters) a common thing to do is to route this DS3 signal to a piece of equipment (such as a Terminal MUX, which in the "SONET Community" is known as a PTE or Path Terminating Equipment). This Terminal MUX will asynchronously map the DS3 signal into a SONET signal. At this point, the SONET network will now transport this asynchronously mapped DS3 signal from one PTE to another PTE (which is located at the other end of the SONET network). Once this SONET signal arrives at the remote PTE, this DS3 signal will then be extracted from the SONET signal, and will be output to some other DS3 Terminal Equipment for further processing.

Similar things are done outside of North America. In this case, this DS3 or E3 signal is routed to a PTE, where it is asynchronously mapped into an SDH signal. This asynchronously mapped DS3 or E3 signal is then transported across the SDH network (from one PTE to the PTE at the other end of the SDH network). Once

this SDH signal arrives at the remote PTE, this DS3 or E3 signal will then be extracted from the SDH signal, and will be output to some other DS3/E3 Terminal Equipment for further processing.

Figure 30 presents an illustration of this approach to transporting DS3 data over a SONET Network

FIGURE 30. A SIMPLE ILLUSTRATION OF A DS3 SIGNAL BEING MAPPED INTO AND TRANSPORTED OVER THE SONET NETWORK



As mentioned above a DS3 or E3 signal will be asynchronously mapped into a SONET or SDH signal and then transported over the SONET or SDH network. At the remote PTE this DS3 or E3 signal will be extracted (or de-mapped) from this SONET or SDH signal, where it will then be routed to DS3 or E3 terminal equipment for further processing.

In order to insure that this "de-mapped" DS3 or E3 signal can be routed to any industry-standard DS3 or E3 terminal equipment, without any complications or adverse effect on the network, the Telcordia and ITU-T standard committees have specified some limits on both the Intrinsic Jitter and Wander that may exist within these DS3 or E3 signals as they are de-mapped from SONET/SDH. As a consequence, all PTEs that maps and de-mapped DS3/E3 signals into/from SONET/SDH must be designed such that the DS3 or E3 data that is de-mapped from SONET/SDH by these PTEs must meet these Intrinsic Jitter and Wander requirements.

As mentioned above, the LIU can assist the System Designer (of SONET/SDH PTE) by ensuring that their design will meet these Intrinsic Jitter and Wander requirements.

This section of the data sheet will present the following information to the user.

- Some background information on Mapping DS3/E3 signals into SONET/SDH and de-mapping DS3/E3 signals from SONET/SDH.
- A brief discussion on the causes of jitter and wander within a DS3 or E3 signal that mapped into a SONET/SDH signal, and is transported across the SONET/SDH Network.
- A brief review of these Intrinsic Jitter and Wander requirements in both SONET and SDH applications.
- A brief review on the Intrinsic Jitter and Wander measurement results (of a de-mapped DS3 or E3 signal) whenever the LIU device is used in a system design.
- A detailed discussion on how to design with and configure the LIU device such that the end-system will meet these Intrinsic Jitter and Wander requirements.

In a SONET system, the relevant specification requirements for Intrinsic Jitter and Wander (within a DS3 signal that is mapped into and then de-mapped from SONET) are listed below.

- Telcordia GR-253-CORE Category I Intrinsic Jitter Requirements for DS3 Applications (Section 5.6), and
- ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement

In general, there are three (3) sources of Jitter and Wander within an asynchronously-mapped DS3 signal that the system designer must be aware of. These sources are listed below.

- Mapping/De-Mapping Jitter
- Pointer Adjustments
- Clock Gapping

Each of these sources of jitter/wander will be defined and discussed in considerable detail within this Section. In order to accomplish all of this, this particular section will discuss all of the following topics in details.

- How DS3 data is mapped into SONET, and how this mapping operation contributes to Jitter and Wander within this "eventually de-mapped" DS3 signal.
- How this asynchronously-mapped DS3 data is transported throughout the SONET Network, and how occurrences on the SONET network (such as pointer adjustments) will further contributes to Jitter and Wander within the "eventually de-mapped" DS3 signal.
- A review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications
- A review of the DS3 Wander requirements per ANSI T1.105.03b-1997
- A review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application
- An in-depth discussion on how to design with and configure the LIU to permit the system to the meet the above-mentioned Intrinsic Jitter and Wander requirements

NOTE: *An in-depth discussion on SDH De-Sync Applications will be presented in the next revision of this data sheet.*

9.2 MAPPING/DE-MAPPING JITTER/WANDER

Mapping/De-Mapping Jitter (or Wander) is defined as that intrinsic jitter (or wander) that is induced into a DS3 signal by the "Asynchronous Mapping" process. This section will discuss all of the following aspects of Mapping/De-Mapping Jitter.

- How DS3 data is mapped into an STS-1 SPE
- How frequency offsets within either the DS3 signal (being mapped into SONET) or within the STS-1 signal itself contributes to intrinsic jitter/wander within the DS3 signal (being transported via the SONET network).

9.2.1 HOW DS3 DATA IS MAPPED INTO SONET

Whenever a DS3 signal is asynchronously mapped into SONET, this mapping is typically accomplished by a PTE accepting DS3 data (from some remote terminal) and then loading this data into certain bit-fields within a given STS-1 SPE (or Synchronous Payload Envelope). At this point, this DS3 signal has now been asynchronously mapped into an STS-1 signal. In most applications, the SONET Network will then take this particular STS-1 signal and will map it into "higher-speed" SONET signals (e.g., STS-3, STS-12, STS-48, etc.) and will then transport this asynchronously mapped DS3 signal across the SONET network, in this manner. As this "asynchronously-mapped" DS3 signal approaches its "destination" PTE, this STS-1 signal will eventually be de-mapped from this STS-N signal. Finally, once this STS-1 signal reaches the "destination" PTE, then this asynchronously-mapped DS3 signal will be extracted from this STS-1 signal.

9.2.1.1 A Brief Description of an STS-1 Frame

In order to be able to describe how a DS3 signal is asynchronously mapped into an STS-1 SPE, it is important to define and understand all of the following.

- The STS-1 frame structure
- The STS-1 SPE (Synchronous Payload Envelope)

- Telcordia GR-253-CORE's recommendation on mapping DS3 data into an STS-1 SPE

An STS-1 frame is a data-structure that consists of 810 bytes (or 6480 bits). A given STS-1 frame can be viewed as being a 9 row by 90 byte column array (making up the 810 bytes). The frame-repetition rate (for an STS-1 frame) is 8000 frames/second. Therefore, the bit-rate for an STS-1 signal is (6480 bits/frame * 8000 frames/sec =) 51.84Mbps.

A simple illustration of this SONET STS-1 frame is presented below in Figure 31.

FIGURE 31. A SIMPLE ILLUSTRATION OF THE SONET STS-1 FRAME

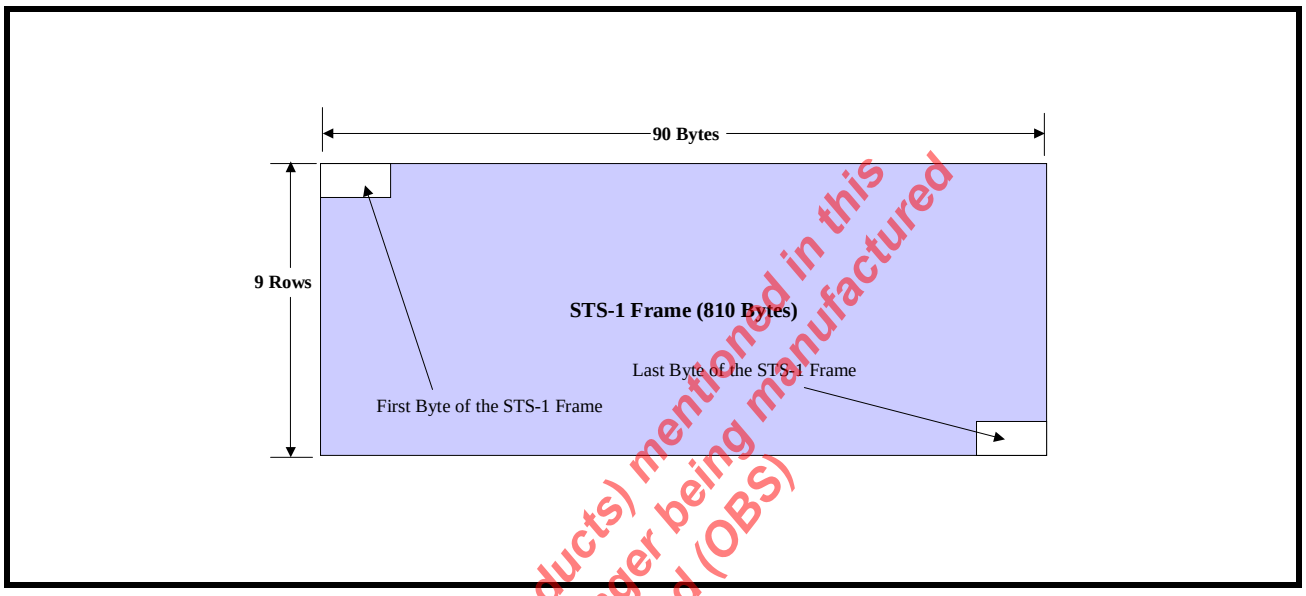


Figure 31 indicates that the very first byte of a given STS-1 frame (to be transmitted or received) is located in the extreme upper left hand corner of the 90 column by 9 row array, and that the very last byte of a given STS-1 frame is located in the extreme lower right-hand corner of the frame structure. Whenever a Network Element transmits a SONET STS-1 frame, it starts by transmitting all of the data, residing within the top row of the STS-1 frame structure (beginning with the left-most byte, and then transmitting the very next byte, to the right). After the Network Equipment has completed its transmission of the top or first row, it will then proceed to transmit the second row of data (again starting with the left-most byte, first). Once the Network Equipment has transmitted the last byte of a given STS-1 frame, it will proceed to start transmitting the very next STS-1 frame.

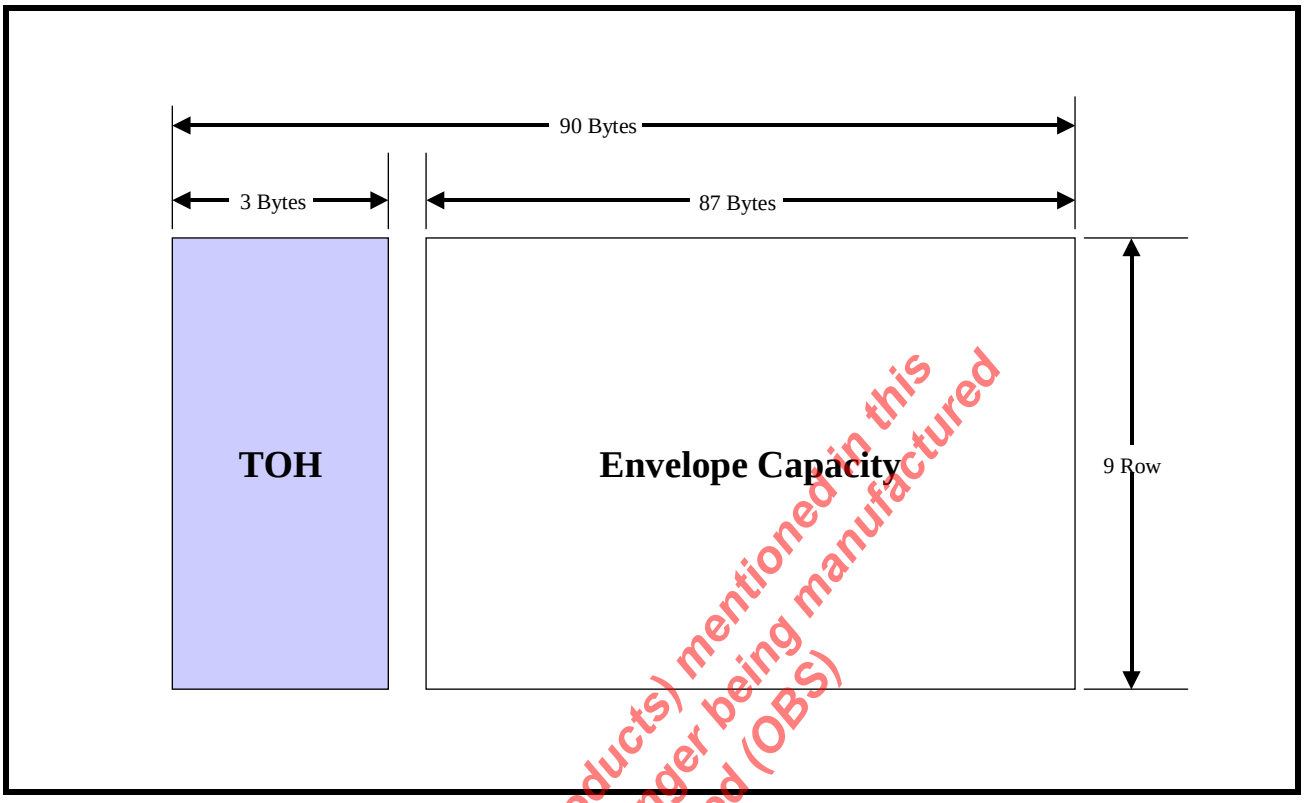
The illustration of the STS-1 frame (in Figure 31) is very simplistic, for multiple reasons. One major reason is that the STS-1 frame consists of numerous types of bytes. For the sake of discussion within this data sheet, the STS-1 frame will be described as consisting of the following types (or groups) of bytes.

- The Transport Overheads (or TOH) Bytes
- The Envelope Capacity Bytes

9.2.1.1.1 The Transport Overhead (TOH) Bytes

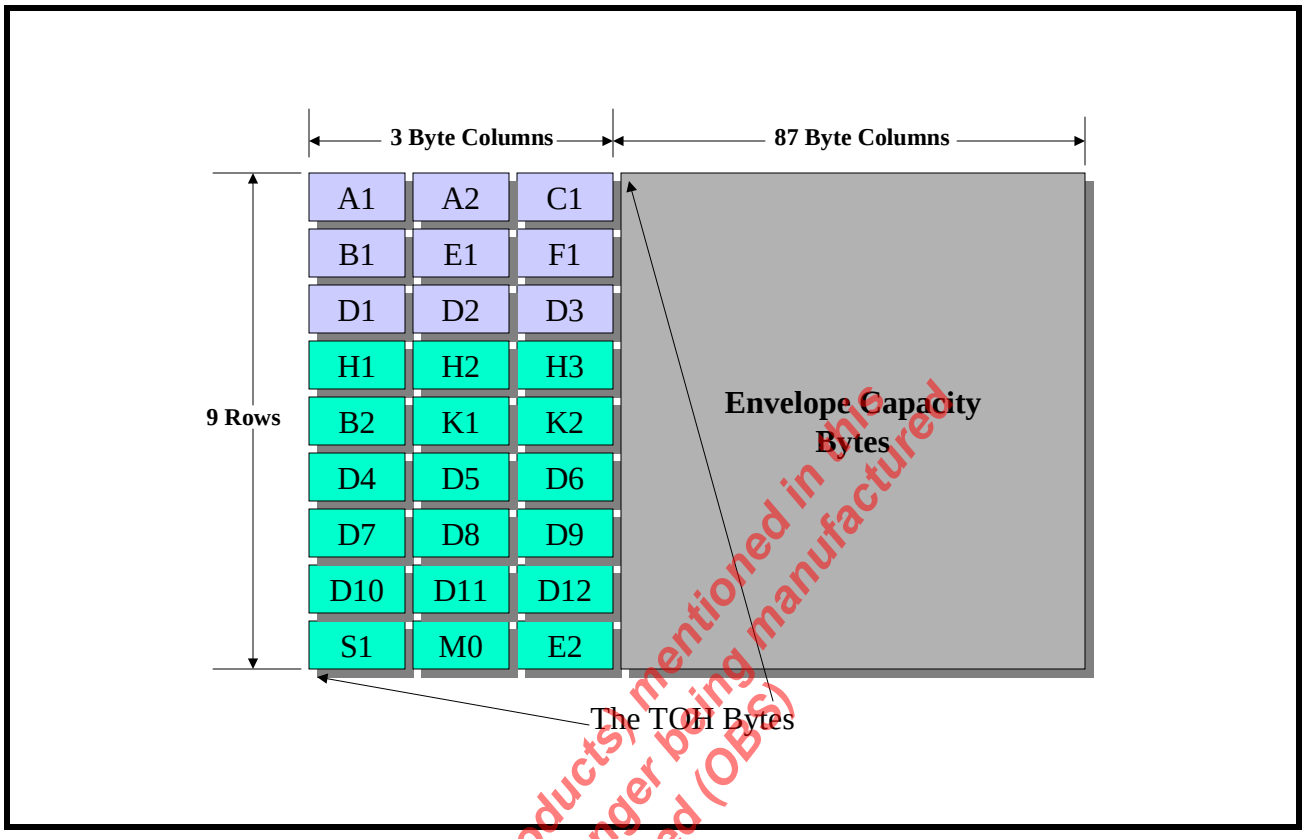
The Transport Overhead or TOH bytes occupy the very first three (3) byte columns within each STS-1 frame. Figure 32 presents another simple illustration of an STS-1 frame structure. However, in this case, both the TOH and the Envelope Capacity bytes are designated in this Figure.

FIGURE 32. A SIMPLE ILLUSTRATION OF THE STS-1 FRAME STRUCTURE WITH THE TOH AND THE ENVELOPE CAPACITY BYTES DESIGNATED



Since the TOH bytes occupy the first three byte columns of each STS-1 frame, and since each STS-1 frame consists of nine (9) rows, then we can state that the TOH (within each STS-1 frame) consists of 3 byte columns x 9 rows = 27 bytes. The byte format of the TOH is presented below in Figure 33.

FIGURE 33. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



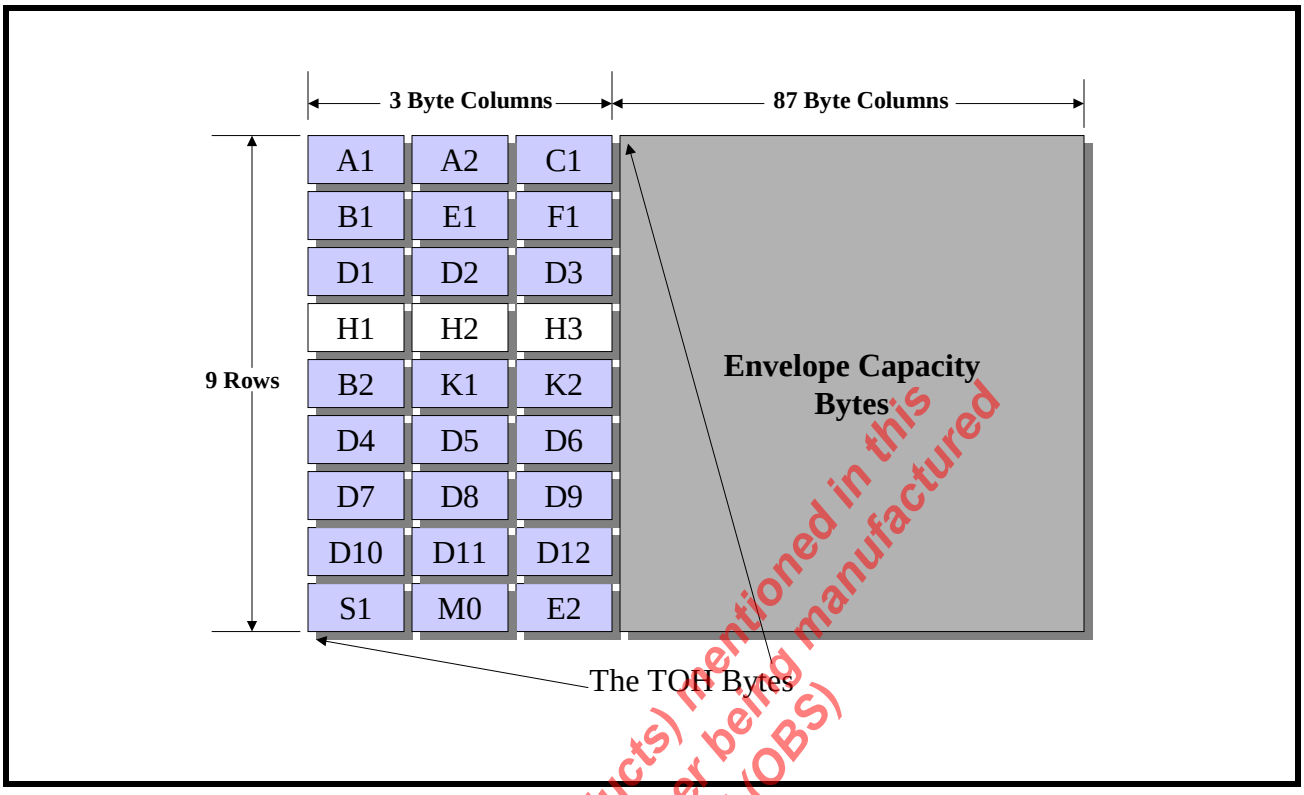
In general, the role/purpose of the TOH bytes is to fulfill the following functions.

- To support STS-1 Frame Synchronization
- To support Error Detection within the STS-1 frame
- To support the transmission of various alarm conditions such as RDI-L (Line - Remote Defect Indicator) and REI-L (Line - Remote Error Indicator)
- To support the Transmission and Reception of "Section Trace" Messages
- To support the Transmission and Reception of OAM&P Messages via the DCC Bytes (Data Communication Channel bytes - D1 through D12 byte)

The roles of most of the TOH bytes is beyond the scope of this Data Sheet and will not be discussed any further. However, there are a three TOH bytes that are important from the stand-point of this data sheet, and will discussed in considerable detail throughout this document. These are the H1 and H2 (e.g., the SPE Pointer) bytes and the H3 (e.g., the Pointer Action) byte.

Figure 34 presents an illustration of the Byte-Format of the TOH within an STS-1 Frame, with the H1, H2 and H3 bytes highlighted.

FIGURE 34. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



Although the role of the H1, H2 and H3 bytes will be discussed in much greater detail in “Section 9.3, Jitter/ Wander due to Pointer Adjustments” on page 60. For now, we will simply state that the role of these bytes is two-fold.

- To permit a given PTE (Path Terminating Equipment) that is receiving an STS-1 data to be able to locate the STS-1 SPE (Synchronous Payload Envelope) within the Envelope Capacity of this incoming STS-1 data stream and,
- To inform a given PTE whenever Pointer Adjustment and NDF (New Data Flag) events occur within the incoming STS-1 data-stream.

9.2.1.1.2 The Envelope Capacity Bytes within an STS-1 Frame

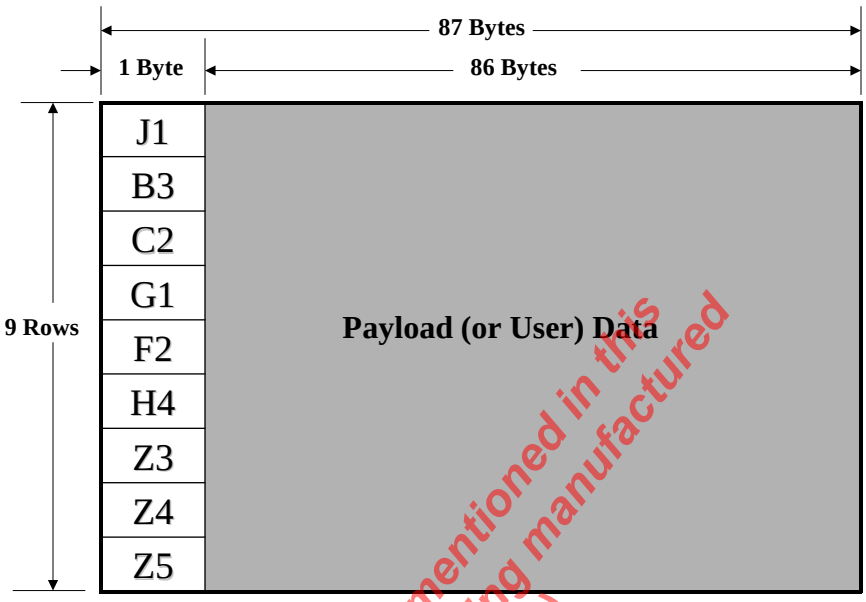
In general, the Envelope Capacity Bytes are any bytes (within an STS-1 frame) that exist outside of the TOH bytes. In short, the Envelope Capacity contains the STS-1 SPE (Synchronous Payload Envelope). In fact, every single byte that exists within the Envelope Capacity also exists within the STS-1 SPE. The only difference that exists between the "Envelope Capacity" as defined in Figure 33 and Figure 34 above and the STS-1 SPE is that the Envelope Capacity is aligned with the STS-1 framing boundaries and the TOH bytes; whereas the STS-1 SPE is NOT aligned with the STS-1 framing boundaries, nor the TOH bytes.

The STS-1 SPE is an "87 byte column x 9 row" data-structure (which is the exact same size as is the Envelope Capacity) that is permitted to "float" within the "Envelope Capacity". As a consequence, the STS-1 SPE (within an STS-1 data-stream) will typically straddle across an STS-1 frame boundary.

9.2.1.1.3 The Byte Structure of the STS-1 SPE

As mentioned above, the STS-1 SPE is an 87 byte column x 9 row structure. The very first column within the STS-1 SPE consists of some overhead bytes which are known as the "Path Overhead" (or POH) bytes. The remaining portions of the STS-1 SPE is available for "user" data. The Byte Structure of the STS-1 SPE is presented below in Figure 35.

FIGURE 35. ILLUSTRATION OF THE BYTE STRUCTURE OF THE STS-1 SPE



In general, the role/purpose of the POH bytes is to fulfill the following functions.

- To support error detection within the STS-1 SPE
- To support the transmission of various alarm conditions such as RDI-P (Path - Remote Defect Indicator) and REI-P (Path - Remote Error Indicator)
- To support the transmission and reception of "Path Trace" Messages

The role of the POH bytes is beyond the scope of this data sheet and will not be discussed any further.

9.2.1.2 Mapping DS3 data into an STS-1 SPE

Now that we have defined the STS-1 SPE, we can now describe how a DS3 signal is mapped into an STS-1 SPE. As mentioned above, the STS-1 SPE is basically an 87 byte column x 9 row structure of data. The very first byte column (e.g., in all 9 bytes) consists of the POH (Path Overhead) bytes. All of the remaining bytes within the STS-1 SPE is simply referred to as "user" or "payload" data because this is the portion of the STS-1 signal that is used to transport "user data" from one end of the SONET network to the other. Telcordia GR-253-CORE specifies the approach that one must use to asynchronously map DS3 data into an STS-1 SPE. In short, this approach is presented below in Figure 36.

FIGURE 36. AN ILLUSTRATION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW MAP DS3 DATA INTO AN STS-1 SPE

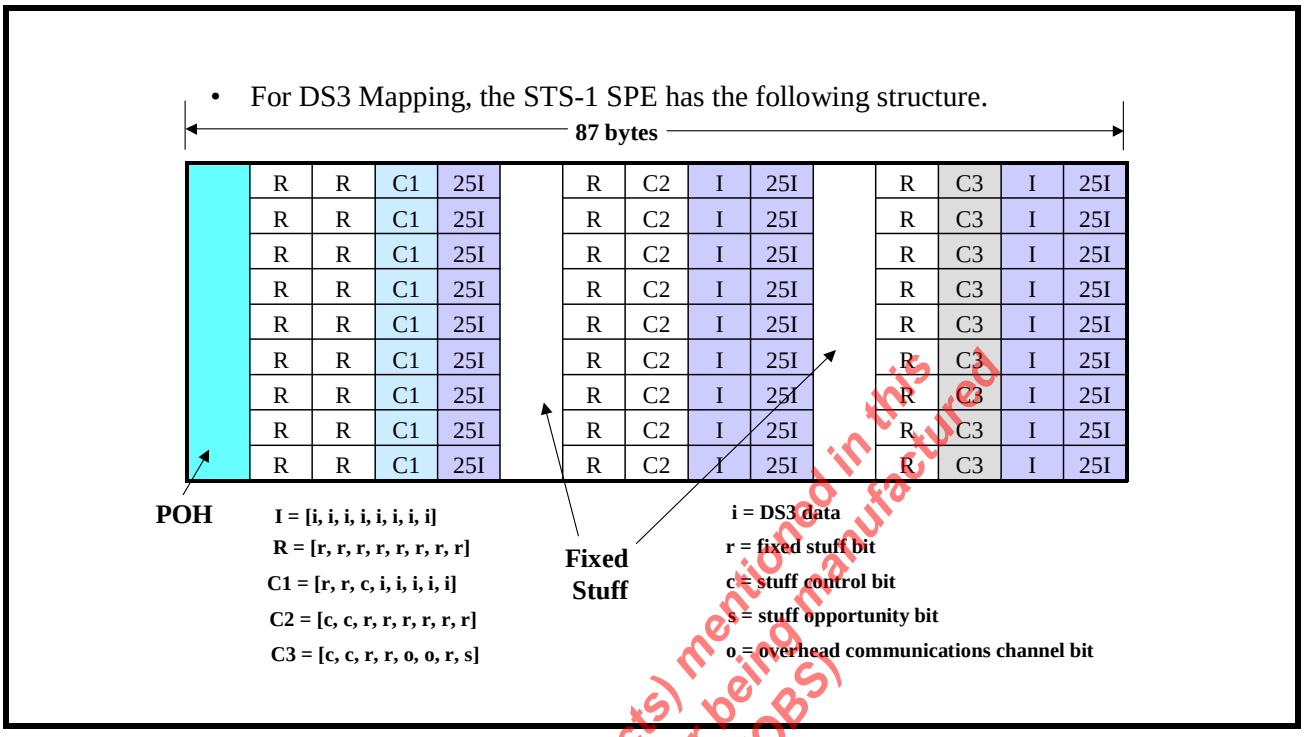


Figure 36 was copied directly out of Telcordia GR-253-CORE. However, this figure can be simplified and redrawn as depicted below in Figure 37.

FIGURE 37. A SIMPLIFIED "BIT-ORIENTED" VERSION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW TO MAP DS3 DATA INTO AN STS-1 SPE

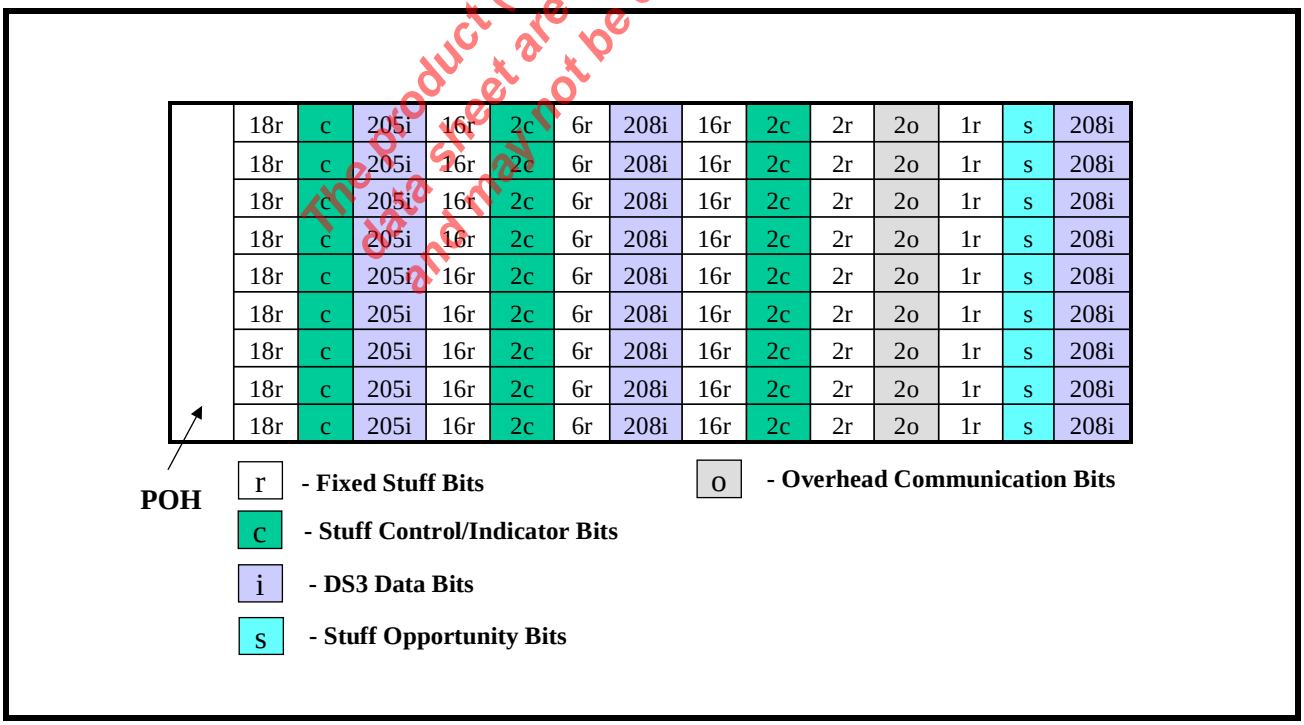


Figure 37 presents an alternative illustration of Telcordia GR-253-CORE's recommendation on how to asynchronously map DS3 data into an STS-1 SPE. In this case, the STS-1 SPE bit-format is expressed purely in the form of "bit-types" and "numbers of bits within each of these types of bits". If one studies this figure closely he/she will notice that this is the same "87 byte column x 9 row" structure that we have been talking about when defining the STS-1 SPE. However, in this figure, the "user-data" field is now defined and is said to consist of five (5) different types of bits. Each of these bit-types play a role when asynchronously mapping a DS3 signal into an STS-1 SPE. Each of these types of bits are listed and described below.

Fixed Stuff Bits

Fixed Stuff bits are simply "space-filler" bits that simply occupy space within the STS-1 SPE. These bit-fields have no functional role other than "space occupation". Telcordia GR-253-CORE does not define any particular value that these bits should be set to. Each of the 9 rows, within the STS-1 SPE will contain 59 of these "fixed stuff" bits.

DS3 Data Bits

The DS3 Data-Bits are (as its name implies) used to transport the DS3 data-bits within the STS-1 SPE. If the STS-1 SPE is transporting a framed DS3 data-stream, then these DS3 Data bits will carry both the "DS3 payload data" and the "DS3 overhead bits". Each of the 9 rows, within the STS-1 SPE will contain 621 of these "DS3 Data bits". This means that each STS-1 SPE contains 5,589 of these DS3 Data bit-fields.

Stuff Opportunity Bits

The "Stuff" Opportunity bits will function as either a "stuff" (or junk) bit, or it will carry a DS3 data-bit. The decision as to whether to have a "Stuff Opportunity" bit transport a "DS3 data-bit" or a "stuff" bit depends upon the "timing differences" between the DS3 data that is being mapped into the STS-1 SPE and the timing source that is driving the STS-1 circuitry within the PTE.

As will be described later on, these "Stuff Opportunity" Bits play a very important role in "frequency-justifying" the DS3 data that is being mapped into the STS-1 SPE. These "Stuff Opportunity" bits also play a critical role in inducing Intrinsic Jitter and Wander within the DS3 signal (as it is de-mapped by the remote PTE).

Each of the 9 rows, within the STS-1 SPE consists of one (1) Stuff Opportunity bit. Hence, there are a total of nine "Stuff Opportunity" bits within each STS-1 SPE.

Stuff Control/Indicator Bits

Each of the nine (9) rows within the STS-1 SPE contains five (5) Stuff Control/Indicator bits. The purpose of these "Stuff Control/Indicator" bits is to indicate (to the de-mapping PTE) whether the "Stuff Opportunity" bits (that resides in the same row) is a "Stuff" bit or is carrying a DS3 data bit.

If all five of these "Stuff Control/Indicator" bits, within a given row are set to "0", then this means that the corresponding "Stuff Opportunity" bit (e.g., the "Stuff Opportunity" bit within the same row) is carrying a DS3 data bit.

Conversely, if all five of these "Stuff Control/Indicator" bits, within a given row are set to "1" then this means that the corresponding "Stuff Opportunity" bit is carrying a "stuff" bit.

Overhead Communication Bits

Telcordia GR-253-CORE permits the user to use these two bits (for each row) as some sort of "Communications" bit. Some Mapper devices, such as the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/ STM-1 Mapper and the XRT94L33 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper IC (both from Exar Corporation) do permit the user to have access to these bit-fields.

However, in general, these particular bits can also be thought of as "Fixed Stuff" bits, that mostly have a "space occupation" function.

9.2.2 DS3 Frequency Offsets and the Use of the "Stuff Opportunity" Bits

In order to fully convey the role that the "stuff-opportunity" bits play, when mapping DS3 data into SONET, we will present a detailed discussion of each of the following "Mapping DS3 into STS-1" scenarios.

- The Ideal Case (e.g., with no frequency offsets)
- The 44.736Mbps + 1 ppm Case

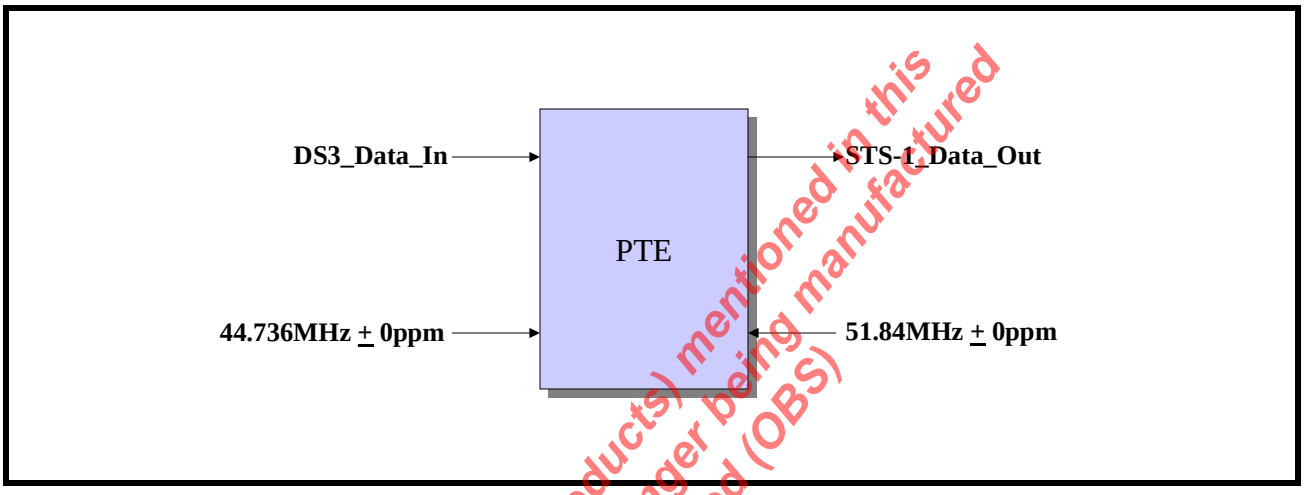
- The 44.736MHz - 1ppm Case

Throughout each of these cases, we will discuss how the resulting "bit-stuffing" (that was done when mapping the DS3 signal into SONET) affects the amount of intrinsic jitter and wander that will be present in the DS3 signal, once it is ultimately de-mapped from SONET.

9.2.2.1 The Ideal Case for Mapping DS3 data into an STS-1 Signal (e.g., with no Frequency Offsets)

Let us assume that we are mapping a DS3 signal, which has a bit rate of exactly 44.736Mbps (with no frequency offset) into SONET. Further, let us assume that the SONET circuitry within the PTE is clocked at exactly 51.84MHz (also with no frequency offset), as depicted below.

FIGURE 38. A SIMPLE ILLUSTRATION OF A DS3 DATA-STREAM BEING MAPPED INTO AN STS-1 SPE, VIA A PTE



Given the above-mentioned assumptions, we can state the following.

- The DS3 data-stream has a bit-rate of exactly 44.736Mbps
- The PTE will create 8000 STS-1 SPE's per second
- In order to properly map a DS3 data-stream into an STS-1 data-stream, then each STS-1 SPE must carry (44.736Mbps/8000 =) 5592 DS3 data bits.

Is there a Problem?

According to Figure 37, each STS-1 SPE only contains 5589 bits that are specifically designated for "DS3 data bits". In this case, each STS-1 SPE appears to be three bits "short".

No there is a Simple Solution

No, earlier we mentioned that each STS-1 SPE consists of nine (9) "Stuff Opportunity" bits. Therefore, these three additional bits (for DS3 data) are obtained by using three of these "Stuff Opportunity" bits. As a consequence, three (3) of these nine (9) "Stuff Opportunity" bits, within each STS-1 SPE, will carry DS3 data-bits. The remaining six (6) "Stuff Opportunity" bits will typically function as "stuff" bits.

In summary, for the "Ideal Case"; where there is no frequency offset between the DS3 and the STS-1 bit-rates, once this DS3 data-stream has been mapped into the STS-1 data-stream, then each and every STS-1 SPE will have the following "Stuff Opportunity" bit utilization.

3 "Stuff Opportunity" bits will carry DS3 data bits.

6 "Stuff Opportunity" bits will function as "stuff" bits

In this case, this DS3 signal (which has now been mapped into STS-1) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination PTE", this PTE will extract (or de-map) this DS3 data-stream from each incoming STS-1 SPE. Now since each and every STS-1 SPE contains exactly 5592 DS3 data bits; then the bit rate of this DS3 signal will be exactly 44.736Mbps (such as it was when it was mapped into SONET, at the "Source" PTE).

As a consequence, no "Mapping/De-Mapping" Jitter or Wander is induced in the "Ideal Case".

9.2.2.2 The 44.736Mbps + 1ppm Case

The "above example" was a very ideal case. In reality, there are going to be frequency offsets in both the DS3 and STS-1 signals. For instance Bellcore GR-499-CORE mandates that a DS3 signal have a bit rate of 44.736Mbps ± 20ppm. Hence, the bit-rate of a "Bellcore" compliant DS3 signal can vary from the exact correct frequency for DS3 by as much of 20ppm in either direction. Similarly, many SONET applications mandate that SONET equipment use at least a "Stratum 3" level clock as its timing source. This requirement mandates that an STS-1 signal must have a bit rate that is in the range of 51.84 ± 4.6ppm. To make matters worse, there are also provisions for SONET equipment to use (what is referred to as) a "SONET Minimum Clock" (SMC) as its timing source. In this case, an STS-1 signal can have a bit-rate in the range of 51.84Mbps ± 20ppm.

In order to convey the impact that frequency offsets (in either the DS3 or STS-1 signal) will impose on the bit-stuffing behavior, and the resulting bit-rate, intrinsic jitter and wander within the DS3 signal that is being transported across the SONET network; let us assume that a DS3 signal, with a bit-rate of 44.736Mbps + 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following things will occur.

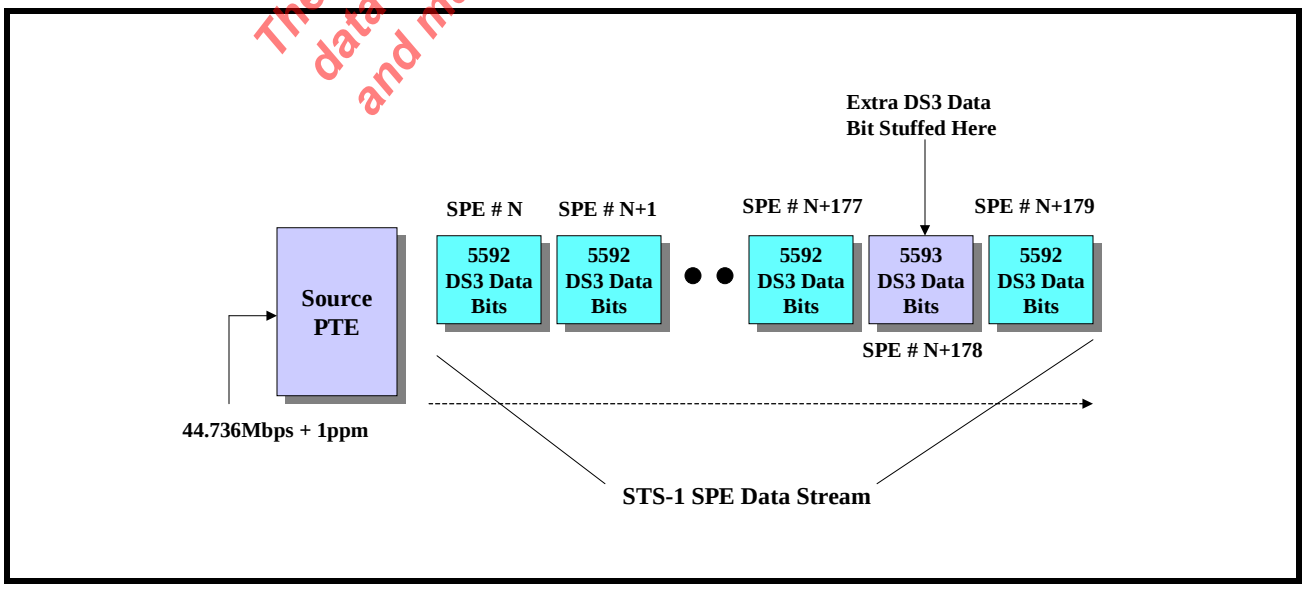
- In general, most of the STS-1 SPE's will each transport 5592 DS3 data bits.
- However, within a "one-second" period, a DS3 signal that has a bit-rate of 44.736Mbps + 1 ppm will deliver approximately 44.7 additional bits (over and above that of a DS3 signal with a bit-rate of 44.736Mbps + 0 ppm). This means that this particular signal will need to "negative-stuff" or map in an additional DS3 data bit every (1/44.736 =) 22.35ms. In other words, this additional DS3 data bit will need to be mapped into about one in every (22.35ms · 8000 =) 178.8 STS-1 SPEs in order to avoid dropping any DS3 data-bits.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps + 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits, as in the "Ideal" case). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need to insert an additional DS3 data bit within this STS-1 SPE. Whenever this occurs, then (for these particular STS-1 SPEs) the SPE will be carrying 5593 DS3 data bits (e.g., 4 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 5 Stuff Opportunity bits are "stuff" bits).

Figure 39 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 39. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE "SOURCE" PTE, WHEN MAPPING IN A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS + 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the "Destination" PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry 5593 DS3 data-bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is greater than 44.736Mbps. These "excursion" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of "mapping/de-mapping" jitter. Since each of these "bit-stuffing" events involve the insertion of one DS3 data bit, we can say that the amplitude of this "mapping/de-mapping" jitter is approximately 1UI-pp. From this point on, we will be referring to this type of jitter (e.g., that which is induced by the mapping and de-mapping process) as "de-mapping" jitter.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

9.2.2.3 The 44.736Mbps - 1ppm Case

In this case, let us assume that a DS3 signal, with a bit-rate of 44.736Mbps - 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following this will occur.

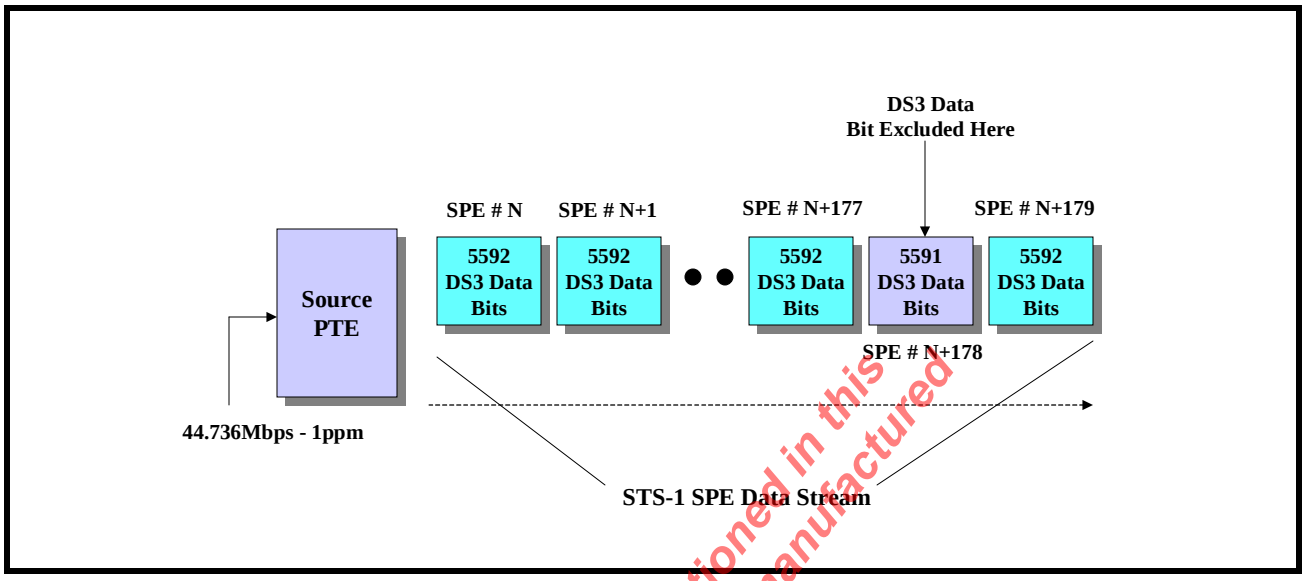
- In general, most of the STS-1 SPEs will each transport 5592 DS3 data bits.
- However, within a "one-second" period a DS3 signal that has a bit-rate of 44.736Mbps - 1ppm will deliver approximately 45 too few bits below that of a DS3 signal with a bit-rate of 44.736Mbps + 0ppm. This means that this particular signal will need to "positive-stuff" or exclude a DS3 data bit from mapping every (1/44.736) = 22.35ms. In other words, we will need to avoid mapping this DS3 data-bit about one in every (22.35ms*8000) = 178.8 STS-1 SPEs.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps - 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need for a "positive-stuffing" event. Whenever these "positive-stuffing" events occur then (for these particular STS-1 SPEs) the SPE will carry only 5591 DS3 data bits (e.g., in this case, only 2 Stuff Opportunity bits will be carrying DS3 data-bits, and the remaining 7 Stuff Opportunity bits are "stuff" bits).

Figure 40 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 40. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE SOURCE PTE, WHEN MAPPING A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS - 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the Destination PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case, most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry only 5591 DS3 data bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is less than 44.736Mbps. These "excursions" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of mapping/de-mapping jitter with an amplitude of approximately 1UI-pp.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

We talked about De-Mapping Jitter. What about De-Mapping Wander?

The Telcordia and Bellcore specifications define "Wander" as "Jitter with a frequency of less than 10Hz". Based upon this definition, the DS3 signal (that is being transported by SONET) will cease to contain jitter and will now contain "Wander", whenever the frequency offset of the DS3 signal being mapped into SONET is less than 0.2ppm.

9.3 Jitter/Wander due to Pointer Adjustments

In the previous section, we described how a DS3 signal is asynchronously-mapped into SONET, and we also defined "Mapping/De-mapping" jitter. In this section, we will describe how occurrences within the SONET network will induce jitter/wander within the DS3 signal that is being transported across the SONET network.

In order to accomplish this, we will discuss the following topics in detail.

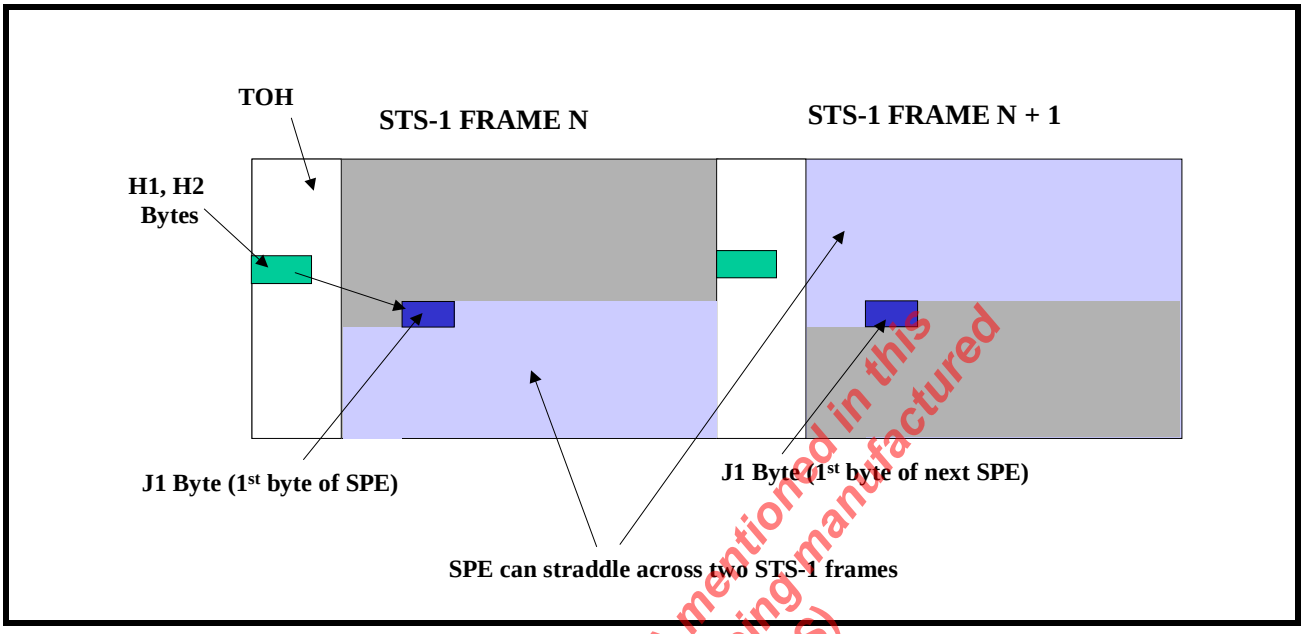
- The concept of an STS-1 SPE pointer
- The concept of Pointer Adjustments
- The causes of Pointer Adjustments
- How Pointer Adjustments induce jitter/wander within a DS3 signal being transported by that SONET network.

9.3.1 The Concept of an STS-1 SPE Pointer

As mentioned earlier, the STS-1 SPE is not aligned to the STS-1 frame boundaries and is permitted to "float" within the Envelope Capacity. As a consequence, the STS-1 SPE will often times "straddle" across two

consecutive STS-1 frames. Figure 41 presents an illustration of an STS-1 SPE straddling across two consecutive STS-1 frames.

FIGURE 41. AN ILLUSTRATION OF AN STS-1 SPE STRADDLING ACROSS TWO CONSECUTIVE STS-1 FRAMES



A PTE that is receiving and terminating an STS-1 data-stream will perform the following tasks.

- It will acquire and maintain STS-1 frame synchronization with the incoming STS-1 data-stream.
- Once the PTE has acquired STS-1 frame synchronization, then it will locate the J1 byte (e.g., the very byte within the very next STS-1 SPE) within the Envelope Capacity by reading out the contents of the H1 and H2 bytes.

The H1 and H2 bytes are referred to (in the SONET standards) as the SPE Pointer Bytes. When these two bytes are concatenated together in order to form a 16-bit word (with the H1 byte functioning as the "Most Significant Byte") then the contents of the "lower" 10 bit-fields (within this 16-bit word) reflects the location of the J1 byte within the Envelope Capacity of the incoming STS-1 data-stream. Figure 42 presents an illustration of the bit format of the H1 and H2 bytes, and indicates which bit-fields are used to reflect the location of the J1 byte.

FIGURE 42. THE BIT-FORMAT OF THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE 10 BITS, REFLECTING THE LOCATION OF THE J1 BYTE, DESIGNATED

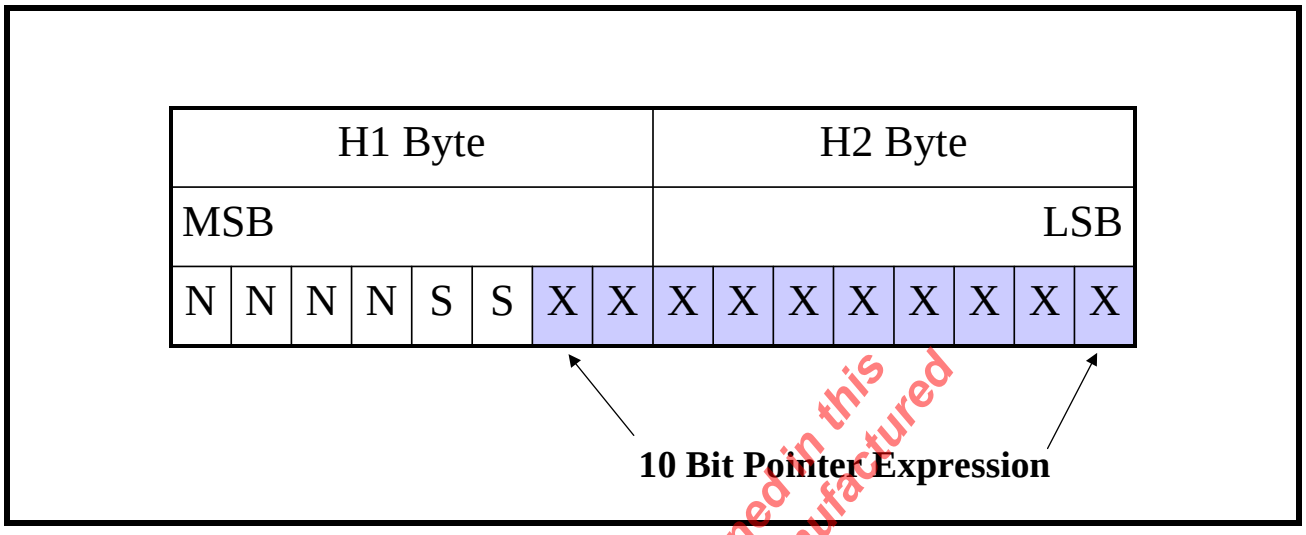
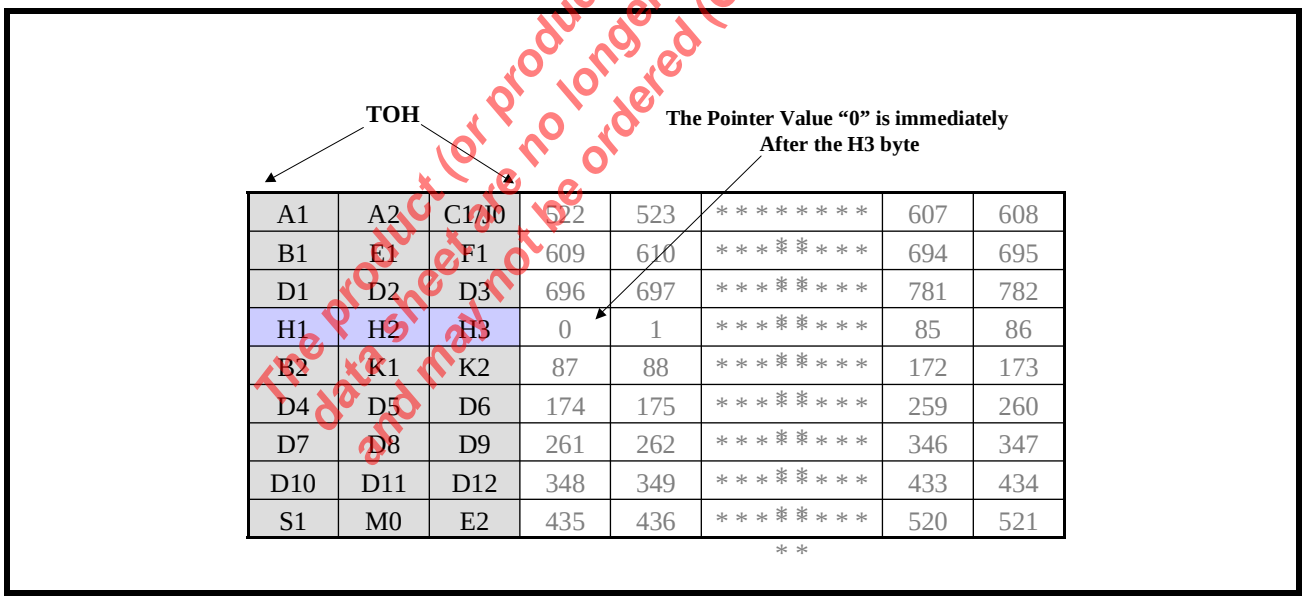


Figure 43 relates the contents within these 10 bits (within the H1 and H2 bytes) to the location of the J1 byte (e.g., the very first byte of the STS-1 SPE) within the Envelope Capacity.

FIGURE 43. THE RELATIONSHIP BETWEEN THE CONTENTS OF THE "POINTER BITS" (E.G., THE 10-BIT EXPRESSION WITHIN THE H1 AND H2 BYTES) AND THE LOCATION OF THE J1 BYTE WITHIN THE ENVELOPE CAPACITY OF AN STS-1 FRAME



A1	A2	C1/J0	522	523	* * * * * * * *	607	608
B1	E1	F1	609	610	* * * * * * * *	694	695
D1	D2	D3	696	697	* * * * * * * *	781	782
H1	H2	H3	0	1	* * * * * * * *	85	86
B2	K1	K2	87	88	* * * * * * * *	172	173
D4	D5	D6	174	175	* * * * * * * *	259	260
D7	D8	D9	261	262	* * * * * * * *	346	347
D10	D11	D12	348	349	* * * * * * * *	433	434
S1	M0	E2	435	436	* * * * * * * *	520	521

NOTES:

1. *If the content of the "Pointer Bits" is "0x00" then the J1 byte is located immediately after the H3 byte, within the Envelope Capacity.*
2. *If the contents of the 10-bit expression exceed the value of 0x30F (or 782, in decimal format) then it does not contain a valid pointer value.*

9.3.2 Pointer Adjustments within the SONET Network

The word SONET stands for "Synchronous Optical NETwork. This name implies that the entire SONET network is synchronized to a single clock source. However, because the SONET (and SDH) Networks can

span thousands of miles, traverse many different pieces of equipments, and even cross International boundaries; in practice, the SONET/SDH network is NOT synchronized to a single clock source.

In practice, the SONET/SDH network can be thought of as being divided into numerous "Synchronization Islands". Each of these "Synchronization Islands" will consist of numerous pieces of SONET Terminal Equipment. Each of these pieces of SONET Terminal Equipment will all be synchronized to a single Stratum-1 clock source which is the most accurate clock source within the Synchronization Island. Typically a "Synchronization Island" will consist of a single "Timing Master" equipment along with multiple "Timing Slave" pieces of equipment. This "Timing Master" equipment will be directly connected to the Stratum-1 clock source and will have the responsibility of distributing a very accurate clock signal (that has been derived from the Stratum 1 clock source) to each of the "Timing Slave" pieces of equipment within the "Synchronization Island". The purpose of this is to permit each of the "Timing Slave" pieces of equipment to be "synchronized" with the "Timing Master" equipment, as well as the Stratum 1 Clock source. Typically this "clock distribution" is performed in the form of a BITS (Building Integrated Timing Supply) clock, in which a very precise clock signal is provided to the other pieces of equipment via a T1 or E1 line signal.

Many of these "Synchronization Islands" will use a Stratum-1" clock source that is derived from GPS pulses that are received from Satellites that operate at Geo-synchronous orbit. Other "Synchronization Islands" will use a Stratum-1" clock source that is derived from a very precise local atomic clock. As a consequence, different "Synchronization Islands" will use different Stratum 1 clock sources. The up-shot of having these "Synchronization Islands" that use different "Stratum-1 clock" sources, is that the Stratum 1 Clock frequencies, between these "Synchronization Islands" are likely to be slightly different from each other. These "frequency-differences" within Stratum 1 clock sources will result in "clock-domain changes" as a SONET signal (that is traversing the SONET network) passes from one "Synchronization Island" to another.

The following section will describe how these "frequency differences" will cause a phenomenon called "pointer adjustments" to occur in the SONET Network.

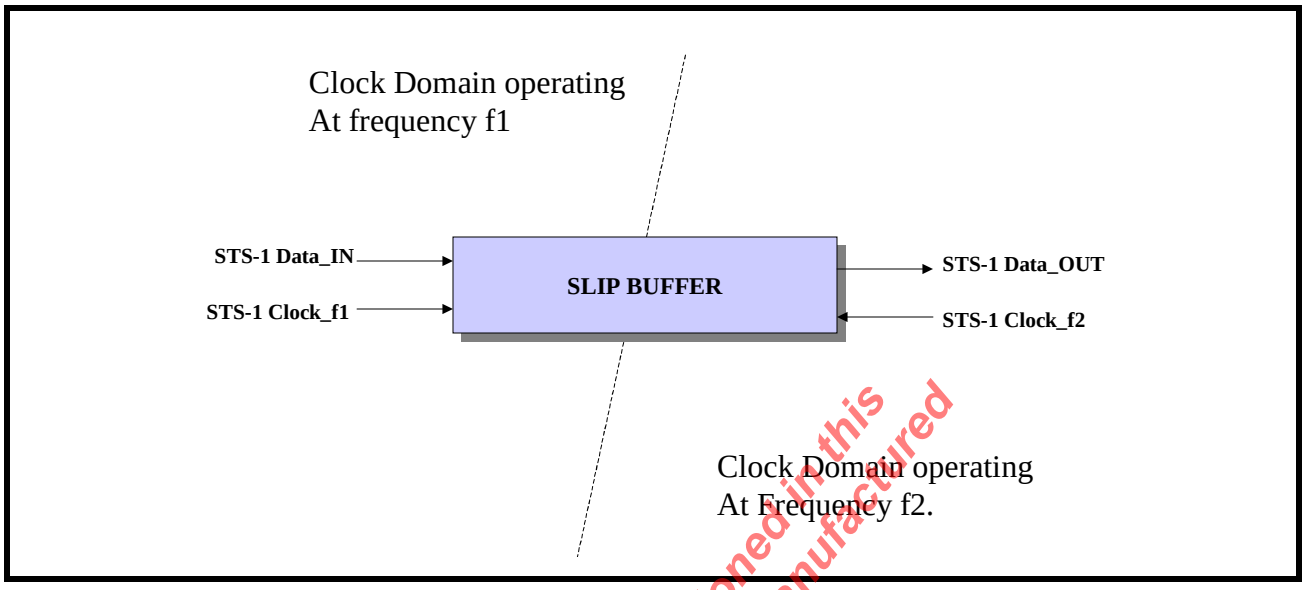
9.3.3 Causes of Pointer Adjustments

The best way to discuss how pointer adjustment events occur is to consider an STS-1 signal, which is driven by a timing reference of frequency f1; and that this STS-1 signal is being routed to a network equipment (that resides within a different "Synchronization Island") and processes STS-1 data at a frequency of f2.

NOTE: *Clearly, both frequencies f1 and f2 are at the STS-1 rate (e.g., 51.84MHz). However, these two frequencies are likely to be slightly different from each other.*

Now, since the STS-1 signal (which is of frequency f1) is being routed to the network element (which is operating at frequency f2), the typical design approach for handling "clock-domain" differences is to route this STS-1 signal through a "Slip Buffer" as illustrated below.

FIGURE 44. AN ILLUSTRATION OF AN STS-1 SIGNAL BEING PROCESSED VIA A SLIP BUFFER



In the "Slip Buffer, the "input" STS-1 data (labeled "STS-1 Data_IN") is latched into the FIFO, upon a given edge of the corresponding "STS-1 Clock_f1" input clock signal. The STS-1 Data (labeled "STS-1 Data_OUT") is clocked out of the Slip Buffer upon a given edge of the "STS-1 Clock_f2" input clock signal.

The behavior of the data, passing through the "Slip Buffer" is now described for each possible relationship between frequencies f1 and f2.

If f1 = f2

If both frequencies, f1 and f2 are exactly equal, then the STS-1 data will be "clocked" into the "Slip Buffer" at exactly the same rate that it is "clocked out". In this case, the "Slip Buffer" will neither fill-up nor become depleted. As a consequence, no pointer-adjustments will occur in this STS-1 data stream. In other words, the STS-1 SPE will remain at a constant location (or offset) within each STS-1 envelope capacity for the duration that this STS-1 signal is supporting this particular service.

If f1 < f2

If frequency f1 is less than f2, then this means that the STS-1 data is being "clocked out" of the "Slip Buffer" at a faster rate than it is being clocked in. In this case, the "Slip Buffer" will eventually become depleted. Whenever this occurs, a typical strategy is to "stuff" (or insert) a "dummy byte" into the data stream. The purpose of stuffing this "dummy byte" is to compensate for the frequency differences between f1 and f2, and attempt to keep the "Slip Buffer, at a somewhat constant fill level.

NOTE: *This "dummy byte" does not carry any valuable information (not for the user, nor for the system).*

Since this "dummy byte" carries no useful information, it is important that the "Receiving PTE" be notified anytime this "dummy byte" stuffing occurs. This way, the Receiving Terminal can "know" not to treat this "dummy byte" as user data.

Byte-Stuffing and Pointer Incrementing in a SONET Network

Whenever this "byte-stuffing" occurs then the following other things occur within the STS-1 data stream.

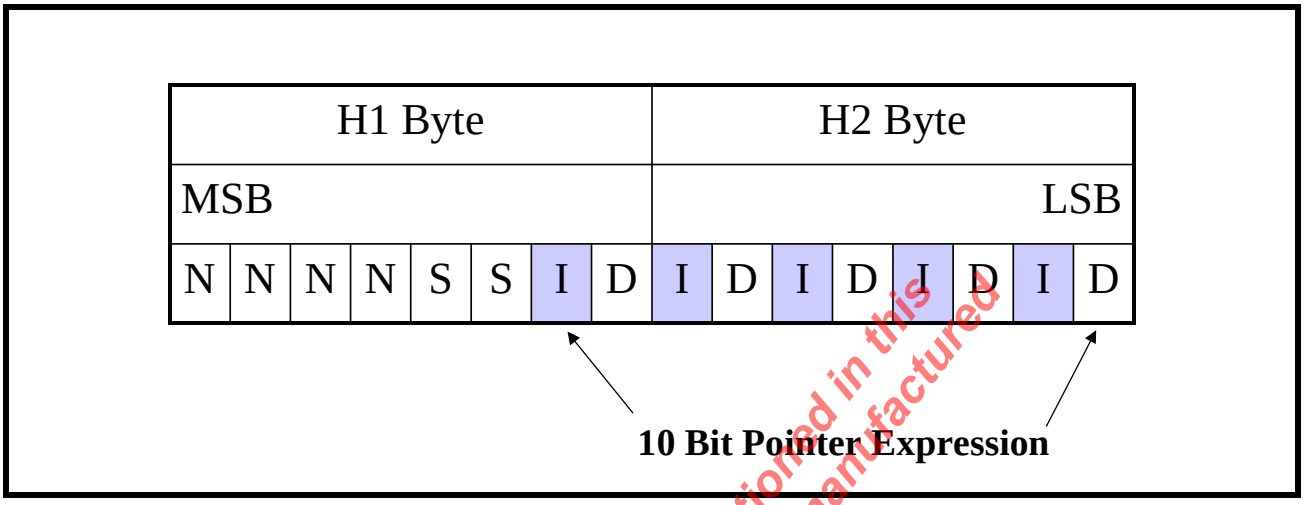
During the STS-1 frame that contains the "Byte-Stuffing" event

a. The "stuff-byte" will be inserted into the byte position immediately after the H3 byte. This insertion of the "dummy byte" immediately after the H3 byte position will cause the J1 byte (and in-turn, the rest of the SPE) to be "byte-shifted" away from the H3 byte. As a consequence, the offset between the H3 byte position and the STS-1 SPE will now have been increased by 1 byte.

b. The "Transmitting" Network Equipment will notify the remote terminal of this byte-stuffing event, by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "I" bits.

Figure 45 presents an illustration of the bit-format within the 16-bit word (consist of the H1 and H2 bytes) with the "I" bits designated.

FIGURE 45. AN ILLUSTRATION OF THE BIT FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "I" BITS DESIGNATED



NOTE: *At this time the "I" bits are inverted in order to denote that an "incrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Byte-Stuffing" event

The "I" bits (within the "pointer-word") will be set back to their normal value; and the contents of the H1 and H2 bytes will be incremented by "1".

If f1 > f2

If frequency f1 is greater than f2, then this means that the STS-1 data is being clocked into the "Slip Buffer" at a faster rate than is being clocked out. In this case, the "Slip Buffer" will start to fill up. Whenever this occurs, a typical strategy is to delete (e.g., negative-stuff) a byte from the Slip Buffer. The purpose of this "negative-stuffing" is to compensate for the frequency differences between f1 and f2; and to attempt to keep the "Slip Buffer" at a somewhat constant fill-level.

NOTE: *This byte, which is being "un-stuffed" does carry valuable information for the user (e.g., this byte is typically a payload byte). Therefore, whenever this negative stuffing occurs, two things must happen.*

a. The "negative-stuffed" byte must not be simply discarded. In other words, it must somehow also be transmitted to the remote PTE with the remainder of the SPE data.

b. The remote PTE must be notified of the occurrence of these "negative-stuffing" events. Further, the remote PTE must know where to obtain this "negative-stuffed" byte.

Negative-Stuffing and Pointer-Decrementing in a SONET Network

Whenever this "byte negative-stuffing" occurs then the following other things occur within the STS-1 data-stream.

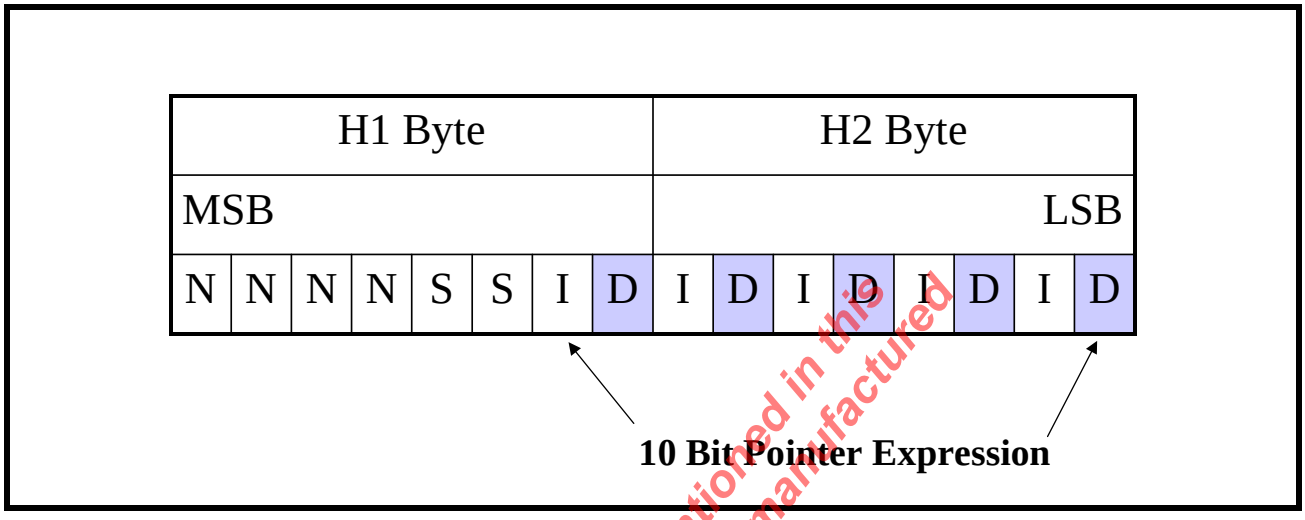
During the STS-1 frame that contains the "Negative Byte-Stuffing" Event

a. The "Negative-Stuffed" byte will be inserted into the H3 byte position. Whenever an SPE data byte is inserted into the H3 byte position (which is ordinarily an unused byte), the number of bytes that will exist between the H3 byte and the J1 byte within the very next SPE will be reduced by 1 byte. As a consequence, in this case, the J1 byte (and in-turn, the rest of the SPE) will now be "byte-shifted" towards the H3 byte position.

b. The "Transmitting" Network Element will notify the remote terminal of this "negative-stuff" event by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "D" bits.

Figure 46 presents an illustration of the bit format within the 16-bit word (consisting of the H1 and H2 bytes) with the "D" bits designated.

FIGURE 46. AN ILLUSTRATION OF THE BIT-FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "D" BITS DESIGNATED



NOTE: *At this time the "D" bits are inverted in order to denote that a "decrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Negative Byte-Stuffing" Event

The "D" bits (within the pointer-word) will be set back to their normal value; and the contents of the H1 and H2 bytes will be decremented by one.

9.3.4 Why are we talking about Pointer Adjustments?

The overall SONET network consists of numerous "Synchronization Islands". As a consequence, whenever a SONET signal is being transmitted from one "Synchronization Island" to another; that SONET signal will undergo a "clock domain" change as it traverses the network. This clock domain change will result in periodic pointer-adjustments occurring within this SONET signal. Depending upon the direction of this "clock-domain" shift that the SONET signal experiences, there will either be periodic "incrementing" pointer-adjustment events or periodic "decrementing" pointer-adjustment events within this SONET signal.

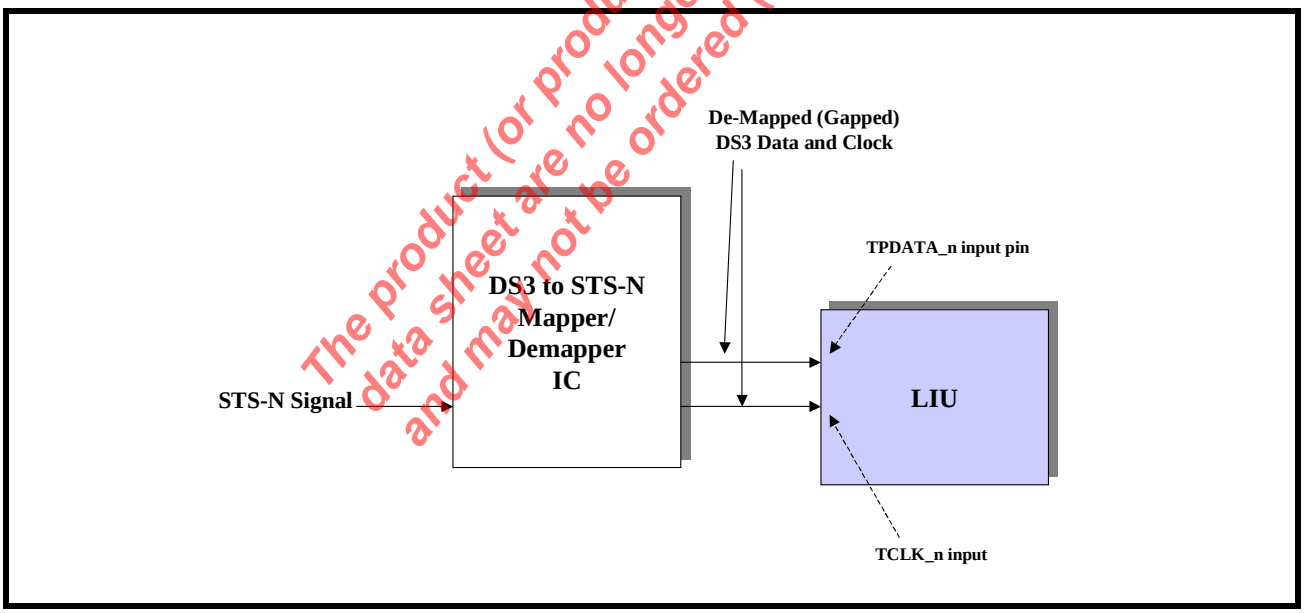
Regardless of whether a given SONET signal is experiencing incrementing or decrementing pointer adjustment events, each pointer adjustment event will result in an abrupt 8-bit shift in the position of the SPE within the STS-1 data-stream. If this STS-1 signal is transporting an "asynchronously-mapped" DS3 signal; then this 8-bit shift in the location of the SPE (within the STS-1 signal) will result in approximately 8UIpp of jitter within the asynchronously-mapped DS3 signal, as it is de-mapped from SONET. In “Section 9.5, A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications” on page 68 we will discuss the "Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE. However, for now we will simply state that this 8UIpp of intrinsic jitter far exceeds these "intrinsic jitter" requirements.

In summary, pointer-adjustments events are a "fact of life" within the SONET/SDH network. Further, pointer-adjustment events, within a SONET signal that is transporting an asynchronously-mapped DS3 signal, will impose a significant impact on the Intrinsic Jitter and Wander within that DS3 signal as it is de-mapped from SONET.

9.4 Clock Gapping Jitter

In most applications (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper Device in the manner as presented below in Figure 47.

FIGURE 47. ILLUSTRATION OF THE TYPICAL APPLICATIONS FOR THE LIU IN A SONET DE-SYNC APPLICATION



In this application, the Mapper IC will have the responsibility of receiving an STS-N signal (from the SONET Network) and performing all of the following operations on this STS-N signal.

- Byte-de-interleaving this incoming STS-N signal into N STS-1 signals
- Terminating each of these STS-1 signals
- Extracting (or de-mapping) the DS3 signal(s) from the SPEs within each of these terminated STS-1 signals.

In this application, these Mapper devices can be thought of as multi-channel devices. For example, an STS-3 Mapper can be viewed as a 3-Channel DS3/STS-1 to STS-3 Mapper IC. Similarly, an STS-12 Mapper can be

viewed as a 12-Channel DS3/STS-1 to STS-12 Mapper IC. Continuing on with this line of thought, if a Mapper IC is configured to receive an STS-N signal, and (from this STS-N signal) de-map and output N DS3 signals (towards the DS3 facility), then it will typically do so in the following manner.

- In many cases, the Mapper IC will output this DS3 signal, using both a "Data-Signal" and a "Clock-Signal". In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data-Signal.
- However, as the Mapper IC output this STS-1 data-stream, it will typically supply clock pulses (via the Clock-Signal output) coincident to whenever a DS3 bit is being output via the Data-Signal. In this case, the Mapper IC will NOT supply a clock pulse coincident to when a TOH, POH, or any "non-DS3 data-bit" is being output via the "Data-Signal".

Now, since the Mapper IC will output the entire STS-1 data stream (via the Data-Signal), the output Clock-Signal will be of the form such that it has a period of 19.3ns (e.g., a 51.84MHz clock signal). However, the Mapper IC will still generate approximately 44,736,000 clock pulses during any given one second period. Hence, the clock signal that is output from the Mapper IC will be a horribly gapped 44.736MHz clock signal. One can view such a clock signal as being a very-jittery 44.736MHz clock signal. This jitter that exists within the "Clock-Signal" is referred to as "Clock-Gapping" Jitter. A more detailed discussion on how the user must handle this type of jitter is presented in “Section 9.8.2, Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU” on page 79.

9.5 A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications

The "Category I Intrinsic Jitter Requirements" per Telcordia GR-253-CORE (for DS3 applications) mandates that the user perform a large series of tests against certain specified "Scenarios". These "Scenarios" and their corresponding requirements is summarized in Table 18, below.

TABLE 18: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
DS3 De-Mapping Jitter		0.4UI-pp	Includes effects of De-Mapping and Clock Gapping Jitter
Single Pointer Adjustment	A1	0.3UI-pp + Ao	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.NOTE: Ao is the amount of intrinsic jitter that was measured during the "DS3 De-Mapping Jitter" phase of the Test.
Pointer Bursts	A2	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Phase Transients	A3	1.2UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

TABLE 18: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
Continuous Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

NOTE: *All of these intrinsic jitter measurements are to be performed using a band-pass filter of 10Hz to 400kHz.*

Each of the scenarios presented in Table 18, are briefly described below.

9.5.1 DS3 De-Mapping Jitter

DS3 De-Mapping Jitter is the amount of Intrinsic Jitter that will be measured within the "Line" or "Facility-side" DS3 signal, (after it has been de-mapped from a SONET signal) without the occurrence of "Pointer Adjustments" within the SONET signal.

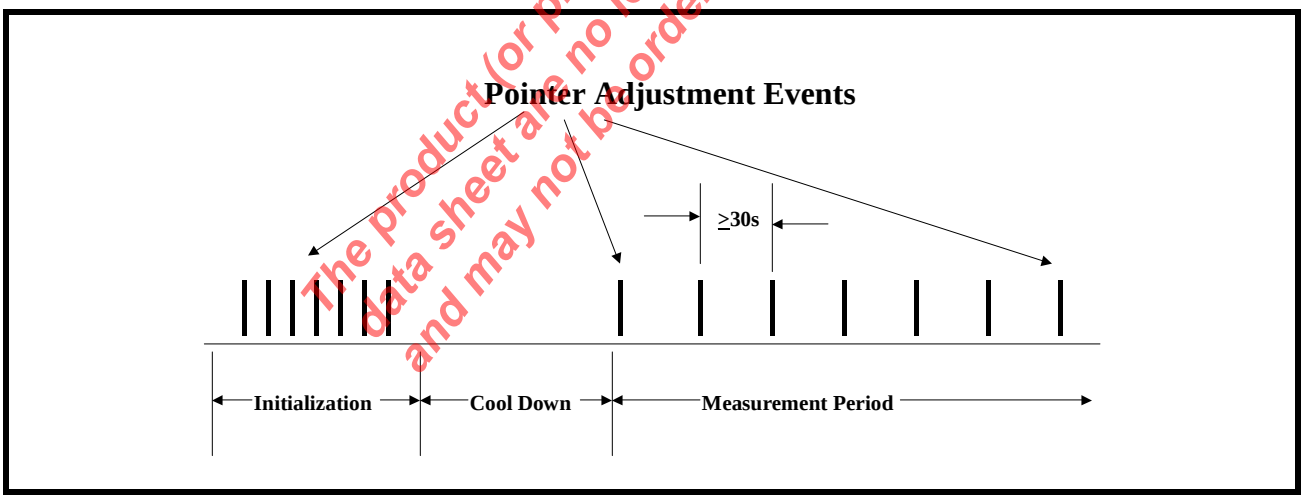
Telcordia GR-253-CORE requires that the "DS3 De-Mapping" Jitter be less than 0.4UI-pp, when measured over all possible combinations of DS3 and STS-1 frequency offsets.

9.5.2 Single Pointer Adjustment

Telcordia GR-253-CORE states that if each pointer adjustment (within a continuous stream of pointer adjustments) is separated from each other by a period of 30 seconds, or more; then they are sufficiently isolated to be considered "Single-Pointer Adjustments".

Figure 48 presents an illustration of the "Single Pointer Adjustment" Scenario.

FIGURE 48. ILLUSTRATION OF SINGLE POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE states that the Intrinsic Jitter that is measured (within the DS3 signal) that is ultimately de-mapped from a SONET signal that is experiencing "Single-Pointer Adjustment" events, must NOT exceed the value 0.3UI-pp + Ao.

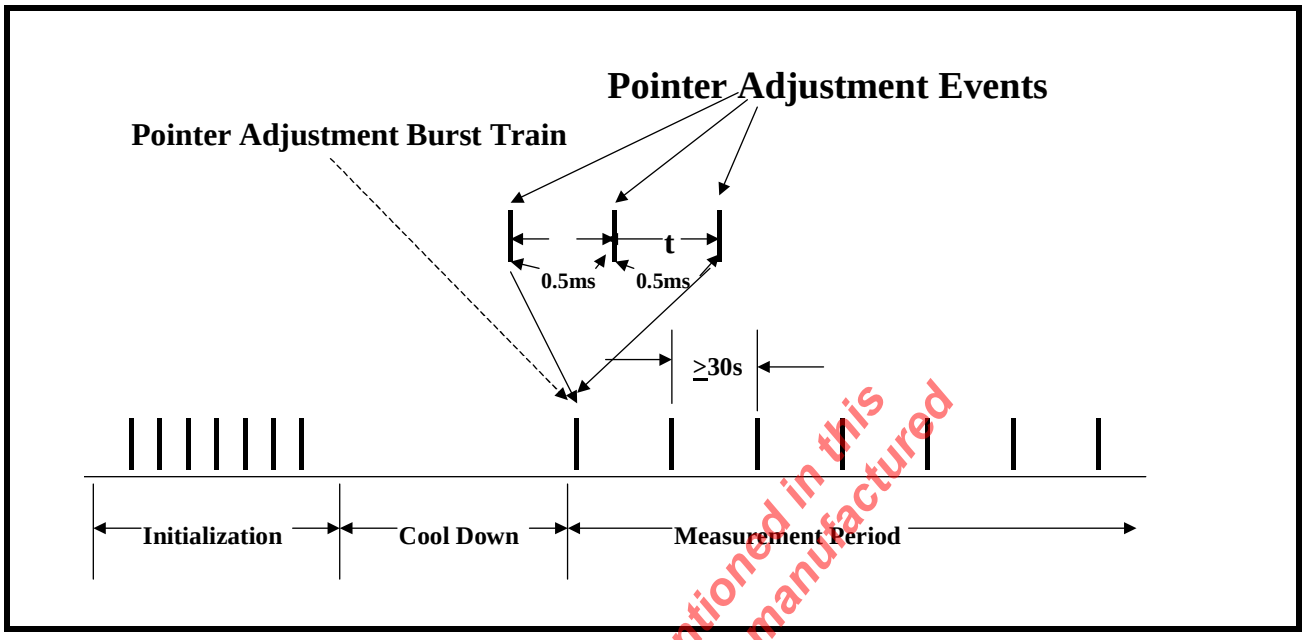
NOTES:

1. *Ao is the amount of Intrinsic Jitter that was measured during the "De-Mapping" Jitter portion of this test.*
2. *Testing must be performed for both Incrementing and Decrementing Pointer Adjustments.*

9.5.3 Pointer Burst

Figure 49 presents an illustration of the "Pointer Burst" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 49. ILLUSTRATION OF BURST OF POINTER ADJUSTMENT SCENARIO

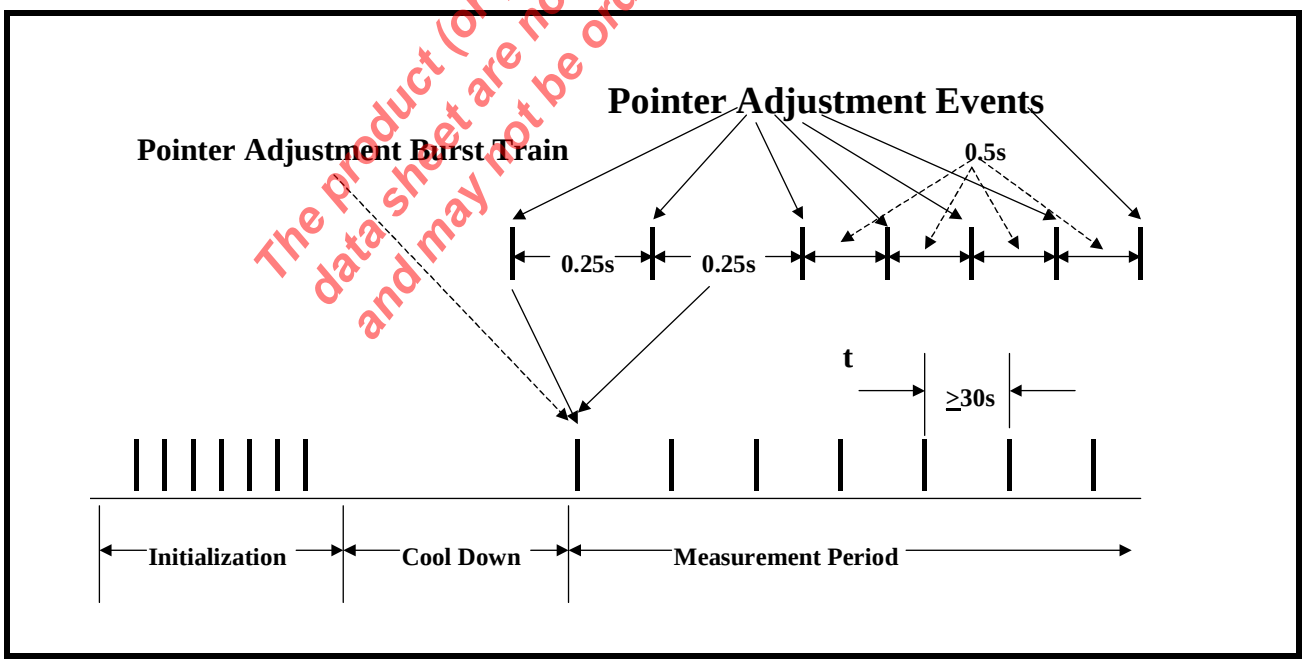


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Burst of Pointer Adjustment" scenario, must NOT exceed 1.3UI-pp.

9.5.4 Phase Transients

Figure 50 presents an illustration of the "Phase Transients" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 50. ILLUSTRATION OF "PHASE-TRANSIENT" POINTER ADJUSTMENT SCENARIO

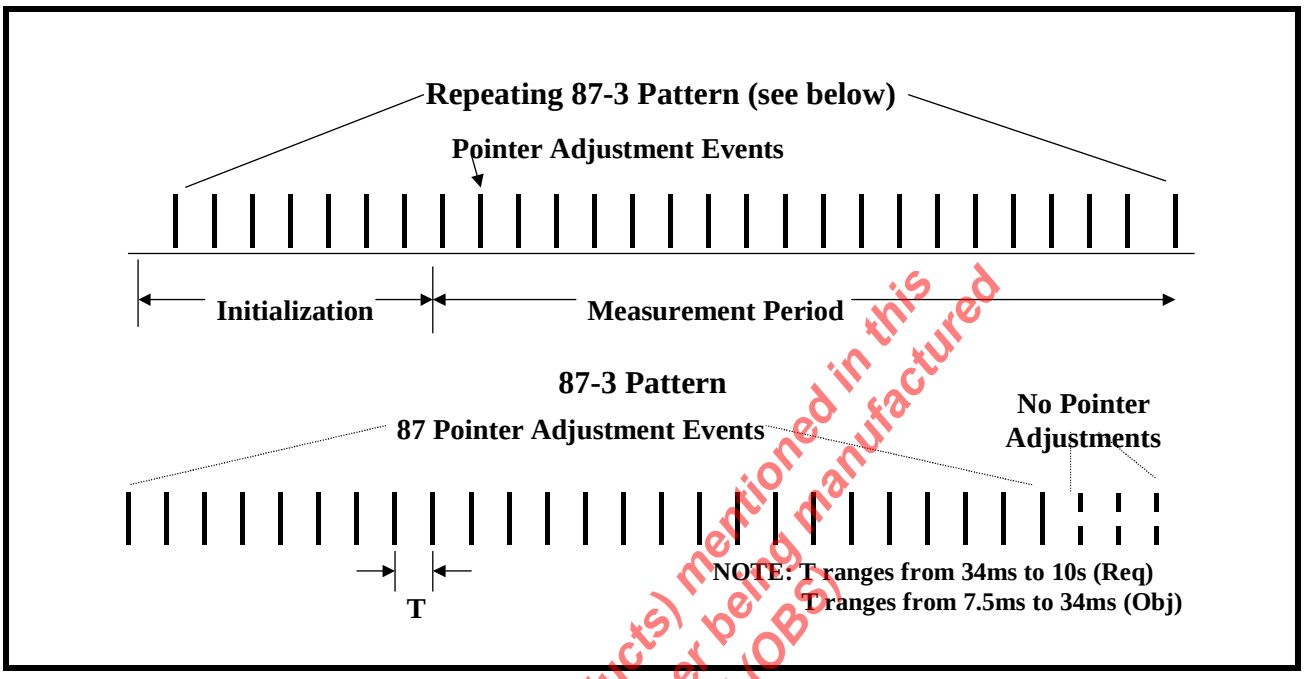


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Phase Transient - Pointer Adjustment" scenario must NOT exceed 1.2UI-pp.

9.5.5 87-3 Pattern

Figure 51 presents an illustration of the "87-3 Continuous Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 51. AN ILLUSTRATION OF THE 87-3 CONTINUOUS POINTER ADJUSTMENT PATTERN



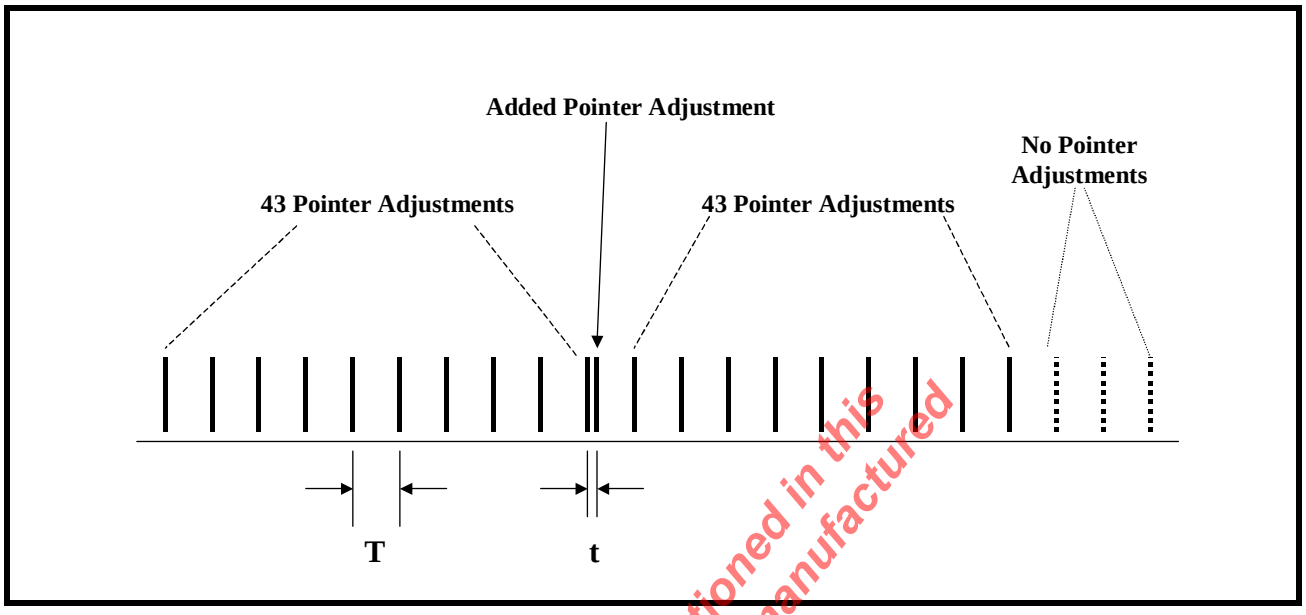
Telcordia GR-253-CORE defines an "87-3 Continuous" Pointer Adjustment pattern, as a repeating sequence of 90 pointer adjustment events. Within this 90 pointer adjustment event, 87 pointer adjustments are actually executed. The remaining 3 pointer adjustments are never executed. The spacing between individual pointer adjustment events (within this scenario) can range from 7.5ms to 10seconds.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp.

9.5.6 87-3 Add

Figure 52 presents an illustration of the "87-3 Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 52. ILLUSTRATION OF THE 87-3 ADD POINTER ADJUSTMENT PATTERN



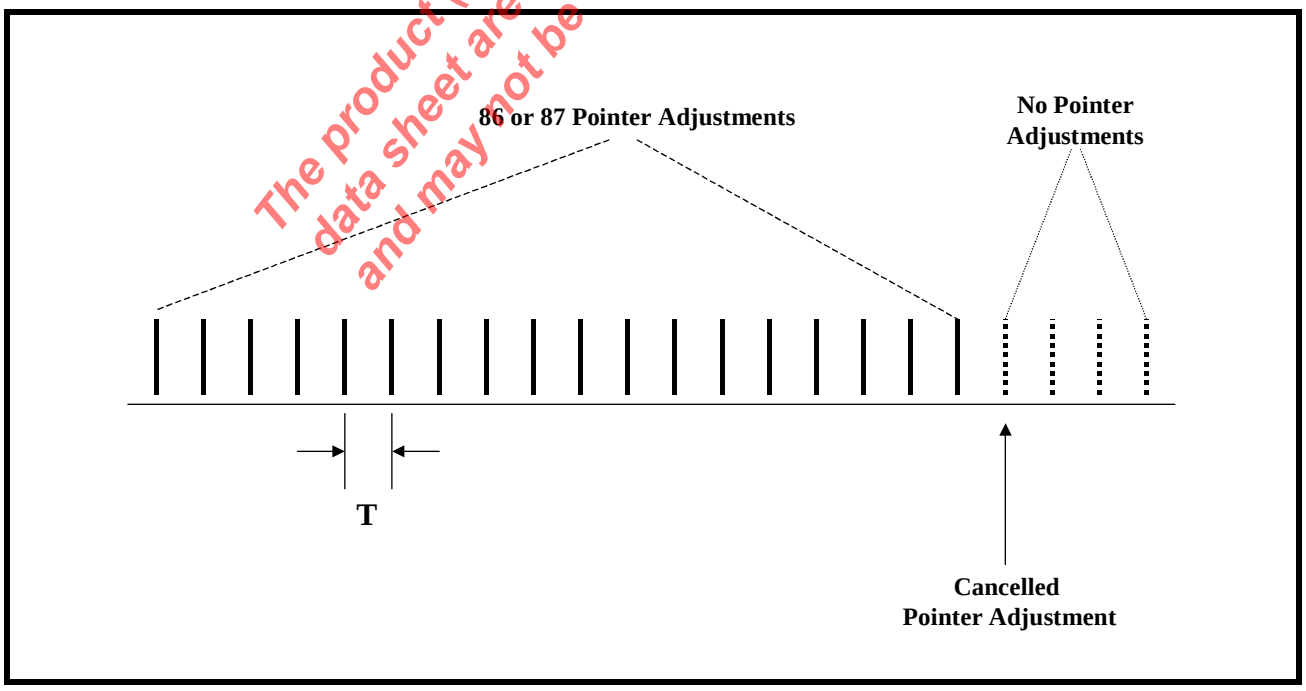
Telcordia GR-253-CORE defines an "87-3 Add" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 52.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.7 87-3 Cancel

Figure 53 presents an illustration of the 87-3 Cancel Pattern Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 53. ILLUSTRATION OF 87-3 CANCEL POINTER ADJUSTMENT SCENARIO



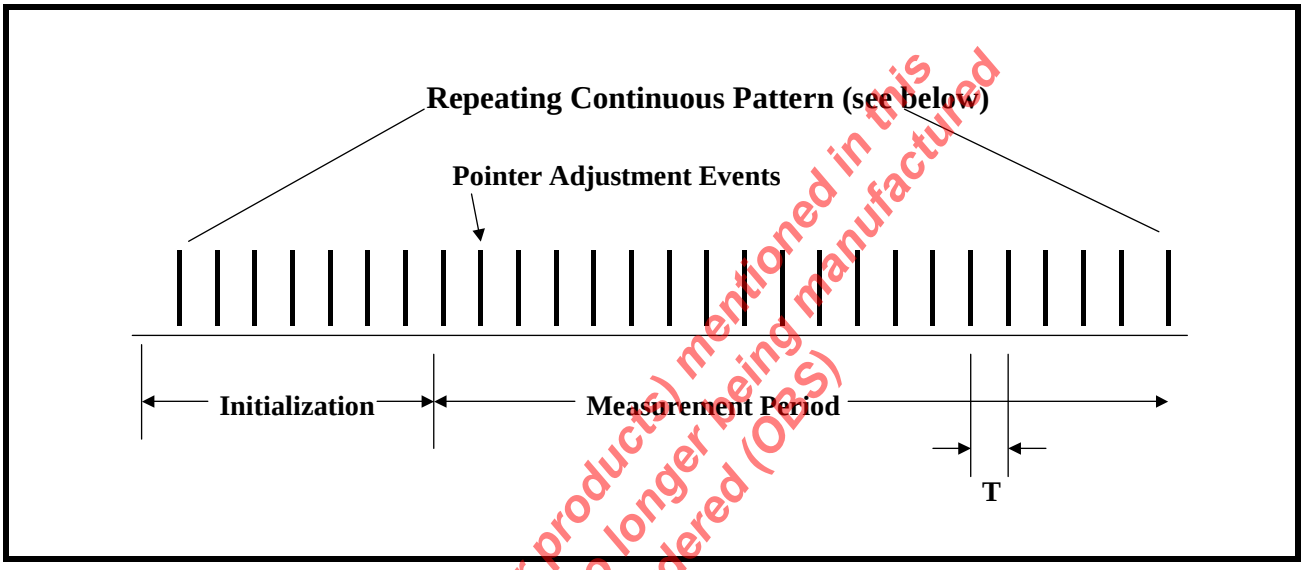
Telcordia GR-253-CORE defines an "87-3 Cancel" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 53.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.8 Continuous Pattern

Figure 54 presents an illustration of the "Continuous" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 54. ILLUSTRATION OF CONTINUOUS PERIODIC POINTER ADJUSTMENT SCENARIO

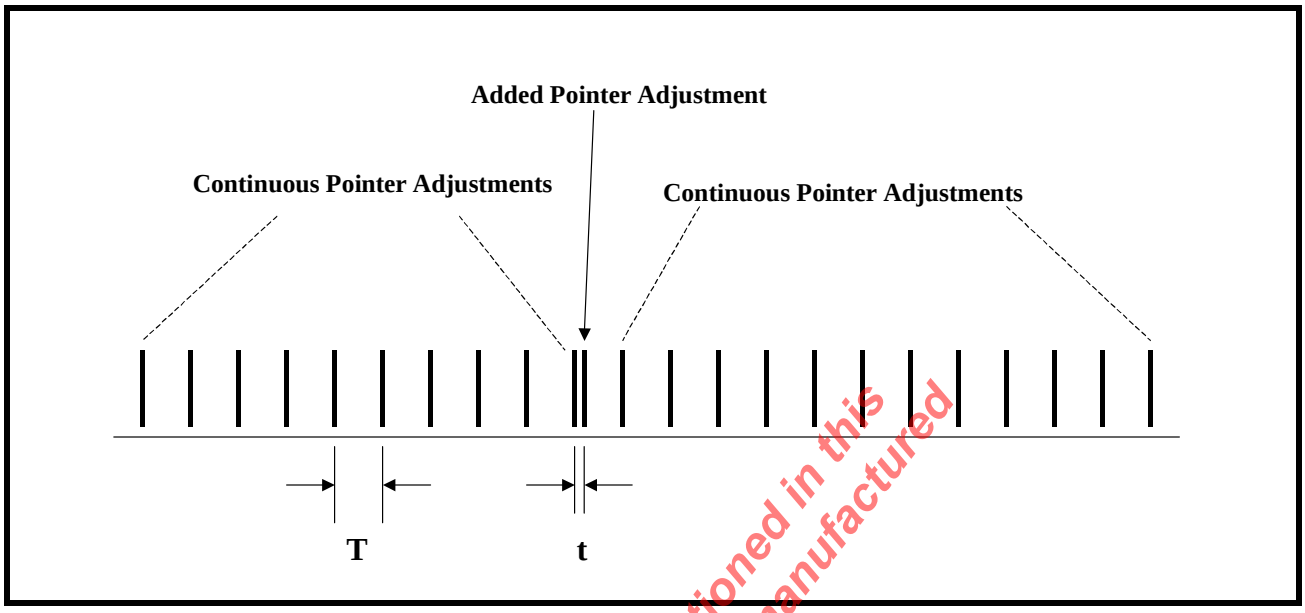


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp. The spacing between individual pointer adjustments (within this scenario) can range from 7.5ms to 10s.

9.5.9 Continuous Add

Figure 55 presents an illustration of the "Continuous Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 55. ILLUSTRATION OF CONTINUOUS-ADD POINTER ADJUSTMENT SCENARIO



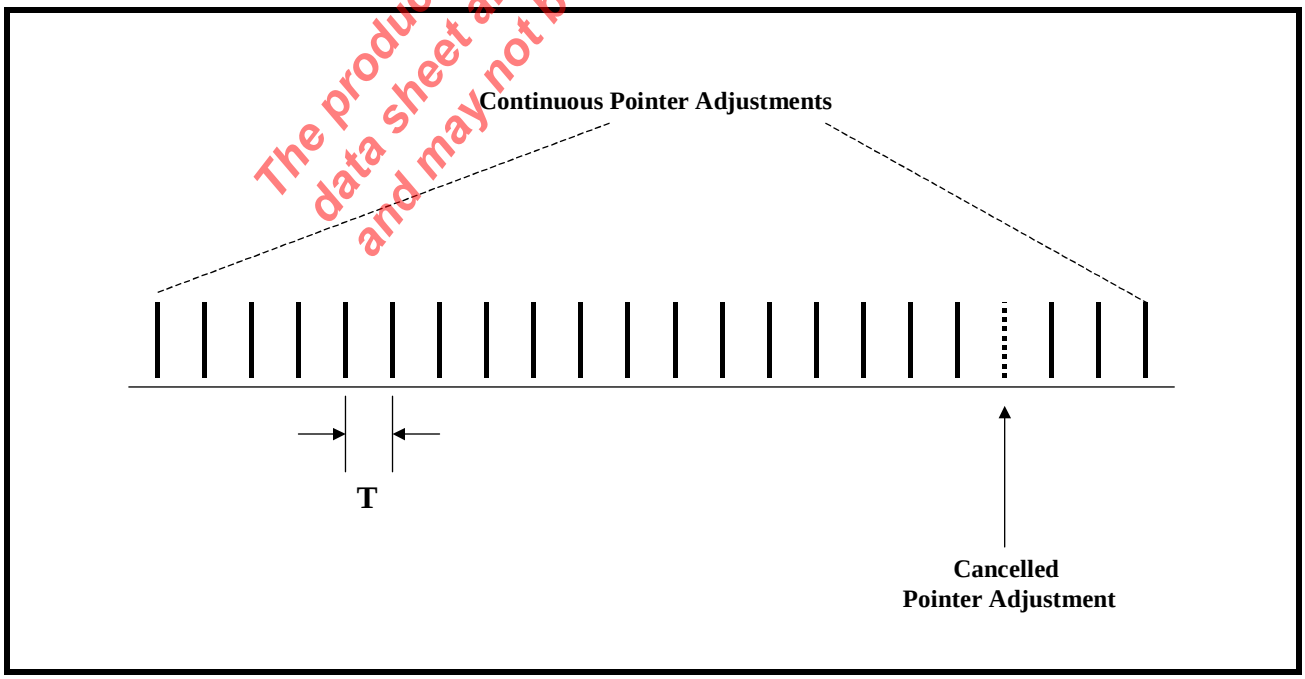
Telcordia GR-253-CORE defines an "Continuous Add" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 55.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.10 Continuous Cancel

Figure 56 presents an illustration of the "Continuous Cancel Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 56. ILLUSTRATION OF CONTINUOUS-CANCEL POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE defines a "Continuous Cancel" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 56.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.6 A Review of the DS3 Wander Requirements per ANSI T1.105.03b-1997.

To be provided in the next revision of this data sheet.

9.7 A Review of the Intrinsic Jitter and Wander Capabilities of the LIU in a typical system application

The Intrinsic Jitter and Wander Test results are summarized in this section.

9.7.1 Intrinsic Jitter Test results

The Intrinsic Jitter Test results for the LIU in DS3 being de-mapped from SONET is summarized below in Table 2.

TABLE 19: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	LIU INTRINSIC JITTER TEST RESULTS	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS
DS3 De-Mapping Jitter		0.13UI-pp	0.4UI-pp
Single Pointer Adjustment	A1	0.201UI-pp	0.43UI-pp (e.g. 0.13UI-pp + 0.3UI-pp)
Pointer Bursts	A2	0.582UI-pp	1.3UI-pp
Phase Transients	A3	0.526UI-pp	1.2UI-pp
87-3 Pattern	A4	0.790UI-pp	1.0UI-pp
87-3 Add	A5	0.926UI-pp	1.3UI-pp
87-3 Cancel	A5	0.885UI-pp	1.3UI-pp
Continuous Pattern	A4	0.497UI-pp	1.0UI-pp
Continuous Add	A5	0.598UI-pp	1.3UI-pp
Continuous Cancel	A5	0.589UI-pp	1.3UI-pp

NOTES:

1. *A detailed test report on our Test Procedures and Test Results is available and can be obtained by contacting your Exar Sales Representative.*
2. *These test results were obtained via the LIUs mounted on our XRT94L43 12-Channel DS3/E3/STS-1 Mapper Evaluation Board.*
3. *These same results apply to SDH/AU-3 Mapping applications.*

9.7.2 Wander Measurement Test Results

Wander Measurement test results will be provided in the next revision of the LIU Data Sheet.

9.8 Designing with the LIU

In this section, we will discuss the following topics.

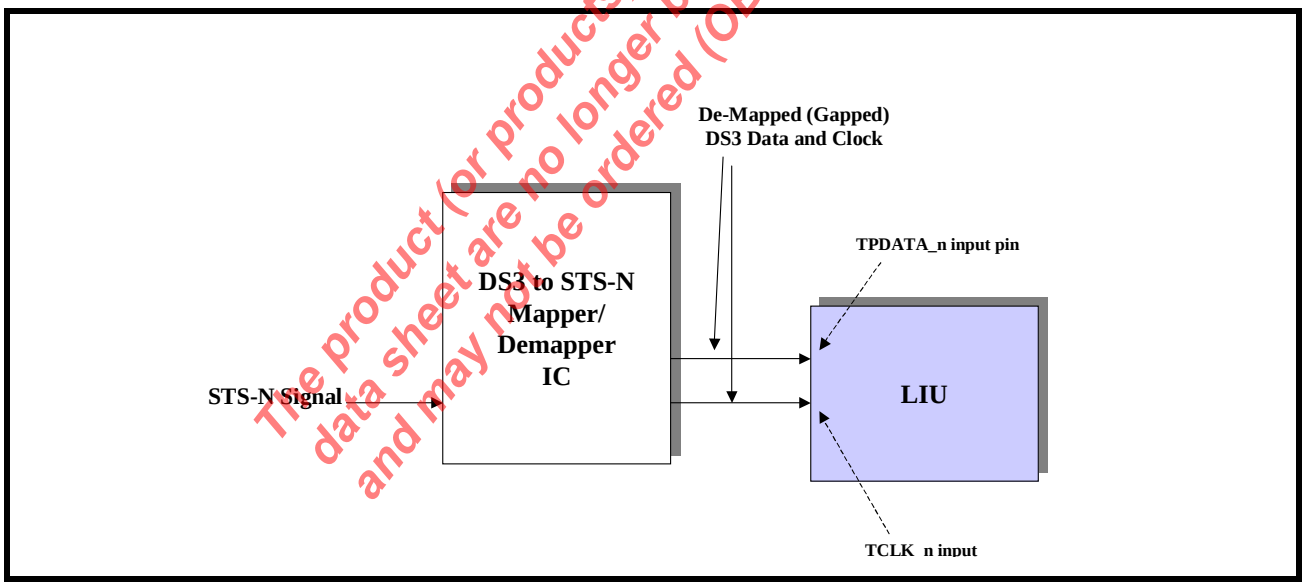
- How to design with and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements.
- How is the LIU able to meet the above-mentioned requirements?
- How does the LIU permits the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?
- How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

9.8.1 How to design and configure the LIU to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements

As mentioned earlier, in most application (in which the LIU will be used in a SONET De-Sync Application) the user will typically interface the LIU to a Mapper device in the manner as presented below in Figure 57.

In this application, the Mapper has the responsibility of receiving a SONET STS-N/OC-N signal and extracting as many as N DS3 signals from this signal. As a given channel within the Mapper IC extracts out a given DS3 signal (from SONET) it will typically be applying a Clock and Data signal to the "Transmit Input" of the LIU IC. Figure 57 presents a simple illustration as to how one channel within the LIU should be connected to the Mapper IC.

FIGURE 57. ILLUSTRATION OF THE LIU BEING CONNECTED TO A MAPPER IC FOR SONET DE-SYNC APPLICATIONS



As mentioned above, the Mapper IC will typically output a Clock and Data signal to the LIU. In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data Signal to the LIU. However, the Mapper IC typically only supplies a clock pulse via the Clock Signal to the LIU coincident to whenever a DS3 bit is being output via the Data Signal. In this case, the Mapper IC would not supply a clock edge coincident to when a TOH, POH or any non-DS3 data-bit is being output via the Data-Signal.

Figure 57 indicates that the Data Signal from the Mapper device should be connected to the TPDATA_n input pin of the LIU IC and that the Clock Signal from the Mapper device should be connected to the TCLK_n input pin of the LIU IC.

In this application, the LIU has the following responsibilities.

- Using a particular clock edge within the "gapped" clock signal (from the Mapper IC) to sample and latch the value of each DS3 data-bit that is output from the Mapper IC.
- To (through the user of the Jitter Attenuator block) attenuate the jitter within this "DS3 data" and "clock signal" that is output from the Mapper IC.
- To convert this "smoothed" DS3 data and clock into industry-compliant DS3 pulses, and to output these pulses onto the line.

To configure the LIU to operate in the correct mode for this application, the user must execute the following configuration steps.

a. *Configure the LIU to operate in the DS3 Mode*

The user can configure a given channel (within the LIU) to operate in the DS3 Mode, by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting both Bits 2 (E3_n) and Bits 1 (STS-1/DS3*_n), within each of the "Channel Control Registers" to "0" as depicted below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06
CHANNEL 1 ADDRESS LOCATION = 0X0E
CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

- **If the LIU has been configured to operate in the Hardware Mode**

The user can accomplish this by pulling all of the following input pins "Low".

Pin 76 - E3_0

Pin 94 - E3_1

Pin 85 - E3_2

Pin 72 - STS-1/$\overline{DS3}$_0

Pin 98 - STS-1/$\overline{DS3}$_1

Pin 81 - STS-1/$\overline{DS3}$_2

b. *Configure the LIU to operate in the Single-Rail Mode*

Since the Mapper IC will typically output a single "Data Line" and a "Clock Line" for each DS3 signal that it demaps from the incoming STS-N signal, it is imperative to configure each channel within the LIU to operate in the Single Rail Mode.

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode**

The user can accomplish this by setting Bit 0 (SR/DR*), within the each of the "Channel Control" Registers to 1, as illustrated below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06

CHANNEL 1 ADDRESS LOCATION = 0X0E

CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/ $\overline{\text{DS3}}$_n	SR/$\overline{\text{DR}}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie the (SR/DR*) pin to "High".

c. *Configure each of the channels within the LIU to operate in the SONET De-Sync Mode*

The user can accomplish this by executing either of the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should set Bit D2 (JA0) to "0" and Bit D0 (JA1) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the LIU has been configured to operate in the Hardware Mode**

Then the user should tie pin 44 (JA0) to a logic "HIGH" and pin 42 (JA1) to a logic "LOW".

Once the user accomplishes either of these steps, then the Jitter Attenuator (within the LIU) will be configured to operate with a very narrow bandwidth.

d. *Configure the Jitter Attenuator (within each of the channels) to operate in the Transmit Direction.*

The user can accomplish this by executing either the following steps.

- **If the LIU has been configured to operate in the Host Mode.**

Then the user should be Bit D1 (JATx/JARx*) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

- **If the LIU has been configured to operate in the Hardware Mode.**

Then the user should tie pin 43 (JATx/JARx*) to "1".

e. *Enable the "SONET APS Recovery Time" Mode*

Finally, if the user intends to use the LIU in an Application that is required to reacquire proper SONET and DS3 traffic, prior within 50ms of an APS (Automatic Protection Switching) event (per Telcordia GR-253-CORE), then the user should set Bit 4 (SONET APS Recovery Time Disable), within the "Jitter Attenuator Control" Register, to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

NOTES:

1. *The ability to disable the "SONET APS Recovery Time" mode is only available if the LIU is operating in the Host Mode. If the LIU is operating in the "Hardware" Mode, then this "SONET APS Recovery Time Mode" feature will always be enabled.*
2. *The "SONET APS Recovery Time" mode will be discussed in greater detail in "Section 9.8.3, How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?" on page 83.*

9.8.2 Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the LIU

In order to minimize the effects of "Clock-Gapping" Jitter within the DS3 signal that is ultimately transmitted to the DS3 Line (or facility), we recommend that some "pre-processing" of the "Data-Signals" and "Clock-Signals" (which are output from the Mapper device) be implemented prior to routing these signals to the "Transmit Inputs" of the LIU.

9.8.2.1 SOME NOTES PRIOR TO STARTING THIS DISCUSSION:

Our simulation results indicate that Jitter Attenuator PLL (within the LIU LIU IC) will have no problem handling and processing the "Data-Signal" and "Clock-Signal" from a Mapper IC/ASIC if no pre-processing has been performed on these signals. In order words, our simulation results indicate that the Jitter Attenuator PLL (within the LIU IC) will have no problem handling the "worst-case" of 59 consecutive bits of no clock pulses in the "Clock-Signal (due to the Mapper IC processing the TOH bytes, an Incrementing Pointer-Adjustment-induced "stuffed-byte", the POH byte, and the two fixed-stuff bytes within the STS-1 SPE, etc), immediately followed be processing clusters of DS3 data-bits (as shown in Figure 37) and still comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE for DS3 applications.

NOTE: *If this sort of "pre-processing" is already supported by the Mapper device that you are using, then no further action is required by the user.*

9.8.2.2 OUR PRE-PROCESSING RECOMMENDATIONS

For the time-being, we recommend that the customer implement the "pre-processing" of the DS3 "Data-Signal" and "Clock-Signal" as described below. Currently we are aware that some of the Mapper products on the Market do implement this exact "pre-processing" algorithm. However, if the customer is implementing their Mapper Design in an ASIC or FPGA solution, then we strongly recommend that the user implement the necessary logic design to realize the following recommendations.

Some time ago, we spent some time, studying (and then later testing our solution with) the PM5342 OC-3 to DS3 Mapper IC from PMC-Sierra. In particular, we wanted to understand the type of "DS3 Clock" and "Data" signal that this DS3 to OC-3 Mapper IC outputs.

During this effort, we learned the following.

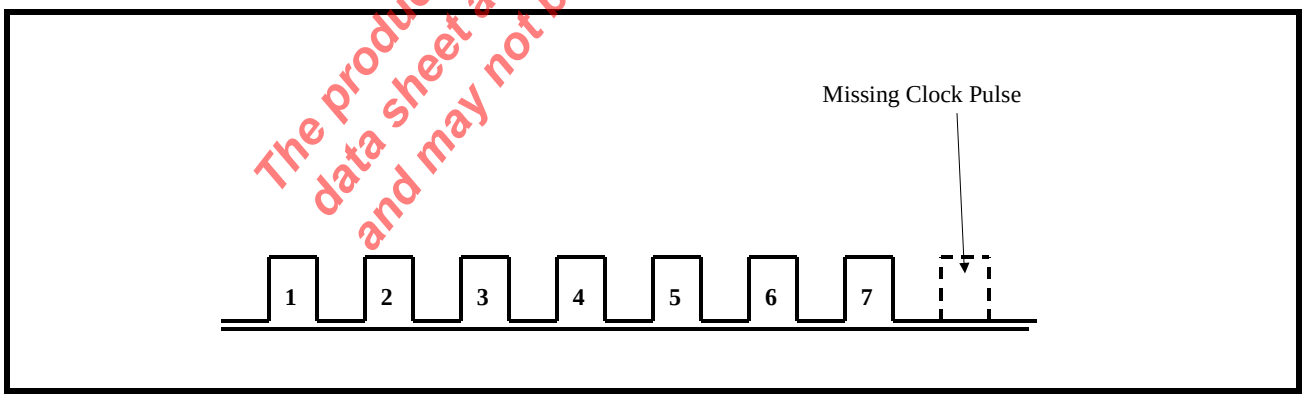
1. This "DS3 Clock" and "Data" signal, which is output from the Mapper IC consists of two major "repeating" patterns (which we will refer to as "MAJOR PATTERN A" and "MAJOR PATTERN B". The behavior of each of these patterns is presented below.

MAJOR PATTERN A

MAJOR PATTERN A consists of two "sub" or minor-patterns, (which we will refer to as "MINOR PATTERN P1 and P2).

MINOR PATTERN P1 consists of a string of seven (7) clock pulses, followed by a single gap (no clock pulse). An illustration of MINOR PATTERN P1 is presented below in Figure 58.

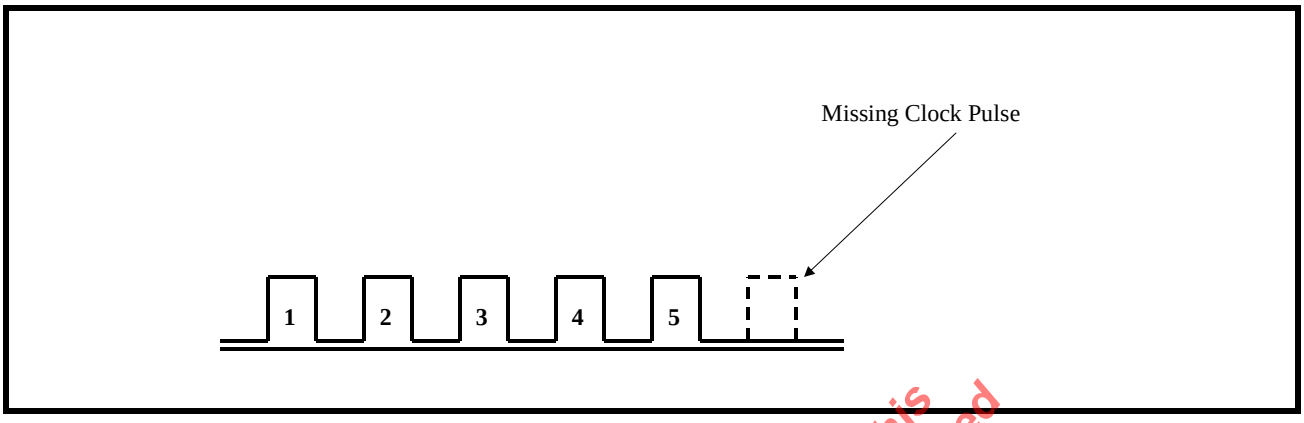
FIGURE 58. ILLUSTRATION OF MINOR PATTERN P1



It should be noted that each of these clock pulses has a period of approximately 19.3ns (or has an "instantaneously frequency of 51.84MHz).

MINOR Pattern P2 consists of string of five (5) clock pulses, which is also followed by a single gap (no clock pulse). An illustration of Pattern P2 is presented below in Figure 59.

FIGURE 59. ILLUSTRATION OF MINOR PATTERN P2



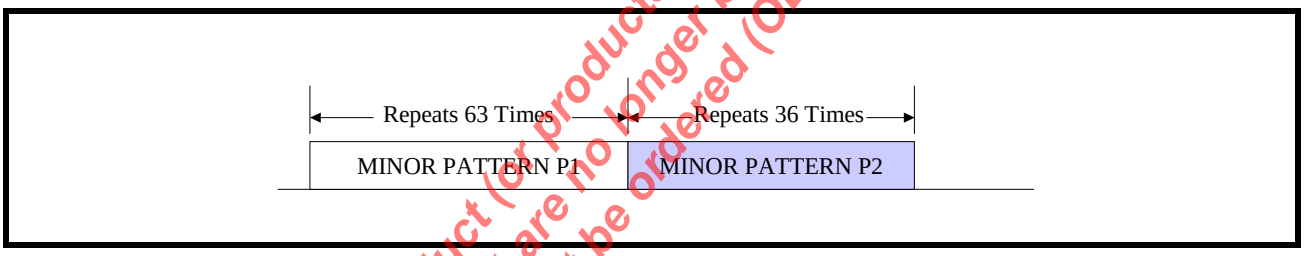
HOW MAJOR PATTERN A IS SYNTHESIZED

MAJOR PATTERN A is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.

Figure 60 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN A

FIGURE 60. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE MAJOR PATTERN A



Hence, MAJOR PATTERN A consists of "(63 x 7) + (36 x 5)" = 621 clock pulses. These 621 clock pulses were delivered over a period of "(63 x 8) + (36 x 6)" = 720 STS-1 (or 51.84MHz) clock periods.

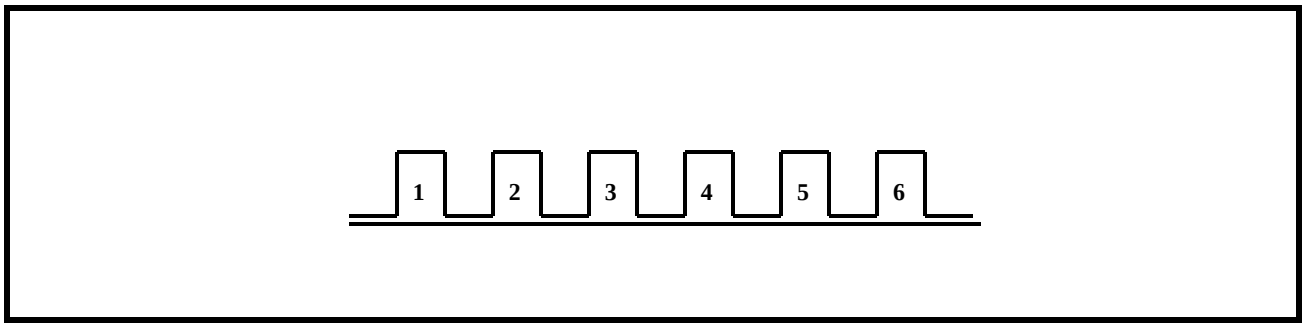
MAJOR PATTERN B

MAJOR PATTERN B consists of three sub or minor-patterns (which we will refer to as "MINOR PATTERNS P1, P2 and P3).

MINOR PATTERN P1, which is used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P1" as was presented above in Figure 30. Similarly, the MINOR PATTERN P2, which is also used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P2" as was presented in Figure 31.

MINOR PATTERN P3 (which has yet to be defined) consists of a string of six (6) clock pulses, which contains no gaps. An illustration of MINOR PATTERN P3 is presented below in Figure 61.

FIGURE 61. ILLUSTRATION OF MINOR PATTERN P3



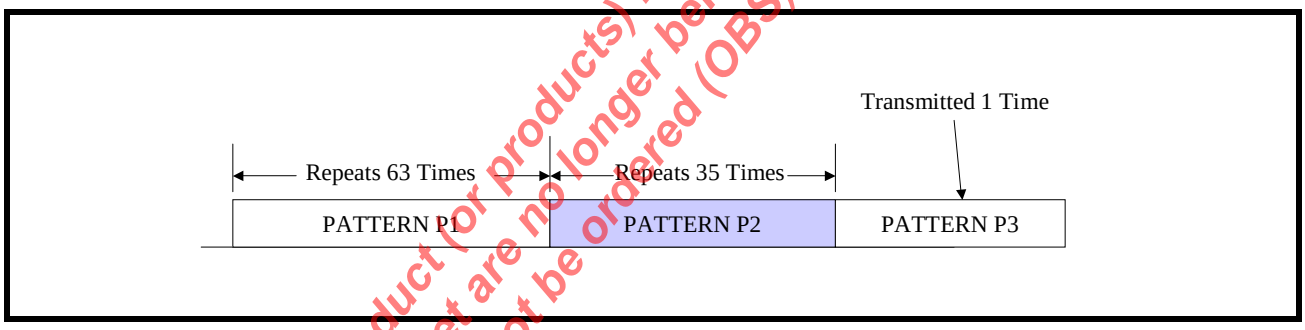
HOW MAJOR PATTERN B IS SYNTHESIZED

MAJOR PATTERN B is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.
- pon completion of the 35th transmission of MINOR PATTERN P2, MINOR PATTERN P3 is transmitted once.

Figure 62 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN B.

FIGURE 62. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE PATTERN B



Hence, MAJOR PATTERN B consists of "(63 x 7) + (35 x 5)" + 6 = 622 clock pulses.

These 622 clock pulses were delivered over a period of "(63 x 8) + (35 x 6) + 6 = 720 STS-1 (or 51.84MHz) clock periods.

PUTTING THE PATTERNS TOGETHER

Finally, the DS3 to OC-N Mapper IC clock output is reproduced by doing the following.

- MAJOR PATTERN A is transmitted two times (repeatedly).
- After the second transmission of MAJOR PATTERN A, MAJOR PATTERN B is transmitted once.
- Then the whole process repeats.

Throughout the remainder of this document, we will refer to this particular pattern as the "SUPER PATTERN".

Figure 63 presents an illustration of this "SUPER PATTERN" which is output via the Mapper IC.

FIGURE 63. ILLUSTRATION OF THE SUPER PATTERN WHICH IS OUTPUT VIA THE "OC-N TO DS3" MAPPER IC

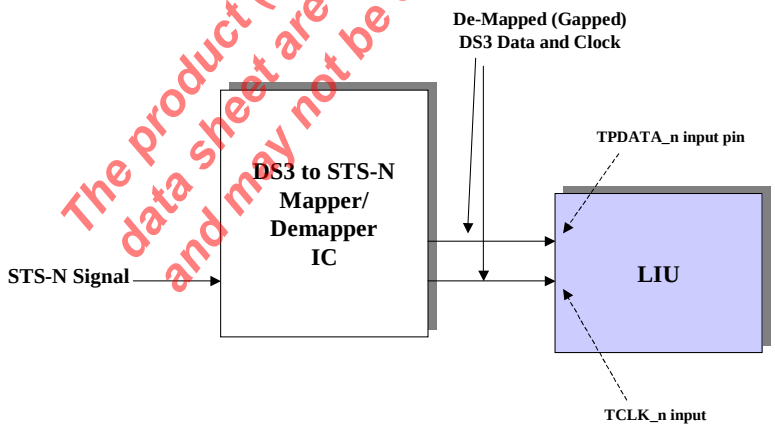
CROSS-CHECKING OUR DATA

- Each SUPER PATTERN consists of (621 + 621 + 622) = 1864 clock pulses.
- The total amount of time, which is required for the "DS3 to OC-N Mapper" IC to transmit this SUPER PATTERN is (720 + 720 + 720) = 2160 "STS-1" clock periods.
- This amount to a period of (2160/51.84MHz) = 41,667ns.
- In a period of 41, 667ns, the LIU (when configured to operate in the DS3 Mode), will output a total (41,667ns x 44,736,000) = 1864 uniformly spaced DS3 clock pulses.
- Hence, the number of clock pulses match.

APPLYING THE SUPER PATTERN TO THE LIU

Whenever the LIU is configured to operate in a "SONET De-Sync" application, the device will accept a continuous string of the above-defined SUPER PATTERN, via the TCLK input pin (along with the corresponding data). The channel within the LIU (which will be configured to operate in the "DS3" Mode) will output a DS3 line signal (to the DS3 facility) that complies with the "Category I Intrinsic Jitter Requirements - per Telcordia GR-253-CORE (for DS3 applications). This scheme is illustrated below in Figure 64.

FIGURE 64. SIMPLE ILLUSTRATION OF THE LIU BEING USED IN A SONET DE-SYNCHRONIZER" APPLICATION



9.8.3 How does the LIU permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?

Telcordia GR-253-CORE, Section 5.3.3.3 mandates that the "APS Completion" (or Recovery) time be 50ms or less. Many of our customers interpret this particular requirement as follows.

"From the instant that an APS is initiated on a high-speed SONET signal, all lower-speed SONET traffic (which is being transported via this "high-speed" SONET signal) must be fully restored within 50ms. Similarly, if the "high-speed" SONET signal is transporting some PDH signals (such as DS1 or DS3, etc.), then those entities

that are responsible for acquiring and maintaining DS1 or DS3 frame synchronization (with these DS1 or DS3 data-streams that have been de-mapped from SONET) must have re-acquired DS1 or DS3 frame synchronization within 50ms" after APS has been initiated."

The LIU was designed such that the DS3 signals that it receives from a SONET Mapper device and processes will comply with the Category I Intrinsic Jitter requirements per Telcordia GR-253-CORE.

Reference 1 documents some APS Recovery Time testing, which was performed to verify that the Jitter Attenuator blocks (within the LIU) device that permit it to comply with the Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE, do not cause it to fail to comply with the "APS Completion Time" requirements per Section 5.3.3.3 of Telcordia GR-253-CORE. However, Table 3 presents a summary of some APS Recovery Time requirements that were documented within this test report.

Table 3,

TABLE 20: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET

DS3 PPM OFFSET (PER W&G ANT-20SE)	MEASURED APS RECOVERY TIME (PER LOGIC ANALYZER)
-99 ppm	1.25ms
-40ppm	1.54ms
-30 ppm	1.34ms
-20 ppm	1.49ms
-10 ppm	1.30ms
0 ppm	1.89ms
+10 ppm	1.21ms
+20 ppm	1.64ms
+30 ppm	1.32ms
+40 ppm	1.25ms
+99 ppm	1.35ms

NOTE: *The APS Completion (or Recovery) time requirement is 50ms.*

Configuring the LIU to be able to comply with the SONET APS Recovery Time Requirements of 50ms

Quite simply, the user can configure a given Jitter Attenuator block (associated with a given channel) to (1) comply with the "APS Completion Time" requirements per Telcordia GR-253-CORE, and (2) also comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 applications) by making sure that Bit 4 (SONET APS Recovery Time Disable Ch_n), within the Jitter Attenuator Control Register is set to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: *The user can only disable the "SONET APS Recovery Time Mode" if the LIU is operating in the Host Mode. If the user is operating the LIU in the Hardware Mode, then the user will have NO ability to disable the "SONET APS Recovery Time Mode" feature.*

9.8.4 How should one configure the LIU, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

Daisy-Chain testing is emerging as a new requirements that many of our customers are imposing on our SONET Mapper and LIU products. Many System Designer/Manufacturers are finding out that whenever their end-customers that are evaluating and testing out their systems (in order to determine if they wish to move forward and start purchasing this equipment in volume) are routinely demanding that they be able to test out these systems with a single piece of test equipment. This means that the end-customer would like to take a single piece of DS3 or STS-1 test equipment and (with this test equipment) snake the DS3 or STS-1 traffic (that this test equipment will generate) through many or (preferably all) channels within the system. For example, we have had request from our customers that (on a system that supports OC-192) our silicon be able to support this DS3 or STS-1 traffic snaking through the 192 DS3 or STS-1 ports within this system.

After extensive testing, we have determined that the best approach to complying with test "Daisy-Chain" Testing requirements, is to configure the Jitter Attenuator blocks (within each of the Channels within the LIU) into the "32-Bit" Mode. The user can configure the Jitter Attenuator block (within a given channel of the LIU) to operate in this mode by settings in the table below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	0

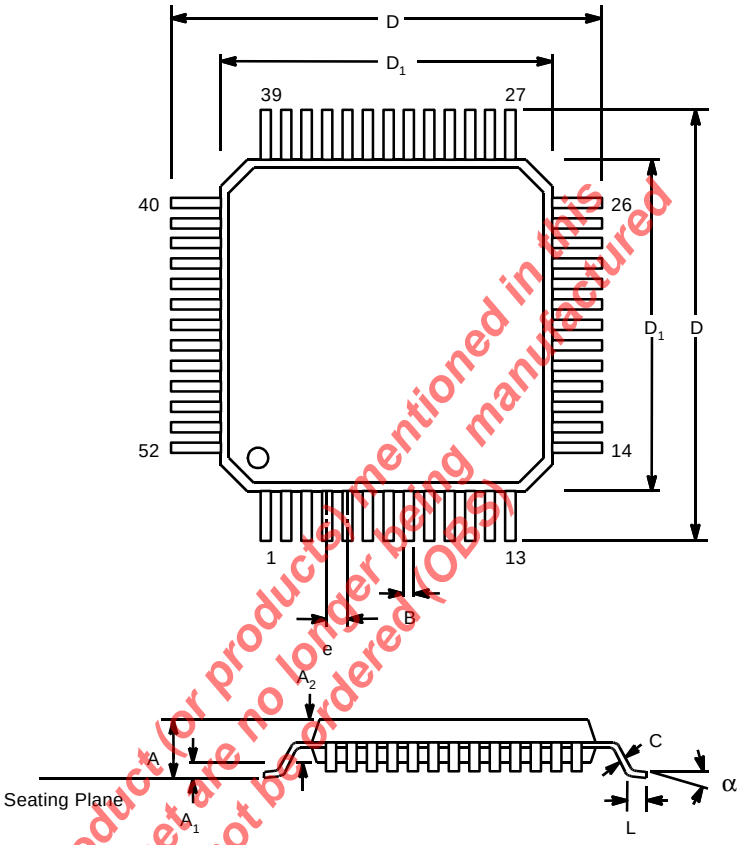
REFERENCES

1. TEST REPORT - AUTOMATIC PROTECTION SWITCHING (APS) RECOVERY TIME TESTING WITH THE XRT94L43 DS3/E3/STS-1 TO STS-12 MAPPER IC - Revision C Silicon

ORDERING INFORMATION

PART NO.	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75VL00DIV	52 Pin TQFP (10mm x 10mm)	-40℃ to +85℃

PACKAGE DIMENSIONS



Note: The control dimension is the millimeter column

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D1	0.390	0.398	9.90	10.10
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	7°typ		7°typ	
aaa	-	0.003	-	0.08

REVISION HISTORY

REVISION	DATE	CHANGES MADE
1.0.1	August 2003	Changed I_{CC} and P_{DD} in the electrical characteristics. Added a detailed section on the De-Sync feature. Removed evaluation schematic. Changed the MTIP/MRING configuration in Figure 16 (Transmit Driver Monitor Setup).
1.0.2	November 2003	Changed I_{CC} and P_{DD} in the electrical characteristics.
1.0.3	February 2004	Incorrect Pin Number references in De-Sync functional description. Added 128-bit FIFO information for the De-Sync function. Changed the device ID to reflect the correct value.
1.0.4	September 2008	Updated datasheet Headers. Corrected Figure 11 block diagram typo. Redefined t_{33} Serial Processor Interface timing.

NOTICE

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Datasheet September 2008.