APPLICATION NOTE ANP22



Filter Design in Continuous Conduction Mode

Filter Design in Continuous Conduction Mode Part 1: Buck Regulator

This white paper will show a graphical explanation of the output filter characteristics for the two basic topologies buck and boost regulators. Part 1 deals with basic Bode plots and the buck regulator filter and part 2 will deal with the boost regulator filter.

There are many items that need to be considered when it comes to designing proper compensation which includes taking a close look at the component selection and its effects, as well as the filter characteristics as related to power conversion. Although many of the topics to be discussed here have been studied in many electronics and circuits classes, this paper will try to bridge some of that into converter design and to show how the designs get affected by non ideal components. Diagram 1 shows the typical output filter for a buck and boost regulator.



The basics of output filters

One important thing to note is that all of the above voltage mode topologies when running in continuous current conduction mode have a 2nd order double pole LC filter associated with them. Thus the first thing that needs to be examined is: what does second order mean when it comes to Bode plots and compensation? In a second order equation, a single pole on the Bode plot contributes a decrease in output gain of 20db/dec and decrease in phase by 90 degrees. A single zero has the opposite effect on the output -- it will increase the gain by 20db/dec and phase will increase by 90 degrees. An LC filter double pole has two poles in the same location; thus this will decrease the gain by 40db/dec and decrease the phase by 180 degrees. The frequency at which the double pole is located is sometimes referred to the corner frequency or the break frequency. In diagram 2 the corner frequency occurs at about 15Khz.

It is important to note here that a well compensated circuit should have the gain cross zero db at a slope of -20dB with a phase margin of at least 45 degrees. Refer to application note ANP15 and ANP16 for further discussions on compensation.

http://www.sipex.com/files/ApplicationNotes/ANP%2015%20Nov20-06.pdf

http://www.sipex.com/files/ApplicationNotes/Type%20III%20Loop%20Compensation%20Oct12-06.pdf

In this document we will discuss how to help the user design output filters to help accomplish this task.



ESR Zero

Another important feature of the output filter is the equivalent series resistance (ESR) zero that is generated by the output capacitor ESR. ESR is very often talked about when choosing the type of compensation that is required to compensate the system to have a stable output. Refer to Application Note ANP18 for a good explanation of compensation types:

http://www.sipex.com/files/ApplicationNotes/ANP18%20select%20typeII%20or%20TypeIII.pdf

Corner Frequency dB/deg ESR zero at 160Khz -20- 60 -100 -140 -1801•10⁴ 1•10⁵ $1 \bullet 10^{6}$ 1•10³ Hz DIAGRAM 3: Bode plot of LC filter with ESR zero gain, of LC function in diagram 2: Solid Red:

Diagram 3 shows the addition of a zero (blue color) into the output filter.

Dashed Red:phase, of LC function in diagram 2Blue:ESR zero added to the function – solid: gain; dashed: phase.The arbitrary ESR zero occurs at a frequency of about 160K

The arbitrary ESR zero occurs at a frequency of about 160KHz. At this point the slope of the gain (solid blue) changes from -40db per decade to -20db per decade, and the phase will start to increase a decade before the zero location as can be seen here. The blue dotted line represents the phase boost created by the ESR zero.

Right Half Plane Zero (RHP)

In some topologies, a right half plane zero exists in the output filter. This zero acts as a boost for gain, thus increasing gain by 20db/dec on the Bode plot, but the phase decreases by 90 degrees. Diagrams 4a and 4b show the addition of a RHP zero (magenta color) when it is added to the Bode plot in diagram 3. The addition of the RHP zero leads to a much sharper decline in phase by another 90 degrees with a maximum decline up to -270 degrees. In this example the final phase settled out at -220 degrees.



DIAGRAM 4a: Gain Bode plot of LC filter with ESR and RHP zero

Magenta: Blue: Red:

filter with RHP, ESR zero, double pole filter with ESR zero , double pole from diagram 3 function without ESR zero or RHP zero from diagram 2



Q and damping factor

Another important feature but less talked about is the Q of the output filter. Q is a combination of inductance and capacitance as well as resistance. Q, or quality factor as it is sometimes referred to, has a damping factor (ζ) associated with it. The inductor DC Resistance (DCR) and the ESR of the output capacitor as well as the load resistance can contribute to the damping factor. The damping factor has two effects on the gain and phase of the output filter. The first is the amount of overshoot that is generated at the frequency that the filter double pole occurs. The second is the rate of change of the phase. The final phase shift is not going to change -- it is just the rate of change that is affected. Diagram 5 shows a set of graphs for a quadratic lag equation with different damping factors. Please refer to the end of this document for an explanation of lead and lag equation as referenced to Bode plots.





Black: small damping factor Red traces intermediate damping factor Green traces large damping factor For application value solutions refer to the different output filter topologies covered in this application note.

One major thing to note is how quickly the phase shifts with a smaller damping factor. The green lines show phase and gain for a larger damping factor and the black gain and phase show the values for a very small damping factor. Since the damping factor is resistive in nature, there is a constant fight between low resistance components to get better efficiency but at a possible sacrifice in phase margin. Equation 1 is a simple 2nd order quadratic expression showing where the poles and zeros are typically located in the equation.

$$Possible_Filter(\omega)\alpha \frac{(1 + ESR_zero)(1 - RHP_Zero)}{LC filterDoublepole \cdot \omega^2 + Q \cdot \omega + 1}$$
(1)

Now that the basics of the Bode plot were discussed, one other thing that needs to be kept in mind is that the phase shift will start to change a decade before the actual location of the poles or zeros.

The buck regulator

The buck regulator has the following equations associated with its output filter. These equations are generated form the open loop transfer function shown in equation 1.

$$Buck_Filter(\omega) = \frac{1 + \omega \cdot ESR \cdot C_{out}}{L \cdot C_{out} \cdot \omega^2 + Cout \cdot \zeta \cdot \omega + 1}$$
(2)

LC double pole filter occurs at frequency
$$f_{LC} = \frac{1}{2^* \pi \cdot \sqrt{L \cdot C_{out}}}$$
 (3)

ESR zero occurs at frequency
$$f_{ESR_ZERO} = \frac{1}{2^* \pi \cdot Cout \cdot ESR}$$
 (4)

Damping factor $\zeta = ESR \cdot DCR$

Q

$$Q = Cout * \zeta \tag{6}$$

(5)

The Buck regulator filter is the easiest to analyze and to generate a transfer function for. The buck regulator is the basic filter building block for output filters.



Solid Blue: Gain of buck regulator Dashed Blue: Phase of buck regulator

The Bode plot in diagram 6 is the actual representation the output filter schematic in Diagram 1a. The corner frequency or the filter double pole occurs at 15kHz; the ESR zero occurs at 160kHz.

Effects of differing values of capacitance

The next set of Bode plots look at the different effects that values will have on the Bode plot in diagram 6. Diagram 7 shows what effects the different values of output capacitance have on the filter. As the capacitance value decreases or increases there are several items to bring to attention.

1) The output filter shifts up in frequency when the capacitance is decreased from 100uF to 40uF; the difference is about 10kHz in the filter that was analyzed.

2) The overshoot on the gain plot also increases with lower capacitance and this affects the way the slope of the phase behaves as well. If all factors are constant for lower capacitance, the phase dips more and stays at –(minus)180 degrees longer. Part of the reason for this is the Q of the filter and the other part is the ESR zero.



Diagram 8 Capacitor values and their effects

Green140uF capacitor.Blue100uF capacitorMagenta80uF capacitorBlack40uF capacitorThe inductor was 1.1uH 5.5mOhms DCR, ESR was 10mOhms

Effects of differing inductor values

Even though the capacitance had effects on the output, the inductor has even more effect. This is due to the fact that inductance tends to run in tens of μ H or less. Diagram 9 shows four curves with different inductors used and their appropriate DCR values.

1) The first thing to note is the filter double pole location is inversely proportional to inductor size. Thus for high values of inductor the location of the filter double pole will shift to lower frequency. This in turn decreases the transient response; hence, this is why low values of inductor are preferred when trying to get good transient response out of buck regulators. This can be helped with compensation but it will require a large gain to shift the crossover frequency high enough to get good transient response; however, large gains in any system have many side effects including more noise sensitivity. Also large gains require a good operational amplifier that has high bandwidth which in turn will make the IC more expensive.

2) The second thing to note is the length of time that the phase stays at -180 degrees for a higher value of inductor. This is because the location of the double pole is located at a lower frequency; thus the ESR zero does not help out much with trying to boost the phase by 90 degrees. Hence the phase stays at -180 degrees for an extended period before starting to recover. It is important to note that it is the inductor DCR and capacitor ESR combination -- and output capacitance to a certain degree -- that has the negative impact on phase slope.





Blue10uH Inductor 30.4mOhmMagenta6.8uF Inductor 19.8mOhmBlack1.0uF Inductor 3.3mOhmGreen.82uF Inductor 2.6mOhmThe capacitor was 100uF .01mOhm ESR

Effects of differing ESR values

ESR is very commonly discussed in the compensation schemes in many data sheets. Below in diagram 10 it shows the effects of differing values of ESR, keeping in mind that the inductor and the output capacitance did not change. Out of all of the component characteristics, ESR is the value that can vary the most without much difference to the capacitance. For example, electrolytic capacitors and tantalum capacitors tend to have higher values of ESR and it is not uncommon that those values are in the hundreds of mOhms. On the other side of the spectrum, the ceramic capacitors have extremely low values of ESR in the tens of mOhms and lower. There are several things that need to be observed about ESR and its effects on the Bode Plot. ESR zero occurs at frequency $f_{ESR_ZERO} = \frac{1}{2 * \pi \cdot Cout \cdot ESR}$ (Equation 4)

- 1 The capacitor ESR not only contributes to the ESR zero but also contributes significantly to the damping factor in the quadratic equation of the filter. For an ESR of .001 Ohms, the green color representing the phase margin decline is so steep that the phase hits -180 degrees and stays there for a whole decade until the ESR zero starts having some effect on the phase plot. This type of system is very hard to compensate, since the compensation scheme will need to have significant boost in phase right at the corner frequency without much margin for error due to the fact that the slope of phase shift occurs very quickly.
- 2 On the other hand, a large value of ESR has very soothing effects on the output filter. For example, there is very little overshoot on the gain Bode plot diagram for ESR value of .04 ohms and higher in the output filter that was analyzed. As an example for an ESR of .1, the output phase has a gentle slope and the phase only reaches -90 degrees since the ESR zero cancels out one of the filter double poles and never lets the phase reach -180 degrees. The drawback of a high ESR capacitor is that to have low ripple and good transient response, the output filter needs to have lower ESR values.

Refer to Application Note ANP18 for compensating a buck converter and choosing compensation type: http://www.sipex.com/files/ApplicationNotes/ANP18%20select%20typeII%20or%20TypeIII.pdf



Considerations in the filter design

From the analysis done in the previous pages for a buck regulator, it can be seen clearly the effects that different variables have on the output filter when it comes to phase and gain Bode plots. So what does this mean in the real world of output filter design? There are several things that a designer needs to consider when designing the output stage of a buck converter.

The first thing to consider is the inductor choice. Inductor value controls the amount of ripple current that the output capacitor will see.

$$L = \frac{V_{out} \cdot (V_{in}_{max} - V_{out})}{V_{in} \cdot f_s \cdot I_{out} * K_r}$$
(6)

Typically the ripple current (K_r) is about 30% of the total output current, although this is not "written in stone" and depending on other requirements it may vary. For example, if the user wants to run a non synchronous converter in continuous conduction current mode, the ripple current needs to be $\frac{1}{2}$ the minimum output current desired. If the user wants to run extremely high currents it might be desirable to have a very small value of inductance greater than 30% so that the inductor DCR stays small, in which case the inductor can carry a high current. It is also desirable to have a small inductor value when a high transient response is required, since the filter double pole is at a higher frequency which was shown in diagrams 9 and 12.

The other consideration is the choice of ESR in the output filter design. Other than for stability criteria, ESR also has an effect on transient and output ripple. The main contributor to output ripple is ESR.

$$ESR = \frac{V_{ripple_pp}}{Iripple}$$
(7)

The total output ripple is

$$\Delta Vout = \sqrt{\left(\frac{Iripple \cdot (1-D)}{fs \cdot Cout}\right)^2 + (Iripple \cdot ESR)^2}$$
(8)

From formula 7 and 8 it is desirable to have a low ESR capacitor to have a good output ripple voltage. Also, the dip in the output voltage during a transient load step is created by the ESR, if sufficient capacitance exists on the output to cover the load step condition.

Typically, but not always, once the designer chooses the inductor, then the output capacitors are chosen to fulfill output ripple requirements. At this point the designer will need to make some choices. There might be other limitations which are imposed such as size, but typically the output capacitors should be chosen to try to help the design with the compensation as well. Below are some guidelines to help with output capacitor selection.

1 If the inductor has a large value of inductance due to the desired outcome of a small ripple current, the output capacitors should be of higher ESR values as well as lower capacitance values if possible. This is due to a couple of aspects of the output filter. One aspect is the lower value of capacitance will try to push out the output filter double pole in frequency, thus giving better transient response. Secondly, the larger value of ESR of the capacitor will help with phase shift slope as well as give the buck regulator a needed phase boost to help with the final compensation. But since the ripple current is smaller with higher inductor values, the higher value of ESR still should deliver a good output ripple.

Example 1A:

For a design with Vout of 3.3V, Vin of 28V, and Iout of 3A with a low output voltage ripple requirement of about 50mV, the inductor is about 10uH with .96A ripple current for a switching frequency of 300Khz.



DIAGRAM 11: Bode Plot for Example 1A

Blue	capacitor value of 100uF with 10 mili-ohms ESR
Magenta	capacitor 68uF capacitor with 50 mili-ohms ESR.

As can be seen from the above example, it will be easier to compensate the output filter with capacitor values of 68uF having 50 m Ω ESR. This still satisfies the ripple requirements and also helps with phase margin, since the ESR zero starts to have an effect earlier thus helping boost the phase. Also, the compensation gain for a good transient response does not have to be as high for filters that already have a higher corner frequency, in order to get a good crossover frequency in the system. Lower gain that needs to be created by the error amplifier has two benefits; one, it helps with noise immunity and the other is with the slew rate of the error amplifier.

2 Low inductor values are desirable for a fast transient response since the filter double pole should be located as high as possible in the frequency. The actual design of this output stage tends to be centered on the output capacitors and the inductor is then selected. Below is an example of a design using five $100 \text{uF} \cdot 005\Omega$ capacitors in parallel with one solution using 2.2uH inductor and the other solution with a .47uH inductor. It can be clearly seen that the output filter which has a higher LC double pole frequency occurs with a lower inductor value. Since in this case a high crossover frequency is desirable, using a lower inductor value contributes to this significantly.



DIAGRAM 12: Output filter with 2.2uH inductor and .47uH inductor



One note of mention is that high transient response circuits are difficult to compensate in general. One reason is that the ESR zero occurs at such high frequency that it does not contribute anything to the phase at the filter double pole where the phase shift occurs. The other reason is that the damping factor of the filter is also very low, generating a rather steep decline in phase.

In conclusion of part 1, the basics of the output filter were discussed using graphs to help the user with visualization of the gain and phase. The buck regulator output filter was also discussed in detail and the effects of components on the output filter. It was also shown that making certain component choices can help in filter design, which can later help with the overall compensation of the buck regulator. In part two; the boost regulator filter will be analyzed.

Terms, Definitions

Lead Network: In a lead network the phase shift of the output leads the phase shift of the input. The phase is represented by a shift of 90 degrees in the positive direction

Lag network : The phase shift of the output lags the phase shift of the input. An example this is a simple RC network.

Explanation of the graph scaling



dB/deg

Where the phase and gain are graphed on the same graph, the X axis was scaled so that both traces are visible. The solid line will represent gain in db and dotted line will represent phase in degrees.

Hz

The frequency is in Hz, unless otherwise noted.

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