XR78020

20A Integrated Power Stage "DrMOS" with Current and Temperature Monitoring

General Description

The XR78020 is an integrated power stage containing a synchronous buck gate driver which is packaged with both half bridge MOSFETs designed to provide output currents up to 20Amps. Also known as "DrMOS" (Driver plus MOSFETs), the package design provides very low thermal impedance and excellent EMI performance by minimizing parasitic inductances. The ratio of the MOSFET $R_{DS(ON)}$ is optimized for conversions from 12V rails to the low output voltages required for the latest processor and memory of computing systems.

Computing systems are demanding more and more telemetry of the power system. The XR78020 monitors internal temperature (TOUT pin) and uses that temperature information to provide a temperature corrected current output (IOUT pin) derived from the inductor DCR. The output current information has minimal phase delay and is suitable for use with current mode PWM and valley current mode constant on-time control.

TOUT serves the secondary function of a fault flag for V_{CC} UVLO, Over-Temp fault, High-Side short fault or OC fault. The XR78020 is offered in a 4 x 5 x 0.9mm QFN package.

FEATURES

- 20A Integrated Power Stage
- Input Voltage Range: 4.5V to 17V
- Output Voltage Range: 0.6V to 3.3V
  - 0.6V to 5.5V without current sense
- IMON output 5mV/A (DCR=0.29mohm) with temperature compensation
  - Suitable for current mode control loops
  - Trimmed and tested at 65°C
- TOUT output 8mV/°C with fault flags for V_{CC} UVLO, OTP, OCP, High-Side Short
- Designed for 3.3V tristate PWM outputs
- Boost pin refresh
- 4 x 5 x 0.9mm RoHS compliant package

APPLICATIONS

- Servers
- Networking Equipment
- Industrial PC

Ordering Information - Back Page

Typical Application

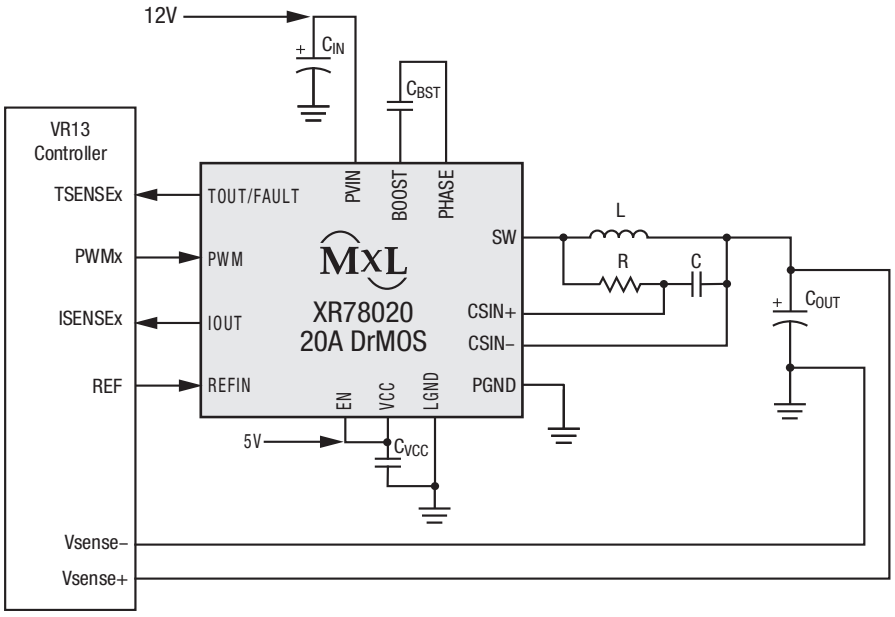


Figure 1: Typical Application Circuit

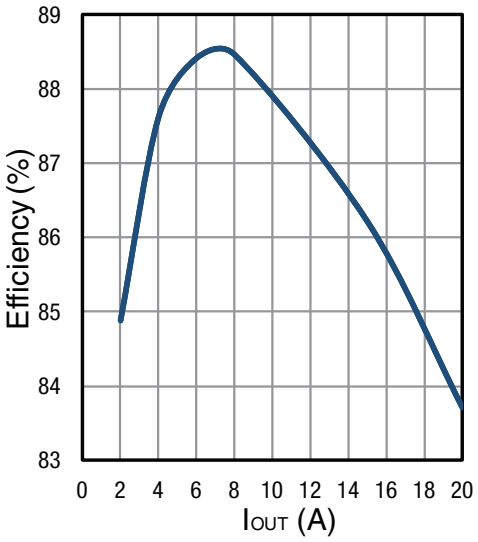


Figure 2: Efficiency $12V_{IN}$ $1V_{OUT}$ 600kHz

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition may affect device reliability and lifetime.

PV_{IN} ..... -0.3V to 25V

SW, PHASE..... -1V to 25V[2]

V_{CC} ..... -0.3V to 6V

BOOST[1] ..... -0.3V to 29V

PWM, IOUT, GATEL, EN, TOUT .....-0.3V to V_{CC}+0.3V

CSIN–, CSIN+ .....-0.3V to V_{CC}+0.3V

REFIN..... -0.3V to 3.5V

Storage Temperature Range..... -65°C to 150°C

Peak Package Body Temperature..... 260°C

MSL 2

ESD rating (HBM – Human Body Model) 2kV

ESD rating (CDM – Charged Device Model) 750V

Operating Conditions

V_{CC} .....4.25V to 5.5V

PV_{IN} .....3V to 17V

SW..... -1V to 17V[2]

V_{CC}, EN ..... -0.3V to 5.5V

CSIN–, CSIN+ ..... -0.3V to 3.3V

Switching Frequency ..... up to 1500kHz

Junction Temperature Range (T_J) ..... -40°C to 125°C

JEDEC51 Package Thermal Resistance Θ_{JA}.....24.2°C/W

Thermal Resistance, Θ_{JCBOT} ..... 4.9°C/W

Note 1: No external voltage applied

Note 2: SW pin's DC range is -1V, transient is -5V for less than 50ns.

Electrical Characteristics

Specifications are for Operating Junction Temperature of T_J = 65°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 65°C, and are provided for reference purposes only. Unless otherwise indicated, PV_{IN}=12V, V_{CC}=5V.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
DC Specifications							
V_{VCC}	V_{CC} input range		•	4.25	5.0	5.5	V
$I_{q_}$DC	Non-switching quiescent current	EN = Vcc, PWM floating				5.1	mA
$I_{q\_shutdown}$	Shutdown quiescent current	EN = 0V				300	uA
$I_{q\_leakage}$	PV_{IN} leakage current in tri-state	EN = 5V, PWM = Tri-state			0.1		uA
V_{UVLO}	V_{CC} UVLO Threshold	V_{CC} rising		3.5	3.7	3.9	V
V_{UVLO_HYST}	V_{CC} UVLO Hysteresis	V_{CC} falling			300		mV
EN Input							
V_{IH_EN}	Logic level high, chip enabled			2			V
V_{IL_EN}	Logic level low, chip shutdown					0.8	V
t_{DLY_ENH}	Delay EN transitions from 0 to 1				4.4		us
t_{DLY_ENL}	Delay EN transitions from 1 to 0				37	45	ns
R_{PLD_EN}	Enable pull down resistance				570		kΩ
PWM Input							
V_{IH_PWM}	Logic level high			2.5			V
V_{IL_PWM}	Logic level low					0.8	V
V_{PWM_HYST}	PWM hysteresis	Active to tristate or tristate to active		80	110	140	mV
V_{TRI_PWM}	Tristate voltage measured on PWM	PWM = FLOAT		1.4	1.65	1.8	V
R_{IN_PWM}	PWM input resistance	EN = HIGH			8		kΩ
t_{PD_IH}	PWM high propagation delay	PWM logic low → high to SW high			40		ns
t_{PD_IL}	PWM low propagation delay	PWM logic high → low to SW low			40		ns
$t_{PD\_IL\_TRI}$	PWM low to tristate propagation delay	PWM logic low → tristate to GL falling			25	45	ns
$t_{PD\_TRI\_IH}$	PWM tristate to high propagation delay	PWM tristate → logic high to SW >1V			25		ns
t_{MIN_ONTIME}	Minimum on-time measured at SW	15ns < PWM Input < 30ns			40		ns
t_{MIN_PWM}	Minimum pulse width resulting in no output pulse				15		ns

Electrical Characteristics (continued)

Specifications are for Operating Junction Temperature of T_J = 65°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 65°C, and are provided for reference purposes only. Unless otherwise indicated, PV_{IN}=12V, V_{CC}=5V.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
TOUT Output							
V_{TOUT_SLOPE}	Temperature sense slope	0°C ≤ T_J ≤ 125°C		7.8	8.0	8.2	mV/°C
$T_{SNSOFFSET}$	Temperature sense offset (65°C)			1.108	1.120	1.132	°C
I_{TOUT_SOURCE}	TOUT source current	TMON driven down 2%			22		mA
I_{TOUT_SINK}	TOUT sink current	TMON driven up 2%			75		uA
R_{PLD_TOUT}	TOUT pull down resistance				30		kΩ
V_{TOUT_IH}	TOUT fault level high	HSS, OC or TEMP fault active		2.6	3.3	3.6	V
I_{TOUT_SC}	TOUT short circuit source current	TOUT = 0V		5			mA
V_{TOUT_IL}	TOUT fault level low	V_{CC} UVLO fault active. HSS, OC or TEMP fault inactive. No external pullup.			1	280	mV
Current Monitor (IMON) Specifications							
I_{BIAS_CSIN}	CSIN+ and CSIN– input bias current			-100	±1	100	nA
V_{OS_CSIN}	Input referred offset voltage	CSIN+ = CSIN– = REFIN; Measure Input Referred Offset from REFIN		-450		450	uV
$G_{65°C\_IMON\_TRIM}$	Gain of IMON amplifier (at trim)[1]	T_J = 65°C, V_{CC} = 5V, V_{REFIN} = 1.2V, V_{OUT} = 1.2V		14.85	15.0	15.15	V/V
$G_{65°C\_IMON}$	Gain of IMON amplifier[2]	T_J = 65°C, V_{CC} = 5V, V_{REFIN} = 1.2V, V_{OUT} = 1.2V		14.5	15.0	15.5	V/V
$G_{27°C\_IMON}$	Gain of IMON amplifier	T_J = 27°C, V_{CC} = 5V, V_{REFIN} = 1.2V, V_{OUT} = 1.2V			17.25		V/V
f_{UNITY_IMON}	Unity Gain Bandwidth of IMON signal path	C_{IOUT}=10pF			10		MHz
t_{DELAY}	IMON propagation delay				90		ns
S_R	Slew rate of IOUT				4		V/us
V_{ICM_CSIN}	Common mode input voltage range	V_{CC} = 4.25V		0		2.5	V
V_{ICM_CSIN}	Common mode input voltage range	V_{CC} ≥ 5.0		0		3.3	V
I_{SINK_IOUT}	IOUT sink current	V_{IOUT} - V_{REFIN} rises 2% from 150mV		1.2	1.5		mA
I_{SOURCE_IOUT}	IOUT source current	V_{IOUT} - V_{REFIN} falls 2% from 150mV		1.4	5.1		mA
Fault Flags – High-Side Short (HSS), Temperature, Over-Current							
V_{HSS_TRIP}	High-side short trip threshold	PWM = tristate. Threshold measured at PHASE pin with PHASE voltage rising			3.5		V
t_{PROP_HSS}	High-side short propagation delay					3	µs
V_{OC_TRIP}	Over current trip threshold	Measured between REFIN and IOUT	•	164	180		mV
$N_{OC\_TO\_FAULT}$	Number of PWM input clock cycles to set OC flag	IOUT – REFIN > V_{OC_TRIP}			10		Cycles
T_{OT_HIGH}	Over temperature rising trip threshold				140		°C
T_{OT_LOW}	Over temperature hysteresis				25		°C
BOOST UVLO and C_{BOOST} Refresh – High Side Gate Drive							
$V_{BOOST\text{-}SW\_START}$	Gate voltage required to start switching	Voltage rising			3.5		V
$V_{BOOST\text{-}SW\_HYST}$	UVLO hysteresis				200		mV
$V_{BOOST\text{-}SW\_REFRESH}$	Gate voltage required to activate C_{BOOST} refresh	Voltage falling, PWM = Tristate > 5us			3.5		V
$V_{REFRESH\_HYST}$	C_{BOOST} Refresh Hysteresis	Voltage rising, PWM = Tristate > 5us			200		mV

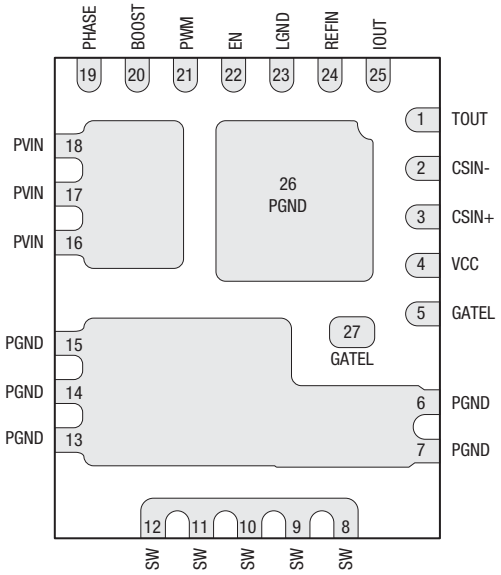
Electrical Characteristics (Continued)

Specifications are for Operating Junction Temperature of T_J = 65°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Typical values represent the most likely parametric norm at T_J = 65°C, and are provided for reference purposes only. Unless otherwise indicated, PV_{IN}=12V, V_{CC}=5V.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
High-Side MOSFET							
BV_{DSS}	Drain to source breakdown voltage	V_{GS} = 0V		30			V
$R_{DS(ON)}$	Drain to source on resistance	T_J = 25°C			4.7		mΩ
		T_J = 65°C, V_{CC} = 5V			5.6		mΩ
Low-Side MOSFET							
BV_{DSS}	Drain to source breakdown voltage	V_{GS} = 0V		30			V
$R_{DS(ON)}$	Drain to source on resistance	T_J = 25°C			2.9		mΩ
		T_J = 65°C, V_{CC} = 5V			3.4		mΩ

NOTES:
1. Trimmed at final test to an accuracy of better than ±1% at 65°C.
2. These limits represent those attainable at QA inspection due to reproducibility and repeatability guard bands.

Pin Configuration



Bottom View, 4mm x 5mm x 0.9mm QFN

Pin Functions

Pin Number	Pin Name	Description
1	TOUT/ FAULT	The voltage at this pin is defined by the equation 8mV * (Celsius Temperature) + 0.6V. This pin will be pulled low under an UVLO condition. This pin will be pulled to 3.3V when an Over Temp fault, High-Side Short fault or OCP fault ($V_{IMON} - V_{REFIN} > 150mV$) is detected.
2	CSIN-	Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
3	CSIN+	Non-inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
4	VCC	Bias voltage for BOTH control logic and gate drivers. This VCC pin is monitored by an UVLO circuit. Connect a high quality low ESR 2.2µF X6S 10V 0402 ceramic capacitor.
5, 27	GATEL	Synchronous MOSFET driver pins that can be connected to a test point in order to observe the waveform.
8-12	SW	Switch node of synchronous buck converter.
6, 7, 13-15, 26	PGND	Power grounds of the synchronous MOSFET and also the MOSFET drivers.
16-18	PVIN	High current input voltage connection. Recommended operating range is 4.5V to 17V. Connect at least two 10uF 1206 ceramic capacitors and a 0.1uF 0402 ceramic capacitor. Place the capacitors as close as possible to PVIN pins and PGND pins (pin 15). The 0.1uF 0402 capacitor should be on the same side of the PCB as the XR78020.
19	PHASE	The internal switch node dedicated for Bootstrap capacitor connection.
20	BOOST	Bootstrap capacitor connection. Connect a 0.22µF capacitor from BOOST to PHASE (pin 19). The bootstrap capacitor provides the charge to turn on the control MOSFET.
21	PWM	Tri-State PWM input: “High” turns control MOSFET on; “Tri-state” turns both MOSFETs off; “Low” turns the synchronous MOSFET on. Body braking and diode emulation can be controlled by placing the PWM input to tri-state. 3.3V logic level PWM input and VCC tolerant.
22	EN	Pulling EN high enables the driver; pulling EN low disables the driver and enter low-quiescent current mode. Floating this pin is not recommended. However a low current pull-down is embedded to keep the driver off if the pin is floating. Pin is VCC tolerant.
23	LGND	Signal ground. All signals are referenced to this pin.
24	REFIN	Reference voltage input from the PWM controller. IOUT signal is referenced to the voltage on this pin. Connect to LGND if the current sense amplifier is not used.
25	IOUT	Current output signal. Voltage on this pin is equal to V_{REFIN} + Gain * ($V_{CSIN+} - V_{CSIN-}$). Float this pin if the current sense amplifier is not used. Gain = 15 @ 65°C, Gain = 17.25 @ 27°C

Typical Performance Characteristics

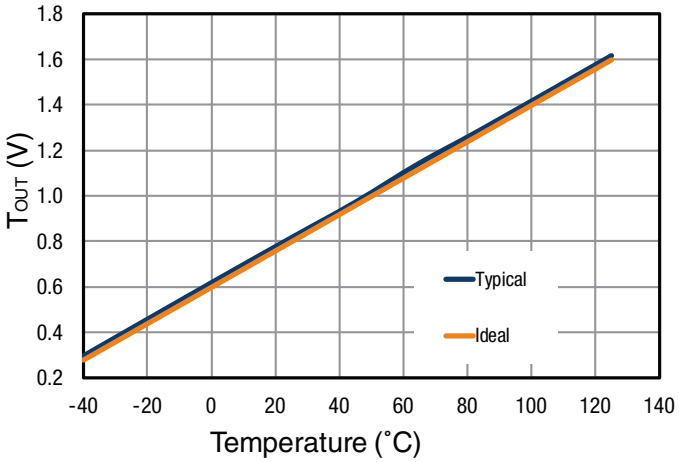


Figure 3: TMON Output vs. Ideal

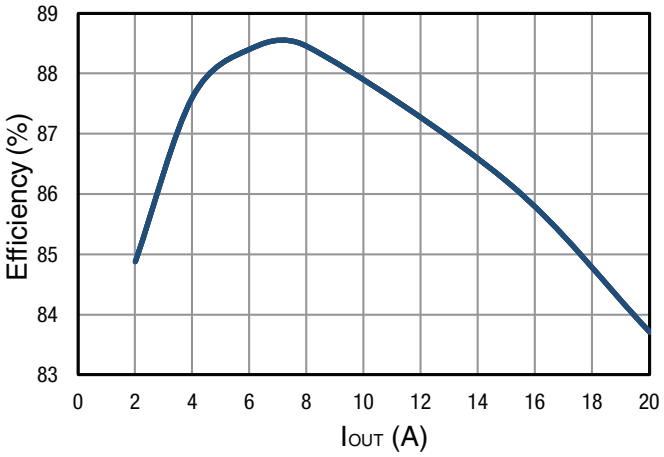


Figure 4: Efficiency – 12Vin, 1Vout, 600kHz

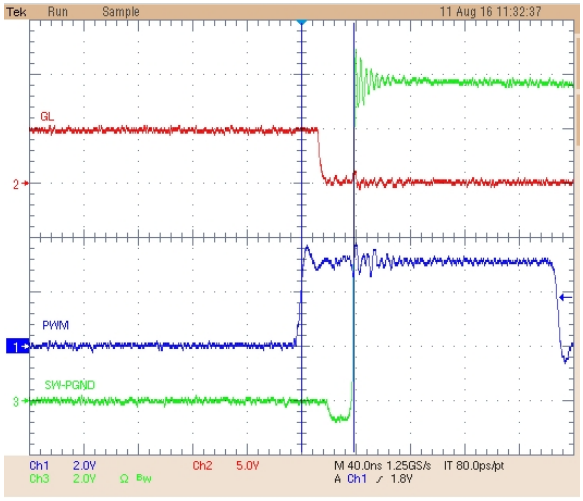


Figure 5: PWM High to SW Delay

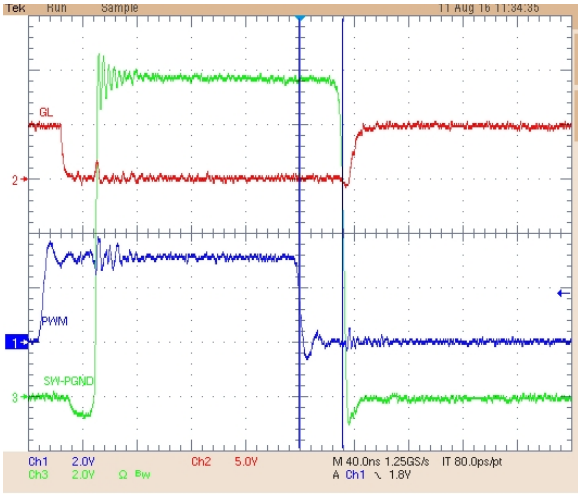


Figure 6: PWM Low to SW Delay

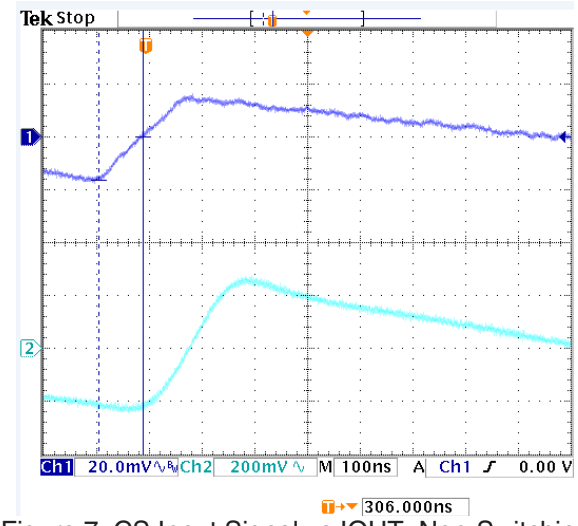


Figure 7: CS Input Signal vs IOUT, Non-Switching

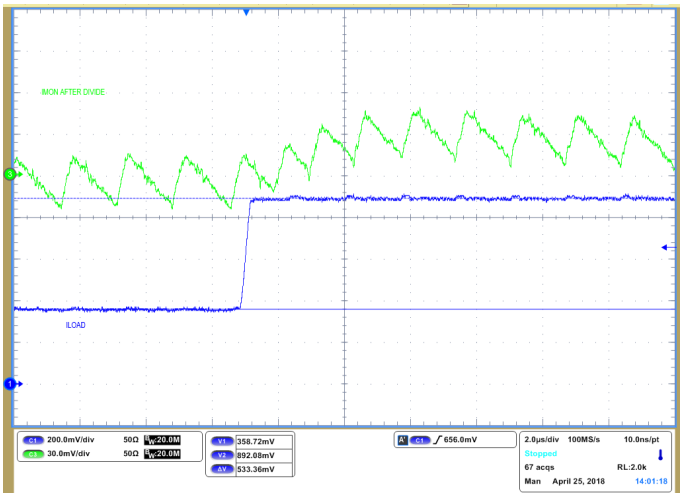


Figure 8: CS Input Signal vs IOUT
(2.5V output, 1A - 8A load, L = 470nH,
using TI TPS53658 controller on HPE G10 DL380 board)

Functional Block Diagram

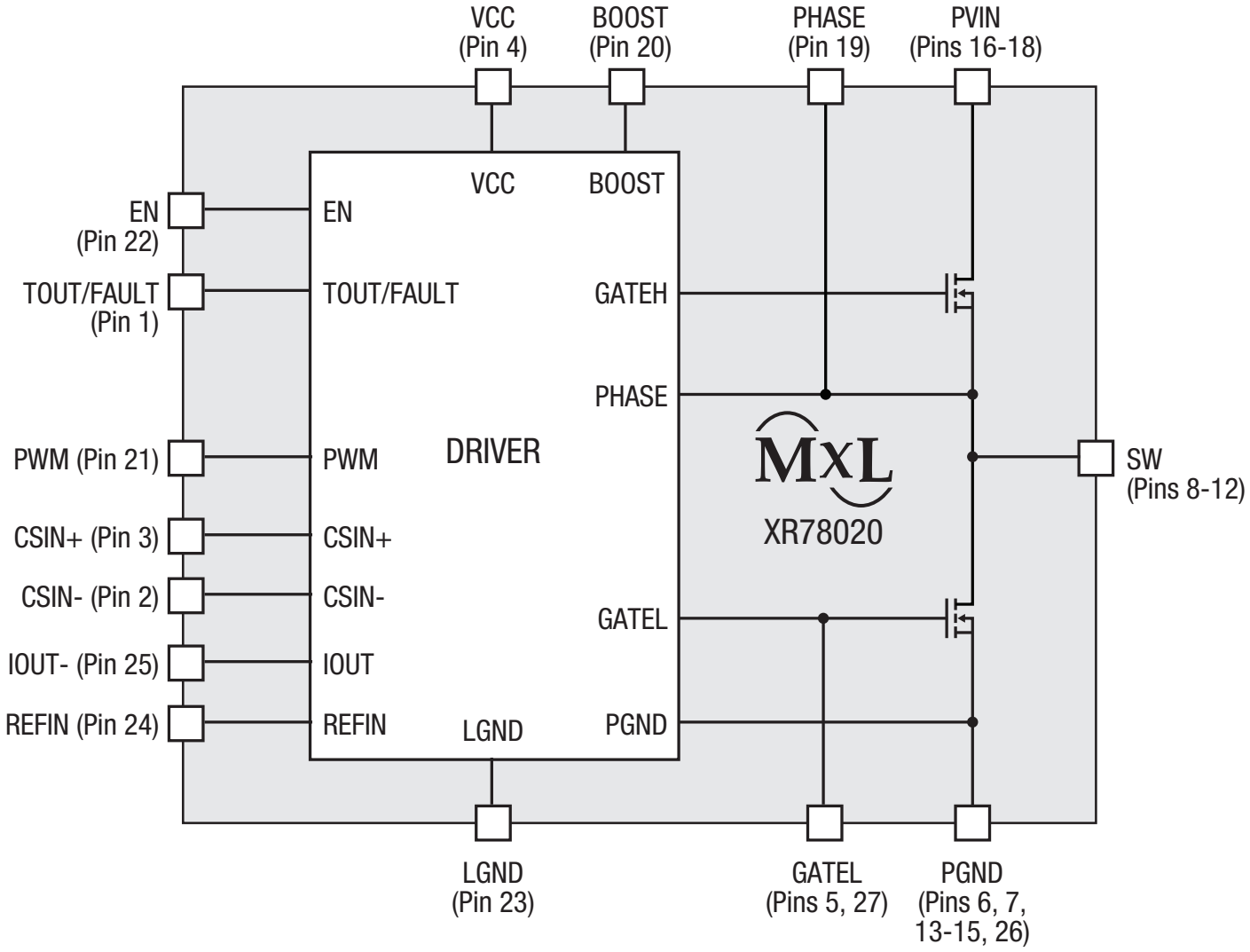


Figure 9: High Level Block Diagram

Functional Block Diagram, continued

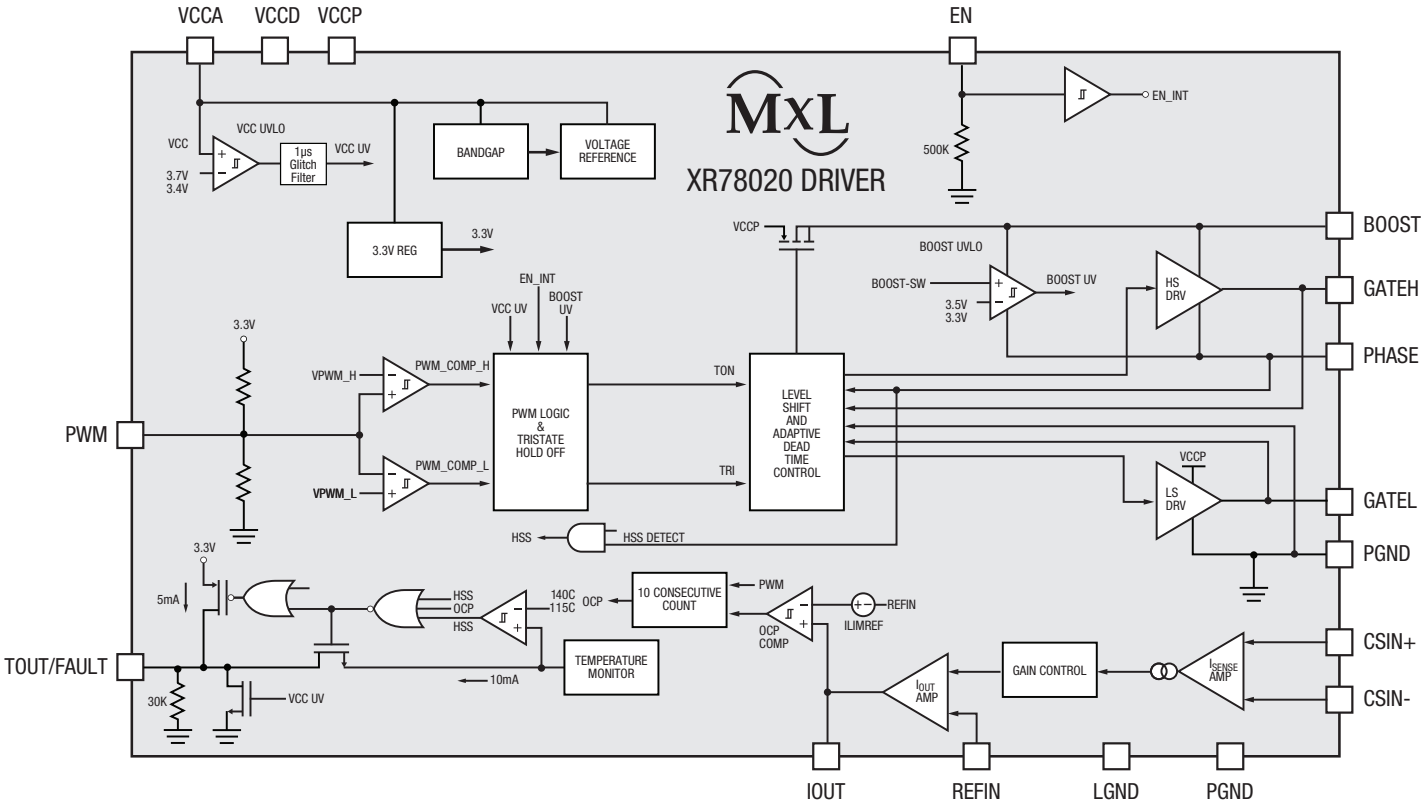


Figure 10: Driver Detailed Block Diagram

Applications Information

Functional Description

The XR78020 is a 20A “DrMOS” (Driver plus MOSFETs) integrating a high speed, MOSFET driver IC and a pair of Power MOSFETs in a half bridge configuration which can operate up to 1.5MHz.

The XR78020 incorporates an accurate, high speed Current Sense Amplifier (CSA) optimized for use with inductor DCR sensing and achieves spot on inductor current sensing and reporting for use by the PWM Controller. The CSA provides noise immunity along with temperature compensated signal gain to compensate for DCR change with temperature. The sensed current information is referenced to the REFIN pin and is available at IOUT pin as an equivalent voltage.

The XR78020 provides real-time temperature monitoring and reporting output along with fault reporting of Over-Temperature (OT), Over-Current (OC), High-Side Short (HSS) and VCC under voltage via the TOUT/FAULT pin. When the temperature exceeds 140°C, temperature reporting ceases and pulls the TOUT/FAULT pin high to flag OT. Once the temperature drops below 115°C, the fault is disabled and temperature reporting continues on the TOUT/FAULT pin. OC and HSS faults also pull the TOUT/FAULT pin high whereas VCC UV pulls the TOUT/FAULT pin low.

The XR78020 monitors the voltage between BOOST and PHASE and automatically refreshes the voltage across the bootstrap capacitor if it is in tristate longer than a preset duration. This feature avoids gradual depletion of the bootstrap capacitor voltage when the power stage stays in tristate for long periods of time.

The EN pin supports deep sleep mode whereby if the EN pin is pulled low, the XR78020 shuts down most of the internal circuits and the driver, thereby drawing less than 200µA of quiescent current.

The PWM input pin is a 3.3V logic input with tristate feature and is VCC tolerant.

PWM Input and Tri-State

The PWM Input receives the PWM control signal from the controller IC. The PWM input is designed to be compatible with standard controllers using two-state logic (HIGH and LOW) and advanced controllers that incorporate “tristate” logic (HIGH, LOW and TRISTATE). When the PWM input is high, the control MOSFET is turned on and the synchronous MOSFET is turned off. When the PWM input is low, the control MOSFET is turned off and the synchronous MOSFET is turned on. If the PWM input is floated, the XR78020 will force the PWM into tristate with a nominal 1.65V. Both MOSFETs are turned off and the SW node will tristate.

Current Sensing and Reporting (IMON)

The current sensing/reporting circuit is called IMON in this datasheet. IMON monitors the instantaneous inductor current using DCR sensing across the CSIN+ and CSIN- pins, gains up this signal by 17.25V/V at 27°C, level shifts up by voltage at REFIN and drives the IOUT pin. In other words:

$$[V_{IOUT} - V_{REFIN}](V) = 17.25(V/V) \times I_L(A) \times DCR(\Omega)$$

REFIN is commonly connected to a controller reference voltage.

DCR sensing is implemented by placing an R-C across the inductor and monitoring the voltage across the C (Figure 11). Inductor current I_L results in a voltage across the DCR which is given by $V = I_L \times DCR$. If the inductor time constant is matched (i.e., $RC = L/DCR$), then voltage across C matches $I_L \times DCR$ in magnitude and phase.

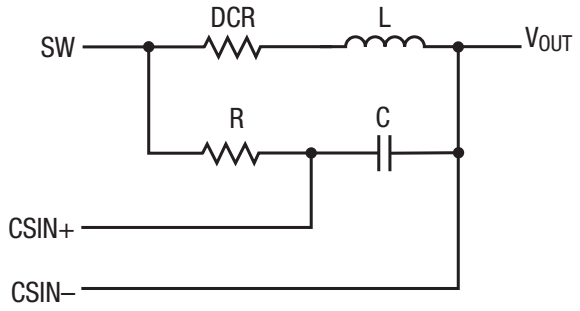


Figure 11: DCR Sensing

As an example consider a 0.33uH-0.29mΩ inductor. The inductor time constant is 0.33uH / 0.29mΩ = 1138us. Let C = 0.22uF, then calculate R = 1138us / 0.22uF = 5173Ω. Now the voltage across C should match magnitude and phase of I_L x DCR. If inductor current I_L = 1A then

V_{IOUT}-V_{REFIN} = 1A x 0.29mΩ x 17.25V/V = 5mV

Therefore the IMON amplifier will produce a 5mV/A signal when DCR = 0.29mΩ. Gain of the IMON is temperature compensated in order to compensate for DCR increase as a function of temperature (Figure 12). In other words IMON will output 5mV/A regardless of operating temperature, when DCR=0.29mΩ.

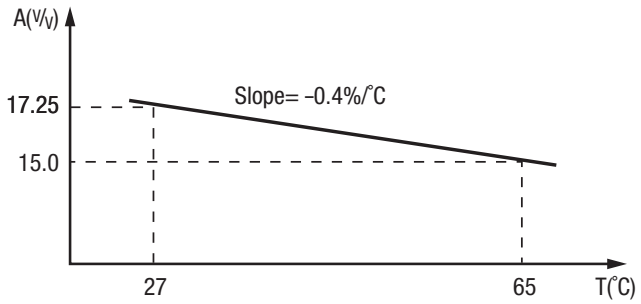


Figure 12: IMON Gain Versus Temperature

If it is required to have IMON output of 5mV/A with a DCR > 0.29mΩ, then a voltage divider must be used. This can be implemented by placing a voltage divider across L as shown in Figure 13. Calculate R1 from:

R1 =R / ((DCR / 0.29mΩ) - 1)

Where R=10kΩ nominal.

To match inductor's time constant, calculate C from:

C = (L / DCR) ((R + R1) / (R1 x R))

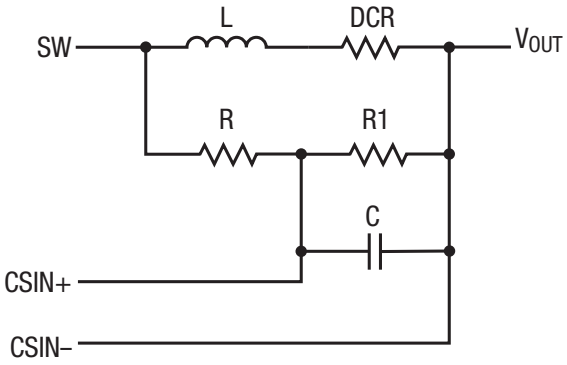


Figure 13: Voltage Divider Across the Inductor

Temperature Sensing And Reporting (TOUT/FAULT)

XR78020 has an integrated internal temperature sensing circuit that produces a linear voltage slope of 8mV/°C with a 0.6V offset at 0°C. This linearly varying voltage is available at the TOUT/FAULT pin under normal operating conditions.

The voltage at TOUT/FAULT pin during temperature reporting is given as:

$V_{TOUT/FAULT}$ (V) = 0.6V + (Temperature in °C X 0.008V/°C)

Therefore at a die temperature of 65°C,

$V_{TOUT/FAULT}$ (V) = 0.6V + (65°C X 0.008V/°C) = 1.12V

A typical graph of TOUT versus temperature is shown in Figure 3. In a multi-phase system, the TOUT/FAULT pins of several XR78020 can be connected together to create a system in which the highest temperature on the bus will drive the bus.

Fault Sensing And Reporting (TOUT/FAULT)

Following faults are constantly monitored and flagged via the TOUT/FAULT pin: VCC under-voltage VCC UVLO, Over-Current OC, Over-Temperature OT and High-Side Short HSS.

The VCC UVLO circuit monitors the VCC input. During power up, the MOSFETs are held off until VCC reaches 3.7V nominal. If at any time VCC drops below 3.4V nominal, the MOSFETs are turned off and a VCC UVLO fault is flagged by pulling the TOUT/FAULT low.

The Over Current comparator monitors the differential signal between IOUT and REFIN, which is a real time representation of the inductor current I_L. The voltage V_{IOUT} - V_{REFIN} is equal to I_L (A) x 5mV/A. The OCP comparator monitors this signal and if the comparator trips over 10 consecutive PWM cycles, then OCP triggers and pulls the TOUT/FAULT pin high.

The Over-Temperature circuit monitors the driver temperature and if it exceeds 140°C, the TOUT/FAULT pin is pulled high. The TOUT/FAULT pin resumes temperature monitoring once the junction temperature falls below 115°C.

The High-Side Short circuit is active during power up and if it detects a short across the control FET, it pulls the TOUT/FAULT pin high.

Boost UVLO and Refresh

The Boost UVLO circuit monitors the voltage between BOOST and SW. During power up, V_{BOOST} - V_{SW} must reach 3.5V before the control FET is allowed to switch. If at any time V_{BOOST} - V_{SW} drops below 3.3V, the control FET is turned off.

The BOOST refresh circuit is activated if PWM stays in tristate and V_{BOOST} - V_{SW} drops below 3.3V. The refresh circuit will then apply short GL pulses to the synchronous FET until V_{BOOST} - V_{SW} reaches 3.5V.

Bootstrap Capacitor (C_{BST})

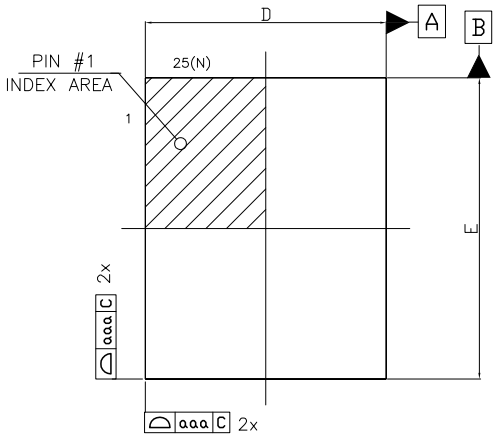
Use a high quality 0.22uF capacitor as close to PHASE and BOOST pins as possible.

VCC Decoupling Capacitor (CVCC)

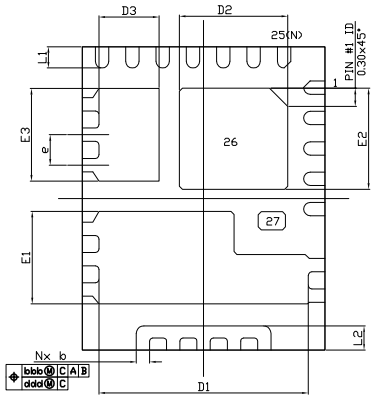
Use a minimum of 2.2uF high quality ceramic capacitor. Place as close as possible to VCC and LGND, and route with low impedance traces.

Mechanical Dimensions

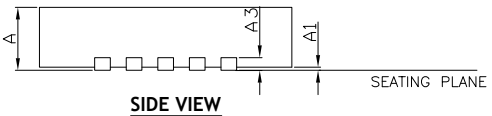
4mm x 5mm x 0.9mm QFN



TOP VIEW



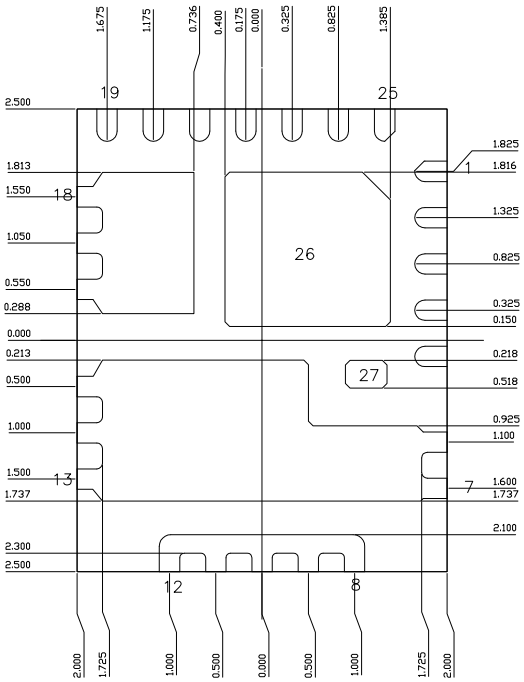
BOTTOM VIEW



SIDE VIEW

Dimension Table				
Thickness / Symbol	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20Ref	---	
b	0.20	0.25	0.30	
D		4.00 BSC		
E		5.00 BSC		
e		0.50 BSC		
D1	3.350	3.450	3.550	
E1	1.424	1.524	1.624	
D2	1.685	1.785	1.885	
E2	1.566	1.666	1.766	
D3	0.889	0.989	1.089	
E3	1.425	1.525	1.625	
L1	0.25	0.35	0.45	
L2	0.30	0.40	0.50	
aaa		0.15		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		25		

TERMINAL DETAILS



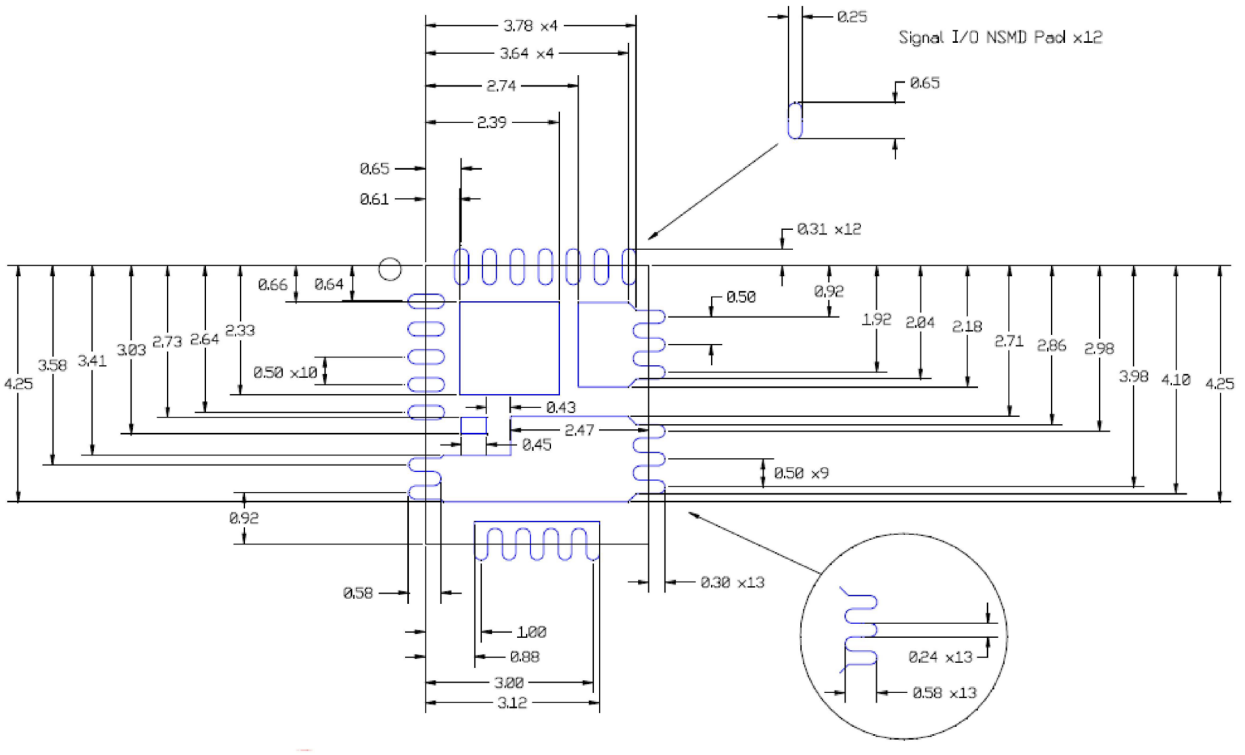
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000085

Revision: B.1

Recommended Land Pattern and Stencil

4mm x 5mm x 0.9mm QFN



Metal and component placement

PCB COPPER

NOTE 1 : LEAD LAND WIDTH SHOULD BE EQUAL TO NOMINAL PART LEAD WIDTH.

NOTE 2 : MINIMUM LEAD SPACE TO SPACE SHOULD BE >/= 0.2mm TO PREVENT SHORTING.

NOTE 3 : LEAD LAND LENGTH SHOULD BE EQUAL TO MAXIMUM PART LEAD LENGTH +0.15 -0.3mm
OUTBOARD EXTENSION AND 0 TO +0.05mm INBOARD EXTENSION.
THE OUTBOARD EXTENSION ENSURES A LARGE AND VISIBLE TOE FILLET AND THE
INBOARD EXTENSION WILL ACCOMODATE ANY PART MISALIGNMENT AND ENSURE A FILLET.

NOTE 4 : CENTER PAD LAND LENGTH AND WIDTH SHOULD BE EQUAL TO MAXIMUM PART PAD LENGTH
AND WIDTH. BUT, MIN 0.2mm SPACE AMONG PADS SHOULD BE KEPT TO PREVENT SHORTING.

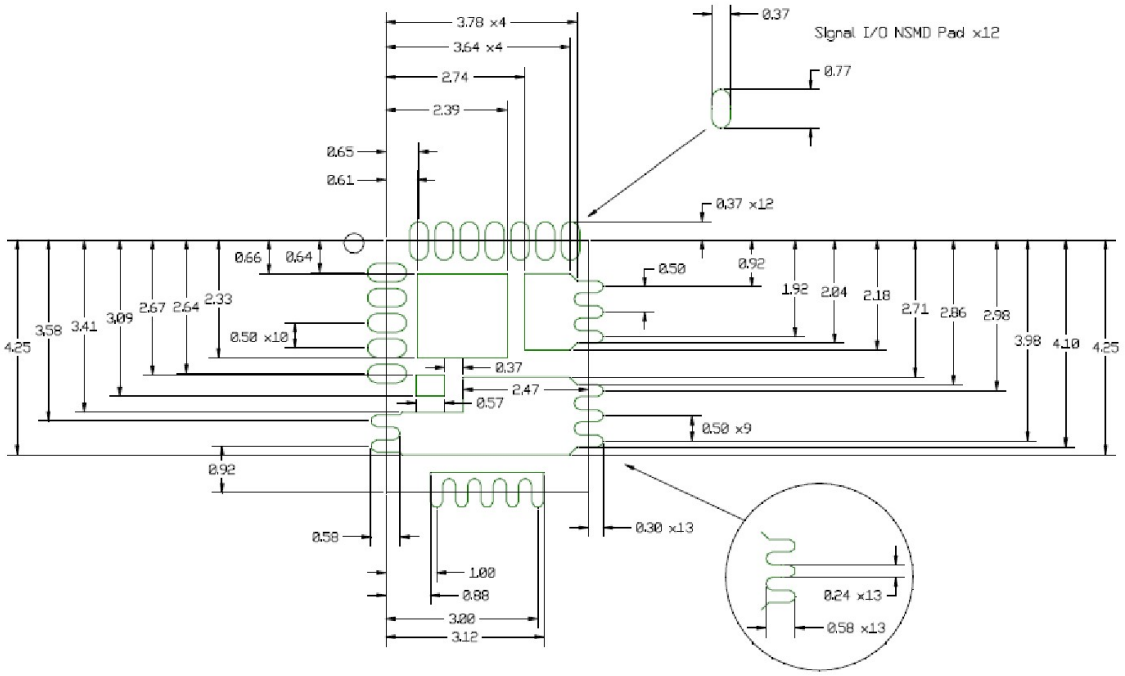
NOTE 5 : ONLY 0.15~0.3mm DIAMETER VIA SHALL BE PLACED IN THE AREA OF THE POWER PAD LANDS
AND CONNECTED TO POWER PLANES TO MINIMIZE THE NOISE EFFECT ON THE IC AND
TO IMPROVE THERMAL PERFORMANCE.

Drawing No.: POD-00000085

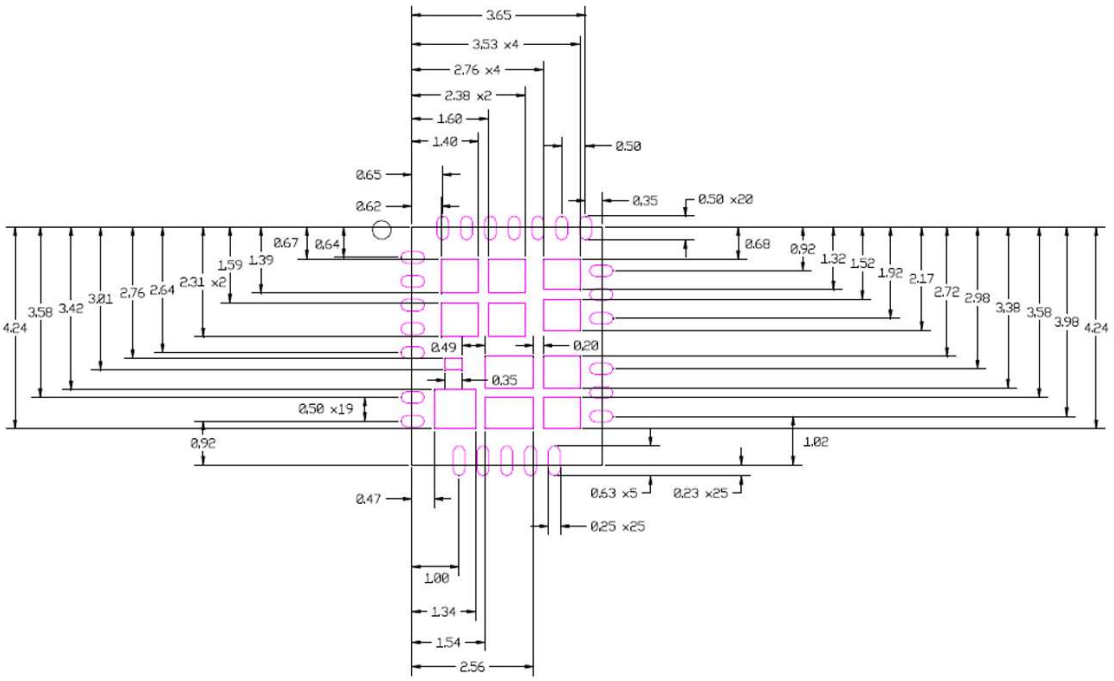
Revision: B.1

Recommended Land Pattern and Stencil, Continued

4mm x 5mm x 0.9mm QFN



PCB SOLDER MASK



TYPICAL RECOMMENDED STENCIL DESIGN

Drawing No.: POD-00000085

Revision: B.1

Ordering Information

Part Number	Operating Temperature Range	Lead-Free	Package	Packaging Method
XR78020ELTR-F	-40°C ≤ T_J ≤ 125°C	No(1)	4mm x 5mm x 0.9mm QFN	Reel

NOTE:
1. RoHS Compliant with 7(a) Exemption taken. Lead based die adhesive is used between the die and the leadframe.

Revision History

Revision	Date	Description
1A	September 2017	Initial Release
2A	October 2018	Limits updated based upon extensive process corner lot simulations as discussed with HPE supply chain as part of the qualification process for G10. IMON Gain specifications updated and line added based on conversations with HPE engineering. There is no change to the end product. Added $T_{SNSOFFSET}$ per HP specification. Updated Figure 7 and added Figure 8.
2B	October 2019	Update pin 25 description and correct labels in Figure 11.

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