APPLICATION NOTE ANP4

CAD Layout Recommendations for the PowerBlox™ Family

Introduction

The Sipex PowerBlox™ family of parts offers designers a very high power density solution for wide input range buck requirements. As a result of down converting power that can be greater than 50W in a 7 x 4 mm package, care is needed with the layout in order to manage the thermal requirements. In addition, the 26 pin DFN package selected for its excellent thermal performance must be used in conjunction with the correct CAD shape, to ensure good solder-ability during the manufacturing stage. This application note will address these, along with more general layout issues.

General Layout Recommendations.

As with all dc to dc designs, good layout practice is essential to getting the correct operation and expected performance from a solution. Below is a list of guidelines for the PowerBlox™ family:

1) A typical application circuit is shown in figure 1. All components in the power path should be located on one side (which will be referred to as the topside) of the PCB, and as physically close as possible to the PowerBlox™ device. For PowerBlox™ designs these components are: Input Capacitors (connected between Vin and PGnd – C1 in Figure 1); Output Capacitors (connected between Vout and PGnd – C3); Inductor (L1); PowerBlox™ (SP765x) device. Note: If an additional Schottky diode and/or snubber network is used connected between LX and Pgnd, these should also be subject to the same constraints.

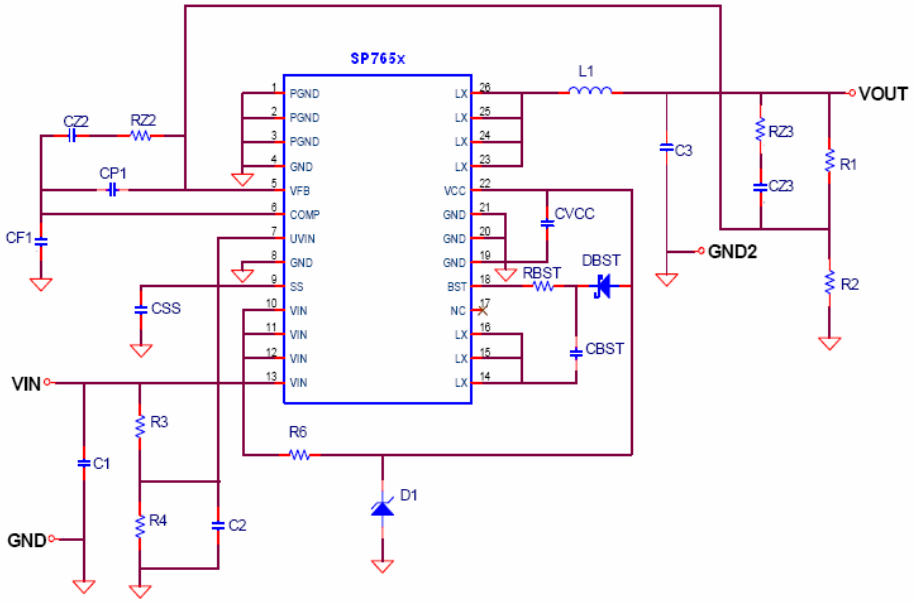

Figure 1 Typical PowerBlox™ Circuit

2) All routing to and from the above components should be done on the topside of the PCB. The routing should be done by making local split topside planes for Vin, Vout, Pgnd and LX or copper fills between the components (see example in Figure 2). Note: The use of vias in the power path is to be avoided.

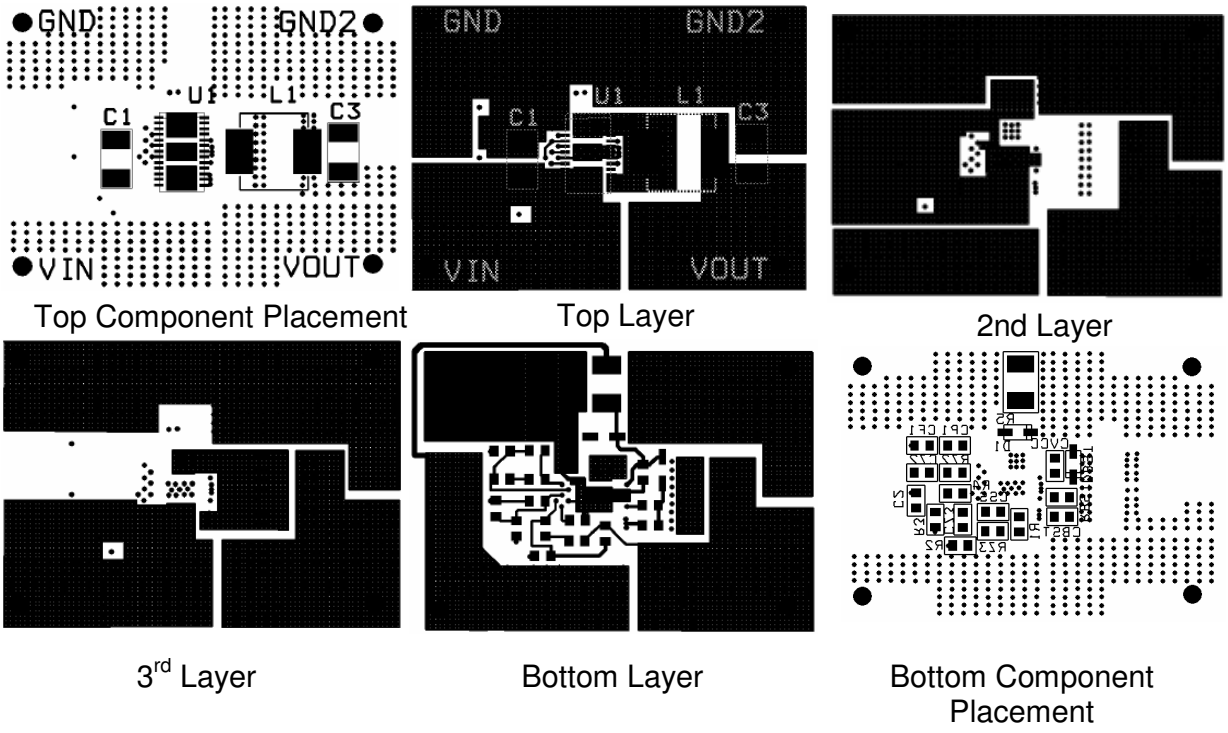

Figure 2 Example PowerBlox™ Layout (2 Sided Component Placement)

3) If components are to be placed on both sides of the PCB then all feedback, compensation and bias supply passives should be on the bottom side of the PCB. Routing to these parts should also be done on the side on which they are mounted (see Figure 2). If an additional routing layer is available and required, then the layer closest to the bottom one is preferred. The path from the feedback resistor chain (R1 and R2 in Figure 1) should not be routed underneath the LX node or inductor.

4) Pgnd and Gnd should be kept as separate nets, with a single common connection (star), made by a short track from Pgnd to Gnd power pad under the device (Figure 3).

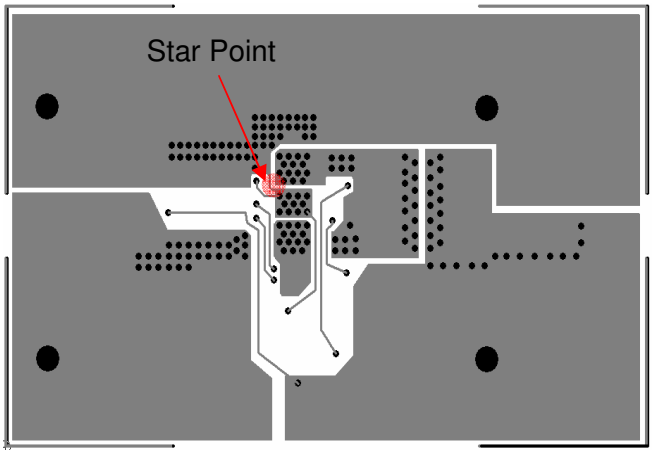

Figure 3 Common Connection point for Pgnd and Gnd

Thermal Considerations

The 26 pin DFN package is thermally enhanced by providing 3 separate pads on its lower side. These are electrically connected to the LX, Gnd and Vin pins. The shape and size of the pads used on the CAD footprint, and the surrounding PCB layout thus determine the thermal performance of the complete assembly. Two sizes of layout are recommended for the PowerBlox™ parts, their performance is a trade off between space available and thermal capacity.

Figure 4 shows the smaller layout. In this set up there are no vias required linking any planes to the power pads beneath the device. It should be noted that although this layout has no vias on the thermal pads, there is some thermal conductivity between the relatively small component layer planes and the much larger inner layer planes and bottom planes, which helps reduce thermal resistance. It has a θ_{ja} of 44˚C/W.

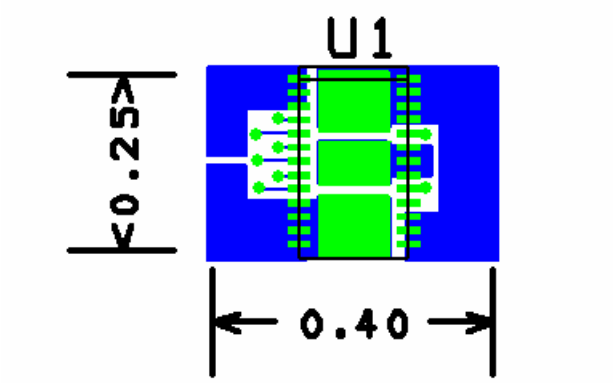

Figure 4 SP765x Minimum Footprint (0.1 in^2)

The larger layout shown in Figure 5 has an improved thermal resistance of θ_{ja} = 36˚C/W. This layout also uses 6 vias per pad onto 3 other PCB planes. Since this layout has vias connecting to much larger planes below, increasing the top area size beyond 0.7 in^2 has little effect in decreasing the thermal resistance.

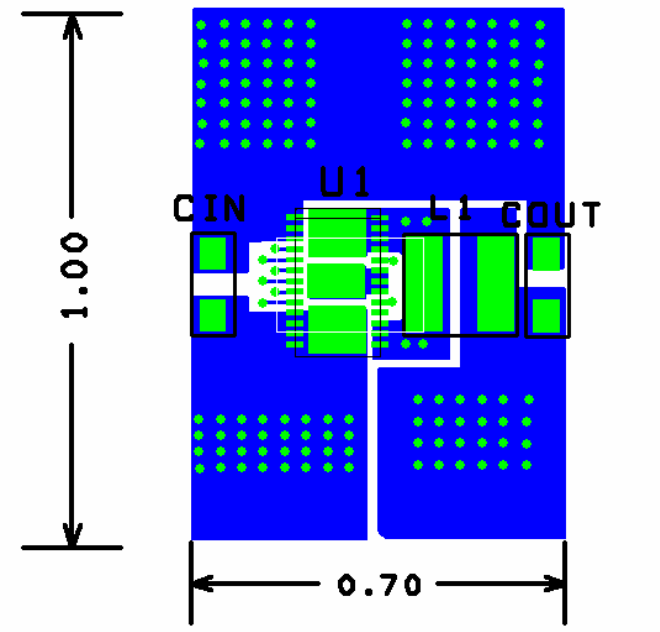

Figure 5 SP765x Maximum Footprint (0.7 in^2)

It should be noted that the above figures are based upon a 4 layer FR4 PCB, with 3oz copper on the top and bottom layers, 1 oz copper on inner layers. For lower densities of copper, since the relationship between area and density with respect to thermal conductivity is linear, a lower density can be compensated for by a proportional increase in area.

CAD Footprint Recommendations

The correct CAD footprint is not only important to effective thermal management of the solution, it can also have a marked effect on the ease of manufacture. To evaluate the reliability of the CAD footprint, a solder test was performed using 3 different footprint shapes. The first shape used a footprint with signal pads 2x the length of PowerBlox™ pads, and the 3 power pads were about the same size as the PowerBlox™ thermal pads. The second footprint also used signal pads 2x the length of the PowerBlox™ signal pads, but the power pads width was reduced to about 15mils less than the PowerBlox™ power pads. The third shape used signal pads 1.5x the length of the PowerBlox™ signal pads and the power pads width reduced about 15mils less than the PowerBlox™ power pads.
The 3 footprints were all tested the way: we made 2 layer PCBs and had a contract manufacturer using pick and place equipment and reflow soldering system to assemble 20 parts of each footprint. The parts were burned in by thermal cycling from 0 to 100degC and -65 to 150degC. All the assembled parts were visually inspected for defects and electrically tested for continuity at read points of 0, 500, 1000 cycles. All passed visual and electrical tests and no there were no solder joint cracks. Footprint number 3 was selected as the recommended footprint for two

reasons: preferences by some customers for the solder land = 1.5x the actual land on the package, plus the thermal pad size was considered better by our packaging engineer to be smaller than the size on the package.

The recommended footprint is reproduced in Figure 6.

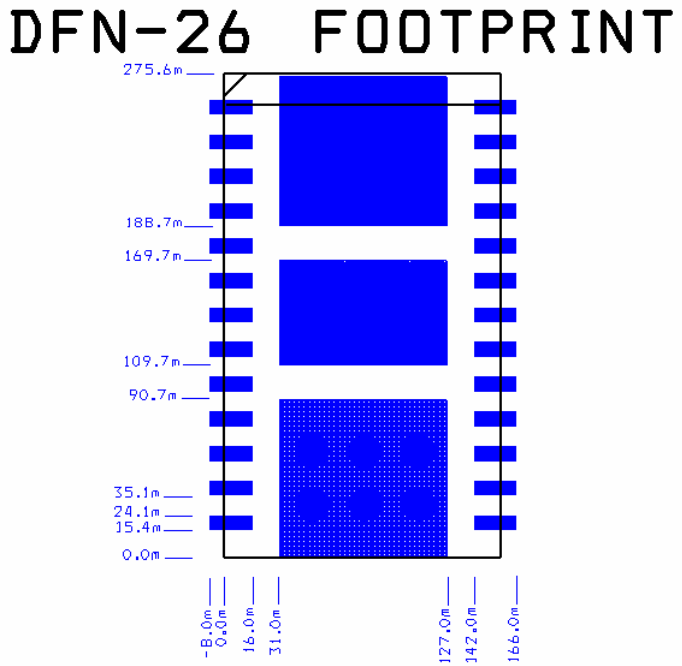

Figure 6 Recommended SP765x CAD Footprint

A 4 mil stencil should be used during the manufacturing stage, with pads the same size as the CAD footprint pads. If vias are determined to be necessary, these should be limited to a maximum of 9 per pad. (Additional ones give very limited improvement to θ_{ja}). The pads should be joined to the corresponding electrically connected power pads by a short, direct track (see Figure 7), not by filling the gap area with copper. Note that special plugging of the vias prior to reflow is not required.

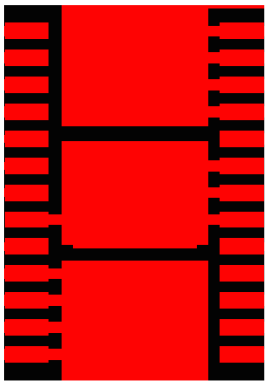

Figure 7 Correct Joining of Signal to Power Pads

