

# T1 / E1 / J1 Eight - Channel Device

## XRT86VX38

### Octal Framer and LIU Integrated Solution Featuring R<sup>3</sup> Technology

The XRT86VX38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framer and Long-haul/Short-haul LIU integrated solution featuring R<sup>3</sup> technology (Reconfigurable, Relayless Redundancy) and BITS Timing element. The physical interface is optimized with internal impedance, and with the patented pad structure, the XRT86VX38 provides protection from power failures and hot swapping.

The XRT86VX38 contains an integrated DS1/E1/J1 framer and LIU which provide DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU-T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats.

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function. There are 3 Transmit HDLC controllers per channel which encapsulate contents of the Transmit HDLC buffers into LAPD Message frames. There are 3 Receive HDLC controllers per channel which extract the payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and write the contents into the Receive HDLC buffers. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames. Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.



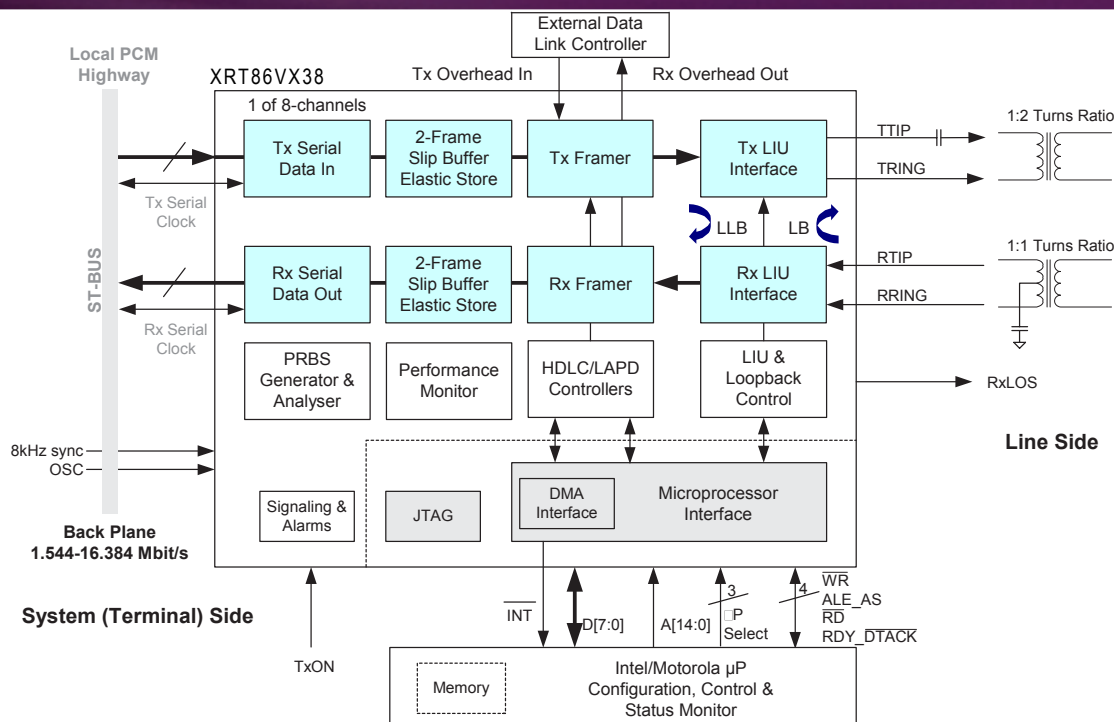
### Applications

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

### Ordering Information

Part Number	Package	Operating Temperature Range
XRT86VX38IB329	329 Plastic BGA	-40°C to 85°C
XRT86VX38IB256	256 Plastic BGA	-40°C to 85°C

### XRT86VX38 8-channel DS1 Diagram



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### Features

- Supports Section 13 - Synchronization Interface in ITU G.703 for both Transmit and Receive Paths
- Supports SSM Synchronous Messaging Generation (BOC for T1, National Bits for E1) on the Transmit Path
- Supports SSM Synchronous Messaging Extraction (BOC for T1, National Bits for E1) on the Receive Path
- Supports BITS timing generation on the Transmit Outputs
- Supports BITS timing extraction from NRZ data on the Analog Receive Path
- DS-0 Monitoring on both Transmit and Receive Time Slots
- Supports SSM Synchronization Messaging per ANSI T1.101-1999 and ITU G.704
- Supports a Customized Section 13 - Synchronization Interface in G.703 at 1.544MHz
- Independent, full duplex DS1 Tx and Rx Framer/LIUs
- Each channel has full featured Long-haul/Short-haul LIU
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 2-channel multiplexed 12.352/16.384 (HMPV/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 Integrated HDLC controllers for transmit and receive, each controller having two 96-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Supports SPRM and NPRM
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: SF/D4, ESF, SLC®96, T1DM and N-Frame (non-signaling)
- Direct access to D and E channels for fast transmission of data link information
- Full BERT Controller for generation and detection on system and line side of the chip
- PRBS, QRSS, and Network Loop Code generation and detection
- Seven Independent, simultaneous Loop Code Detectors per Channel
- Programmable Interrupt output pin
- Supports programmed I/O and DMA modes of Read-Write access
- The framer block encodes and decodes the T1/E1/J1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core
- 3.3V CMOS operation with 5V tolerant inputs

