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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER – SDH REGISTERS

Rev 2.0.0

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GENERAL DESCRIPTION

The XRT94L33 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L33 interfaces directly to the optical transceiver

The XRT94L33 processes the section, line and path overhead in the SONET/SDH data stream and also performs ATM and PPP PHY-layer processing. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L33 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L33 memory map or from external interface. A1, A2 framing pattern, Ch byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L33 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L33 provides 3 Mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

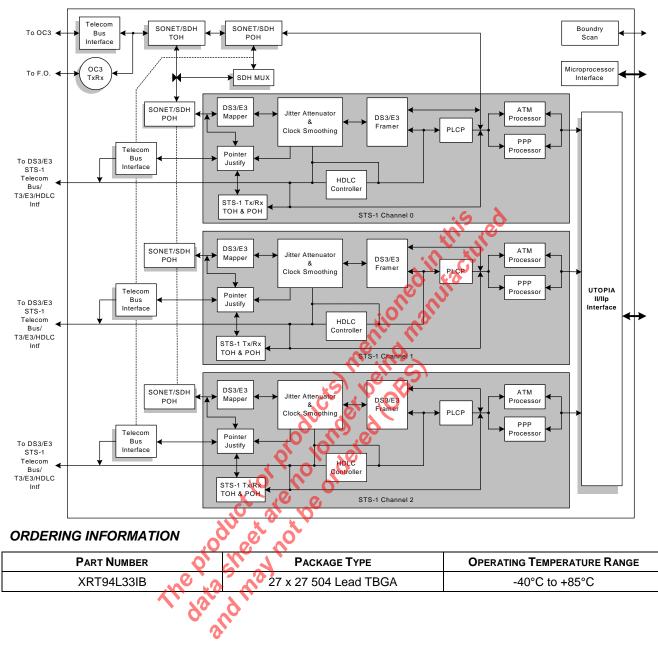
- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/19.4477.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05Ulpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- UTOPIA Level 2 interface for ATM or level 2P for Packets
 - E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range

Available in a 504 Ball TBGA package

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Block Diagram of the XRT94L33





1.0 XRT94L33 REGISTERS FOR SDH

1.1 THE OVERALL REGISTER MAP WITHIN THE XRT94L33

As mentioned earlier, the XRT94L33 employs a direct Addressing Scheme. The Address Locations for each of the "Register Groups" (or Register pages) is presented in the Table below.

Table 1: The Address Register Map for the XRT94L33

Address Location	REGISTER NAME	DEFAULT VALUE
	OPERATION CONTROL BLOCK REGISTERS	
0x0000 - 0x00FF	Reserved	
0x0100	Operation Control Register – Byte 3	0x00
0x0101	Operation Control Register – Byte 2	0x00
0x0102	Reserved	0x00
0x0103	Operation Control Register – Byte 0	0x00
0x0104	Operation Status Register – Byte 3 (Device ID)	0xE3
0x0105	Operation Status Register – Byte 2 (Revision D)	0x01
0x0106 – 0x010A	Reserved	0x00
0x010B	Operation Interrupt Status Register – Byte 0	0x00
0x010C - 0x010E	Reserved	0x00
0x010F	Operation Interrupt Enable Register Byte 0	0x00
0x0110 – 0x0111	Reserved	0x00
0x0112	Operation Block Interrupt Status Register – Byte 1	0x00
0x0113	Operation Block Interrupt Status Register – Byte 0	0x00
0x0114 - 0x0115	Reserved	0x00
0x0116	Operation Block Interrupt Enable Register – Byte 1	0x00
0x0117	Operation Block Interrupt Enable Register – Byte 0	0x00
0x0118 - 0x0119	Reserved	0x00
0x011A	Reserved	0x00
0x011B	Mode Control Register – Byte 0	0x00
0x011C - 0x011E	Reserved	0x00
0x011F	Loop-back Control Register – Byte 0	0x00
0x0120	Channel Interrupt Indicator Register – ReceiveTransmit TUG-3/AU-3 Mapper VC-3 POH Processor Block	0x00
0x0121	Reserved	0x00
0x0122	Channel Interrupt Indicator Register – DS3/E3 framer Block	0x00
0x0123	Channel Interrupt Indicator Register – Receive STM-0 POH Processor Block	0x00
0x0124	Channel Interrupt Indicator Register – Receive STM-0 SOH Processor Block	0x00

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0x0125	Reserved	0x00
0x0126	Channel Interrupt Indicator Register – STM-0/DS3/E3 Mapper Block	0x00
0x0127 – 0x0129	Reserved	0x00
0x012A – 0x012F	Reserved	0x00
0x0130 – 0x0131	Reserved	0x11
0x0132	Interface Control Register – Byte 1	0x00
0x0133	Interface Control Register – Byte 0	0x00
0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3	0x00
0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00
0x0136	Reserved	0x00
0x0137	STS-3/STM-1 Telecom Bus Control Register – Byte 0	0x00
0x0138	Reserved	0x00
0x0139	Interface Control Register – Byte 2 – STM-1 Telecom Bus 2	0x00
0x013A	Interface Control Register – Byte 1 – STM-1 Telecom Bus 1	0x00
0x013B	Interface Control Register – Byte 0 – STM Telecom Bus 0	0x00
0x013C	Interface Control Register – STM-0 Telecom Bus Interrupt Register	0x00
0x013D	Interface Control Register – STM Telecom Bus Interrupt Status Register	0x00
0x013E	Interface Control Register – STM-0 Telecom Bus Interrupt Register # 2	0x00
0x013F	Interface Control Register STM0 Telecom Bus Interrupt Enable Register	0x00
0x0140 - 0x0146	Reserved	0x00
0x0147	Operation General Purpose Input/Output Register	0x00
0x0148 – 0x014A	Reserved	0x00
0x014B	Operation General Purpose Input/Output Direction Register – Byte 0	0x00
0x014C -0x014F	Reserved	0x00
0x0150	Operation Output Control Register – Byte 1	0x00
0x0151 –0x0152	Reserved	0x00
0x0153	Operation Output Control Register – Byte 0	0x00
0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00
0x0155 – 0x0156	Reserved	0x00
0x0157	Operation Slow Speed Port Control Register –Byte 0	0x00
0x0158	Operation – DS3/E3/STM-0 Clock Frequency Out of Range Detection – Direction Register	0x00
0x0159	Reserved	0x00
0x015A	Operation – DS3/E3/STM-0 Clock Frequency – DS3 Out of Range Detection	0x00



	Threshold Register	
0x015B	Operation – DS3/E3/STM-0 Clock Frequency – STM-0/E3 Out of Range Detection Threshold Register	0x00
0x015C	Reserved	0x00
0x015D	Operation – DS3/E3/STM-0 Frequency Out of Range Interrupt Enable Register – Byte 0	0x00
0x015E	Reserved	0x00
0x015F	Operation – DS3/E3/STM-0 Frequency Out of Range Interrupt Status Register – Byte 0	0x00
0x0160 – 0x017F	Reserved	0x00
0x0180	APS Mapping Register	0x00
0x0181	APS Control Register	0x00
0x0182 - 0x0193	Reserved	0x00
0x0194	APS Status Register	0x00
0x0195	Reserved	0x00
0x0196	APS Status Register	0x00
0x0197	APS Status Register	0x00
0x0198	APS Interrupt Register	0x00
0x0199	Reserved	0x00
0x019A	APS Interrupt Register	0x00
0x019B	APS Interrupt Register	0x00
0x019C	APS Interrupt Register	0x00
0x019D	Reserved	0x00
0x019E	APS Interrupt Enable Register	0x00
0x019F	APS Interrupt Enable Register	0x00
0x01A0 - 0x01FF	Reserved	0x00
	LINE INTERFACE CONTROL REGISTERS	
0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x0304 - 0x0306	Reserved	0x00
0x0307	Receive Line Status Register	0x00
0x0308 -0x030A	Reserved	0x00
0x030B	Receive Line Interrupt Register	0x00
0x030C - 0x030E	Reserved	0x00
0x030F	Receive Line Interrupt Enable Register	0x00



0x0310 – 0x0382	Reserved	0x00
0x0383	Transmit Line Interface Control Register	0x00
	RECEIVE STM-1 SOH PROCESSOR BLOCK CONTROL REGISTERS	
0x1000 - 0x1102	Reserved	
0x1103	Receive STM-1 Section Control Register – Byte 0	0x00
0x1104 - 0x1105	Reserved	0x00
0x1106	Receive STM-1 Section Status Register – Byte 1	0x00
0x1107	Receive STM-1 Section Status Register – Byte 0	0x02
0x1108	Reserved	0x00
0x1109	Receive STM-1 Section Interrupt Status Register – Byte 2	0x00
0x110A	Receive STM-1 Section Interrupt Status Register – Byte 1	0x00
0x110B	Receive STM-1 Section Interrupt Status Register – Byte 0	0x00
0x110C	Reserved	0x00
0x110D	Receive STM-1 Section Interrupt Enable Register – Byte 2	0x00
0x110E	Receive STM-1 Section Interrupt Enable Register + Byte 1	0x00
0x110F	Receive STM-1 Section Interrupt Enable Register - Byte 0	0x00
0x1110	Receive STM-1 Section B1 Byte Error Count – Byte 3	0x00
0x1111	Receive STM-1 Section B1 Byte Error Count Byte 2	0x00
0x1112	Receive STM-1 Section B1 Byte Error Count – Byte 1	0x00
0x1113	Receive STM-1 Section B1 Byte Error Count – Byte 0	0x00
0x1114	Receive STM-1 Section B2 Byte Error Count – Byte 3	0x00
0x1115	Receive STM-1 Section B2 Byte Error Count – Byte 2	0x00
0x1116	Receive STM-1 Section B2 Byte Error Count – Byte 1	0x00
0x1117	Receive STM-1 Section B2 Byte Error Count – Byte 0	0x00
0x1118	Receive STM-1 Section MS-REI Event Count – Byte 3	0x00
0x1119	Receive STM-1 Section MS-REI Event Count – Byte 2	0x00
0x111A	Receive STM-1 Section MS-REI Event Count – Byte 1	0x00
0x111B	Receive STM-1 Section MS-REI Event Count – Byte 0	0x00
0x111C	Reserved	0x00
0x111D - 0 x111E	Reserved	0x00
0x111F	Receive STM-1 Section K1 Byte Value Register	0x00
0x1120 - 0x1122	Reserved	0x00
0x1123	Receive STM-1 Section K2 Byte Value Register	0x00



0x1124 – 0x1126	Reserved	0x00
0x1127	Receive STM-1 Section S1 Byte Value Register	0x00
0x1128 – 0x112A	Reserved	0x00
0x112B	Receive STM-1 Section – In-Sync Threshold Value Register	0x00
0x112C, 0x112D	Reserved	0x00
0x112E	Receive STM-1 Section – LOS Threshold Value – MSB	0xFF
0x112F	Receive STM-1 Section – LOS Threshold Value – LSB	0xFF
0x1130	Reserved	0x00
0x1131	Receive STM-1 Section – SF Set Monitor Interval – Byte 2	0x00
0x1132	Receive STM-1 Section – SF Set Monitor Interval – Byter	0x00
0x1133	Receive STM-1 Section – SF Set Monitor Interval – Byte 0	0x00
0x1134 – 0x1135	Reserved	0x00
0x1136	Receive STM-1 Section – SF Set Threshold Byte	0x00
0x1137	Receive STM-1 Section – SF Set Threshold – Byte 0	0x00
0x1138, 0x1139	Reserved	0x00
0x113A	Receive STM-1 Section – SF Clear Threshold – Byte 1	0x00
0x113B	Receive STM-1 Section – SF Clear Threshold – Byte 0	0x00
0x113C	Reserved	0x00
0x113D	Receive STM-1 Section – SD Set Monitor Interval – Byte 2	0x00
0x113E	Receive STM-1 Section 2SD Set Monitor Interval – Byte 1	0x00
0x113F	Receive STM Section – SD Set Monitor Interval – Byte 0	0x00
0x1140, 0x1141	Reserved	0x00
0x1142	Receive STM-1 Section – SD Set Threshold – Byte 1	0x00
0x1143	Receive STM-1 Section – SD Set Threshold – Byte 0	0x00
0x1144, 0x1145	Reserved 0	0x00
0x1146	Receive STM-1 Section – SD Clear Threshold – Byte 1	0x00
0x1147	Receive STM-1 Section – SD Clear Threshold – Byte 0	0x00
0x1148 – 0x114A	Reserved	0x00
0x114B	Receive STM-1 Section – Force SEF Condition	0x00
0x114C, 0x114E	Reserved	0x00
0x114F	Receive STM-1 Section – Receive Section Trace Message Buffer Control Register	0x00
0x1150, 0x1151	Reserved	0x00
0x1152	Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 1	0x00



0.4450		0.00
0x1153	Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 0	0x00
0x1154, 0x1155	Reserved	0x00
0x1156	Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 1	0x00
0x1157	Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 0	0x00
0x1158	Reserved	0x00
0x1159	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x115A	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x115B	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x115C	Reserved	0x00
0x115D	Receive STM-1 Section – Receive SF Clear Monitor Interval Byte 2	0xFF
0x115E	Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x115F	Receive STM-1 Section – Receive SF Clear Monitor Byte	0xFF
0x1160 - 0x1162	Reserved	0x00
0x1163	Receive STM-1 Section – Auto AIS Control Register	0x00
0x1164 - 0x1166	Reserved	0x00
0x1167	Receive STM-1 Section – Serial Port Control Register	0x00
0x1168 – 0x116A	Reserved	0x00
0x116B	Receive STM-1 Section – Auto AIS (in Downstream STM-0s) Control Register	0x000
0x116C – 0x1179	Reserved	0x00
0x117A	Receive STM-1 Section – SOB Capture Indirect Address	0x00
0x117B	Receive STM-1 Section - SOH Capture Indirect Address	0x00
0x117C	Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x117D	Receive STM-1 Section 2SOH Capture Indirect Data	0x00
0x117E	Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x117F	Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x1180	Reserved	0x00
	RECEIVE AU-4 MAPPER/VC-4 POH PROCESSOR BLOCK	•
0x1181	Reserved	0x00
0x1182	Receive AU-4 Mapper/VC-4 Path – Control Register – Byte 1	0x00
0x1183	Receive AU-4 Mapper/VC-4 Path – Control Register – Byte 0	0x00
0x1184 – 0x1185	Reserved	0x00
0x1186	Receive AU-4 Mapper/VC-4 Path – Status Register – Byte 1	0x00
0x1187	Receive AU-4 Mapper/VC-4 Path – Status Register – Byte 0	0x00



0x1188	Reserved	0x00
0x1189	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 2	0x00
0x118A	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 1	0x00
0x118B	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 0	0x00
0x118C	Reserved	0x00
0x118D	Receive AU-4 Mapper/VC-4 Path – Interrupt Enable Register – Byte 2	0x00
0x118E	Receive AU-4 Mapper/VC-4 Path – Interrupt Enable Register – Byte 1	0x00
0x118F	Receive AU-4 Mapper/VC-4 Path – Interrupt Enable Register – Byte 0	0x00
0x1190 - 0x1192	Reserved	0x00
0x1193	Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Register	0x00
0x1194 – 0x1195	Reserved	0x00
0x1196	Receive AU-4 Mapper/VC-4 Path – Receive Path Label Byte (C2) Byte Register	0x00
0x1197	Receive AU-4 Mapper/VC-4 Path - Expected Path Label Byte (C2) Byte Register	0x00
0x1198	Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Byte 3	0x00
0x1199	Receive AU-4 Mapper/VC-4 Path B3 Byte Error Count Register – Byte 2	0x00
0x119A	Receive AU-4 Mapper/VC-4 Path - B3 Byte Error Count Register - Byte 1	0x00
0x119B	Receive AU-4 Mapper/VC-4 Path - B3 Byte Error Count Register - Byte 0	0x00
0x119C	Receive AU-4 MapperVC-4 Path - HP-REI Event Count Register – Byte 3	0x00
0x119D	Receive AU-4 Mapper/VC-4 Path – HP-REI Event Count Register – Byte 2	0x00
0x119E	Receive AU-4 Mapper/VC-4 Path – HP-REI Event Count Register – Byte 1	0x00
0x119F	Receive AU-4 Mapper/VC-4 Path – HP-REI Event Count Register – Byte 0	0x00
0x11A0 – 0x11A2	Reserved	0x00
0x11A3	Receive AU-4 Mapper/VC-4 Path – Receive Path Trace Message Byte Control Register	0x00
0x11A4 – 0x11A5	Reserved	0x00
0x11A6	Receive AU-4 Mapper/VC-4 Path – Pointer Value Register – Byte 1	0x00
0x11A7	Receive AU-4 Mapper/VC-4 Path – Pointer Value Register – Byte 0	0x00
0x11A8 – 0x11AA	Reserved	0x00
0x11AB	Receive AU-4 Mapper/VC-4 Path – Loss of Pointer – Concatenation Status Register	0x00
0x11AC - 0x11B2	Reserved	0x00
0x11B3	Receive AU-4 Mapper/VC-4 Path – AIS – Concatenation Status Register	0x00
0x11B4 – 0x11BA	Reserved	0x00

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0x11BB	Receive AU-4 Mapper/VC-4 Path – Auto AIS Control Register	0x00
0x11BC – 0x11BE	Reserved	0x00
0x11BF	Receive AU-4 Mapper/VC-4 Path – Serial Port Control Register	0x00
0x11C0 - 0x11C2	Reserved	0x00
0x11C3	Receive AU-4 Mapper/VC-4 Path - Receive SONET Auto Alarm Register – Byte 0	0x00
0x11C4 -0x11D2	Reserved	0x00
0x11D3	Receive AU-4 Mapper/VC-4 Path – Receive J1 Byte Capture Register	0x00
0x11D4 - 0x11D6	Reserved	0x00
0x11D7	Receive AU-4 Mapper/VC-4 Path – Receive B3 Byte Capture Register	0x00
0x11D8 – 0x11DA	Reserved	0x00
0x11DB	Receive AU-4 Mapper/VC-4 Path – Receive C2 Byte Capture Register	0x00
0x11DC – 0x11DE	Reserved	0x00
0x11DF	Receive AU-4 Mapper/VC-4 Path – Receive G1 Byte Capture Register	0x00
0x11E0-0x11E2	Reserved	0x00
0x11E3	Receive AU-4 Mapper/VC-4 Path – Receive F2 Byte Capture Register	0x00
0x11E4 – 0x11E6	Reserved	0x00
0x11E7	Receive AU-4 Mapper/VC-4 Path Receive H4 Byte Capture Register	0x00
0x11E8 – 0x11EA	Reserved	0x00
0x11EB	Receive AU-4 Mapper/VO-4 Path – Receive Z3 Byte Capture Register	0x00
0x11EC - 0x11EE	Reserved	0x00
0x11EF	Receive AU-4 Mapper/VC-4 Path – Receive Z4 (K3) Byte Capture Register	0x00
0x11F0 - 0x11F2	Reserved Q G A	0x00
0x11F3	Receive AU-4 Mapper/VC-4 Path – Receive Z5 Byte Capture Register	0x00
0x11F4 – 0x12FF	Reserved	0x00
Receive	STS-3/STM-1 SOH PROCESSOR BLOCK - RECEIVE JO (SECTION) TRACE MESSAGE B	UFFER
0x1300 – 0x133F	Receive STS-3/STM-1 SOH Processor Block – Receive J0 (Section) Trace Message Buffer – Expected and Received	0x00
0x1340 – 0x13FF	Reserved	0x00
RECEIVE AU-4 MAPP	ER/VC-4 POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFER – A	U-4 MAPPER/VC
0x1500 – 0x153F	Receive AU-4 Mapper/VC-4 POH Processor Block – Receive J1 (Path) Trace Message Buffer	0x00
0x1540 – 0x15FF	Reserved	0x00
	REDUNDANT RECEIVE STM-1 SOH PROCESSOR BLOCK CONTROL REGISTERS	
0x1600 - 0x1702		



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0x1703	Redundant Receive STM-1 Section Control Register – Byte 0	0x00
0x1704 - 0x1705	Reserved	0x00
0x1706	Redundant Receive STM-1 Section Status Register – Byte 1	0x00
0x1707	Redundant Receive STM-1 Section Status Register – Byte 0	0x02
0x1708	Reserved	0x00
0x1709	Redundant Receive STM-1 Section Interrupt Status Register – Byte 2	0x00
0x170A	Redundant Receive STM-1 Section Interrupt Status Register – Byte 1	0x00
0x170B	Redundant Receive STM-1 Section Interrupt Status Register – Byte 0	0x00
0x170C	Reserved	0x00
0x170D	Redundant Receive STM-1 Section Interrupt Enable Register - Byte 2	0x00
0x170E	Redundant Receive STM-1 Section Interrupt Enable Register – Byte 1	0x00
0x170F	Redundant Receive STM-1 Section Interrupt Enable Register – Byte 0	0x00
0x1710	Redundant Receive STM-1 Section B1 Byte Error Count – Byte 3	0x00
0x1711	Redundant Receive STM-1 Section B1 Byte Error Count – Byte 2	0x00
0x1712	Redundant Receive STM-1 Section B1 Byte Error Count – Byte 1	0x00
0x1713	Redundant Receive STM-1 Section B1 Byte Error Count – Byte 0	0x00
0x1714	Redundant Receive STM-1 Section B2 Byte Error Count – Byte 3	0x00
0x1715	Redundant Receive STM Section B2 Byte Error Count – Byte 2	0x00
0x1716	Redundant Receive STM-1 Section B2 Byte Error Count – Byte 1	0x00
0x1717	Redundant Receive STM1 Section B2 Byte Error Count – Byte 0	0x00
0x1718	Redundant Receive STM-1 Section MS-REI Event Count – Byte 3	0x00
0x1719	Redundant Receive STM-1 Section MS-REI Event Count – Byte 2	0x00
0x171A	Redundant Receive STM-1 Section MS-REI Event Count – Byte 1	0x00
0x171B	Redundant Receive STM-1 Section MS-REI Event Count – Byte 0	0x00
0x171C - 0 x171E	Reserved	0x00
0x171F	Redundant Receive STM-1 Section K1 Byte Value Register	0x00
0x1720 – 0x1722	Reserved	0x00
0x1723	Redundant Receive STM-1 Section K2 Byte Value Register	0x00
0x1724 – 0x1726	Reserved	0x00
0x1727	Redundant Receive STM-1 Section S1 Byte Value Register	0x00
0x1728 – 0x172A	Reserved	0x00
0x172B	Redundant Receive STM-1 Section – In-Sync Threshold Value	0x00
0x172C, 0x172D	Reserved	0x00



0x172E	Redundant Receive STM-1 Section – LOS Threshold Value – MSB	0xFF
0x172F	Redundant Receive STM-1 Section – LOS Threshold Value – LSB	0xFF
0x1730	Reserved	0x00
0x1731	Redundant Receive STM-1 Section – SF Set Monitor Interval – Byte 2	0x00
0x1732	Redundant Receive STM-1 Section – SF Set Monitor Interval – Byte 1	0x00
0x1733	Redundant Receive STM-1 Section – SF Set Monitor Interval – Byte 0	0x00
0x1734 – 0x1735	Reserved	0x00
0x1736	Redundant Receive STM-1 Section – SF Set Threshold – Byte 1	0x00
0x1737	Redundant Receive STM-1 Section – SF Set Threshold – Byte 0	0x00
0x1738, 0x1739	Reserved	0x00
0x173A	Redundant Receive STM-1 Section – SF Clear Threshold Byte	0x00
0x173B	Redundant Receive STM-1 Section – SF Clear Threshold – Byte 0	0x00
0x173C	Reserved	0x00
0x173D	Redundant Receive STM-1 Section – SD Set Monitor Interval – Byte 2	0x00
0x173E	Redundant Receive STM-1 Section – SD Set Monitor Interval – Byte 1	0x00
0x173F	Redundant Receive STM-1 Section - SD Set Monitor Interval - Byte 0	0x00
0x1740, 0x1741	Reserved	0x00
0x1742	Redundant Receive STM-1 Section - SD Set Threshold – Byte 1	0x00
0x1743	Redundant Receive STM-1 Section – SD Set Threshold – Byte 0	0x00
0x1744, 0x1745	Reserved	0x00
0x1746	Redundant Receive STM-1 Section – SD Clear Threshold – Byte 1	0x00
0x1747	Redundant Receive STM-1 Section – SD Clear Threshold – Byte 0	0x00
0x1748 – 0x174A	Reserved	0x00
0x174B	Redundant Receive STM-1 Section – Force SEF Condition	0x00
0x174C, 0x1751	Reserved	0x00
0x1752	Redundant Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 1	0x00
0x1753	Redundant Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 0	0x00
0x1754, 0x1755	Reserved	0x00
0x1756	Redundant Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 1	0x00
0x1757	Redundant Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 0	0x00
0x1758	Reserved	0x00
0x1759	Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x175A	Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte	0xFF



	1	
0x175B	Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x175C	Reserved	0x00
0x175D	Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x175E	Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte	0xFF
0x175F	Redundant Receive STM-1 Section – Receive SF Clear Monitor – Byte 0	0xFF
0x1760 - 0x1766	Reserved	0x00
0x1767	Redundant Receive STM-1 Section – Serial Port Control Register	0x00
0x1768 – 0x1779	Reserved	0x00
0x177A	Redundant Receive STM-1 Section – SOH Capture Indirect Address	0x00
0x177B	Redundant Receive STM-1 Section – SOH Capture Indirect Address	0x00
0x177C	Redundant Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x177D	Redundant Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x177E	Redundant Receive STM-1 Section - SOH Capture Indirect Data	0x00
0x177F	Redundant Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x1780 – 0x17FF	Reserved	0x00
	TRANSMIT STM-1 SOH PROCESSOR BLOCK CONTROL REGISTERS	
0x1800 – 0x1901	Reserved	0x00
0x1902	Transmit STM-1 Section SOMET Transmit Control Register – Byte 1	0x00
0x1903	Transmit STMT Section - SONET Transmit Control Register – Byte 0	0x00
0x1904 – 0x1916	Reserved	0x00
0x1917	Transmit STM-1 Section – Transmit A1 Error Mask – Low Register – Byte 0	0x00
0x1918 – 0x191E	Reserved	0x00
0x191F	Transmit STM-1 Section – Transmit A2 Error Mask – Low Register – Byte 0	0x00
0x1920 - 0x1921	Reserved	0x00
0x1923	Transmit STM-1 Section – B1 Byte Error Mask Register	0x00
0x1924 – 0x1926	Reserved	0x00
0x1927	Transmit STM-1 Section – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0x1928 – 0x192A	Reserved	0x00
0x192B	Transmit STM-1 Section – Transmit B2 Bit Error Mask Register – Byte 0	0x00
0x192C – 0x192D	Reserved	0x00
0x192E	Transmit STM-1 Section – K1K2 (APS) Byte Value Register – Byte 1	0x00



0x192F	Transmit STM-1 Section – K1K2 (APS) Byte Value Register – Byte 0	0x00
0x1930 - 0x1931	Reserved	0x00
0x1933	Transmit STM-1 Section – MS-RDI Control Register	0x00
0x1934 - 0x1936	Reserved	0x00
0x1937	Transmit STM-1 Section – M0M1 Byte Value Register	0x00
0x1938 – 0x193A	Reserved	0x00
0x193B	Transmit STM-1 Section – S1 Byte Value Register	0x00
0x193C – 0x193E	Reserved	0x00
0x193F	Transmit STM-1 Section – F1 Byte Value Register	0x00
0x1940 - 0x1942	Reserved	0x00
0x1943 - 0x1946	Transmit STM-1 Section – E1 Byte Value Register	0x00
0x1947	Transmit STM-1 Section – E2 Byte Value Register	0x00
0x1948 – 0x194A	Reserved	0x00
0x194B	Transmit STM-1 Section – J0 Byte Value Register	0x00
0x194C – 0x194E	Reserved	0x00
0x194F	Transmit STM-1 Section – J0 Byte Control Register	0x00
0x1950 - 0x1952	Reserved	0x00
0x1953	Transmit STM-1 Section – Serial Port Control Register	0x00
0x1954 –0x1980	Reserved	0x00
	TRANSMIT AU-4 MAPPER VC-4 POH PROCESSOR BLOCK	
0x1981	Reserved	0x00
0x1982	Transmit AU-4 Mapper VC-4 Path – SONET Control Register – Byte 1	0x00
0x1983	Transmit A0-4 Mapper/VC-4 Path – SONET Control Register- Byte 0	0x00
0x1984 - 0x1992	Reserved	0x00
0x1993	Transmit AU-4 Mapper/VC-4 Path – Transmit J1 Byte Value Register	0x00
0x1994 – 0x1996	Reserved	0x00
0x1997	Transmit AU-4 Mapper/VC-4 Path – B3 Byte Mask Register	0x00
0x1998 – 0x199A	Reserved	0x00
0x199B	Transmit AU-4 Mapper/VC-4 Path – Transmit C2 Byte Value Register	0x00
0x199C – 0x199E	Reserved	0x00
0x199F	Transmit AU-4 Mapper/VC-4 Path – Transmit G1 Byte Value Register	0x00
0x19A0 – 0x19A2	Reserved	0x00
0x19A3	Transmit AU-4 Mapper/VC-4 Path – Transmit F2 Byte Value Register	0x00



0x19A4 –0x19A6	Reserved	0x00
0x19A7	Transmit AU-4 Mapper/VC-4 Path – Transmit H4 Byte Value Register	0x00
0x19A8 – 0x19AA	Reserved	0x00
0x19AB	Transmit AU-4 Mapper/VC-4 Path – Transmit Z3 Byte Value Register	0x00
0x19AC - 0x19AE	Reserved	0x00
0x19AF	Transmit AU-4 Mapper/VC-4 Path – Transmit Z4 Byte Value Register	0x00
0x19B0 - 0x19B2	Reserved	0x00
0x19B3	Transmit AU-4 Mapper/VC-4 Path – Transmit Z5 Byte Value Register	0x00
0x19B4 - 0x19B6	Reserved	0x00
0x19B7	Transmit AU-4 Mapper/VC-4 Path – Transmit Path Control Register – Byte 0	0x00
0x19B8 – 0x19BA	Reserved	0x00
0x19BB	Transmit AU-4 Mapper/VC-4 Path- Transmit J1 Byte Control Register	0x00
0x19BC -0x19BE	Reserved	0x00
0x19BF	Transmit AU-4 Mapper/VC-4 Path - Transmit Arbitrary H1 Byte Pointer Register	0x00
0x19C0 - 0x19C2	Reserved	0x00
0x19C3	Transmit AU-4 Mapper/VC-4 Path Transmit Arbitrary H2 Byte Pointer Register	0x00
0x19C4 - 0x19C5	Reserved	0x00
0x19C6	Transmit AU-4 Mapper/VC-4 Path + Transmit Pointer Byte Register –Byte 1	0x00
0x19C7	Transmit AU-4 Mapper/VC-4 Path – Transmit Pointer Byte Register – Byte 0	0x00
0x19C8	Reserved	0x00
0x19C9	Transmit AU-4 Mapper/VC-4 Path – HP-RDI Control Register – Byte 2	0x00
0x19CA	Transmit AU-4 Mapper/VC-4 Path –HP-RDI Control Register – Byte 1	0x00
0x19CB	Transmit AU-4 Mapper/VC-4 Path – HP-RDI Control Register – Byte 0	0x00
0x19CC -0x19CE	Reserved of	0x00
0x19CF	Transmit AU-4 Mapper/VC-4 Path – Transmit Path Serial Port Control Register	0x00
0x19D0 – 0x1AFF	Reserved	0x00
TRAN	SMIT STM-1 SOH PROCESSOR BLOCK – TRANSMIT J0 (SECTION) TRACE MESSAGE BUF	FER
0x1B00 – 0x1B3F	Transmit STM-1 SOH Processor Block – Transmit J0 (Section) Trace Message Buffer	0x00
0x1B40 – 0x1BFF	Reserved	0x00
TRANSMIT	AU-4 MAPPER/VC-4 POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE	BUFFER
0x1D00 – 0x1D3F	Transmit AU-4 Mapper/VC-4 POH Processor Block –Transmit J1 (Path) Trace Message Buffer	0x00

0xN19D

0xN19E

2

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Receive TUG-3/AU-3 Mapper VC-3 Path – REI-P Event Count Register – Byte

Receive TUG-3/AU-3 Mapper VC-3 Path - REI-P Event Count Register - Byte

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0x1D40 – 0x1DFF	Reserved	0x00
	RECEIVE TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK CONTROL REGISTERS	
Note: N represer	nts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xN000 – 0xN181	Reserved	0x00
0xN182	Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 1	0x00
0xN183	Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 0	0x00
0xN184, 0xN185	Reserved	0x00
0xN186	Receive TUG-3/AU-3 Mapper VC-3 Path – Status Register – Byte 1	0x00
0xN187	Receive TUG-3/AU-3 Mapper VC-3 Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive TUG-3/AU-3 Mapper VC-3 Path - Interrupt Enable Register - Byte 2	0x00
0xN18E	Receive TUG-3/AU-3 Mapper VC-3 Path + Interrupt Enable Register - Byte 1	0x00
0xN18F	Receive TUG-3/AU-3 Mapper VC-3 Path Onterrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive TUG-3/AU-3 Mapper VC-3 Path - SONET Receive HP-RDI/LP-RDI Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Register	0x00
0xN197	Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Register	0x00
0xN198	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 3	0x00
0xN199	Receive TUG-3/40-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 2	0x00
0xN19A	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 1	0x00
0xN19B	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 0	0x00
0xN19C	Receive TUG-3/AU-3 Mapper VC-3 Path – REI-P Event Count Register – Byte 3	0x00



0x00

0x00

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0xN19F	Receive TUG-3/AU-3 Mapper VC-3 Path – REI-P Event Count Register – Byte 0	0x00
0xN1A0 – 0xN1A2	Reserved	0x00
0xN1A3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receiver Path Trace Message Control Register	0x00
0xN1A4, 0xN1A5	Reserved	
0xN1A6	Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value – Byte 1	0x00
0xN1A7	Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value – Byte 0	0x00
0xN1A8 – 0xN1AA	Reserved	0x00
0xN1AB	Receive TUG-3/AU-3 Mapper VC-3 Path – Loss of Pointer – Concatenation Status Register	0x00
0xN1AC – 0xN1B2	Reserved	0x00
0xN1B3	Receive TUG-3/AU-3 Mapper VC-3 Path - AS - Concatenation Status Register	0x00
0xN1B4 – 0xN1BA	Reserved	0x00
0xN1BB	Receive TUG-3/AU-3 Mapper VC-3 Path AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive TUG-3/AU-3 Mapper VC-3 Path – Serial Port Control Register	0x00
0xN1C0 – 0xN1C2	Reserved	0x00
0xN1C3	Receive TUG-3/AU-3 Mapper VC3 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 – 0xN1D2	Reserved	0x00
0xN1D3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive C2 Byte Capture Register	0x00
0xN1DC – 0xN1DE	Reserved	0x00
0xN1DF	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00
0xN1E3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



0xN1EB	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN2FF	Reserved	
	DS3/E3 FRAMER BLOCK REGISTERS	
Note: N represer	nts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xN300	Operating Mode Register	0x23
0xN301	I/O Control Register	0xA0
0xN302 – 0xN303	Reserved	0x00
0xN304	Block Interrupt Enable Register	0x00
0xN305	Block Interrupt Status Register	0x00
0xN306 – 0xN30B	Reserved	0x00
0xN30C	Test Register	0x00
0xN30D	Payload HDLC Control Register	0x00
0xN30E – 0xN30F	Reserved	0x00
0xN310	RxDS3 Configuration and Status Register	0x02
	RxE3 Configuration and Status Register # 1 – G.832	
	RxE3 Configuration and Status Register # 2 – G.751	
0xN311	RxDS3 Status Register	0x67
	RxE3 Configuration and Status Register # 2 – G.832	
	RxE3 Configuration and Status Register # 2 – G.751	
0xN312	RxDS3 Interrupt Enable Register	0x00
	RxE3 Interrupt Enable Register # 1 – G.832	
	RxE3 Interrupt Enable Register # 1 – G.751	
0xN313	RxDS3 Interrupt Status Register	0x00
	RxE3 Interrupt Enable Register # 2 – G.832	
	RxE3 Interrupt Enable Register # 2 – G.751	
0xN314	RxDS3 Sync Detect Enable Register	0x00
	RxE3 Interrupt Status Register # 1 – G.832	
	RxE3 Interrupt Status Register # 1 – G.751	
0xN315	RxE3 Interrupt Status Register # 2 – G.832	0x00
	RxE3 Interrupt Status Register # 2 – G.751	



0xN316	RxDS3 FEAC Register	0x7E
0xN317	RxDS3 FEAC Interrupt Enable/Status Register	0x00
0xN318	RxDS3 LAPD Control Register	0x00
	RxE3 LAPD Control Register	
0xN319	RxDS3 LAPD Status Register	0x00
	RxE3 LAPD Status Register	
0xN31A	RxE3 NR Byte Register – G.832	0x00
	RxE3 Service Bit Register –G.751	
0xN31B	RxE3 GC Byte Register – G.832	0x00
0xN31C	RxE3 TTB-0 Register – G.832	0x00
0xN31D	RxE3 TTB-1 Register – G.832	0x00
0xN31E	RxE3 TTB-2 Register – G.832	0x00
0xN31F	RxE3 TTB-3 Register –G.832	0x00
0xN320	RxE3 TTB-4 Register –G.832	0x00
0xN321	RxE3 TTB-5 Register –G.832	0x00
0xN322	RxE3 TTB-6 Register – G.832	0x00
0xN323	RxE3 TTB-7 Register – G.832	0x00
0xN324	RxE3 TTB-8 Register – G.832	0x00
0xN325	RxE3 TTB-9 Register – 6832	0x00
0xN326	RxE3 TTB-10 Register - G 832	0x00
0xN327	RxE3 TTB-11 Register G.832	0x00
0xN328	RxE3 TTB-12 Register – G 832	0x00
0xN329	RxE3 TTB-13 Register – G.832	0x00
0xN32A	RxE3 TTB-14 Register – G.832	0x00
0xN32B	RxE3 TTB-15 Register –G.832	0x00
0xN32C	RxE3 SSM Register –G.832	0x00
0xN32D - 0xN32E	Reserved	0x00
0xN32F	RxDS3 Pattern Register	0x00
0xN330	TxDS3 Configuration Register	0x00
	TxE3 Configuration Register – G.832	
	TxE3 Configuration Register – G.751	
0xN331	TxDS3 FEAC Configuration and Status Register	0x00
0xN332	TxDS3 FEAC Register	0x7E
0xN333	TxDS3 LAPD Configuration Register	0x08



	TxE3 LAPD Configuration Register	
0xN334	TxDS3 LAPD Status/Interrupt Register	0x00
	TxE3 LAPD Status/Interrupt Register	
0xN335	TxDS3 M-Bit Mask Register	0x00
	TxE3 GC Byte Register – G.832	
	TxE3 Service Bits Register – G.751	
0xN336	TxDS3 F-Bit Mask # 1 Register	0x00
	TxE3 MA Byte Register – G.832	
0xN337	TxDS3 F-Bit Mask # 2 Register	0x00
	TxE3 NR Byte Register – G.832 TxDS3 F-Bit Mask # 3 Register TxE3 TTB-0 Register – G.832 TxDS3 F-Bit Mask # 4 Register TxE3 TTB-1 Register – G.832	
0xN338	TxDS3 F-Bit Mask # 3 Register	0x00
	TxE3 TTB-0 Register – G.832	
0xN339	TxDS3 F-Bit Mask # 4 Register	0x00
	TxE3 TTB-1 Register – G.832	
0xN33A	TxE3 TTB-2 Register – G.832	0x00
0xN33B	TxE3 TTB-3 Register – G.832	0x00
0xN33C	TxE3 TTB-4 Register – G.832	0x00
0xN33D	TxE3 TTB-5 Register – G.832	0x00
0xN33E	TxE3 TTB-6 Register – G.832	0x00
0xN33F	TxE3 TTB-7 Register – G.832	0x00
0xN340	TxE3 TTB-8 Register - 0.832	0x00
0xN341	TxE3 TTB-9 Register - G.832	0x00
0xN342	TxE3 TTB-10 Register - G.832	0x00
0xN343	TxE3 TTB-11 Register – G-832	0x00
0xN344	TxE3 TTB-12 Register - G.832	0x00
0xN345	TxE3 TTB-13 Register – G.832	0x00
0xN346	TxE3 TTB-14 Register – G.832	0x00
0xN347	TxE3 TTB-15 Register –G.832	0x00
0xN348	TxE3 FA1 Error Mask Register – G.832	0x00
	TxE3 FAS Error Mask Upper Register – G.751	
0xN349	TxE3 FA2 Error Mask Register – G.832	0x00
	TxE3 FAS Error Mask Lower Register – G.751	
0xN34A	TxE3 BIP-8 Mask Register – G.832	0x00
	TxE3 BIP-4 Mask Register – G.751	
0xN34B	Tx SSB Register – G.832	0x00



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

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0.01240		0.00
0xN34C	TxDS3 Pattern Register	0x0C
0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0xN34F	PMON Excessive Zero Count Register- LSB	0x00
0xN350	PMON LCV Event Count Register - MSB	0x00
0xN351	PMON LCV Event Count Register - LSB	0x00
0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0xN354	PMON Parity Error Event Count Register - MSB	0x00
0xN355	PMON Parity Error Event Count Register - LSB	0x00
0xN356	PMON FEBE Event Count Register- MSB	0x00
0xN357	PMON FEBE Event Count Register – LSB	0x00
0xN358	PMON CP-Bit Error Count Register - MSB	0x00
0xN359	PMON CP-Bit Error Count Register - LSB	0x00
0xN35A – 0xN367	Reserved	0x00
0xN368	PMON PRBS Bit Error Count Register - MSB	0x00
0xN369	PMON PRBS Bit Error Count Register - LSB	0x00
0xN36A – 0xN36B	Reserved	0x00
0xN36C	PMON Holding Register	0x00
0xN36D	One Second Error Status Register	0x00
0xN36E	One Second - LCV Count Accumulator Register - MSB	0x00
0xN36F	One Second – LOV Count Accumulator Register - LSB	0x00
0xN370	One Second – Parity Error Accumulator Register - MSB	0x00
0xN371	One Second – Parity Error Accumulator Register - LSB	0x00
0xN372	One Secon CP Bit Error Accumulator Register - MSB	0x00
0xN373	One Second – CP Bit Error Accumulator Register - LSB	0x00
0xN374 – 0xN37F	Reserved	0x00
0xN380	Line Interface Drive Register	0x00
0xN381	Reserved	0x00
0xN382	Reserved	0x00
0xN383	Transmit LAPD Byte Count Register	0x00
0xN384	Receive LAPD Byte Count Register	0x00
0xN385 – 0xN3AF	Reserved	0x00



0xN3B0	Transmit LAPD Memory InAddress LocationRegister	0x00
0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xN3B2	Receive LAPD Memory InAddress LocationRegister	0x00
0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xN3B4 – 0xN3EF	Reserved	0x00
0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xN3F1	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 0	0x10
0xN3F2	Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F3 – 0xN3F7	Reserved	0x00
0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00
0xN3FA – 0xN4FF	Reserved	0x00
RECEIVE TUC	G-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK RECEIVE J1 (PATH) TRACE MESS	AGE BUFFER
Note: N represe	nts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xN500 – 0xN53F	Receive TUG-3/AU-3 Mapper VC 3 POH Processor Block – Receive J1 (Path) Trace Message Buffer – Expected and Received	0x00
0xN540 – 0xN7FF	Reserved	0x00
	TRANSMIT TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK REGISTERS	
Note: N represen	ts the "Channel Number" and ranges in value from 0x02 to 0x04)	
0xN800 – 0xN981	Reserved 0	0x00
0xN982	Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit TUG-3AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN8992	Reserved	0x00
0xN993	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Control Register	0x00
0xN997	Transmit TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit G1 Byte Value Register	0x00
	1	



0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 – 0xN9B2	Reserved	0x00
0xN9B3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit TUG-3/AU-3 Mapper VC-3 Path Transmit Path Trace Message Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit TUG-3/AU-3 Mapper VC-3 Path Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved of the contract of th	0x00
0xN9C3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit TUG-3/AU-3 Mapper VC-3 Path – HP-RDI/LP-RDI Control Register – Byte 2	0x40
0xN9CA	Transmit TUG-3/AU-3 Mapper VC-3 Path – HP-RDI/LP-RDI Control Register – Byte 1	0xC0
0xN9CB	Transmit TUG-3/AU-3 Mapper VC-3 Path – HP-RDI/LP-RDI Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Serial Port Control Register	0x00

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0xN9D0 – 0xN9FF	Reserved	0x00
	DS3/E3 MAPPER BLOCK REGISTER	
Note: N represen	ts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xNA00 – 0xNB00	Unused	0x00
0xNB01	Mapper Control Register – Byte 2	0x00
0xNB02	Mapper Control Register – Byte 1	0x03
0xNB03	Mapper Control Register – Byte 0	0x80
0xNB04, 0xNB05	Unused	0x00
0xNB06	Receive Mapper Status Register – Byte 1	0x03
0xNB07	Receive Mapper Status Register – Byte 0	0x00
0xNB08 – 0xNB0A	Unused	0x00
0xNB0B	Receive Mapper Interrupt Status Register – Byte 0	0x00
0xNB0C – 0xNB0E	Unused	0x00
0xNB0F	Receive Mapper Interrupt Enable Register – Byte 0	0x00
0xNB10 – 0xNB12	Unused	0x00
0xNB13	T3/E3 Routing Register Byte	0x00
0xNB14 – 0xNB16	Reserved	0x00
0xNB17	Jitter Attenuator – Clock Smoother/Routing Register	0x00
0xNB18 – 0xNCFF	Reserved	0x00
	G-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESS	AGE BUFFER
Note: N represen	ts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xND00 – 0xND3F	Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block – Transmit J1 (Path) Trace Message Buffer	0x00
0xND40 – 0xNEFF	Reserved	0x00
	RECEIVE STM-0 SOH AND POH PROCESSOR BLOCK REGISTERS	
Note: N represen	ts the "Channel Number" and ranges in value from 0x05 to 0x07	
0xN000 – 0xN102	Reserved	0x00
0xN103	Receive STM-0 Section Control Register – Byte 0	0x00
0xN104 – 0xN105	Reserved	0x00
0xN106	Receive STM-0 Section Status Register – Byte 1	0x00
0xN107	Receive STM-0 Section Status Register – Byte 0	0x02
0xN108	Reserved	0x00
0xN109	Receive STM-0 Section Interrupt Status Register – Byte 2	0x00
0/11/03		



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0xN10B	Receive STM-0 Section Interrupt Status Register – Byte 0	0x00
0xN10C	Reserved	0x00
0xN10D	Receive STM-0 Section Interrupt Enable Register – Byte 2	0x00
0xN10E	Receive STM-0 Section Interrupt Enable Register – Byte 1	0x00
0xN10F	Receive STM-0 Section Interrupt Enable Register – Byte 0	0x00
0xN110	Receive STM-0 Section B1 Byte Error Count – Byte 3	0x00
0xN111	Receive STM-0 Section B1 Byte Error Count – Byte 2	0x00
0xN112	Receive STM-0 Section B1 Byte Error Count – Byte 1	0x00
0xN113	Receive STM-0 Section B1 Byte Error Count – Byte 0	0x00
0xN114	Receive STM-0 Section B2 Byte Error Count – Byte 3	0x00
0xN115	Receive STM-0 Section B2 Byte Error Count – Byte	0x00
0xN116	Receive STM-0 Section B2 Byte Error Count – Byte 1	0x00
0xN117	Receive STM-0 Section B2 Byte Error Count Byte	0x00
0xN118	Reserved	0x00
0xN119	Receive STM-0 Section MS-REI Event Count – Byte 3	0x00
0xN11A	Receive STM-0 Section MS-REI Event Count – Byte 2	0x00
0xN11B	Receive STM-0 Section MS-REI Event Count – Byte 1	0x00
0xN11C	Receive STM-0 Section MS-RELEvent Count – Byte 0	0x00
0xN11D – 0xN11E	Reserved 6	0x00
0xN11F	Receive STM-0 Section - Received K1 Byte Value Register	0x00
0xN120 – 0xN122	Reserved	0x00
0xN123	Receive STM-0 Section Received K2 Byte Value Register	0x00
0xN124 – 0xN126	Reserved	0x00
0xN127	Receive STM-0 Section – Received S1 Byte Value Register	0x00
0xN128 – 0xN12D	Reserved 🔗	0x00
0xN12E	Receive STM-0 Section – LOS Threshold Value – MSB	0xFF
0xN12F	Receive STM-0 Section – LOS Threshold Value – LSB	0xFF
0xN130	Reserved	0x00
0xN131	Receive STM-0 Section – Receive SF Set Monitor Interval – Byte 2	0x00
0xN132	Receive STM-0 Section – Receive SF Set Monitor Interval – Byte 1	0x00
0xN133	Receive STM-0 Section – Receive SF Set Monitor Interval – Byte 0	0x00
0xN134, 0xN135	Reserved	0x00
0xN136	Receive STM-0 Section – Receive SF Set Threshold – Byte 1	0x00



0xN137	Receive STM-0 Section – Receive SF Set Threshold – Byte 0	0x00				
0xN138 – 0xN139	Reserved	0x00				
0xN13A	Receive STM-0 Section – Receive SF Clear Threshold – Byte 1	0x00				
0xN13B	Receive STM-0 Section – Receive SF Clear Threshold – Byte 0	0x00				
0xN13C	Reserved	0x00				
0xN13D	Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 2	0x00				
0xN13E	Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 1	0x00				
0xN13F	Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 0	0x00				
0xN140 – 0xN141	Reserved	0x00				
0xN142	Receive STM-0 Section – Receive SD Set Threshold – Byte	0x00				
0xN143	Receive STM-0 Section – Receive SD Set Threshold – Byte 0	0x00				
0xN144, 0xN145	Reserved	0x00				
0xN146	Receive STM-0 Section – Receive SD Clear Threshold Byte 1	0x00				
0xN147	Receive STM-0 Section – SD Clear Threshold Byte 0	0x00				
0xN14B – 0xN14A	Reserved	0x00				
0xN14B	Receive STM-0 Section – Force SEF condition	0x00				
0xN14C – 0xN14E	Reserved 8	0x00				
0xN14F	Receive STM-0 Section – Receive Section Trace Message Buffer Control Register	0x00				
0xN150 – 0xN151	Reserved Contraction					
0xN152	Receive STM-0 Section – Receive SD Burst Error Count Tolerance – Byte 1	0x00				
0xN153	Receive STM-0 Section Receive SD Burst Error Count Tolerance – Byte 0	0x00				
0xN154, 0xN155	Reserved C S	0x00				
0xN156	Receive STM-0 Section - Receive SF Burst Error Count Tolerance - Byte 1	0x00				
0xN157	Receive STM-0 Section – Receive SF Burst Error Count Tolerance – Byte 0	0x00				
0xN158	Reserved	0x00				
0xN159	Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 2	0x00				
0xN15A	Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 1	0x00				
0xN15B	Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 0	0x00				
0xN15C	Reserved	0x00				
0xN15D	Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 2	0x00				
0xN15E	Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 1	0x00				
0xN15F	Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 0					
0xN160 – 0xN162	Reserved	0x00				



0xN163	Receive STM-0 Section – Auto AIS Control Register	0x00			
0xN164 – 0xN16A	Reserved	0x00			
0xN16B	Receive STM-0 Section – Auto AIS (in Downstream STM-0s) Control Register	0x00			
0xN16C - 0xN182	Reserved	0x00			
0xN183	Receive STM-0 Path – Control Register – Byte 2	0x00			
0xN184 - 0xN185	Reserved	0x00			
0xN186	Receive STM-0 Path – Control Register – Byte 1				
0xN187	Receive STM-0 Path – Status Register – Byte 0	0x00			
0xN188	Reserved	0x00			
0xN189	Receive STM-0 Path – Interrupt Status Register – Byte 2	0x00			
0xN18A	Receive STM-0 Path – Interrupt Status Register – Byte 1	0x00			
0xN18B	Receive STM-0 Path – Interrupt Status Register Byte	0x00			
0xN18C	Reserved	0x00			
0xN18D	Receive STM-0 Path – Interrupt Enable Register Byte 2	0x00			
0xN18E	Receive STM-0 Path – Interrupt Enable Register Byte 1	0x00			
0xN18F	Receive STM-0 Path – Interrupt Enable Register – Byte 0	0x00			
0xN190 - 0xN192	Reserved 8	0x00			
0xN193	Receive STM-0 Path – SONET Receive HP-RDI Register	0x00			
0xN194, 0xN195	Reserved	0x00			
0xN196	Receive STM-0 Path – Received Path Label Value (C2 Byte) Register	0x00			
0xN197	Receive STM 0 Path – Expected Path Label Value (C2 Byte) Register	0x00			
0xN198	Receive STM-0 Path – B3 Byte Error Count Register – Byte 3	0x00			
0xN199	Receive STM-0 Path - B3 Byte Error Count Register - Byte 2	0x00			
0xN19A	Receive STM-0 Path – B3 Byte Error Count Register – Byte 1	0x00			
0xN19B	Receive STM-0 Path – B3 Byte Error Count Register – Byte 0	0x00			
0xN19C	Receive STM-0 Path – REI-P Event Count Register – Byte 3	0x00			
0xN19D	Receive STM-0 Path – REI-P Event Count Register – Byte 2	0x00			
0xN19E	Receive STM-0 Path – REI-P Event Count Register – Byte 1 0x0				
0xN19F	Receive STM-0 Path – REI-P Event Count Register – Byte 0	0x00			
0xN1A0 – 0xN1A5	Reserved	0x00			
0xN1A6	Receive STM-0 Path – Pointer Value Register – Byte 1	0x00			
0xN1A7	Receive STM-0 Path – Pointer Value Register – Byte 0	0x00			
0xN1A8 – 0xN1BA	Reserved	0x00			



0xN1BB	Dessitive CTM & Deth. ALITO ALC Constral Destinator	0x00				
	Receive STM-0 Path – AUTO AIS Control Register					
0xN1BC – 0xN1BE	Reserved	0x00				
0xN1BF	Receive STM-0 Path – Serial Port Control Register	0x00				
0xN1C0 - 0xN1C2	Reserved	0x00				
0xN1C3	Receive STM-0 Path – SONET Receive Auto Alarm Register – Byte 0	0x00				
0xN1C4 -0xN1D2	Reserved	0x00				
0xN1D3	Receive STM-0 Path – Receive J1 Byte Capture Register	0x00				
0xN1D4 – 0xN1D6	Reserved	0x00				
0xN1D7	Receive STM-0 Path – Receive B3 Byte Capture Register	0x00				
0xN1D8 – 0xN1DA	Reserved	0x00				
0xN1DB	Receive STM-0 Path – Receive C2 Byte Capture Register	0x00				
0xN1DC – 0xN1DE	Reserved	0x00				
0xN1DF	Receive STM-0 Path – Receive G1 Byte Capture Register	0x00				
0xN1E0 - 0xN1E2	Reserved	0x00				
0xN1E3	Receive STM-0 Path – Receive F2 Byte Capture Register	0x00				
0xN1E4 – 0xN1E6	Reserved	0x00				
0xN1E7	Receive STM-0 Path – Receive H4 Byte Capture Register	0x00				
0xN1E8 – 0xN1EA	Reserved	0x00				
0xN1EB	Receive STM-0 Path - Receive Z3 Byte Capture Register	0x00				
0xN1EC – 0xN1EE	Reserved	0x00				
0xN1EF	Receive STM-0 Path Receive Z4 (K3) Byte Capture Register	0x00				
0xN1F0 – 0xN1F2	Reserved	0x00				
0xN1F3	Receive STM-0 Path - Receive Z5 Byte Capture Register	0x00				
0xN1F4 – 0xN1FF	Reserved 🔗	0x00				
Rec	EIVE STM-0 SOH PROCESSOR BLOCK – RECEIVE J0 (SECTION) TRACE MESSAGE BUFF	ER				
Note: N represen	ts the "Channel Number" and ranges in value from 0x05 to 0x07					
0xN300 – 0xN33F	Receive STM-0 POH Processor Block – Receive J0 (Section) Trace Message Buffer – Expected and Received	0x00				
0xN340 – 0xN3FF	Reserved 0x00					
Re	CEIVE STM-0 POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFE	R				
Note: N represen	ts the "Channel Number" and ranges in value from 0x05 to 0x07					
0xN500 – 0xN53F	Receive STM-0 POH Processor Block – Receive J1 (Path) Trace Message Buffer – Expected and Received	0x00				



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0xN540 – 0xN5FF	Reserved	0x00				
	TRANSMIT STM-0 SOH AND POH PROCESSOR BLOCK REGISTERS					
Note: N represer	nts the "Channel Numbers" and ranges in value from 0x05 to 0x07)					
0xN800 - 0xN901	0x00					
0xN902	Transmit STM-0 Section – SONET Transmit Control Register – Byte 1	0x00				
0xN903	Transmit STM-0 Section – SONET Transmit Control Register – Byte 0	0x00				
0xN904 – 0xN922	Reserved	0x00				
0xN923	Transmit STM-0 Section – B1 Byte Error Mask Register	0x00				
0xN924 – 0xN92A	Reserved	0x00				
0xN92B	Transmit STM-0 Section – Transmit B2 Bit Error Mask Register Byte 0	0x00				
0xN92C – 0xN92D	Reserved	0x00				
0xN92E	Transmit STM-0 Section – K1K2 (APS) Byte Value Register – Byte 1	0x00				
0xN92F	Transmit STM-0 Section – K1K2 (APS) Byte Value Register – Byte 0	0x00				
0xN930 – 0xN932	Reserved	0x00				
0xN933	Transmit STM-0 Section – MS-RDI Control Register	0x00				
0xN934 – 0xN936	Reserved	0x00				
0xN937	ransmit STM-0 Section – M0M1 Byte Value Register 0x00					
0xN938 - 0xN93A	Reserved	0x00				
0xN93B	Transmit STM-0 Section - S1 Byte Value Register	0x00				
0xN93C – 0xN93E	Reserved	0x00				
0xN93F	Transmit STM-0 Section – F1 Byte Value Register	0x00				
0xN940 – 0xN942	Reserved	0x00				
0xN943	Transmit STM 9 Section – E1 Byte Value Register	0x00				
0xN944 – 0xN946	Reserved	0x00				
0xN947	Transmit STM-0 Section – E2 Byte Value Register	0x00				
0xN948 – 0xN94A	Reserved	0x00				
0xN94B	Transmit STM-0 Section – J0 Byte Value Register	0x00				
0xN94C – 0xN94E	Reserved	0x00				
0xN94F	Transmit STM-0 Section – Section Trace Message Control Register	0x00				
0xN950 – 0xN981	Reserved	0x00				
0xN982	Transmit STM-0 Path – SONET Control Register – Byte 1	0x00				
0xN983	Transmit STM-0 Path – SONET Control Register – Byte 0	0x00				
0xN984 – 0xN992	Reserved	0x00				

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0xN993	Transmit STM-0 Path – Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995		0x00
	Reserved	
0xN996	Transmit STM-0 Path – B3 Byte Control Register	0x00
0xN997	Transmit STM-0 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit STM-0 Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit STM-0 Path – Transmit G1 Byte Value Register	0x00
0xN9A0 - 0xN9A2	Reserved	0x00
0xN9A3	Transmit STM-0 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit STM-0 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit STM-0 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit STM-0 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 - 0xN9B2	Reserved	0x00
0xN9B3	Transmit STM-0 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 - 0xN9B6	Reserved O P O	0x00
0xN9B7	Transmit STM-0 Path Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit STM0 Path Transmit Path Trace Message Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit STM-0 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved	0x00
0xN9C3	Transmit STM-0 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit STM-0 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit STM-0 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit STM-0 Path – HP-RDI Control Register – Byte 2	0x40
0xN9C2	Transmit STM-0 Path – HP-RDI Control Register – Byte 1	0xC0



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

0xN9CB	Transmit STM-0 Path – HP-RDI Control Register – Byte 0					
0xN9CC – 0xN9CE	Reserved 0x0					
0xN9CF	Transmit STM-0 Path – Transmit Path Serial Port Control Register	0x00				
0xN9D0 –0xN9FF	Reserved	0x00				
Tra	NSMIT STM-0 SOH PROCESSOR BLOCK – TRANSMIT J0 (PATH) TRACE MESSAGE BUFF	ER				
Note: N represe	nts the "Channel Number" and ranges in value from 0x05 to 0x07					
0xNB00 – 0xNB3F	ransmit STM-0 POH Processor Block – Transmit J0 (Path) Trace Message					
0xNB40 – 0xNBFF	Reserved 0x0					
TRA	NSMIT STM-0 POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFF	ER				
Note: N represei	nts the "Channel Number" and ranges in value from 0x05 to 0x07					
0xND00 – 0xND3F	Transmit STM-0 POH Processor Block – Transmit J1 (Path) Trace Message C Buffer					
0xND40 – 0xNDFF	Reserved 0x00					

He data in many notices in the intermediates in the product are be ordered to be order

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



1.2 THE OPERATION CONTROL BLOCK

The Operation Control Block is responsible for the following functions.

- Control of the Interrupt Structure (at the Highest Level within the XRT94L33)
- Control of the Clock Synthesizer block
- Control of the STS-3/STM-1 Telecom Bus Interface
- Control of the STM-0 Telecom Bus Interfaces

The register map for the Operation Control block is presented in the Table below. Additionally, a detailed description of each of the "Operation Control" Block registers is presented below.

1.2.1 OPERATION CONTROL BLOCK REGISTER

Table 2: Operation Control Register Address Map

Address Location	REGISTER NAME	DEFAULT VALUE			
0x0000 – 0x00FF	Reserved	0x00			
0x0100	Operation Control Register – Byte 3	0x00			
0x0101	Operation Control Register – Byte 2	0x00			
0x0102	Reserved	0x00			
0x0103	Operation Control Register – Byte 0	0x00			
0x0104	Operation Status Register – Byte 3 (Device ID)	0xE3			
0x0105	Operation Status Register – Byte 2 (Revision 4D)	0x01			
0x0106 – 0x010A	Reserved	0x00			
0x010B	Operation Interrupt Status Register - Byte 0	0x00			
0x010C - 0x010E	Reserved	0x00			
0x010F	Operation Interrupt Enable Register – Byte 0				
0x0110 - 0x0111	Reserved	0x00			
0x0112	Operation Block Interrupt Status Register – Byte 1	0x00			
0x0113	Operation Block Interrupt Status Register – Byte 0	0x00			
0x0114 – 0x0115	Reserved	0x00			
0x0116	Operation Block Interrupt Enable Register – Byte 1	0x00			
0x0117	Operation Block Interrupt Enable Register – Byte 0	0x00			
0x0118 – 0x0119	Reserved	0x00			
0x0111A	Reserved 0x00				
0x011B	Mode Control Register – Byte 0	0x00			
0x011C – 0x011E	Reserved				
0x011F	Loop-back Control Register – Byte 0	0x00			
0x0120	Channel Interrupt Indicator – Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block	0x00			



Address Location	Address Location Register Name				
0x0121	Reserved	0x00			
0x0122	Channel Interrupt Indicator – DS3/E3 framer Block	0x00			
0x0123	Channel Interrupt Indicator – Receive STM-0 POH Processor Block	0x00			
0x0124	Channel Interrupt Indicator – Receive STM-0 SOH Processor Block	0x00			
0x0125	Reserved	0x00			
0x0126	Channel Interrupt Indicator – STM-0/DS3/E3 Mapper Block	0x00			
0x0127	Reserved	0x00			
0x0128	Reserved	0x00			
0x0129	Reserved	0x00			
0x012A	Reserved	0x00			
0x012B – 0x012F	Unused	0x00			
0x012E	Reserved	0x00			
0x012F	Reserved	0x00			
0x0130	Reserved	0x00			
0x0131	Reserved	0x00			
0x0132	Interface Control Register - Byte	0x00			
0x0133	Interface Control Register – Byte 0.00	0x00			
0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3 0x00				
0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00			
0x0136	Reserved	0x00			
0x0137	STS-3/STM-1/Telecom Bus Control Register – Byte 0	0x00			
0x0138	Reserved	0x00			
0x0139	Interface Control Register – Byte 2 – STM-0 Telecom Bus 2	0x00			
0x013A	Interface Control Register – Byte 1 – STM-0 Telecom Bus 1	0x00			
0x013B	Interface Control Register – Byte 0 – STM-0 Telecom Bus 0 0x00				
0x013C	Interface Control Register – STM-0 Telecom Bus Interrupt Register 0x00				
0x013D	Interface Control Register – STM-0 Telecom Bus Interrupt Status Register 0				
0x013E	Interface Control Register – STM-0 Telecom Bus Interrupt Register # 2 0x00				
0x013F	Interface Control Register – STM-0 Telecom Bus Interrupt Enable Register	0x00			
0x0140 – 0x0145	Reserved	0x00			
0x0146	Reserved	0x00			
0x0147	Operation General Purpose Input/Output Register	0x00			

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Address Location	REGISTER NAME	DEFAULT VALUE	
0x0148 - 0x0149	Reserved	0x00	
0x014A	Reserved	0x00	
0x014B	Operation General Purpose Input/Output Direction Register	0x00	
0x014C - 0x014F	Reserved	0x00	
0x0150	Operation Output Control Register – Byte 1	0x00	
0x0151 –0x0152	Reserved	0x00	
0x0153	Operation Output Control Register – Byte 0	0x00	
0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00	
0x0155 – 0x0156	Reserved	0x00	
0x0157	Operation Slow Speed Port Control Register –Byte	0x00	
0x0158	Operation – DS3/E3/STM-0 Clock Frequency Out of Range Detection – Direction Register	0x00	
0x0159	Reserved	0x00	
0x015A	Operation – DS3/E3/STM-0 Clock Frequency – DS3 Out of Range Detection Threshold Register	0x00	
0x015B	Operation – DS3/E3/STM-0 Clock Frequency STM-0/E3 Out of Range Detection Threshold Register	0x00	
0x015C	Reserved of the second	0x00	
0x015D	Operation – DS3/E3/STM-0 Prequency Out of Range Interrupt Enable Register – Byte 0	0x00	
0x015E	Reserved	0x00	
0x015F	Operation – DS3/E3/STM-0 Frequency Out of Range Interrupt Status Register – Byte 0	0x00	
0x0160 – 0x017F	Reserve	0x00	
0x0180	APS Mapping Register	0x00	
0x0181	APS Control Register	0x00	
0x0182 - 0x0193	Reserved	0x00	
0x0194	APS Status Register	0x00	
0x0195	Reserved	0x00	
0x0196	APS Status Register	0x00	
0x0197	APS Status Register	0x00	
0x0198	APS Interrupt Register	0x00	
0x0199	Reserved	0x00	
0x019A	APS Interrupt Register	0x00	
0x019B	APS Interrupt Register	0x00	



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Address Location	REGISTER NAME	DEFAULT VALUE
0x019C	APS Interrupt Register	0x00
0x019D	Reserved	0x00
0x019E	APS Interrupt Enable Register	0x00
0x019F	APS Interrupt Enable Register	0x00
0x01A0 – 0x01FF	Reserved	0x00

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

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1.2.2 OPERATION CONTROL REGISTER DESCRIPTION

Table 3: Operation Control Register – Byte 3 (Address Location= 0x0100)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused						Configura	ation Control
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
Bit 7 – Bit 2	Unused	R/O	Please set to "0" for normal operation.
Bit 1 – Bit 0	Configuration Control	R/W	Configuration Control:
	Control		These two READ/WRITE bit-fields permits the user to specify the mode/configuration that the XRT94L33 device should operate in. Please set to "01" for Mapper applications.



Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused					Enable Interrupt Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Table 4: Operation Control Register – Byte 2 (Address Location= 0x0101)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
Bit 7 – Bit 3	Unused	R/O	Please set to "0" for normal operation.
Bit 2	Interrupt Write to Clear/RUR	R/W	Interrupt – Write to Clear/RUR Select:
	to Clean/ROR		This READ/WRITE bit-field permits the user to configure all of the "Source- Level" Interrupt Status bits (within the XRT94L33) to either be "Write to Clear" (WTC) or "Reset-upon-Read" (RUR) bits.
			0 – Configures all "Source-Level" Interrupt Status register bits to function as "Reset-upon-Read" (RUR).
			1 – Configures all "Source-Level" Interrupt Status register bits to function as "Write-to-Clear" (WTC)
Bit 1	Enable Interrupt	R/W	Enable Auto-Clear of Interrupts Select:
	Clear		This READ/WRITE bit field permits the user to configure the XRT94L33 to automatically disable all interrupts that are activated.
			0 Configures the chip to NOT automatically disable any Interrupts following their activation.
		K	1 – Configures the chip to automatically disable all Interrupts following their activation.
Bit 0	Interrupt Enable	R/W	Interrupt Enable:
	or	o ree	This READ/WRITE bit-field permits the user to configure the XRT94L33 to generate interrupt requests to the Microprocessor.
	thet	9 M3	0 – Configures the chip to NOT generate interrupt to the Microprocessor. All interrupts are disabled and the Microprocessor must poll the register bits.
	` 8°°	²	1 – Configures the chip to generate interrupts the Microprocessor.
	l f	2	



						,			
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Reserved								
R/W	R/W	R/O	R/O	R/W	R/O	R/O	R/W		
1	1	0	0	0	0	0	0		

Table 5: Operation Control Register – Byte 0 (Address Location= 0x0103)

BIT NUMBER	NAME	Түре	DESCRIPTION				
Bits 7 - 1	Unused	R/O	Please set to "0" for normal operation				
Bit 0	SW Reset	R/W	 Software Reset – SONET Block: This READ/WRITE bit-field permits the user to command a software reset to the SONET/SDH block. If the user invokes a software reset to the SONET/SDH blocks then all of the internal state machines will be reset to their default conditions; and each of the Receive STM-0/STM-1 SOH Processor blocks will undergo a re-frame operation. A "0" to "1" transition, within this bit-field commands this Software Reset. Notes: This Software Reset does not reset the command registers to their default state. This can only be achieved by executing a "Hardware RESET" (e.g., by pulling the RESET_L* input pin "LOW"). This Software Reset does not affect the DS3/E3 Framer blocks. The Software Reset bit-field, for the DS3/E3 Framer block can be found in each of the 3 "DS3/E3 Operating Mode" registers (Address Location= 0xNF00). 				

LOW"). Ti blocks. The can be found (Address Lou Address Lou Address Lou Address Lou Address Lou Address Lou Address Lou



Table 6: Operation Status Register – Byte 3 (Address Location= 0x0104)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Device ID Value									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
1	1	1	0	0	0	1	1			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Device ID Value	R/O	Device ID Value:
			This READ-ONLY bit-field is set to the value "0xE3" and permits the user's software code to uniquely identify this device as being the XRT94L33.
			this rec

Table 7: Operation Status Register – Byte 2 (Address Location 20x0105)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
Revision Number Value											
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O				
0	0	0	0	0 0	0	0	1				
	<u> </u>										

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	
7 – 0	Revision Number Value	R/O	Revision NumberValue: This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value "0x01". This register permits the user's software code to uniquely identify the revision number of this device.
	The production of the producti	ines n	othe

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Віт 7 Віт 6 Віт 5 Віт 4 Віт 3 Віт 2 Віт 1 BIT 0 Unused TB Parity Error Interrupt Status RUR/WTC R/O R/O R/O R/O R/O R/O R/O 0 0 0 0 0 0 0 0

Table 8: Operation Interrupt Status Register – Byte 0 (Address Location= 0x010B)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
Bit 7 – Bit 1	Unused	R/O	Please set to "0" for normal operation
Bit 0	TB Parity Error Interrupt Status	RUR/ WTC	 Telecom Bus Parity Error Interrupt Status: This "RESET-upon-READ" bit-field indicates whether or not the "Detection of 155.52Mbps Telecom Bus - Parity Error" interrupt has occurred since the last read of this register bit. 0 – Indicates that the "Detection of 155.52Mbps Telecom Bus - Parity Error" interrupt has NOT occurred since the last read of this register bit. 1 – Indicates that the "Detection of 155.52Mbps Telecom Bus - Parity Error" interrupt has occurred since the last read of this register bit. 1 – Indicates that the "Detection of 155.52Mbps Telecom Bus - Parity Error" interrupt has occurred since the last of this register bit. Note: This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.

Table 9: Operation Interrupt Enable Register – Byte 0 (Address Location= 0x010F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2	Віт 1	Віт 0				
			Unused		2 C	Telecom Bus Parity Error				
				Q. V. XO.		Interrupt Enable				
R/O	R/O	R/O	R/O	R/O R/O	R/O	R/W				
0	0	0	0	00 00 0	0	0				
	NU X X X									

0

		<u> </u>	
BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 1	Unused	B /O	Please set to "0" for normal operation
Bit 0	TB Parity Error	R/W	Telecom Bus Parity Error Interrupt Enable:
	Interrupt Enable	an	This "READ/WRITE" bit-field permits the user to either enable or disable the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			0 – Disables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			1 – Enables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			Note: This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.



Table 10: Operation Block Interrupt Status Register – Byte 1 (Address Location= 0x0112)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Operation Control Block Interrupt Status	DS3/E3 Mapper Block Interrupt Status	Unused	Receive STM-0 SOH Processor Block Interrupt Status	Receive STM-0 POH Processor Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Receive Line Interface Block Interrupt Status	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Bit Number	Nаме	Түре	DESCRIPTION
7	Operation Control	R/O	Operation Control Block Interrupt Status:
	Block Interrupt Status		This READ-ONLY bit-field indicates whether or not an Operation Control Block-related Interrupt is awaiting service.
			0 – Indicates that no Operation Control Block Interrupts are awaiting service.
			1 – Indicates that at least one "Operation Control Block" Interrupt is awaiting service.
6	DS3/E3 Mapper Block	R/O	DS3/E3 Mapper Block Interrupt Status:
	Interrupt Status		This READ-ONLY bit-field indicates whether or not a DS3/E3 Mapper Block-related interrupt is awaiting service.
			0, Indicates that no DS3/E3 Mapper Block interrupt is awaiting service.
		.0	1 – Indicates that at least one "DS3/E3 Mapper Block" Interrupt is awaiting service.
5	Unused	R/O	le le
4	Receive STM-0 SOH	R/O	Receive STM-0 SOH Processor Block Interrupt Status:
	Processor Block Interrupt Status	new	This READ-ONLY bit-field indicates whether or not an "Receive STM-0 SOH Processor" Block Interrupt is awaiting service.
	the ta	d may	0 – Indicates that no "Receive STM-0 SOH Processor" block interrupt is awaiting service.
	0.2		1 – Indicates that at least one "Receive STM-0 SOH Processor" block interrupt is awaiting service.
3	Receive STM-0 POH Processor Block	R/O	Receive STM-0 Path Overhead (POH) Processor Block Interrupt Status:
	Interrupt Status		This READ-ONLY bit-field indicates whether or not an "Receive STM-0 POH Processor" Block Interrupt is awaiting service.
			0 – Indicates that no "Receive STM-0 POH Processor" block interrupt is awaiting service.
			1 – Indicates that at least one "Receive STM-0 POH Processor" block interrupt is awaiting service.
2	DS3/E3 Framer Block	R/O	DS3/E3 Framer Block Interrupt Status
	Interrupt Status		This READ-ONLY bit-field indicates whether or not a "DS3/E3 Framer Block" interrupt is awaiting service.

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			 0 – Indicates that no "DS3/E3 Framer" block interrupt is awaiting service. 1 – Indicates that at least one "DS3/E3 Framer" block interrupt is awaiting service.
1	Receive Line Interface Block Interrupt Status	R/O	 Receive Line Interface Block Interrupt Status This READ-ONLY bit-field indicates whether or not a "Receive Line Interface Block" interrupt is awaiting service. 0 – Indicates that no "Receive Line Interface" block interrupt is awaiting service. 1 – Indicates that at least one "Receive Line Interface" block interrupt is awaiting service.
0	Unused	R/O	

Table 11: Operation Block Interrupt Status Register – Byte 0 (Address Location= 0x0113)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Receive STM-1 SOH Processor Block Interrupt Status	Receive TUG-3/AU-3 Mapper VC- 3 POH Processor Block Interrupt Status		s mentione	Unused		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	00	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Unused	R/O	a le se
6	Receive STM-1 SOH Processor Block Interrupt Status	RO STO	 Receive STM-1 SOH Processor Block Interrupt Status: This READ-ONLY bit-field indicates whether or not a "Receive STM-1 SOH Processor Block" interrupt is awaiting service. 0 – Indicates that no "Receive STM-1 SOH Processor Block" Interrupt is awaiting service. 1 – Indicates that at least one "Receive STM-1 SOH Processor Block" interrupt is awaiting service.
5	Receive SONET POH Processor Block Interrupt Status	R/O	 Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Interrupt Status: This READ-ONLY bit-field indicates whether or not a "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" interrupt is awaiting service. 0 – Indicates that no "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" Interrupt is awaiting service. 1 – Indicates that at least one "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" Interrupt is awaiting service.
4 - 0	Unused	R/O	



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Table 12: Operation Block Interrupt Enable Register – Byte 1 (Address Location= 0x0116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Operation Control Block Interrupt Enable	DS3/E3 Mapper Block Interrupt Enable	Unused	Receive STM-0 SOH Processor Block Interrupt Enable	Receive STM-0 POH Processor Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Receive Line Interface Block Interrupt Enable	Unused
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Operation Control Block Interrupt Enable	R/W	 Operation Control Block Interrupt Enables This READ/WRITE bit-field permits the user to either enable or disable the Operation Control Block for interrupt generation. If the user writes a "0" into this register bit and disables the "Operation Control Block, then all "Operation Control Block" interrupts will be disabled for interrupt generation. If the user writes a "1" into this register bit, he/she will still need to enable the individual "Operation Control Block" interrupt. 0 – Disables all "Operation Control Block" interrupts within the device. 1 – Enables the "Operation Control Block" at the "Block-Level" for interrupt generation
6	DS3/E3 Mapper Block Interrupt Enable	R/W	 DS3/E3 Mapper Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Mapper Block for interrupt generation. If the user writes a "0" into this register bit then all "DS3/E3 Mapper Block" interrupts will be disabled for interrupt generation. If the user writes a "1" into this register bit, he/she will still need to enable the individual "DS3/E3 Mapper Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "DS3/E3 Mapper Block" interrupts within the device. 1 – Enables the "DS3/E3 Mapper Block" at the "Block-Level"
5	Unused	R/0	
4	Receive STM- 0 SOH Block Interrupt Enable	B W	 Receive STM-0 SOH (Section Overhead) Processor Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the Receive STM-0 SOH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STM-0 SOH Processor Block" (for interrupt generation), then all "Receive STM-0 SOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STM-0 SOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STM-0 SOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disables all "Receive STM-0 SOH Processor Block" interrupts within the device. 1 - Enables the "Receive STM-0 SOH Processor Block" at the "Block-Level". Note: This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.



2	Possive STM		Ressive STM (DOH (Deth Overhead) Processor Black Interview Fright-
3	Receive STM- 0 POH Block	R/W	Receive STM-0 POH (Path Overhead) Processor Block Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the Receive STM-0 POH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STM-0 POH Processor Block" (for interrupt generation), then all "Receive STM-0 POH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STM-0 POH Processor Block" or POH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt.
			0 – Disables all "Receive STM-0 POH Processor Block" interrupts within the device.
			1 – Enables the "Receive STM-0 POH Processor Block" at the "Block-Level".
			Note: This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.
2	DS3/E3	R/W	DS3/E3 Framer Block Interrupt Enable
	Framer Block Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Framer Block for interrupt generation. If the user writes a "0" to this register bit and disables the "DS3/E3 Framer Block" (for interrupt generation), then all "DS3/E3 Framer Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "DS3/E3 Framer Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt.
			0 – Disables all "DS3/E3 Framer Block" interrupts within the device.
			1 – Enables the "DS3/E3 Framer Block" at the "Block-Level".
1	Receive Line	R/W	Receive Line Interface Block Interrupt Enable:
	Interface Block Interrupt Enable	8	This READ/WRITE bit permits the user to either enable or disable the Receive Line Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive Line Interface Block" (for interrupt generation), then all "Receive Line Interface Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive Line Interface Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive Line Interface Block" interrupts within the device.
		40	
		0	Enables the "Receive Line Interface Block" at the "Block-Level".
0	Unused	CR/O	No
		80	8
		ં જે	



Table 13: Operation Block Interrupt Enable Register – Byte 0 (Address Location= 0x0117)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Receive STM-1 SOH Block Interrupt Enable	Receive TUG-3/AU-3 Mapper VC- 3 POH Block Interrupt Enable			Unused		
R/O	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	th ure
6	Receive STM-1 SOH Block Interrupt Enable	R/W	 Receive STM-1 SOH Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Receive STM-1 SOH Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STM-1 SOH Processor Block" (for interrupt generation), then all "Receive STM-1 SOH Processor Block" (for interrupt generation), then all "Receive STM-1 SOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STM-1 SOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive STM-1 SOH Processor Block" interrupts within the device 1 Enables the "Receive STM-1 SOH Processor Block" at the "Block Level" for interrupt generation.
5	Receive TUG- 3/AU-3 Mapper VC- 3 POH Block Interrupt Enable	RMO	 Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" for interrupt generation. If the user writes a "0" into this register bit and disables the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" (for interrupt generation), then all "Receive SONET Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, then he/she will still need to enable the individual "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" Interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" Interrupts within the device. 1 – Enables the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block" at the "Block Level" for interrupt generation.
4 - 0	Unused	R/O	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 14: Mode Control Register – Byte 0 (Address Location= 0x011B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Disable Jitter Attenuator Fast Lock	TBUS0_IS _SDH	V1_PULSE _EN	TBUS0_ MASTER		RESERVED		AU-3/TUG-3* Mapping Select
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	DISFASTLOCK	R/W	Disable Jitter Attenuator Fast lock:
			This READ/WRITE bit field is used to disable the fast lock feature for the Jitter Attenuator block
			0 – Fast Lock feature is enabled
			1 – Fast Lock feature is disabled
			Note: To configure the XRT94L33 such that it will comply with the Telcordia GR-253-CORE APS Recovery time requirements of 50ms, then the "Fast Lock" feaure MUST be enabled within the Jitter Attenuator block, by setting this bit-field to "0"
6	TBUS0_IS_SDH	R/W	Telecom Bus 0 operating in SDH Mode
			This bit is used to qualify and process a Highrate SDH signal for Subrate Telecom Bus 0 operation.
			0 - Clearing this bit will disable SDH format signal validation on Telecom Bus 0 Subrate Telecom Bus 0 RxD[7:0] data bus ouput will be disabled.
			1 - Setting this bit will enable SDH format signal validation on Telecom Bus 0. It enables RxD[7:0] data bus output upon reception of a valid SDH signal format structure.
		du	Note: This bit must be enabled in SDH mode for Subrate Telecom Bus 0 operation. This bit is ignored and does not apply in SONET mode of operation.
5	V1_PULSE_EN	R/W	V1 Pulse Enable
	the	atand	This bit provides theo ption of using an additional pulse on the Telecom Drop Bus RxD_C1J1 output pin and Telecom Add Bus TxA_C1J1 pin to denote the location or onset of V1 Byte within the Synchronous Payload Envelope/Virtual Container of the SONET/SDH frame whenever the Telecom Bus is processing the Virtual Tributary Group/Virtual Container multi-frame boundary
			0 - Telecom Bus 0 in STS-3/STM-1 mode will not indicate a V1 pulse on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary.
			1 - Telecom Bus 0 in STS-3/STM-1 mode has V1 pulse added on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary
4	TBUS0_MASTER	R/W	Select Phase Timing Reference
			This bit selects TxA_C1J1V1 and TxA_PL phase timing reference when operating the Subrate Add Telecom Bus 0 in Rephase OFF mode.
			0 - Add Telecom Bus 0 timing in Slave Mode. TxA_C1J1V1 and TxA_PL pins are inputs.



			1 - Add Telecom Bus 0 timing in Master Mode. TxA_C1J1V1 and TxA_PL pins are outputs.
3– 1	Unused	R/O	
0	AU-3/TUG-3*	R/W	AU-3/TUG-3 Mapping Select:
	Mapping Select		This READ/WRITE bit-field is used to to specify how the DS3/E3 data, associated with Channels 0, 1 and 2 are mapped into an SDH signal, as indicated below.
			0 – DS3/E3 Channels are mapped into a VC-3, a TU-3, and then finally a TUG-3 structure, when being mapped into an STM-1 signal.
			1 – DS3/E3 Channels are mapped into a VC-3 and then an AU-3 when being mapped into an STM-1 signal.
			Note: This register bit is only active if the XRT94L33 has been configured to operate in the SDH Mode.

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 15: Loop-back Control Register – Byte 0 (Address Location= 0x011F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Unused				Loop-back[3:0]					
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION			
7 - 4	Unused	R/O					
3 - 0	Loop-back[3:0]	R/W	Loop-back Mode[3:0]				
				VRITE bits-fields permit the user to configure the e in a variety of loop-back modes, as is tabulated			
			Loop-back[3:0]	Resulting Loop back Mode			
			0000	Normal Mode (e.g., No Loop-back Mode)			
			0001	Remote Line Loop-back:			
			me	In this mode, all data that is received by the "Receive STM-1 SOH Processor" block will be routed to the "Transmit STM-1 SOH Processor block.			
			or products in a construct of products in a construct of the construct of	Note: If the user invokes this loop-back, then he/she must configure the Transmit STM-0/STM-1 circuitry to operate in the Loop-timing mode by setting Bit 6 (STM-1 Loop-Timing Mode) within the Receive Line Interface Control Register – Byte 1, to "1" (Address Location: 0x0302).			
			0010	Local Section Loop-back:			
	e	roche	anot	In this mode, all data that is being output via the "Transmit STM-1 SOH Processor" block will also be internally routed to the "Receive STM-1 SOH Processor" block.			
		8° 8°		NOTES:			
		SIL		1. If the user configures the XRT94L33 device to operate in the "Local Section Loop-back" Mode, then, in addition to "routing" the Transmit Output STM-1 data back into the "Receive Path", the Transmit Output STM-1 data is still output via either the Transmit STM-1 PECL Interface or the Transmit STM-1 Telecom Bus Interface.			
				2. The user must disable all "Automatic Transmission of AU-AIS/TU-AIS/AIS indicator upon Defects" features (within the chip) in order to permit this loop- back to function properly.			
			0011	Local Path Loop-back:			
				In this mode, all data that is output by the			



			Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block (e.g., towards the "Transmit STM-1 SOH Processor" block) will be internally routed to the "Receive TUG-3/AU-3 Mapper VC- 3 POH Processor" block.
			NOTES:
			 This setting applies to all 3 Transmit TUG-3/AU-3 Mapper VC-3 POH Processor and Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks within the XRT94L33 device.
			2. The user must disable all "Automatic Transmission of AU-AIS/TU-AIS/AIS indicator upon Defects" features (within the chip) in order to permit this loop- back to function properly.
		0100 - 1111	Reserved – Do Not Use
the data	uct of	0100 - 1111 0100 - 1111	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 16: Channel Interrupt Indicator – Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block (Address Location= 0x0120)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
	Ma Pr		Receive AU- 4 Mapper/VC- 4 POH Processor Block Interrupt	Receive AU-4 Mapper/ VC-3 POH Block Interrupt	Receive TUG-3/AU-3 Mapper VC- 3 POH Block Interrupt Ch 2	Receive TUG-3/AU-3 Mapper VC- 3 POH Block Interrupt Ch 1	Receive TUG-3/AU-3 Mapper VC- 3 POH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7-5	Unused		in the
4	Receive AU-4	R/O	Receive AU-4 Mapper/VC-4 POH Processor Block Interrupt:
	Mapper/VC-4 POH Block Interrupt		This READ/ONLY bit-field indicates whether or not the "Receive AU-4 Mapper/VC-4 POH Processor" block is current requesting interrupt service, as described below.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT declaring an Interrupt.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring an Interrupt.
			Note: This register bit is only active if the XRT94L33 has been configured to support an AU-4 Mapper/VC-4 signal via Channel 0.
3	Receive AU-4	R/O	Receive AU-4 Mapper/VC-3 POH Processor Block Interrupt:
	Mapper/VC-3 POH Block Interrupt		This READ/ONLY bit-field indicates whether or not the "Receive AU-4 Mapper/VC-3, POH Processor" block is currently requesting Interrupt service, as described below.
		rodu	0 Indicates that the Receive AU-4 Mapper/VC-3 POH Processor block is NOT currenty declaring an Interrupt.
	the	8.9	1 Indicates that the Receive AU-4 Mapper/VC-3 POH Processor block is currently declaring an interrupt.
		93 UG	Note: This register bit is only if the XRT94L33 device has been configured to operate in the SDH/TUG-3 Mapper Mode.
2	Receive TUG- 3/AU-3 Mapper	R/Ŏ	Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Interrupt – Channel 2:
	VC-3 POH Block Interrupt Channel 2		This READ/ONLY bit-field indicates whether or not the "Receive TUG-3/AU- 3 Mapper VC-3 POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below.
			0 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 2 is NOT currently declaring an Interrupt.
			1 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 2 is currently declaring an interrupt.
1	Receive TUG- 3/AU-3 Mapper	R/O	Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Interrupt – Channel 1:
	VC-3 POH Block Interrupt Channel 1		This READ/ONLY bit-field indicates whether or not the "Receive TUG-3/AU- 3 Mapper VC-3 POH Processor" block, associated with Channel 1 is dependence on Interrupt, as described below.



			declaring an Interrupt, as described below.
			0 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 9 is NOT declaring an Interrupt.
			1 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 9 is currently declaring an interrupt.
0	Receive TUG- 3/AU-3 Mapper VC-3 POH Block Interrupt Channel 0	R/O	 Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, associated with Channel 0 is currently declaring an interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 17: Channel Interrupt Indicator – DS3/E3 Framer Block (Address Location= 0x0122)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				DS3/E3 Framer Block Interrupt Ch 2	DS3/E3 Framer Block Interrupt Ch 1	DS3/E3 Framer Block Interrupt Ch 0	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 –3	Unused	R/O	
2	DS3/E3 Framer Block Interrupt Ch 2	R/O	 DS3/E3 Framer Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 2 is NOT currently declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 2 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 2 has been configured to operate in the DS3/E3 Mode.
1	DS3/E3 Framer Block Interrupt Ch 1	R/O Produ data and	 DS3/E3 Framer Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 1 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 1 has been configured to operate in the DS3/E3 Mode.
0	DS3/E3 Framer Block Interrupt Ch 0	R/O	 DS3/E3 Framer Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 0 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 0 has been configured to operate in the DS3/E3 Mode.



Table 18: Channel Interrupt Indicator – Receive STM-0 POH Processor Block (Address Location= 0x0123)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused					Receive STM-0 POH Block Interrupt Ch 2	Receive STM- 0 POH Block Interrupt Ch 1	Receive STM- 0 POH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive STM-0 POH Block Interrupt Channel 2	R/O	 Receive STM-0 POH Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STM-0 POH Processor block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive STM-0 POH Processor block, associated with Channel 2 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 2 has been configured to operate in the STM-0 Mode.
1	Receive STM-0 POH Block Interrupt Channel 1	R/O	 Receive STM-9 POH Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 POH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0. The Receive STM-0 POH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 1 - The Receive STM-0 POH Processor block, associated with Channel 1 is ourrently declaring an interrupt. NOTE: This bit-field is only active if Channel 1 has been configured to operate in the STM-0 Mode.
0	Receive STM-0 POH Block Interrupt Channel 0	ŇŘ/O	 Receive STM-0 POH Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STM-0 POH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STM-0 POH Processor block, associated with Channel 0 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 0 has been configured to operate in the STM-0 Mode.

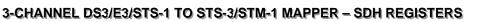




Table 19: Channel Interrupt Indicator – Receive STM-0 SOH Processor Block (Address Location= 0x0124)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused		Receive STM- 0 SOH Block Interrupt Ch 2	Receive STM- 0 SOH Block Interrupt Ch 1	Receive STM-0 SOH Block Interrupt Ch 0	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive STM-0 SOH Block Interrupt Channel 2	R/O	 Receive STM-0 SOH Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 SOH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STM-0 SOH Processor block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive STM-0 SOH Processor block, associated with Channel 2 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 2 has been configured to operate in the STM-0 Mode.
1	Receive STM-0 SOH Block Interrupt Channel 1	R/O Produ data	 Receive STM-0 SOH Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 SOH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive STM-0 SOH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 14 The Receive STM-0 SOH Processor block, associated with Channel 1 is ourrently declaring an interrupt. NOTE: This bit-field is only active if Channel 1 has been configured to operate in the STM-0 Mode.
0	Receive STM-0 SOH Block Interrupt Channel 0	R	 Receive STM-0 SOH Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive STM-0 SOH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STM-0 SOH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STM-0 SOH Processor block, associated with Channel 0 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 0 has been configured to operate in the STM-0 Mode.

Table 20: Channel Interrupt Indicator –DS3/E3 Mapper Block (Address Location= 0x0126)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3		Віт 2	Віт 1	Віт 0
		Unused			DS3/E3	DS3/E3	DS3/E3
			Mapper Block Interrupt Ch 2	Mapper Block Interrupt Ch 1	Mapper Block Interrupt Ch 0		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 3	Unused	R/O	
2	DS3/E3 Mapper Block Interrupt Channel 2	R/O	 DS3/E3 Mapper Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 2 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 2 has been configured to operate in the DS3/E3 Mode.
1	DS3/E3 Mapper Block Interrupt Channel 1	R/O	 DS3/E3 Mapper Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 1 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 1 has been configured to operate in the DS3/E3 Mode.
0	DS3/E3 Mapper Block Interrupt Channel 0	R/O	 DS3/E3 Mapper Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 0 is currently declaring an interrupt. NOTE: This bit-field is only active if Channel 0 has been configured to operate in the DS3/E3 Mode.





Table 21: Interface Control Register – Byte 1 (Address Location= 0x0132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	Receive STS- Selec	·3/STM-1 Line xt[1:0]	Unu	ised	Transmit STS-3/STM-1 L Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Receive STS- 3/STM-1 Line	R/W	Receive STS-3/STM-1 Line Select[1:0]:
	Select[1:0]		These two READ/WRITE bit-fields permit the user to configure the Receive STM-1 SOH Processor block to either accept its STS-3/STM-1 data from the Receive STS-3/STM-1 Telecom Bus Interface, or from the Receive STS-3/STM-1 PECL Interface.
			0, 0 – Configures the Receive STM, SOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 PECL Interface block
			0, 1 – Configures the Receive STM-1 SOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 Telecom Bus Interface block
			1, 0 and 1, 1 - Do not use
3 – 2	Unused	R/O	
1 – 0	Transmit STS- 3/STM-1 Line Select[1:0]	R/W	 Transmit STS-3/STM-1 Line Select[1:0]: These two READ/WRITE bit-fields permit the user to configure the Transmit STM-1 SOH Processor block to output its outbound STS-3/STM-1 data to either the Transmit STS-3/STM-1 Telecom Bus Interface, or to the Transmit STS-3/STM-1 PECL Interface. 0,0 - Configures the Transmit STM-1 SOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface. 0,0 - Configures the Transmit STM-1 SOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block 1 - Configures the Transmit STM-1 SOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block
			1, 0 and 1, 1 – Do not use.



Table 22: Interface Control Register – Byte 0 (Address Location= 0x0133)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SBSYNC_Delay[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	SBSYNC_Delay[7:0]	R/W	STM-0 Telecom Bus – Sync Delay:
			The Transmit STM-0 Telecom Bus is aligned to the "TxSBFP_in" input pin.
			The user is expected to apply a pulse (with the period of a 6.48MHz clock signal) at a rate of 8kHz to the "TxSBFP in input (pin number G4). Each Transmit STM-0 Telecom Bus will align its transmission of the very first byte of a new STM-0 frame, with a pulse at this input pin.
			These READ/WRITE bit-fields permit the user to specify the amount of delay (in terms of 6.48MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STM-0 via the Transmit STM-0 Telecom Bus.
			Setting this register to "0x00" configures each of the Transmit STM-0 Telecom Bus Interfaces to transmit the very first byte of a new STM-0 frame, upon detection of the rising edge of the "TxSBFP_in".
			Setting this register to "0x01" configures each of the Transmit STM-0 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STM-0 frame, by one 6.48MHz clock period, and so on.
			Note: This register is only active if at least one of the three STM-0 Telecom Bus Interfaces are enabled.

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 23: STS-3/STM-1 Telecom Bus Control Register – Byte 3 (Address Location= 0x0134)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	HRSYNC_Delay[15:8]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
0	0	0	0	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	HRSYNC_Delay[15:8]	R/W	STM-1 Telecom Bus – Sync Delay – Upper Byte:
			The Transmit STM-1 SOH Processor block will generate the outbound STS-3/STM-1 frames in alignment with the 8kHz pulse that is being applied to the "TxSBFP_in" input pin.
			The user is expected to apply a pulse (with the period of a 19.44MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS-3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin.
			These READ/WRITE bit fields permit the user to specify the amount of delay (in terms of 19,44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STM-1 via the Transmit STS-3/STM-1 Telecom Bus.
			Setting these two registers to "0x0000" configures each of the Transmit STS-3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STM-1 frame, upon detection of the rising edge of the "TxSBFP in".
			Setting these register to "0x0001" configures each of the Transmit STM-1 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STM-1 frame, by one 19.44MHz clock period, and so on.
	A	duct	Note: This register is also active if the user has configured the XRT94L33 device to transmit its outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block. As a consequence, the user can configure the XRT94L33 device to align its transmission of STS-3/STM-1 frames (via the Transmit STS-3/STM-1 PECL Interface) to the 8kHz signal that is being applied to the "TxSBFP_in" input pin.
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Table 24: STS-3/STM-1 Telecom Bus Control Register – Byte 2 (Address Location= 0x0135)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
HRSYNC_Delay[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	HRSYNC_Delay[7:0]	R/W	STM-1 Telecom Bus – Sync Delay – Lower Byte:
			The Transmit STM-1 SOH Processor block will generate the outbound STS-3/STM-1 frame in alignment with the 8KHz pulse that is being applied to the "TxSBFP_in" input pin.
			The user is expected to apply a pulse (with the period of a 19.44MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS-3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin.
			These READ/WRITE bit-fields (along with that within the "Interface Control Register — Byte 3) permit the user to specify the amount of delay (in terms of 19.44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STM-1 via the Transmit STS-3/STM-1 Telecom Bus.
			Setting this register to "0x0000" configures each of the Transmit STS- 3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STM-1 frame, upon detection of the rising edge of the "TxSBFP_in".
		Ś	Setting this register to "0x0001" configures each of the Transmit STM-1 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STM-1 frame, by one 19.44MHz clock period, and so on.
	The produces		Note: This register is also active if the user has configured the XRT94L33 device to transmit its outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block. As a consequence, the user can configure the XRT94L33 device to align its transmission of STS-3/STM-1 frames (via the Transmit STS-3/STM-1 PECL Interface) to the 8KHz signal that is being applied to the TxSBFP_in input pin.
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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 25: STS-3/STM-1 Telecom Bus Control Register – Byte 0 (Address Location= 0x0137)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-3/STM- 1 Telecom Bus ON	Telecom Bus Disable	ls STS-3 Payload	Telecom Bus Parity Type	Telecom Bus J1 Only	Telecom Bus Parity Odd	Telecom Bus Parity Disable	STM-1 Rephase OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
Bit 7	STS-3/STM-1	R/W	STS-3/STM-1 Telecom Bus Interface Enable:
	Telecom Bus ON		This READ/WRITE permits the user to either enable or disable the STS- 3/STM-1 Telecom Bus Interface, as described below.
			0 – Disables the STS-3/STM-1 Telecom Bus Interface is Disabled:
			STS-3/STM-1 data will output via "Interleave/De-Interleave" or "Clock/Data" Interface.
			1 – Telecom Bus Interface is Enabled:
			In this selection, the STS-3/STM-1 Transmit and Receive Telecom Bus Interface will be enabled.
Bit 6	Telecom Bus Tri-	R/W	Telecom Bus Tri-state
	State		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
		Å	Note: This RE AD/WRITE bit-field is ignored if the STS-3/STM-1 Transmit and Receive STM-1 Telecom Bus Interface is disabled.
Bit 5	Is STS-3 Payload	R/W	Is STS-3 Payload:
	C C	10 he	This READ/WRITE bit-field permits the user to configure STM-0 Telecom Bys Interface # 0 to support the STS-3 rate, as described below.
	the	10,0	O - Configures all three STM-0 Telecom Bus Interfaces to operate in the STM-0 Mode.
	6	3110	1 – Configures STM-0 Telecom Bus Interface # 0 to operate in the STS-3 Mode. In this configuration setting, only STM-0 Telecom Bus Interface # 0 will be active and will be operating at a rate of 19.44MHz. STM-0 Telecom Bus Interfaces # 1 and 2 will be disabled.
Bit 4	Telecom Bus	R/W	Telecom Bus Parity Type:
	Parity Type		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.
			0 – Parity is computed/verified over the STS-3/STM-1 Transmit and Receive Telecom Bus – data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]).
			If the user implements this selection, then the following will happen.
			a. The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output pin) based upon and coincident with the data being output via the "TXA_D[7:0]" output pins.



			b.	The STS-3/STM-1 Receive Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon the data which is being input (and latched) via the "RXD_D[7:0]" input pins.	
			Receive	rity is computed/verified over the STS-3/STM-1 Transmit and Telecom Bus – data bus pins (e.g., TXA_D[7:0] and 7:0]); the C1J1 and PL input/output pins.	
			If the us	er implements this selection, then the following will happen.	
			a.	The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output) based upon and coincident with (1) the data being output via the "TXA_D[7:0]" output pins, (2) the state of the "TXA_PL" output pin, and (3) the state of the "TXA_C1J1" output pin.	
			b.	The STS-3/STM-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon (1) the data which is being input (and latched) via the "RXD_D[7:0]" input pins, (2) the state of the "RXD_PL" input pin, and (3) the state of the "RXD_C1J1" input pin.	
			Note:	This bit-field is disabled if the STS-3/STM-1 Telecom Bus is disabled. The user can configure the STS-3/STM-1 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.	
Bit 3	Telecom Bus J1	R/W	Telecon	n Bus – J1 Indicator Only:	
	Only		3/STM-1 "TXA_C	ADWRITE bit field permits the user to configure how the STS- Transmit and Receive Telecom Bus interface handles the 1J1" and RXD_C1J1" signals, as described below.	
				ection configures the following.	
		3	C.	The STS-3/STM-1 Transmit Telecom Bus to pulse the	
		A C C C C C C C C C C C C C C C C C C C	heet a	1000	TXA_C1J1" output coincident to whenever the C1 and J1 bytes are being output via the "TXA_D[7:0]" output pins.
	oroč			not d.	The STS-3/STM-1 Receive Telecom Bus will expect the "RXD_C1J1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "RXD_D[7:0]" input pins.
		n3	1 – J1 B	sytes Only	
	11,310	20	This sele	ection configures the following.	
	۲ ۲		е.	The STS-3/STM-1 Transmit Telecom Bus Interface to only pulse the "TXA_C1J1" output pin coincident to whenever the J1 byte is being output via the "TXA_D[7:0]" output pins.	
			Note:	The "TXA_C1J1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "TXA_D[7:0]" output pins	
			f.	The STS-3/STM-1 Receive Telecom Bus Interface will expect the "RXD_C1J1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "RXD_D[7:0]" input pins.	
			Note:	The "RXD_C1J1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "RXD_D[7:0]" input pins	
Bit 2	Telecom Bus	R/W	Telecon	n Bus Parity – ODD Parity Select:	
	Parity Odd			AD/WRITE bit-field permits the user to configure the STS-3/STM- om Bus Interface to do the following.	
	1				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			In the Transmit (Drop) Direction
			The STS-3/STM-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) $TxD_D[7:0]$ output pins, or (2) $TxD_D[7:0]$ output pins, the states of the TxD_PL and TxD_C1J1 output pins (depending upon user setting for Bit 3).
			In the Receive (Add) Direction
			Receive STS-3/STM-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) RxA_D[7:0] input pins, or (2) RxA_D[7:0] input pins, the states of the RxA_PL and RxA_C1J1 input pins (depending upon user setting for Bit 3).
			0 – Configures Transmit (Drop) Telecom Bus to compute EVEN parity and configures the Receive (Add) Telecom Bus to verify EVEN parity.
			1 – Configures Transmit (Drop) Telecom Bus to compute ODD parity and configures the Receive (Add) Telecom Bus to verify ODD parity.
Bit 1	Telecom Bus	R/W	Telecom Bus Parity Disable:
	Parity Disable		This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "TxA_DP" output pin. This bit field also permits the user to enable or disable parity verification by the Receive Telecom Bus. 0 – Enables Parity Calculation (on the Transmit Telecom Bus) and
			Disables Parity Verification (on the Receive Telecom Bus.
			1 – Disables Parity Calculation and Verification
Bit 0	Rephase OFF	R/W	Telecom Bus Rephase Disable:
	Only		This READ/WRITE bit-field permits the user to configure the Receive STS-3/STM-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins.
			Note: If the Receive STS-3/STM-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.
		811C	1 – Disables Rephase 0 – Enables Rephase
	the	ata di	lath

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Table 26: Interface Control Register – Byte 2 – STS-1/STM-0 Telecom Bus Interface – Channel 2 (Address Location= 0x0139)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
STM-0 Telecom Bus ON Channel 2	STM-0 Telecom Bus Tri- State Channel 2	Unused	STM-0 Telecom Bus Parity Type Channel 2	STM-0 Telecom Bus J1 ONLY	STM-0 Telecom Bus Parity Odd	STM-0 Telecom Bus Parity Disable	STM-0 REPHASE OFF	
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
Bit 7	STM-0	R/W	STM-0 Telecom Bus ON – Channel 2:
	Telecom Bus ON – Channel 2		 This READ/WRITE bit-field permits the user to either enable or disable the STM-0 Telecom Bus Interface associated with Channel 2. If this particular STM-0 Telecom Bus Interface is enabled, then all of the following events will occur. The Transmit STM-0 Telecom Bus Interface (associated with Channel 2) will accept an STM-0 Telecom Bus Interface (associated with Channel 2) will accept an STM-0 signal (in the Ingress Direction) and the XRT94L33 device will map this signal into an STM-1 signal. The XRT94L33 device will de-map out the STM-0 signal (associated with Channel 2) and will output this STM-0 data-stream via the Receive STM-0 Telecom Bus Interface (associated with Channel 2).
			then Channel 2 will support the mapping (de-mapping) of DS3, E3 or STM-0 data into (from) the STM-1 signal via the "LIU Interface".
		duct	In this mode, the LIU Interface (associated with Channel 2) will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 2) will now be enabled.
	3	್ಸ್ಟ್	If Channel 2 is configured to operate in the DS3/E3 Mode:
	Q	5 1	DS3/E3 Framer Block
	Alle a	3. 6	DS3/E3 Mapper Block
	. 80	10	DS3/E3 Jitter Attenuator/De-Sync Block
		S.	If Channel 2 is configured to operate in the STM-0 Mode
			Receive STM-0 SOH Processor Block
			Receive STM-0 POH Processor Block
			Transmit STM-0 POH Processor Block
			Transmit STM-0 SOH Processor Block
			1 – Enables the STM-0 Telecom Bus Interface, associated with Channel 2.
			In this mode, all DS3/E3 Framer block and STM-0 SOH/POH Processor block circuitry associated with Channel 2 will be disabled.
Bit 6	STM-0	R/W	STM-0 Telecom Bus Tri-state – Channel 2:
	Telecom Bus Tri-State # 2		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus



			Interface associated with Channel 2.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			<i>Note:</i> This READ/WRITE bit-field is ignored if the Transmit and Receive STM-0 Telecom Bus Interface (associated with Channel 2) is
			disabled.
Bit 5	Unused	R/W	
Bit 4	STM-0 Telecom Bus	R/W	STM-0 Telecom Bus Parity Type – Channel 2:
	Parity Type – Channel 2		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.
			0 – Parity is computed/verified over the STM-0 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_2[7:0] and STS1RXD_D_2[7:0]).
			If the user implements this selection, then the following will happen.
			g. The Receive STM-0 Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_2" output pin) based upon and coincident with the data being output via the "STS1RXD_2_D[7:0]" output pins.
			h. The Transmit STM-0 Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon the data which is being input (and latched) via the "STS1TXA_2_DI7:0]" input pins.
			1 – Parity is computed/verified over the Transmit and Receive STM-0 Telecom Bus – data bus pins (e.g., STS1TXA_2_D[7:0] and STS1RXD_2_D[7:0]); the STS1TXA_C1J1_2, STS1RXD_C1J1_2, STS1TXA_PL_2 and STS1RXD_PL_2 input/output pins.
			If the user implements this selection, then the following will happen.
		orodu	a. The Receive STM-0 Telecom Bus Interface will compute and output parity (via the "RXD_DP_2" output) based upon and coincident with (1) the data being output via the "STS1RXD_2_D[7:0]" output pins, (2) the state of the "STS1RXD_PL_2" output pin, and (3) the state of the "STS1RXD_C1J1_2" output pin.
	414	or share	b. The Transmit STM-0 Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_2_D[7:0]" input pins, (2) the state of the "STS1TXA_PL_2" input pin, and (3) the state of the "STS1TXA_C1J1_2" input pin.
			Note: This bit-field is disabled if the STM-0 Telecom Bus is disabled. The user can configure the STM-0 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	STM-0	R/W	STM-0 Telecom Bus Interface – J1 Indicator Only – Channel 2:
	Telecom Bus J1 ONLY		This READ/WRITE bit-field permits the user to configure how the Transmit and Receive STM-0 Telecom Bus interface handles the "STS1TXA_C1J1_2" and STS1RXD_C1J1_2" signals, as described below.
			0 – C1 and J1 Bytes
			This selection configures the following.
			a. The Receive STM-0 Telecom Bus Interface to pulse the



			"STS1RXD_C1J1_2" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_2_D[7:0]" output pins.	
			b. The Transmit STM-0 Telecom Bus Interface will expect the "STS1TXA_C1J1_2" input to be pulsed "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_2_D[7:0]" input pins.	
			1 – J1 Bytes Only	
			This selection configures the following.	
			a. The Receive STM-0 Telecom Bus Interface to only pulse the "STS1RXD_C1J1_2" output pin coincident to whenever the J1 byte is being output via the "STSRXD_2_D[7:0]" output pins.	
			Note: In this setting, the "STS1RXD_C1J1_2" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_2[7:0]" output pine	
			b. The Transmit STM-0 Telecom Bus Interface will expect the "STS1TXA_C1J1_2" input to only be pulsed "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_2_D[7:0]" input pins.	
			Note: In this setting the "STS1TXA_C1J1_2" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_2_D[7:0]" input pins	
Bit 2	STM-0 Telecom Bus	R/W	STM-0 Telecom Bus Interface Parity – ODD Parity Select – Channel 2:	
	Parity Odd		This READ/WRITE bit-field permits the user to configure the STM-0 Telecom Bus Interface, associated with Channel 2 to do the following.	
			In the Receive (Drop) Direction	
			Receive STM-D Telecom Bus Interface will compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_2_D[7:0] output pins, or (2) STS1RxD_2_D[7:0] output pins, the states of the STS1RxD_PL_2 and STS1RxD_C1J1_2 output pins (depending upon user setting for Bit 3).	
			In the Transmit (Add) Direction	
	చ	oducet	Transmit STM-0 Telecom Bus Interface will compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_2_D[7:0] input pins, or (2) STS1TxA_2_D[7:0] input pins, the states of the STS1TxA_PL_2 and STS1TxA_C1J1_2 input pins (depending upon user setting for Bit 3).	
	the s	39113	3 112	 Configures Receive STM-0 (Drop) Telecom Bus Interface to compute EVEN parity and configures the Transmit STM-0 (Add) Telecom Bus Interface to verify EVEN parity.
		31	1 – Configures Receive STM-0 (Drop) Telecom Bus Interface to compute ODD parity and configures the Transmit STM-0 (Add) Telecom Bus Interface to verify ODD parity.	
Bit 1	STM-0 Telecom Bus	R/W	STM-0 Telecom Bus Interface - Parity Disable – Channel 2:	
	Parity Disable		This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_2" output pin. Further, this bit-field also permits the user to enable or disable parity verification via the "STS1TxA_DP_2" input pin by the Transmit Telecom Bus.	
			1 – Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus.	
			0 – Enables Parity Calculation and Verification	
Bit 0	STM-0	R/W	STM-0 Telecom Bus Interface – Rephase Disable – Channel 2:	
	REPHASE OFF		This READ/WRITE bit-field permits the user to configure the Receive STM-0	

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OFF	Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins.
	Note: If the Receive STM-0 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.
	1 – Disable Rephase
	If the user implements this selection, then the Transmit STM-0 Telecom Bus Interface (associated with Channel 2) will rely on the signaling that is provided via the "STS1TXA_C1J1_2" and "STS1TXA_PL_2" input pins, in order to determine the location of the STM-0 SPE (within the Ingress Direction STM-0 signal) with respect to the STM-0 frame boundaries.
	0 – Enable Rephase
	If the user implements this selection, then the Transmti STM-0 Telecom Bus Interface (associated with Channel 2) will NOT rely on the signaling that is provided via the "STS1TXA_C1J1_2" and the "STS1TXA_PL_2" input pins in order to determine the location of the STM-0 SPE (within the Ingress Direction STM-0 signal) with respect to the STM-0 frame boundaries. In this case the Transmit STM-0 SOH and POH Processor blocks (will be enabled) and will take on the role of locating the STM-0 SPE within the Ingress Direction STM-0 signal.

in STM-0 SO in will take on the role ingress Direction STM-0 signal



Table 27: Interface Control Register – Byte 1 – STS-1/STM-0 Telecom Bus Interface - Channel 1 (Address Location= 0x013A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STM-0 Telecom Bus ON Channel 1	STM-0 Telecom Bus Tri- State Channel 1	Unused	STM-0 Telecom Bus Parity Type Channel 1	STM-0 Telecom Bus J1 ONLY	STM-0 Telecom Bus Parity ODD	STM-0 Telecom Bus Parity Disable	STM-0 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION		
Bit 7	STM-0	R/W	STM-0 Telecom Bus ON – Channel 1		
	Telecom Bus ON - Channel 1		 This READ/WRITE bit-field permits the user to either enable or disable the STM-0 Telecom Bus Interface associated with Channel 1. If this particular STM-0 Telecom Bus Interface is enabled, then all of the following events will occur. The Transmit STM-0 Telecom Bus Interface (associated with Channel 1) will accept an STM-0 signal (in the Ingress Direction) and the XRT94L33 device will map this signal into an STM-1 signal. 		
			• The XRT94L33 device will de-map out the STM-0 signal (associated with Channel 1) and will output this STM-0 data-stream via the Receive STM-0 Telecom Bus Interface (associated with Channel 1).		
			If the STM-0 Telecom Bus Interface associated with Channel 1 is disabled, then Channel 1 will support the mapping (de-mapping) of DS3, E3 or STM-0 data into (from) the STM-1 signal via the "LIU Interface".		
		, C	AT De		
		8	0 – Disables the STM-0 Telecom Bus Interface associated with Channel 1.		
	thepr	Shee	she	she	In this mode, the LIU Interface (associated with Channel 1) will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 1) will now be enabled.
	AN A		If Channel 1 is configured to operate in the DS3/E3 Mode:		
	. 90	0	DS3/E3 Framer Block		
		<u></u> .	DS3/E3 Mapper Block		
			 DS3/E3 Jitter Attenuator/De-Sync Block 		
			If Channel 1 is configured to operate in the STM-0 Mode:		
			Receive STM-0 SOH Processor Block		
			Receive STM-0 POH Processor Block		
			Transmit STM-0 POH Processor Block		
			Transmit STM-0 SOH Processor Block		
			1 – Enabes the STM-0 Telecom Bus Interface, associated with Channel 1.		
			In this mode, all DS3/E3 Framer block and STM-0 SOH/POH Processor block circuitry associated with Channel 1 will be disabled.		



Bit 6	STM-0	R/W	STM-0 Telecom Bus Tri-state – Channel 1:
2 0	Telecom Bus		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus
	Tri-State # 1		Interface.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STM-0 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	Unused	R/O	
Bit 4	STM-0	R/W	STM-0 Telecom Bus Parity Type – Channel 1:
	Telecom Bus Parity Type # 1		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.
			0 – Parity is computed/verified over the STM-0 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]).
			If the user implements this selection, then the following will happen.
			a. The STM-0 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_1" output pin) based upon and coincident with the data being output via the "STS1RXD_D_17:0]" output pins.
			b. The STM-0 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins.
			1 – Parity is computed/verified over the STM-0 Transmit and Receive Telecom Bus data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]); the STS1TXA_C1J1_1, STS1RXD_C1J1_1, STS1TXA_PL_1 and STS1RXD_PL_1 input/output pins.
			If the user implements this selection, then the following will happen.
	0	Produ	at The STM-0 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_1" output) based upon and opincident with (1) the data being output via the "STS1RXD_D_1[7:0]" output pins, (2) the state of the "STS1RXD_PL_1" output pin, and (3) the state of the "STS1RXD_C1J1_1" output pin.
	4h	Pro Share	b. The STM-0 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins, (2) the state of the "STS1TXA_PL_1" input pin, and (3) the state of the "STS1TXA_C1J1_1" input pin.
			Note: This bit-field is disabled if the STM-0 Telecom Bus is disabled. The user can configure the STM-0 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	STM-0	R/W	Telecom Bus – J1 Indicator Only – Channel 1:
	Telecom Bus J1 ONLY		This READ/WRITE bit-field permits the user to configure how the STM-0 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_1" and STS1RXD_C1J1_1" signals, as described below.
			0 – C1 and J1 Bytes
			This selection configures the following.
l	1		L



			a.	The STM-0 Receive Telecom Bus to pulse the "STS1RXD_C1J1_1" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_1[7:0]" output pins.
			b.	The STM-0 Transmit Telecom Bus will expect the "STS1TXA_C1J1_1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_1[7:0]" input pins.
			1 – J1 E	Bytes Only
			This sel	lection configures the following.
			i.	The STM-0 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_1" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D_1[7:0]" output pins.
			Note:	The "STS1RXD_C1J1_1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_1[7:0]" output pins).
			j.	The STM-0 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_1[7:0]" input pins.
			Note:	The "STS1TXA_C1)1_1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_1[7:0]" input pins.
Bit 2	STM-0	R/W	Teleco	m Bus Parity + ODD Parity Select – Channel 1:
	Telecom Bus Parity Odd		This R Telecor	EAD/WRITE bit field permits the user to configure the STM-0 n Bus Interface, associated with Channel 1 to do the following.
			In the F	eceive (Drop) Direction
		(C	over th	STM-0 Telecom Bus to compute either the EVEN or ODD parity the contents of the (1) STS1RxD_D_1[7:0] output pins, or (2) D_D_1[7:0] output pins, the states of the STS1RxD_PL_1 and RxD_C1J1_1 output pins (depending upon user setting for Bit 3).
		. Č [*] .	In the T	ansmit (Add) Direction
	the pr	asheet	parity c STS1T> STS1T> Configu configu	it STM-0 Telecom Bus to compute and verify the EVEN or ODD over the contents of the (1) STS1TxA_D_1[7:0] input pins, or (2) (A_D_1[7:0] input pins, the states of the STS1TxA_PL_1 and (A_C1J1_1 input pins (depending upon user setting for Bit 3).0 – irres Receive (Drop) Telecom Bus to compute EVEN parity and res the Transmit (Add) Telecom Bus to verify EVEN parity1 –
	0	SUN CO		res Receive (Drop) Telecom Bus to compute ODD parity and res the Transmit (Add) Telecom Bus to verify ODD parity.
Bit 1	STM-0	R/W		Telecom Bus Parity Disable – Channel 1:
	Telecom Bus Parity Disable		This RI parity o Further, verificat Bus.1 -	EAD/WRITE bit-field permits the user to either enable or disable calculation and placement via the "STSRxD_DP_1" output pin., this bit field also permits the user to enable or disable parity ion via the "STS1TxA_DP_1" input pin by the Transmit Telecom - Disables Parity Calculation (on the Receive Telecom Bus) and s Parity Verification (on the Transmit Telecom Bus.
			0 – Ena	bles Parity Calculation and Verification
Bit 0	STM-0	R/W	STM-0	Telecom Bus – Rephase Disable – Channel 1:
	REPHASE OFF		Telecor	AD/WRITE bit-field permits the user to configure the Receive STM-0 n Bus to internally compute the Pointer Bytes, based upon the data eccives via the "RxD_D[7:0] input pins. <i>If the Receive STM-0 Telecom</i> <i>Bus is being provided with pulses denoting the C1 and J1 bytes</i>

(via the "RxD_C1J1" input pin), then this feature is unnecessary.1 – Disables Rephase
0 – Enables Rephase

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Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STM-0 Telecom Bus ON # 0	STM-0 Telecom Bus Tri- State # 0	AU-4 Mapper/VC- 4 REPHASE OFF	STM-0 Telecom Bus Parity Type # 0	STM-0 Telecom Bus J1 ONLY	STM-0 Telecom Bus Parity Odd	STM-0 Telecom Bus Parity Disable	STM-0 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Table 28: Interface Control Register – Byte 0 – STS-1/STM-0 Telecom Bus 0 (Address Location= 0x013B)

BIT NUMBER	NAME	Түре	DESCRIPTION
Bit 7	STM-0	R/W	STM-0 Telecom Bus ON – Chappel 0:
	Telecom Bus ON # 0		This READ/WRITE bit-field permits the user to either enable or disable the Telecom Bus associated with STM-0 Telecom Bus # 0. If the STM-0 Telecom Bus is enabled then an STM-0 signal will be mapped into (demapped from) the STM-1 signal. If STM-0 Telecom Bus Interface – Channel 3 is disabled then Channel 0 will support the mapping of DS3, E3 or STM-0 into the STM-1 signal.
			0 – STM-0 Telecom Bus # 0 is disabled.
			In this mode, DS3/E3/STM-0 Channel 0 will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 0) will now be enabled.
			If DS3/E3 Framing is supported
			DS3/E3 Framer Block
			OS3/E3 Mapper Block
			D\$3/E30tter Attenuator/De-Sync Block
		ouct	Framing is supported
			Receive STM-0 SOH Processor Block
	or		Receive STM-0 POH Processor Block
ne		\$ N	Transmit STM-0 POH Processor Block
	1.23	andli	Transmit STM-0 SOH Processor Block
			1 – STM-0 Telecom Bus # 0 is enabled.
			In this mode, all DS3/E3 Framer block and STM-0 circuitry associated with Channel 0 will be disabled.
Bit 6	STM-0	R/W	STM-0 Telecom Bus Tri-state – Channel 0:
	Telecom Bus Tri-State # 0		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STM-0 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	AU-4	R/O	AU-4 Mapper/VC-4 While Rephase Off:
	Mapper/VC-4 REPHASE OFF		This READ/WRITE bit-field permits the user to configure the STM-0 Telecom Bus # 0 to process AU-4 Mapper/VC-4 data while the "Rephase"



	OFF		feature is disabled. If the user configures the STM-0 Telecom Bus Interface to process AU-4/VC-4 data then the following functional blocks (within the XRT94L33 device) will now become active.	
			The Transmit AU-4 Mapper/VC-4 POH Processor block	
			 The Receive AU-4 Mapper/VC-4 POH Processor block 	
			0 – Configures STM-0 Telecom Bus # 0 to process STM-1 data.	
			1 – Configures STM-0 Telecom Bus # 0 to process AU-4/VC-4 data.	
			Note: This bit-field is only active if STM-0 Telecom Bus Interface # 0 has been configured to support "STM-1" Operation. This bit-field ignored if STM-0 Telecom Bus Interface # 0 has been configured to operate in the STM-0 Mode.	
Bit 4	STM-0		STM-0 Telecom Bus Parity Type – Channel 0:	
	Telecom Bus Parity Type # 0		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.	
			0 – Parity is computed/verified, over the Transmit and Receive STM-0 Telecom Bus – data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]).	
			If the user implements this selection, then the following will happen.	
			a. The STM-0 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output pin) based upon and coincident with the data being output via the "STS1RXD_D_0[7:0]" output pins.	
	the		b. The STM-0 Dansmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins.	
			1 – Parity is computed/verified over the STM-0 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]); the STS1TXA_C1J1_0, STS1RXD_C1J1_0, STS1TXA_PL_0 and STS1RXD_PL_0 input/output pins.	
			If the user implements this selection, then the following will happen.	
			a. The STM-0 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output) based upon and coincident with (1) the data being output via the "STS1RXD_D_0[7:0]" output pins, (2) the state of the "STS1RXD_PL_0" output pin, and (3) the state of the "STS1RXD_C1J1_0" output pin.	
			b. The STM-0 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins, (2) the state of the "STS1TXA_PL_0" input pin, and (3) the state of the "STS1TXA_C1J1_0" input pin.	
			Note: This bit-field is disabled if the STM-0 Telecom Bus is disabled. The user can configure the STM-0 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.	
Bit 3	STM-0	R/W	Telecom Bus – J1 Indicator Only – Channel 0:	
	Telecom Bus J1		This READ/WRITE bit-field permits the user to configure how the STM-0	
	ONLY		Transmit and Receive Telecom Bus interface handles the "STS1TXA C1.11.0" and STS1PXD C1.11.0" signals as described below	



			"STS1T	XA_C1J1_0" and STS1RXD_C1J1_0" signals, as described below.				
			0 – C1 a	and J1 Bytes				
			This sel	ection configures the following.				
			a.	The STM-0 Receive Telecom Bus to pulse the "STS1RXD_C1J1_0" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_0[7:0]" output pins.				
			b.	The STM-0 Transmit Telecom Bus will expect the "STS1TXA_C1J1_0" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_0[7:0]" input pins.				
			1 – J1 Bytes Only					
			This sel	ection configures the following.				
			k.	The STM-0 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_0" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D_0[7:0]" output pins.				
			Note:	The "STS1RXD_C111_0" output pin will NOT be pulsed "high" whenever the C1. Obyte is being output via the "STS1RXD_D_0[7:0]" output pins				
			I.	The STM-0 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins.				
			Note:	The "STS17XA_C1J1_0" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_0[7:0]" input pins				
Bit 2	STM-0	R/W	Teleco	m Bus Parity – ODD Parity Select – Channel 0:				
	Telecom Bus Parity Odd			EAD/WRITE bit-field permits the user to configure the STM-0 Bus interface, associated with Channel 0 to do the following.				
			In the F	Receive (Drop) Direction				
	d	duct	over th	STM-0 Telecom Bus to compute either the EVEN or ODD parity e contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) xD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and xD_C1J1_0 output pins (depending upon user setting for Bit 3).				
	e T	$\sum_{i=1}^{n} x_{i}^{2}$	In the T	ransmit (Add) Direction				
	11.93	andn	parity o STS1T>	it STM-0 Telecom Bus to compute and verify the EVEN or ODD over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) (A_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and (A_C1J1_0 input pins (depending upon user setting for Bit 3).				
				nfigures Receive (Drop) Telecom Bus to compute EVEN parity and res the Transmit (Add) Telecom Bus to verify EVEN parity				
				nfigures Receive (Drop) Telecom Bus to compute ODD parity and res the Transmit (Add) Telecom Bus to verify ODD parity.				
Bit 1	STM-0	R/W	STM-0	Telecom Bus Parity Disable – Channel 0:				
	Telecom Bus Parity Disable		parity of Further,	EAD/WRITE bit-field permits the user to either enable or disable calculation and placement via the "STSRxD_DP_0" output pin. this bit field also permits the user to enable or disable parity ion via the "STS1TxA_DP_0" input pin by the Transmit Telecom				
				ables Parity Calculation (on the Receive Telecom Bus) and Disables erification (on the Transmit Telecom Bus.				



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			0 – Enables Parity Calculation and Verification			
Bit 0	STM-0 REPHASE OFF	R/W	 STM-0 Telecom Bus – Rephase Disable – Channel 0: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 Telecom Bus (associated with Channel 0) to internally compute the Pointer Bytes, based upon the data that it receives via the "STS1TxA_D[7:0] input pins. Note: If the Transmit STM-0 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "STS1TxA_C1J1" input pin), then this feature is unnecessary. 1 – Disables Rephase 0 – Enables Rephase 			

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Table 29: Interface Control Register – STS-1/STM-0 Telecom Bus Interrupt Enable/Status Register (Address Location= 0x013C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	STM-0 Telecom Bus # 2 RxParity Error Interrupt Status	TB1 RxParity Error Interrupt Status	TB0 RxParity Error Interrupt Status	Unused	TB2 RxParity Error Interrupt Enable	TB1 RxParity Error Interrupt Enable	TB0 RxParity Error Interrupt Enable
R/O	RUR	RUR	RUR	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

			.5 8
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	in cur
6	Telecom Bus # 2	RUR	STM-0 Telecom Bus # 2 - Receive Parity Error Interrupt Status:
	Receive Parity Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or "STM-0 Telecom Bus – Channel 2" has declared a "Receive Parity Error" Interrupt since the last read of this register.
			0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register.
			1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
5	Telecom Bus # 1 Receive Parity	RUR	STM-0 Telecom Bus # 1 – Receive Parity Error Interrupt Status:
	Error Interrupt Status	. Jot	This RESET-upon-READ bit-field indicates whether or "STM-0 Telecom Bus — Channel 1" has declared a "Receive Parity Error" Interrupt since the last read of this register.
	all	o e	0 - The "Receive Parity Error" Interrupt has not occurred since the last read of this register.
	net	8 N?	- The "Receive Parity Error" Interrupt has occurred since the last read of this register.
	1.93	and .	Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
4	Telecom Bus # 0	RUR	STM-0 Telecom Bus # 0 – Receive Parity Error Interrupt Status:
	Receive Parity Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or "STM-0 Telecom Bus – Channel 3" has declared a "Receive Parity Error" Interrupt since the last read of this register.
			0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register.
			1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.
3	Unused	R/O	
	1	1	1



2	Telecom Bus # 2	R/W	STM-0 Telecom Bus # 2 – Receive Parity Error Interrupt Enable
	 Receive Parity Error Interrupt Enable 		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STM-0 Telecom Bus – Channel 2. If the user enables this interrupt, then STM-0 Telecom Bus – Channel 2 will generate an interrupt anytime the "Receive STM-0 Telecom Bus" detects a parity error within the incoming STM-0 data.
			0 – Disables the "Receive Parity Error" Interrupt.
			1 – Enables the "Receive Parity Error" Interrupt.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
1	Telecom Bus # 1	R/W	STM-0 Telecom Bus # 1 – Receive Parity Error Interrupt Enable
	 Receive Parity Error Interrupt Enable 	able C	This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STM-0Telecom Bus – Channel 1. If the user enables this interrupt, then STM-0 Telecom Bus – Channel 1 will generate an interrupt anytime the "Receive STM-0 Telecom Bus" detects a parity error within the incoming STM-0 data
			0 – Disables the "Receive Parity Error" Interrupt.
			1 – Enables the "Receive Parity Error" Interrupt.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled
0	Telecom Bus # 0	R/W	STM-0 Telecom Bus # 0 - Receive Parity Error Interrupt Enable
	 Receive Parity Error Interrupt Enable 		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STM-0 Telecom Bus – Channel 0. If the user enables this interrupt, then STM-0 Telecom Bus – Channel 0 will generate an interrupt anytime the "Receive STM-0 Telecom Bus" detects a parity error within the incoming STM-0 data.
			0 – Disables the "Receive Parity Error" Interrupt.
			1 Enables the "Receive Parity Error" Interrupt.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.
	1		

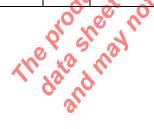




Table 30: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Status Register (Address Location = 0x013D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STM-0 Telecom Bus Tx Overrun Bus 2	STM-0 Telecom Bus Tx Underrun Bus 2	STM-0 Telecom Bus Tx Overrun Bus 1	STM-0 Telecom Bus Tx Underrun Bus 1	STM-0 Telecom Bus Tx Overrun Bus 0	STM-0 Telecom Bus Tx Underrun Bus 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	thister
6	Unused	R/O	il de
5	STM-0 Telecom Bus –	R/O	STM-0 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 2:
	TxFIFO Overrun # 2		This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition.
			0 – Indicates that "STM-0 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Overrun" condition.
			1 – Indicates that "STM-0 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
4	STM-0	R/O	STM-0 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 2:
	Telecom Bus – TxFIFO Underrun # 2		This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 3" is currently declaring a "Transmit FIFO Underrun" condition.
		AUC	0 Indicates that "STM-0 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Underrun" condition.
	C C	No re	1 – Indicates that "STM-0 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Underrun" condition.
	the	10,0	Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
3	STM-0	R/O	STM-0 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 1:
	Telecom Bus – TxFIFO Overrun # 1	.0.	This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition.
			0 – Indicates that "STM-0 Telecom Bus – Channel 1" is NOT declaring a "Transmit FIFO Overrun" condition.
			1 – Indicates that "STM-0 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
2	STM-0	R/O	STM-0 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 1:
	Telecom Bus – TxFIFO Underrun # 1		This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition.
			0 - Indicates that "STM-0 Telecom Bus - Channel 1" is NOT declaring a

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			"Transmit FIFO Underrun" condition.			
			1 – Indicates that "STM-0 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition.			
			<i>Note:</i> This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.			
1	STM-0	R/O	STM-0 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 0:			
	Telecom Bus – TxFIFO Overrun # 0		This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition.			
			0 – Indicates that "STM-0 Telecom Bus – Channel 0" is NOT declaring a "Transmit FIFO Overrun" condition.			
			1 – Indicates that "STM-0 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition.			
			Note: This bit-field is only active if "STM=0 Telecom Bus – Channel 0" has been enabled.			
0	STM-0	R/O	STM-0 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 0:			
	Telecom Bus – TxFIFO Underrun # 0		This READ-ONLY bit-field indicates whether or not "STM-0 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition.			
			0 – Indicates that "STM-0 Telecom Bus – Channel 0" is NOT declaring a "Transmit FIFO Underrun" condition.			
			1 – Indicates that "STM 0 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition			
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.			
Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled						

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Table 31: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Status Register (Address Location= 0x013E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STM-0 Telecom Bus # 2 Tx Overrun Interrupt Status	STM-0 Telecom Bus # 2 Tx Underrun Interrupt Status	STM-0 Telecom Bus # 1 Tx Overrun Interrupt Status	STM-0 Telecom Bus # 1 Tx Underrun Interrupt Status	STM-0 Telecom Bus # 0 Tx Overrun Interrupt Status	STM-0 Telecom Bus # 0 Tx Underrun Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Type	Drá Sura Ó
			DESCRIPTION
7	Unused	R/O	
6	Unused	R/O	0 × 0
5	STM-0 Telecom	RUR	STM-0 Telecom Bus – TxFIFQ Overrun Interrupt Status – Channel 2:
	Bus # 2 – TxFIFO Overrun Interrupt Status		This RESET-upon-READ bit field indicates whether or not "STM-0 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STM-0 Telecom Bus – Channel 2" has NOT declared a
			"TxFIFO Overun" Interrupt since the last read of this register.
			1 – Indicates that "STM-0 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
4	STM-0 Telecom	RUR	STM-0 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 2:
	Bus # 2 – TxFIFO Underrun Interrupt Status	duct	This RESET-upon-READ bit-field indicates whether or not "STM-0 Telecom Bus – Channel 2" has declared a "TxFIFO Underrun" Interrupt since the last read of this register.
	Pr	she	0 Indicates that "STM-0 Telecom Bus – Channel 2" has NOT declared a TxFIFO Underrun" Interrupt since the last read of this register.
	Thest	3 M.	1 – Indicates that "STM-0 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
	0	an	Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 2" has been enabled.
3	STM-0 Telecom	RUR	STM-0 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 1:
	Bus # 1 – TxFIFO Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STM-0 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			0 – Indicates that "STM-0 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			1 – Indicates that "STM-0 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
2	STM-0 Telecom Bus # 1 –	RUR	STM-0 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 1:



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	TxFIFO Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STM-0 Telecom Bus – Channel 1" has declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			0 – Indicates that "STM-0 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			1 – Indicates that "STM-0 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
1	STM-0 Telecom	RUR	STM-0 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 0:
	Bus # 0 – TxFIFO Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STM-0 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			0 – Indicates that "STM-0 Telecom Bus? Channel 0" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			1 – Indicates that "STM-0 Telecon Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if STM-0 Telecom Bus – Channel 0" has been enabled.
0	STM-0 Telecom	RUR	STM-0 Telecom Bus – TxFIFQ Underrun Interrupt Status – Channel 0:
	Bus # 0 – TxFIFO Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STM-0 Telecom Bus – Channel 0" has declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			0 – Indicates that "STM-0 Telecom Bus – Channel 0" has NOT declared a "TxFIFO Underrun" interrupt since the last read of this register.
			1 – Indicates that "STM-0 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.

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Table 32: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Enable Register (Address Location= 0x013F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STM-0 Telecom Bus # 2 Tx Overrun Interrupt Enable	STM-0 Telecom Bus # 2 Tx Underrun Interrupt Enable	STM-0 Telecom Bus # 1 Tx Overrun Interrupt Enable	STM-0 Telecom Bus # 1 Tx Underrun Interrupt Enable	STM-0 Telecom Bus # 0 Tx Overrun Interrupt Enable	STM-0 Telecom Bus # 0 Tx Underrun Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	th ur
6	Unused	R/O	0 40°
5	STM-0 Telecom Bus # 2 TxFIFO Overrun Interrupt Enable		 STM-0 Telecom Bus TxFIFO Overrun Interrupt Enable – Channel 2: This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STM-0 Telecom Bus – Channel 2. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 2" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 Enables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 Enables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 Enables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 Enables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2.
4	STM-0 Telecom Bus # 2 TxFIFO Underrun Interrupt Enable	J. B. W. B.	 As been enabled. STM- Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 2: This READ/WRITE bit-field permits the user to either enable or disable the TxFIFO Underrun" Interrupt, associated with STM-0 Telecom Bus – Channel 2. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 2" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition. 0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 2.
3	STM-0 Telecom Bus # 1 TxFIFO Overrun Interrupt Enable	R/W	STM-0 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 1: This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STM-0 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 1.

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			1 – Enables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 1.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
2	STM-0 Telecom Bus # 1 TxFIFO Underrun Interrupt Enable	R/W	STM-0 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 1: This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STM-0 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition.
			0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 1.
			1 – Enables the "TxFIFO Underrun" onterrupt, associated with "STM-0 Telecom Bus – Channel 1.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 1" has been enabled.
1	STM-0 Telecom	R/W	STM-0 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 0:
	Bus # 0 TxFIFO Overrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STM-0 Telecom Bus – Channel 0. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition.
			0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel O
			1 – Enables the "TXFIFO Overrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 0.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.
0	STM-0 Telecom Bus # 0 TxFIFO Underrun Interrupt Enable	R/W	STM-0 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel O: This READ/WRITE bit-field permits the user to either enable or disable the "TxRFO Underrun" Interrupt, associated with STM-0 Telecom Bus – Channel 3. If the user enables this interrupt, then the "STM-0 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition.
	~`8	and	0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 0.
		•	1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STM-0 Telecom Bus – Channel 0.
			Note: This bit-field is only active if "STM-0 Telecom Bus – Channel 0" has been enabled.





Table 33: Operation General Purpose Input/Output Register – Byte 0 (Address Location= 0x0147)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R/W							
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	GPIO_7	R/W	General Purpose Input/Output Pin # 7:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_7" pin is configured to be an input or an output pin.
			If GPIO_7 is configured to be an input pin:
			If GPIO_7 is configured to be an input pint then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_7" (pin number AA25) input pin.
			If the "GPIO_7" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_7" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_7 is configured to be an output pin:
			If GPIO_7 is configured to be an output pin, then the user can control the logic level of "GPIO_7" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_7 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_7 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 2 is enabled.
6	GPIO_6	R/W	General Purpose Input/Output Pin # 6:
		JUC S	The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_6" pin is configured to be an input or an output pin.
		.000	of GRO_6 is configured to be an input pin:
	the	ata di	If GPIO_6 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_6" (pin number W24) input pin.
	8	3110	If the "GPIO_6" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_6" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_6 is configured to be an output pin:
			If GPIO_6 is configured to be an output pin, then the user can control the logic level of "GPIO_6" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_6 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_6 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 2 is enabled.
5	GPIO_5	R/W	General Purpose Input/Output Pin # 5:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_5" pin is configured to be an input or an output pin.

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			If GPIO_5 is configured to be an input pin:
			If GPIO_5 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_5" (pin number AC26) input pin.
			If the "GPIO_5" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_5" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_5 is configured to be an output pin:
			If GPIO_5 is configured to be an output pin, then the user can control the logic level of "GPIO_5" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_5 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_5 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 1 is enabled.
4	GPIO_4	R/W	General Purpose Input/Output Pin#4:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_4" pin is configured to be an input or an output pin.
			If GPIO_4 is configured to be an input pin:
			If GPIO_4 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_4" (pin number Y25) input pin.
			If the "GPIO_4" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_4" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_4 is configured to be an output pin:
			If GPIO_4 is configured to be an output pin, then the user can control the logic level of "GPIO_4" by writing the appropriate value into this bit-field.
		2	Setting this bit-field to "0" causes the GPIO_4 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_4 output pin to be driven "HIGH".
		prot	Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 1 is enabled.
3	GPIO_3	R/W	General Purpose Input/Output Pin # 3:
		935	The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_3" pin is configured to be an input or an output pin.
		.0.	If GPIO_3 is configured to be an input pin:
			If GPIO_3 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_3" (pin number AB26) input pin.
			If the "GPIO_3" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_3" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_3 is configured to be an output pin:
			If GPIO_3 is configured to be an output pin, then the user can control the logic level of "GPIO_3" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_3 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_3 output pin to be driven "HIGH".



			is enabled.
2	GPIO_2	R/W	General Purpose Input/Output Pin # 2:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_2" pin is configured to be an input or an output pin.
			If GPIO_2 is configured to be an input pin:
			If GPIO_2 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_2" (pin number V23) input pin.
			If the "GPIO_2" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_2" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_2 is configured to be an output pin:
			If GPIO_2 is configured to be an output pin then the user can control the logic level of "GPIO_2" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_2 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_2 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 0 is enabled.
1	GPIO_1	R/W	General Purpose Input/Output Pin # 1:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_1" pin is configured to be an input or an output pin.
			If GPIO_1 is configured to be an input pin:
			If GPIO_1 is configured to be an input pin, then this register bit operates as a READ ONL 9 bit-field that reflects the state of the "GPIO_1" (pin number AC27) input pin.
		Ċ	Here "GPIO_1" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_1" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
		d'	GFIO_1 is configured to be an output pin:
		il she	If GPIO_1 is configured to be an output pin, then the user can control the logic level of "GPIO_1" by writing the appropriate value into this bit-field.
	They	ato de	Setting this bit-field to "0" causes the GPIO_1 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_1 output pin to be driven "HIGH".
		'0'	Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 0 is enabled.
0	GPIO_0	R/W	General Purpose Input/Output Pin # 0:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_0" pin is configured to be an input or an output pin.
			If GPIO_0 is configured to be an input pin:
			If GPIO_0 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_0" (pin number W25) input pin.
			If the "GPIO_0" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_0" input pin is pulled to a logic "LOW", then this register bit will be set to "0".



If GPIO_0 is configured to be an output pin:
If GPIO_0 is configured to be an output pin, then the user can control the logic level of "GPIO_0" by writing the appropriate value into this bit-field.
Setting this bit-field to "0" causes the GPIO_0 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_0 output pin to be driven "HIGH".
Note: This register bit-field is only active if STM-0 Telecom Bus – Channel 0 is enabled.

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Table 34: Operation General Purpose Input/Output Direction Register 0 (Address Location= 0x014B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	GPIO_DIR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	GPIO_DIR[7]	R/W	GPIO_7 Direction Select:
			This READ/WRITE bit-field permits the user to configure the "GPIO_7" pin (pin number AA25) to function as either an input or an output pin.
			0 – Configures GPIO_7 to function as an input pin.
			1 – Configures GPIO_7 to function as an output pin.
			Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 2 is enabled.
6	GPIO_DIR[6]	R/W	GPIO_6 Direction Select
			This READ/WRITE bit field permits the user to configure the "GPIO_6" pin (pin number W24) to function as either an input or an output pin.
			0 – Configures GPIO_6 to function as an input pin.
			1 – Configures GPIO 6 to function as an output pin.
			Note: This register bit field is only active if STM-0 Telecom Bus Interface Channel 2 is enabled.
5	GPIO_DIR[5]	R/W	GPIO_5 Direction Select:
		N N	This READ/WRITE bit-field permits the user to configure the "GPIO_5" pin (pin number AC26) to function as either an input or an output pin.
		X	0 - Configures GPIO_5 to function as an input pin.
		210	12- Configures GPIO_5 to function as an output pin.
	C C	ro hee	Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 1 is enabled.
4	GPIO_DIR[4]	R/W	GPIO_4 Direction Select:
	1.8		This READ/WRITE bit-field permits the user to configure the "GPIO_4" pin (pin number Y25) to function as either an input or an output pin.
		Q.	0 – Configures GPIO_4 to function as an input pin.
			1 – Configures GPIO_4 to function as an output pin.
			Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 1 is enabled.
3	GPIO_DIR[3]	R/W	GPIO_3 Direction Select:
			This READ/WRITE bit-field permits the user to configure the "GPIO_3" pin (pin number AB26) to function as either an input or an output pin.
			0 – Configures GPIO_3 to function as an input pin.
			1 – Configures GPIO_3 to function as an output pin.
			Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 1 is enabled.



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GPIO_DIR[2]	R/W	GPIO_2 Direction Select:
		This READ/WRITE bit-field permits the user to configure the "GPIO_2" pin (pin number V23) to function as either an input or an output pin.
		0 – Configures GPIO_2 to function as an input pin.
		1 – Configures GPIO_2 to function as an output pin.
		<i>Note:</i> This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 0 is enabled.
GPIO_DIR[1]	R/W	GPIO_1 Direction Select:
		This READ/WRITE bit-field permits the user to configure the "GPIO_1" pin (pin number AC27) to function as either an input or an output pin.
		0 – Configures GPIO_1 to function as an input pin.
		1 – Configures GPIO_1 to function as an output pin.
		Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 0 is enabled.
GPIO_DIR[0]	R/W	GPIO_0 Direction Select:
		This READ/WRITE bit-field permits the user to configure the "GPIO_0" pin (pin number W25) to function as either an input or an output pin.
		0 – Configures GPIO_0 o function as an input pin.
		1 – Configures GPIQ to function as an output pin.
		Note: This register bit-field is only active if STM-0 Telecom Bus Interface – Channel 0 is enabled.
×	le piodici	Note: This register bit field is only active if STM-0 Telecom Bus Interface – Channel 0 is enabled.
	GPIO_DIR[1]	GPIO_DIR[1] R/W



Table 35: Operation Output Control Register – Byte 1 (Address Location= 0x0150)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
8kHz or STUFF Out Enable	8kHz OUT Select	Egress Direction Monitored – STUFF Output			Unused		
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION				
7	8kHz or STUFF Out Enable	R/W	8kHz or STUFF Output Enable – LOF Output Pin: This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select) permits the user to define the role of the LOF output pin (pin AD11). The relationship between the states of these bit-fields and the corresponding role of the LOF output pin is presented below.				
			Bit 7 (8kHz or STUFF Out Enable)	Bit 6 (8kHz OUT Select)	Role of LOF output pin		
			0		OF or MS-AIS Indicator		
			25		OF or MS-AIS Indicator		
			119 101	<u>0</u> E	Bit Stuff Indicator Output		
			10 10 e	1 8	kHz Output		
6	8kHz OUT Select	d na R/W	 Note: 1. If Bit is set to "0", then Bit 1 (MS-AIS Output Enable) within the Receive STM-1 Section – Auto AIS (in Downstream STM-0s) Control Register (Address Location= 0x116B) will indictate whether or not pin AD11 is the "LOF" or the "MS-AIS" output indicator. 2. If Bit 1 (MS-AIS Output Enable) is set to "0", then pin AD11 will function as the LOF output indicator. 3. If Bit 1 (MS-AIS Output Enable) is set to "1", then pin AD11 will function as the MS-AIS output indicator. 8kHz OUT – LOF Output Pin: This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select) permits the user to define the role of the LOF output pin (pin AD11). The relationship between the states of these bit-fields and the corresponding 				
			role of the LOF ou Bit 7 (8kHz or	itput pin is presente Bit 6 (8kHz OUT			
			STUFF Out Enable)	Select)			
			0	0	LOF or MS-AIS Indicator		
			0	1	LOF or MS-AIS Indicator		
			1	0	Bit Stuff Indicator Output		
			1	1	8kHz Output		

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5	Egress Direct	R/W	Egress Direction Monitored – STUFF Output:
	Monitored –STUFF Output		If the LOF output pin has been configured to function as a "STUFF Indicator" output, then it can be configured to reflect the current stuff opportunities of the channel designated by Bits 7 through 4 (Stuff Indicator Channel Select[3:0]) within the Operation Output Control Register – Byte 0.
			This READ/WRITE bit-field permits the user to configure the LOF output pin to either reflect the "current stuff opportunities" for the Ingress or Egress Path of the selected channel.
			0 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Ingress Path of the "selected" channel.
			1 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Egress Path of the "selected" channel.
			Note: This bit-field will be ignored if the "selected" channel has been configured to operate in the STM-0 Mode.
4 – 0	Unused	R/O	in ctu

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Table 36: Operation Output Control Register – Byte 0 (Address Location= 0x0153)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused Stuff Indicator Channel Select[1:0]		Unused		8kHz Source Channel Select[1:0]			
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Stuff Indicator	R/W	Stuff Indicator – Channel Select[1:0]:
	Channel Select[1:0]		These two (2) READ/WRITE bit fields permit the user to identify which of the 3 channels should have their "bit-stuff opportunity" status reflected on the LOF output pin.
			Setting these bit-fields to [0, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 0. Likewise, setting these bit- fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2.
			Note: These off-fields are ignored if any of the following are true.
			1. If the corresponding channel has been configured to operate in the STM-0 Mode.
			2. If the LOF output pin has been configured to function as the LOF or MS-AIS indicator output.
			3 If the LOF output pin has been configured to function as an 8kHz output pin.
3 – 2	Unused	R/O	0.0
1 – 0	8kHz Source Channel	R/W	8kHz Source Channel Select[1:0]:
	Select[1:0]		If the LOF output pin has been configured to output an 8kHz clock output signal, then the XRT94L33 will derive this 8kHz clock signal, from the Ingress DS3/E3 or Receive STM-0 signal of the "Selected" channel.
	the ta	ma	These two(2) READ/WRITE bit-fields permit the user to specify the "Selected" channel.
	- 0 8kHz Source Channel Select[1:0] The produce the pr	Setting these bit-fields to [0, 0] configures the LOF output pin to output an 8kHz clock signal, that is derived from the Ingress DS3/E3 or Receive STM-0 input signal of Channel 0. Likewise, setting these bit- fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2.	
			Note: These bit-fields are ignored if any of the following are true.
			1. If the LOF output pin has been configured to function as the LOF or MS-AIS indicator output.
			2. If the LOF output pin has been configured to function as the "Stuff Indicator" output pin.



Table 37: Operation Slow Speed Port Control Register – Byte 1 (Address Location= 0x0154)

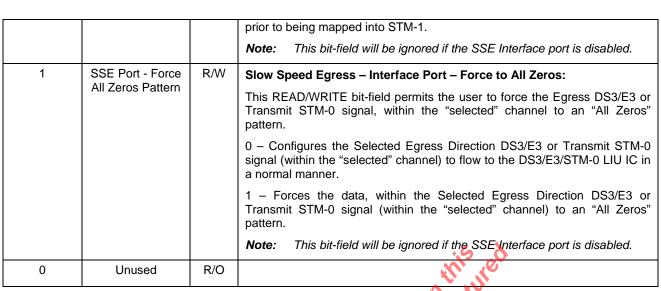
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SSI Port Enable	SSI Port – Insert Direction	SSI Port - Force All Zeros Pattern	Unused	SSE Port Enable	SSE Port – Insert Direction	SSE Port - Force All Zeros Pattern	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7	SSI Port Enable	R/W	Slow-Speed Ingress – Interface Port Enable:				
			This READ/WRITE bit-field permits the user to enable or disable the SSI (Slow-Speed Ingress) Interface Port.				
			If the SSI Interface port is enabled, then it can be used to do either of the following.				
			 To monitor (e.g., to drop out a replica of) the DS3, E3 or STM-0 signal, that is traveling in the Ingress Direction DS3/E3 or Receive STM-0 path of the "Selected" channel within the XRT94L33 device. 				
			• To insert (e.g., to add in) and overwrite the DS3, E3 or STM-0 signal, that is traveling in the Ingress Direction DS3/E3 or Receive STM-0 path of the "Selected" Channel within the XRT94L33 device.				
			ts pogs				
			0 – Disables the SSI Interface Port.				
			1 – Enables the SSI Interface Port.				
6	SSI Port – Insert	R/W	Slow-Speed Ingress – Interface Port – Insert Direction:				
	Direction	e produ data no	Produ datand	produ data d	Pro du	produ datant	This READ/WRITE bit-field permits the user to configure the SSI Interface port to either monitor (e.g., extract) an "Ingress Direction DS3/E3" or "Receive STM-0" signal, or to replace (e.g., insert) a DS3, E3 or STM-0 signal into the Ingress DS3/E3 or Receive STM-0 path of the "Selected" channel. If the user configures the SSI Interface port to monitor a given DS3, E3 or STM-0 signal, then the SSI Interface will then be configured to be an "output" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" output signals. Additionally, a copy of the Selected Ingress Direction DS3/E3 or Receive STM-0 signal will be output via this output port.
	₿	If the user configures the SSI Interface port to replace (e.g., insert) an "Ingress DS3/E3" or Receive STM-0 signal, then the SSI Interface will then be configured to be an "input" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" input signals. Additionally, the DS3, E3 or STM-0 signal that is applied at this input port will overwrite that of the selected "Ingress Direction DS3/E3" or the Receive STM-0 signal.					
			0 – Configures the SSI Interface as an output port that will permit the user to monitor the "selected" Ingress DS3/E3 or Receive STM-0 signal.				
		1 – Configures the SSI Interface as an input port. In this configuration, the DS3, E3 or STM-0 signal that is input via this port will replace/overwrite the "Ingress" DS3/E3 or Receive STM-0 signal, within the "selected" channel, prior to being mapped into STM-1.					
			<i>Note:</i> This bit-field will be ignored if the SSI Interface port is disabled.				



5	SSI Port - Force	R/W	Slow Speed Ingress – Interface Port – Force All Zeros Pattern:
	All Zeros Pattern		This READ/WRITE bit-field permits the user to force the Ingress DS3/E3 or Receive STM-0 signal, within the "selected" channel to an "All Zeros" pattern.
			0 – Configures the Selected Ingress Direction DS3/E3 or Receive STM-0 signal (within the "selected" channel) to flow to the DS3/E3 Mapper Block or to the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block, in a normal manner.
			1 – Forces the data, within the Selected Ingress Direction DS3/E3 or Receive STM-0 signal (within the "selected" channel) to an "All Zeros" pattern.
			Note: This bit-field will be ignored if the SSI Interface port is disabled.
4	Unused	R/O	.6 8
3	SSE Port Enable	R/W	Slow-Speed Egress – Interface Port Enable:
			This READ/WRITE bit-field permits the user to enable or disable the SSE (Slow Speed Egress) Interface Port.
			If the SSE Interface port is enabled, then it can be used to do either of the following.
			• To monitor (e.g., to drop out a replica of) the DS3, E3 or STM-0 signal, that is traveling in the Egress Direction DS3/E3 or Transmit STM-0 path of the "Selected" channel within the XRT94L33 device.
			• To insert (e.g., to add in) and overwrite the DS3, E3 or STM-0 signal, that is traveling in the Engress Direction DS3/E3 or Transmit STM-0 path of the "Selected" Channel within the XRT94L33 device.
			0 Disables the SSE Interface Port
			1 - Enables the SSE Interface Port.
2	SSE Port – Insert	R/W	Slow Speed Egress – Interface Port – Insert Direction:
	Direction	duce	This READ/WRITE bit-field permits the user to configure the SSE Interface port to either monitor (e.g., extract) an "Egress Direction DS3/E3" or "Transmit STM-0" signal, or to replace (e.g., insert) a DS3, E3 or STM-0 signal into the Egress Direction DS3/E3 or Transmit STM-0 path of the Selected" channel.
	111-13	andri	If the user configures the SSE Interface port to monitor a given DS3, E3 or STM-0 signal, then the SSE Interface wil then be configured to be an "output" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" output signals. Additionally, a copy of the Selected Egress Direction DS3/E3 or Transmit STM-0 signal will be output via this output port.
			If the user configures the SSE Interface port to replace (e.g., insert) an "Egress DS3/E3" or Transmit STM-0 signal, then the SSE Interface will then be configured to be an "input" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" input signals. Additionally, the DS3, E3 or STM-0 signal, that is applied at this input port will overwrite that of the selected "Egress Direction DS3/E3" or the Transmit STM-0 signal.
			0 – Configures the SSE Interface as an output port that will permit the user to monitor the "selected" Egress DS3/E3 or Transmit STM-0 signal
			1 – Configures the SSE Interface as an input port. In this configuration, the DS3, E3 or STM-0 signal that is input via this port will replace/overwrite the "Egress" DS3/E3 or Transmit STM-0 signal, within the "selected" channel,

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



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Rev 2.0.0



Table 38: Operation Slow Speed Port Control Register – Byte 0 (Address Location= 0x0157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	SSI_Channel_Select[1:0]		Unused		SSE_Channel_Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Bit Number	NAME	Түре	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	SSI_Channel_Select[1:0]:	R/W	Slow-Speed Ingress – Interface Port – Channel Select[1:0]: These READ/WRITE bit-fields permit the user to select which of the 3 Ingress Direction DS3/E3 or Receive STM-0 signals will be processed via the SSI Interface port.
			Setting SSI_Channel_Select[1:0] to [0, 0] configures the SSI Interface port to process the Ingress Direction DS3/E3 or Receive STM-0 signal associated with Channel 0. Likewise, setting SSI_Channel_Select[1:0] to [1, 0] configures the SSI Interface port to process the Ingress DS3/E3 or Receive STM-0 signal associated with Channel 2.
			Note: These Dit-fields are ignored if the SSI Interface port is disabled.
3 –2	Unused	R/O	al off as
1 – 0	SSE_Channel_Select [1:0]	R/W	Slow Speed Egress - Interface Port - Channel Select[1:0]: These READ/WRITE bit-fields permit the user to select which of the 3 Egress Direction DS3/E3 or Receive STM-0 signals will be processed via the SSE Interface port. Setting SSE_Channel_Select[1:0] to [0, 0] configures the SSE Interface port to process the Egress Direction DS3/E3 or Transmit STM-0 signal associated with Channel 0. Likewise, setting SSE_Channel_Select[1:0] to [1, 0] configures the SSE Interface port to process the Egress DS3/E3 or Transmit STM-0 signal associated with Channel 2. Note: These bit-fields are ignored if the SSE Interface port is disab led.
	The proc	id ma	



Table 39: Operation – DS3/E3/STM-0 Clock Frequency Out of Range Detection – Direction Register (Address Location= 0x0158)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	ON_EGRESS DIRECTION						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	ON_EGRESS_DIRECTION	R/W	 Frequency Out of Range Detection on Egress Direction: This READ/WRITE bit-field permits the user to configure the "DS3/E3/STM-0 Clock Frequency – Out of Range Detector" to operate in either the Ingress of Egress direction. 0 – Configures the DS3/E3/STM-0 Clock Frequency – Out of Range Detector" to operate on the DS3, E3 or STM-0 clock signals in the Ingress Direction. 1 – Configures the DS3/E3/STM-0 Clock Frequency – Out of Range Detector" to operate on the DS3, E3 or STM-0 clock signals in the Egress Direction.
			uct at Or

Table 40: Operation – DS3/E3/STM-0Clock Frequency DS3 Out of Range Detection Threshold Register (Address Location= 0x015A)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0	
DS3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit Number		PE	DESCRIPTION
7 – 0	DS3_OUT_OF_RANGER/ DETECTION_THR	/W	DS3 Out of Range – Detection Threshold[7:0]: These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given DS3 signal (in either the Ingress or Egress direction) and that of the REFCLK45 input clock signal; before the XRT94L33 will declare a "DS3 Clock Frequency – Out of Range" condition.



Table 41: Operation – DS3/E3/STM-0Clock Frequency – STM-0/E3 Out of Range Detection Threshold Registers (Address Location= 0x015B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	STM-0/E3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	STS1/E3_OUT_OF_RAN GE_DETECTION_THR	R/W	STM-0/E3 Out of Range – Detection Threshold[7:0]: These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given STM-0 or E3 signal (in either the Ingress or Egress direction) and that of the REFCLK51/REFCLK34 input clock signal; before the XRT94L33 will declare a "STM-0/E3 Clock Frequency – Out of Range" condition.

Table 42: Operation – DS3/E3/STM-0 Frequency Out of Range Interrupt Enable Register – Byte 0 (Address Location=0x015D)

Віт 7	Віт 6	Віт 5	Віт 4	Вгт 3	Br 2	Віт 1	Віт 0
		Unused	5	uctoel	Out of Range – Channel 2 Interrupt enable	Out of Range – Channel 1 Interrupt Enable	Out of Range – Channel 0 Interrupt Enable
R/O	R/O	R/O	R/Q	R/O	R/W	R/W	R/W
0	0	0	8	.0	0	0	0
			10, 4,	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Enable	R/W	DS3/E3/STM-0 Frequency – Out of Range – Channel 2 – Interrupt Enable:
	Interrupt Enables		This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 2.
	<u>o`</u>		If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STM-0 signal (in the selected direction – Ingress or Egress) within Channel 2, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.
			0 – Disables the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 2.
			1 – Enables the "DS3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 2.
1	Out of Range – Channel 1 Interrupt Enable	R/W	DS3/E3/STM-0 Frequency – Out of Range – Channel 1 – Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt



			for Channel 1.				
			If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STM-0 signal (in the selected direction – Ingress or Egress) within Channel 1, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.				
			0 – Disables the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 1.				
			1 – Enables the "DS3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 1.				
0	Out of Range – Channel 0 Interrupt Enable	R/W	DS3/E3/STM-0 Frequency – Out of Range – Channel 0 – Interrupt Enable:				
			This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 0.				
			If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STM-0 signal (in the selected direction – Ingress or Egress) within Channel 0, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.				
			0 – Disables the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 0				
			1 – Enables the "DS3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 0.				
	1 – Enables the "DS3/E3/STM-0 Frequency - Out of Range"						



Table 43: Operation – DS3/E3/STM-0 Frequency Out of Range Interrupt Status Register – Byte 0 (Address Location=0x015F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused		Out of Range – Channel 2 Interrupt Status	Out of Range – Channel 1 Interrupt Status	Out of Range – Channel 0 Interrupt Status	
R/O	R/O	R/O	R/O	R/O	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Status	RUR	DS3/E3/STM-0 Frequency – Out of Range – Channel 2 – Interrupt Status: This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 2, since the last read of this register.
			 0 – Indicates that the "D\$3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 2 has NOT occurred since the last read of this register. 1 – Indicates that the "D\$3/E3/STM-0 Frequency – Out of Range"
			Interrupt for Channel 2 has occurred since the last read of this register.
1	Out of Range – Channel 1 Interrupt Status	RUR	DS3/E3/STM-0 Frequency – Out of Range – Channel 1 – Interrupt Status: This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 1, since the last read of this register.
			0 Indicates that the "DS3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 1 has NOT occurred since the last read of this register.
	jo,	ee	1 Indicates that the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 1 has occurred since the last read of this register.
0	Out of Range Channel 0 Interrupt	RUR	DS3/E3/STM-0 Frequency – Out of Range – Channel 0 – Interrupt Status:
	Status 32	9	This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 0, since the last read of this register.
			0 – Indicates that the "DS3/E3/STM-0 Frequency - Out of Range" Interrupt for Channel 0 has NOT occurred since the last read of this register.
			1 – Indicates that the "DS3/E3/STM-0 Frequency – Out of Range" Interrupt for Channel 0 has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 44: APS Mapping Register (Address Location= 0x0180)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Protection C	Channel[3:0]		Working Channel[3:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-4	Protection	R/W	Protection Channel[3:0]:
	Channel[3:0]		These register bits are only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over the AU-4/VC-4 Mode. These register bits are not active for Aggregation Applications.
3-0	Working Channel[3:0]	R/W	Working Channel[3:0]:
			These register bits are only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over the AU-4/VC-4 Mode. These register bits are not active for Aggregation Applications.

Table 45: APS Control Register - 1:1 & 1:N Protection Map (Address Location= 0x0181)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
APS Group Enable	Invoke Payload APS	Protection Channel Timing Source	Receive Payload Bypass	ABS Group Reset	Line Port In Use	Line APS Auto Switch Enable	Line APS Switch		
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W		
0	0	0	00	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7	APS Group Enable	P [™] S [™] C	APS Group Enable: This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over AU-4/VC-4 Mode. This register bit is not active for Aggregation Applications.
6	Invoke Payload APS	RAW	Invoke Payload APS: This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over AU-4/VC-4 Mode. This register bit is not active for Aggregation Applications.
5	Protection Channel Timing Source	R/W	Protection Channel Timing Source: This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI over PPP over AU-4/VC-4 Mode. This register bit is not active for Aggregation Applications.
4	Receive Payload Bypass	R/W	Receive Payload Bypass:This READ/WRITE bit-field permits the user to bypass the receive payload of protection channel.0 - Receive payload is not bypassed.1 - Receive payload is bypassed.



3 APS Group Reset This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over AU-4/VC-4 Mode. This register bit is not active for Aggregation Applications. 2 Line Port In Use R/O Line Port In Use: This READ-ONLY bit-field permits the user to check and identify which Receive STS-3/STM-1 PECL Interface Port is currently being used to receive the incoming STS-3/STM-1 data 1 Line APS Auto O - Indicates that the Primary Receive STS-3/STM-1 PECL Interface Port is the "current port in use". 1 Line APS Auto R/W Line APS Auto Switch Enable: This READ-WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 1 Line APS Auto R/W Line APS Auto Switch feature. In this mode, the XRT94L33 to automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 1 Line APS Switch N Line Enables: This "PS Auto Switch feature. In this mode, the XRT94L33 to automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch N Line APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the	0			
0 Line Port In Use R/O Line Port In Use: This register bit is not active for Aggregation Applications. 2 Line Port In Use: This READ-ONLY bit-field permits the user to check and identify which Receive STS-3/STM-1 PECL Interface Port is currently being used to receive the incoming STS-3/STM-1 data 0 - Indicates that the Primary Receive STS-3/STM-1 PECL Interface Port is the "current port in use". 1 Line APS Auto Switch Enable R/W Line APS Auto Switch Enable: This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary To the "Redundant" port, whenever the Primary Receive STM-1 SQI Processor block declares the LOS (Loss of Signal) defect condition. 0 Line APS Switch Disables the APS Auto Switch feature. In this mode, the XRT94L33 will not automatically switch from the "Primary" port to the "Redundant" port, whenever, the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch N/W Line APS Auto Switch feature cannot be used to support revertive" Switching (e.g., switching from the "Primary" port to the "Redundant" port, whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the ref.) Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software co	3	APS Group Reset	R/W	APS Group Reset:
0 Line APS Muto This READ-ONLY bit-field permits the user to check and identify which Receive STS-3/STM-1 PECL Interface Port is currently being used to receive the incoming STS-3/STM-1 data 0 Indicates that the Primary Receive STS-3/STM-1 PECL Interface Port is the "current port in use". 1 Line APS Auto Switch Enable 1 Line APS Auto Switch Enable: 1 Line APS Auto Switch Enable 1 Line APS Auto Switch Enable 1 Line APS Auto Switch Enable: 1 Line APS Auto Switch Feature. 1 Line APS Auto Switch Feature. In this mode, the XRT94L33 to automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS delect condition. 1 Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS delect condition. 0 Line APS Switch This READ/WRITE bit-field permits the user to command a Line APS switch whenever the Redundant Receive STM-1 SOH Processor block declares the LOS delect condition. 0				configured to operate in either the ATM UNI or PPP over AU-4/VC-4
0 Line APS Auto Switch Enable R/W Line APS Auto Switch Enable: This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch 1 Line APS Switch 1 Line APS Auto Switch Enable 7 Line APS Auto Switch Enable 8 R/W 1 Line APS Auto Switch Enable 1 Line APS Auto Switch Enable 7 Line APS Auto Switch Enable 8 R/W 1 Line APS Auto Switch Frable: Switch Enable 1 Line APS Auto Switch Frable: This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch" feature cannot be used to support revertive" Switching (e.g., switching from the Redundant to the Primary port, whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS	2	Line Port In Use	R/O	Line Port In Use:
0 Line APS Auto 1 Line APS Auto Switch Enable R/W 1 Line APS Auto Switch Enable: This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 0 D – Disables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 1 Line APS Switch 0 R/W 0 Line APS Switch: 0 Not Re				Receive STS-3/STM-1 PECL Interface Port is currently being used to
Port is the "current port in use." 1 Line APS Auto Switch Enable R/W Line APS Auto Switch Enable: This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 0 - Disables the APS Auto Switch feature. In this mode, the XRT94L33 will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature cannot be used to support revertive", switching (e.g., switching from the Redundant to the Primary Pon whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch 0 Line APS Switch 1 Fils READ/WRITE bit-field permits the user to command a Line APS witch (from one port to the other) via software control. 0 Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block.				
Switch Enable This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS (Loss of Signal) defect condition. 0 D - Disables the APS Auto Switch feature. In this mode, the XRT94L33 to automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch 1 End APS Switch ge.g., switching from the Redundant to the Primary Port whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch 1 This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. 0 Line APS Switch 1 This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. 0 Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH				
0 Line APS Switch 0 Configures the Cost of the Redundant Receive STM-1 SOH Processor block 0 Line APS Switch 0 Line APS Switch 0 Line APS Switch 0 Configures each of the three (3) Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 to the condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch 0 NOTE: This "APS Auto Switch" feature cannot be used to support recervive" switching (e.g., switching from the Redundant to the Primary Port whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. 0 Line APS Switch: 0 This READ/WRITE bit-field permits the user to command a	1		R/W	Line APS Auto Switch Enable:
 will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Enables the Ar6 Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block declares the LOS defect condition. NOTE: This "APS Auto Switch" feature cannot be used to support "revertive" switching (e.g., switching from the Redundant to the Primary Pon whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition. Line APS Switch This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. 		Switch Enable		automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STM SOH Processor block declares the LOS
0 Line APS Switch 0 Line APS Switch 0 Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block				will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Rrimary Receive STM-1 SOH Processor block
0 Line APS Switch 0 Difference 0 Line APS Switch 0 Difference 0 Line APS Switch 0 Difference 0 Difference 0 Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. 1 Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block.				device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STM-1 SOH Processor block
 Line APS Switch Line APS Switch: This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. 			lot	reventive" switching (e.g., switching from the Redundant to the Primary Port whenever the Redundant Receive STM-1 SOH Processor block
 This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. 0 - Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. 1 - Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Redundant Receive STM-1 SOH Processor block. 	0	Line APS Switch	R/W	Line APS Switch:
0 – Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block. 1 – Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Redundant Receive STM-1 SOH Processor block.		or	neet	witch (from one port to the other) via software control.
1 – Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Redundant Receive STM-1 SOH Processor block.		theat	adman	0 – Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STM-1 SOH Processor block.
			an	1 – Configures each of the three (3) Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks to accept the incoming SONET traffic from the Redundant Receive STM-1 SOH Processor block.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 46: APS Status Register (Address Location= 0x0194)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	Unused Receive APS Receive APS Parity Check Parity - ODD Enable		Transmit APS Parity Check Enable	Transmit APS Parity - ODD	Transmit APS Parity Error Detected	Receive APS Parity Error Detected	
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-6	Unused	R/O	
5	Receive APS Parity Check Enable	R/W	Receive APS Parity Check Enable This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
4	Receive APS Parity – ODD	R/W	Receive APS Parity - ODD: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
3	Transmit APS Parity Check Enable	R/W	Transmit APS Parity Check Enable: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
2	Transmit APS Parity - ODD	R/W	Transmit APS Parity - ODD: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
1	Transmit APS Parity Error Detected	d R/O	Transmit APS Parity Error Detected: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
0	Receive APS Parity Error Detected	RIO	Receive APS Parity Error Detected: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.



Table 47: APS Status Register (Address Location= 0x0196)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused				APS Group FIFO Overflow Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	ΤΥΡΕ	DESCRIPTION
7-1	Unused	R/O	
0	APS Group FIFO Overflow Status	R/O	APS Group FIFO Overflow Status: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.

		J	ress Location= 0x01			
Віт 7	Віт 6	Віт 5	Віт 4 Ві	т.3 Віт 2	Віт 1	Віт 0
			Unused Viel	851		APS Grou FIFO Underflov Status
R/O	R/O	R/O	R/O R/O	/0 R/0	R/O	R/O
0	0	0		0 0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-1	Unused	R/0	
0	APS Group FIFO Underflow Status	R/O	APS Group FIFO Underflow Status: This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over AU-4/VC-4" Mode. This register bit is NOT active for Aggregation Applications.
	2		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 49: APS Interrupt Register (Address Location= 0x0198)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
		Transmit APS Parity Error Interrupt Status	Receive APS Parity Error Interrupt Status				
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Status	RUR	 Transmit APS Parity Error Interrupt Status: This RESET-upon-READ bit field indicates whether or not the transmit APS module has declared a "Transmit APS Parity Error" Interrupt since the last read of this register. 0 – The "Transmit APS Parity Error" Interrupt has not occurred since the last read of this register. 1 - The "Transmit APS Parity Error" Interrupt has occurred since the last read of this register.
7-0	Receive APS Parity Error Interrupt Status	RUR	 Receive APS Parity Error Interrupt Status: This RESET-upon READ bit-field indicates whether or not the receive APS module has declared a "Receive APS Parity Error" Interrupt since the last read of this register. The "Receive APS Parity Error" Interrupt has not occurred since the last read of this register. The "Receive APS Parity Error" Interrupt has occurred since the last read of this register.

The produce and be



Table 50: APS Interrupt Register (Address Location= 0x019A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Group Overflow Interrupt Status									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-0	Group Overflow Interrupt	RUR	Group Overflow Interrupt Status:
	Status		 This RESET-upon-READ bit-field indicates whether or not group n (0-7) APS protection channel has declared a "FIFO overflow" Interrupt since the last read of this register. 0 - The "FIFO overflow" Interrupt has not occurred since the last read of this register. 1 - The "FIFO overflow" Interrupt has occurred since the last read of this register.

Table 51: APS Interrupt Register (Address Location=0x019B)

Віт 7	Віт 6	Віт 5	Віт 4 🧹	BIT 3	Віт 2	Віт 1	Віт 0			
	Group Underflow Interrupt Status									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			
	aro on ste									

BIT NUMBER	ΝΑΜΕ	Түре	0,	DESCRIPTION
7-0	Group Underflow Interrupt Status	RUR	This F 7) AP since 0 – T read c	Underflow Interrupt Status: ESET-upon-READ bit-field indicates whether or not group n (0- S protection channel has declared a "FIFO underflow" Interrupt the last read of this register. ne "FIFO underflow" Interrupt has not occurred since the last f this register. e "FIFO underflow" Interrupt has occurred since the last read of gister.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2		Віт 1	Віт 0
		Transmit APS Parity Error Interrupt Enable	Receive APS Parity Error Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

Table 52: APS Interrupt Enable Register (Address Location= 0x019C)

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Enable	R/W	Transmit APS Parity Error Interrupt Enable:This READ/WRITE bit-field permits the user to enable or disable the"Transmit APS Parity Error" Interrupt in Transmit APS module0 – Disables the "Transmit APS Parity Error" Interrupt1 – Enables the "Transmit APS Parity Error" Interrupt
7-0	Receive APS Parity Error Interrupt Enable	R/W	Receive APS Parity Error Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "Receive APS Parity Error" Interrupt in Receive APS module 0 – Disables the "Receive APS Parity Error" Interrupt 1 – Enables the "Receive APS Parity Error" Interrupt
			10 ms ev

Table 53: APS Interrupt Enable Register (Address Location= 0x019E)

Віт 7	Віт 6	Віт 5	О Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Group Overflow Interrupt Enable							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	8	N N	0	0	0	0	
	pt show t							

BIT NUMBER	NAME	TYPE	DESCRIPTION			
7-0	Group Overflow	R/W	Group Overflow Interrupt Enable:			
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "FIFO overflow" interrupt in group n APS protection channel.			
			0 – Disables "FIFO overflow" interrupt .			
			1 – Enables "FIFO overflow" Interrupt			



Table 54: APS Interrupt Enable Register (Address Location= 0x019F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Group Underflow Interrupt Enable							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-0	Group Underflow	R/W	Group Underflow Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "FIFO underflow" interrupt in group n APS protection channel.
			0 – Disables "FIFO underflow" interrupt
			1 – Enables "FIFO underflow Interrupt

res "FIFO underflow" inte 1 - Enables "FIFO underflow" inte 1 - Enables "FIFO underflow" inte international int

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1.3 LINE INTERFACE CONTROL BLOCK

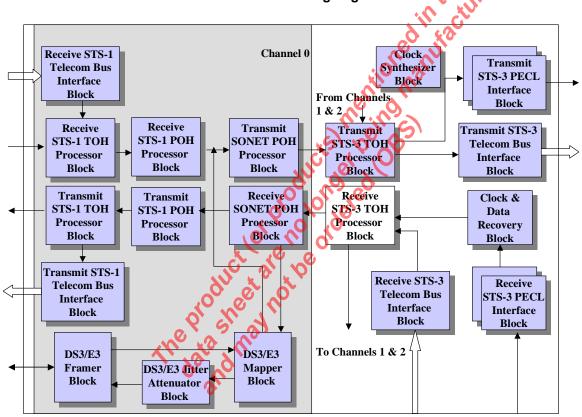
The register map for the Line Interface Control block is presented in the Table below. Additionally, a detailed description of each of the "Line Interface Control" Block registers is presented below.

The Line Interface Control Block registers provide the user with "Command and Control" over the following functional blocks.

- The Transmit STS-3/STM-1 PECL Interface block
- The Receive STS-3/STM-1 PECL Interface block
- The Clock Synthesizer Block

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with each of these "above-mentioned" functional blocks "highlighted" is presented below in Figure 1.

Figure 1: Illustration of the Functional Block Diagram of the XRT94L33, with the Line-Interface-related blocks "High-lighted".





1.3.1 LINE INTERFACE CONTROL REGISTER

Table 55: Line Interface Control Register – Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x0304 – 0x0306	Reserved	0x00
0x0307	Receive Line Status Register	0x00
0x0308 -0x030A	Reserved	0x00
0x030B	Receive Line Interrupt Register	0x00
0x030C – 0x030E	Reserved	0x00
0x030F	Receive Line Interrupt Enable Register	0x00
0x0310 – 0x0382	Reserved	0x00
0x0383	Transmit Line Interface Control Register	0x00



1.3.2 LINE INTERFACE CONTROL REGISTER DESCRIPTION

Table 56: Receive Line Interface Control Register – Byte 1 (Address Location= 0x0302)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	STM-1 Loop-timing Mode	Split Loop Back	Unused	Remote Serial Loop Back	Unused	Analog Local Loop Back Enable	Digital Local Loop Back Enable
R/W	R/W	R/W	R/O	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	thisted
6	STM-1 Loop Timing Mode	R/W	 STM-1 Loop-Timing Mode: This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the Loop-timing Mode. If the user implements this configuration, then the following Transmit STM-1-related functional blocks will use the "Recovered Clock" (Receive STM-1 timing) as its timing source. All three (3) Transmit TUG-3/AU-3 Mapper VC-3 POH Processor blocks The Transmit AU-4 Mapper/VC-4 POH Processor block (if enabled) The Transmit STM-1 SOH Processor block The Transmit STM-1 PECL Interface block The Transmit STM-1 Telecom Bus Interface Block. O – Configures all of the Transmit STM-1 circuitry to operate in the "Local-Timing" Mode (e.g., the above-mentioned functional blocks will use the Clock Synthesizer block as its timing source). 1 – Configures the Transmit STM-1 circuitry to operate in the "Loop-Timing" Mode.
5	Split Loop Back	R/W Atand	 Split Loop-back Enable: This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Split Loop-back" Mode. If the user implements this configuration, then two types of loop-backs will exist within the chip simultaneously. a. A Local Loop-back This loop-back path will originate from the Transmit STM-1 SOH Processor block. It will be routed through a portion of the "Transceiver circuitry" (through the "Transmit Parallel-to-Serial Converter" block) and then back to the "Receive Serial-to-Parallel Converter" block, before being routed to the Receive STM-1 SOH Processor block. b. A Remote Loop-back This loop-back path will originate from the Receive STS-3/STM-1 PECL Interface input. It will be routed through the CDR (Clock & Data Recovery) block; before being routed to the Transmit STS-3/STM-1 PECL Interface output. 0 – Configures the 94L33 to NOT operate in the Split Loop-back Mode 1 – Configures the 94L33 to operate in the Split Loop-back Mode



4	Unused	R/W	
3	Remote Serial		Remote Serial Loop-back Enable:
	Loop Back		This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Remote Serial Loop-back" Mode. In this mode, the incoming (Received Data) will enter the device via the Receive STS-3/STM-1 PECL Interface Input. This signal will then be processed via the CDR (Clock and Data Recovery) Block. At this point, this input signal will proceed via two paths in parallel. In one path, the signal will proceed onto the "Receive Serial-to-Parallel" Converter and then the Receive STM-1 SOH Processor block (and so on). The other path will not proceed through the "Receive Serial-to Parallel" Converter block. Instead this signal will proceed on towards the "Transmit STS-3/STM-1 PECL Interface Output, thereby completing the loop-back path.
			0 – Configures the 94L33 to NOT operate in the Remote Serial Loop-back Mode.
			1 – Configures the 94L33 to operate in the Remote Serial Loop-back Mode.
2	Unused	R/O	
1	Analog Local Loop Back Enable	R/W	Analog Local Loop Back: This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Analog Local Loop Back" Mode. If the user implements this configuration, analog local loop back including data and clock recovery will be enabled 0 – Analog local loop back is disabled 1 – Analog local loop back is enabled
0	Digital Local Loop Back Enable	R/W	Digital Local Loop Back: This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Digital Local Loop Back" Mode. If the user implements this configuration, digital local loop back NOT including data and clock recovery will be enabled. 0 – Digital local loop back is disabled 1 – Digital local loop back is enabled
L	The prot	id ma	

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Table 57: Receive Line Interface Control Register – Byte 0 Address Location= 0x0303)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Primary Receive STS- 3/STM-1 PECL Interface Module Power Down	Redundant Receive STS- 3/STM-1 PECL Interface Module Power Down	Force Training Mode Upon LOS			Unused		
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7	Primary Receive	R/W	Primary Receive STS-3/STM-1 PECL Interface Module Power Down:
	STS-3/STM-1 PECL Interface Module Power		This READ/WRITE bit field permits the user to power down the Primary Receive STS-3/STM-1 PECL Interface Port as described below.
	Down		0 – Powers on Primary Receive ST 33/STM-1 PECL Interface block.
			1 – Powers down the Primary Receive STS-3/STM-1 PECL Interface block. In this mode, the user will not be able to receive STS-3/STM-1 data via the Primary Receive PECC Interface port.
			NOTE: If the user wishes to configure the XRT94L33 device to receive STS-3/STM-1 data via the Primary Receive STS-3/STM-1 PECL Interface port, then he/she MUSTset this bit-field to "0".
6	Redundant	R/W	Redudant Receive STS-3/STM-1 PECL Interface Module Power Down:
	Receive STS- 3/STM-1 PECL Interface Module		This READ/WRITE bit field permits the user to power down the Redundant Receive STS-3/STM-1 PECL Interface Port as described below.
	Power Down		0 + Powers on the Redundant Receive STS-3/STM-1 PECL Interface
		2110	1 – Powers down the Redundant Receive STS-3/STM-1 PECL Interface block. In this mode, the user will not be able to receive STS-3/STM-1 data via the Redundant Receive PECL Interface port.
	ner	No gr	NOTE: If the user wishes to configure the XRT94L33 device to receive STS-3/STM-1 data via the Redundant Receive STS-3/STM-1 PECL Interface port, then he/she MUST set this bit-field to "0".
5	Force Training	R/W	Force Training Mode Upon LOS:
	Mode Upon LOS	31	This READ/WRITE bit field permits the user to configure the Receive STS- 3/STM-1 PECL Interface – CDR (Clock and Data Recovery) phase lock loop to stay in training mode as long as the external LOS is asserted. If the user implements this feature, then the Receive STS-3/STM-1 PECL Interface block CDR PLL will lock onto a clock signal that is ultimately derived from the REFCLK input pin and remain locked onto this signal for the duration that the Receive STS-3/STM-1 PECL Interface block is declaring the LOS_Detect condition.
			0 - Receive Line Interface PLL will NOT stay in training mode
			1 - Receive Line Interface PLL will stay in training mode
4-0	Unused	R/O	



				•			
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Clock Lock Status	Loss of Signal Status	Redundant Receiver Clock Lock Status	Redundant Receiver Loss of Signal Status
R/W	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Table 58: Receive Line Interface Status Register (Address Location= 0x0307)

BIT NUMBER	NAME	Түре	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Status	RUR	Clock Lock Status:
	Status		This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by transceiver
			0 – Indicates clock lock is NOT detected by transceiver
			1 – Indicates clock lock is detected by transceiver
2	Loss of Signal Status	RUR	Loss of Signal Status
	Status		This RESET-upon READ bit field indicates whether or not the loss of signal status is detected by transceiver
			0 – Indicates loss of signal is NOT detected by transceiver
			1 – Indicates loss of signal is detected by transceiver
1	Redundant	RUR	Redundant Receiver Clock Lock Status:
	Receiver Clock Lock Status	10	This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by redundant receiver
			⁶² Indicates clock lock is NOT detected by redundant receiver
	8		1 -Indicates clock lock is detected by redundant receiver
0	Redundant Receiver Loss of	RUR	Redundant Receiver Loss of Signal Status:
	Signal Status	3 13	This RESET-upon-READ bit field indicates whether or not the loss of signal status is detected by redundant receiver
	<u>, 93, </u>	6	0 – Indicates loss of signal is NOT detected by redundant receiver
	ँ रु		1 – Indicates loss of signal is detected by redundant receiver

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Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	lsed		Clock Lock Interrupt	Loss of Signal Interrupt	Redundant Receiver Clock Lock Interrupt	Redundant Receiver Loss of Signal Interrupt
R/W	R/O	R/O	R/O	RUR	RUR	R/O	R/O
0	0	0	0	0	0	0	0

Table 59: Receive Line Interface Interrupt Register (Address Location= 0x030B)

BIT NUMBER	NAME	Түре	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Interrupt	RUR	Clock Lock Interrupt:
	menupt		This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location 0x0307) makes a "0" to "1" or "1" to "0" transition.
			0 – Indicates clock lock interrupt is NOT declared.
			1 – Indicates clock lock is declared
2	Loss of Signal Interrupt	RUR	Loss of Signal Interrupt:
	interrupt		This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition.
			0 – Indicates a loss of signal interrupt is NOT declared.
			1 - Indicates a loss of signal is declared
1	Redundant	RUR	Redundant Receiver Clock Lock Interrupt:
	Receiver Clock Lock Interrupt	nodul	This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location: 0x0307) makes a "0" to "1" or "1" to "0" transition.
	, e	5	Indicates clock lock interrupt is NOT declared.
	A 1.8	2.9	1 – Indicates clock lock is declared
0	Redundant	RUR	Redundant Receiver Loss of Signal Interrupt:
	Receiver Loss of Signal Interrupt		This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition.
			0 – Indicates a loss of signal interrupt is NOT declared.
			1 – Indicates a loss of signal is declared



Table 60: Receive Line Interface Interrupt Register (Address Location= 0x030F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Clock Lock Interrupt Enable	Loss of Signal Interrupt Enable	Redundant Receiver Clock Lock Interrupt Enable	Redundant Receiver Loss of Signal Interrupt Enable
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-4	Unused	R/O	is d
3	Clock Lock Interrupt Enable	R/W	Clock Lock Interrupt Enable: This READ/WRITE bit field disables or enables the clock lock interrupt. 0 – Disables clock lock interrupt 1 – Enables clock lock interrupt
2	Loss of Signal Interrupt	R/W	Loss of Signal Interrupt Enable: This READ/WRITE bit field disables or enables the loss of signal interrupt. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt
1	Redundant Receiver Clock Lock Interrupt Enable	R/W	Redundant Receiver Clock Lock Interrupt Enable: This READ/WRITE bit field disables or enables the clock lock interrupt for the redundant receiver block. 0- Disables clock lock interrupt 1 - Enables clock lock interrupt
0	Redundant Receiver Loss of Signal Interrupt	R/W	 Redundant Receiver Loss of Signal Interrupt Enable: This READ/WRITE bit field disables or enables the loss of signal interrupt for the redundant receiver block. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt



Table 61: Transmit Line Interface Control Register (Address Location= 0x0383)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Primary Transmit STS-3/STM- 1 PECL Interface Enable	Transmit Clock Enable	Clock Synthesizer Block as Timing Source	Redundant Transmit STS-3/STM- 1 PECL Interface Block Enable	Unused	Unused	REFCLK	SEL[1:0]
R/W	R/W	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	
7	Primary Transmit STS-3/STM-1	R/W	Primary Transmit STS-3/STM-1 PECL Interface Enable:
	PECL Interface Enable		This READ/WRITE bit field permits the user to enable or disable the Transmit STS-3/STM-1 PECL Interface output drivers as described below.
			0 – Disables the Transmit STS-3/STM-1 PECL Interface output drivers.
			1 – Enables the Transmit STS-3/STM-1 PECL Interface output drivers.
			NOTE: The user MUST set this bit-field to "1" in order to transmit any traffic via the Transmit STS-3/STM-1 PECL Interface output.
6	Transmit Clock	R/W	Transmit Clock Enable:
	Enable		This READ WRITE bit field permits the user to enable or disable the transmitter clock output.
			0 – Disables transmitter clock output
			1 – Enables transmitter clock output
5	Clock	R/W	Clock Synthesizer as Timing Source:
	Synthesizer as Timing Source	oduc	This READ/WRITE bit field permits the user to select either the Clock Synthesizer block or the signal applied at the REFTTL input as the source of the Transmit 19.44MHz clock.
	the	to a	0 This setting configures the "Transmit SONET" circuitry to by-pass the Clock Synthesizer block and to directly use the 19.44MHz clock signal that is provided to the REFTTL input pin) as its timing source. In this case, the "Clock Synthesizer" block is by-passed.
	0	and	1 – This setting configures the "Transmit SONET" circuitry to use the output of the Clock Synthesizer block as its timing source.
			NOTE: If the user opts to by-pass the Clock Synthesizer (by setting this register bit to "0") then he/she MUST apply a 19.44MHz clock signal to the REFTTL input pin.
4	Redundant Transmit STS-	R/W	Redundant Transmit STS-3/STM-1 PECL Interface Enable:
	3/STM-1 PECL Interface Enable		This READ/WRITE bit field permits the user to enable or disable the Redundant Transmit STS-3/STM-1 PECL Interface output pads. If the user enables the "Redundant Transmit STS-3/STM-1 PECL Interface" block, then it will begin to transmit the exact same data as is the "Primary Transmit STS-3/STM-1 PECL Interface" block.
			0 – Disables the Redundant Transmit STS-3/STM-1 PECL Interface block
			1 – Enables the Redundant Transmit STS-3/STM-1 PECL Interface block



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			NOTE: If the user wishes to use the "Line APS" features within the XRT94L33 device, then he/she MUST enable the "Redundant Transmit STS-3/STM-1PECL Interface block.
3	Unused	R/W	Serial Loopback:
			This READ/WRITE bit field permits the user to enable or disable serial loopback.
			0 – Disables Serial loopback
			1 – Enables Serial loopback
2	Unused	R/O	
1-0	Clock	R/W	Clock Synthesizer Block Frequency Select[1:0]:
	Synthesizer Block Frequency Select[1:0]		This READ/WRITE bit field permits the user to select the desired reference clock speed as follows:
			00 = 19.44 MHz
			01 = 38.88 MHz
			clock speed as follows: 00 = 19.44 MHz 01 = 38.88 MHz 10 = 51.85 MHz 11 = 77.76 MHz
			11 = 77.76 MHz

11 = 77.76 MHz 11 = 77.76 MHz 11 = 77.76 MHz 10 mar 10 ma

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



1.4 RECEIVE STM-1 SOH PROCESSOR BLOCK

The register map for the Receive STM-1 SOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STM-1 SOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 whenever it has been configured to operate in the SDH/TUG-3 and the SDH/AU-3 Modes, with the "Receive STM-1 SOH Processor Block "highlighted" is presented below in Figure 2 and 3

Figure 2: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the SDH/TUG-3 Mode), with the Receive STM-1 SOH Processor Block "High-lighted".

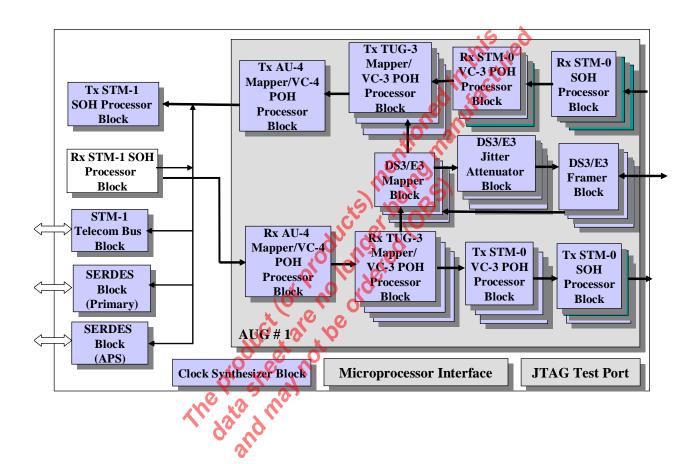
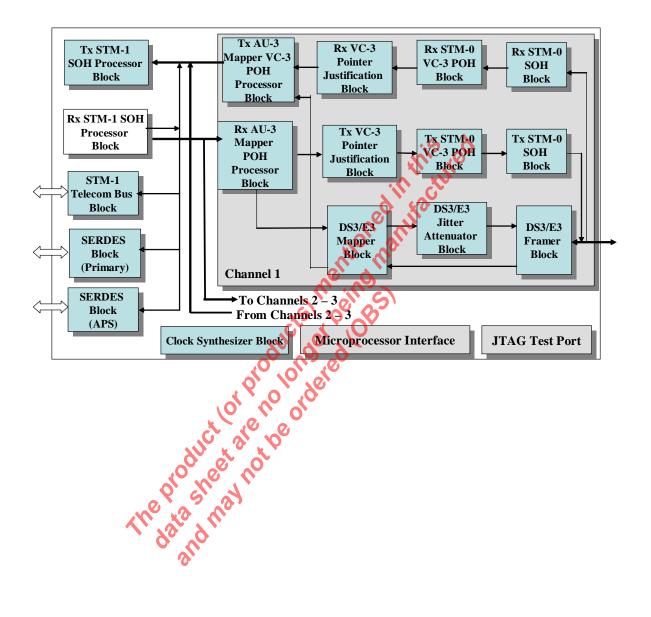




Figure 3: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the "SDH/AU-3" Mode), with the Receive STM-1 SOH Processor Block "highlighted"



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RECEIVE STM-1 SOH PROCESSOR BLOCK REGISTERS

Table 62: Receive STM-1 SOH Processor Block Control Register – Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x1000 - 0x1102	Reserved	
0x1103	Receive STM-1 Section Control Register – Byte 0	0x00
0x1104 – 0x1105	Reserved	0x00
0x1106	Receive STM-1 Section Status Register – Byte 1	0x00
0x1107	Receive STM-1 Section Status Register – Byte 0	0x02
0x1108	Reserved	0x00
0x1109	Receive STM-1 Section Interrupt Status Register – Byte 2	0x00
0x110A	Receive STM-1 Section Interrupt Status Register – Byte 1	0x00
0x110B	Receive STM-1 Section Interrupt Status Register – Byte 0	0x00
0x110C	Reserved	0x00
0x110D	Receive STM-1 Section Interrupt Enable Register - Byte 2	0x00
0x110E	Receive STM-1 Section Interrupt Enable Register Byte 1	0x00
0x110F	Receive STM-1 Section Interrupt Enable Register - Byte 0	0x00
0x1110	Receive STM-1 Section - B1 Byte Error Sount Register – Byte 3	0x00
0x1111	Receive STM-1 Section - B1 Byte Error Count Register – Byte 2	0x00
0x1112	Receive STM-1 Section - B) Byte Error Count Register – Byte 1	0x00
0x1113	Receive STM-1 Section B1 Byte Error Count Register – Byte 0	0x00
0x1114	Receive STM-1 Section B2 Byte Error Count Register – Byte 3	0x00
0x1115	Receive STM-Section - B2Byte Error Count Register – Byte 2	0x00
0x1116	Receive STM-1 Section - B2 Byte Error Count Register – Byte 1	0x00
0x1117	Receive STM Section - B2 Byte Error Count Register – Byte 0	0x00
0x1118	Receive STM-1 Section - MS-REI Event Count Register – Byte 3	0x00
0x1119	Receive STM-1 Section - MS-REI Event Count Register – Byte 2	0x00
0x111A	Receive STM-1 Section - MS-REI Event Count Register - Byte 1	0x00
0x111B	Receive STM-1 Section - MS-REI Event Count Register – Byte 0	0x00
0x111E	Reserved	0x00
0x111F	Receive STM-1 Section K1 Byte Value Register	0x00
0x1120 - 0x1122	Reserved	0x00
0x1123	Receive STM-1 Section K2 Byte Value Register	0x00
0x1124 – 0x1126	Reserved	0x00
0x1127	Receive STM-1 Section S1 Byte Value Register	0x00



Address Location	REGISTER NAME	DEFAULT VALUES
0x1128 – 0x112A	Reserved	0x00
0x112B	Receive STM-1 Section – In-Sync Threshold Value Register	0x00
0x112C, 0x112D	Reserved	0x00
0x112E	Receive STM-1 Section – LOS Threshold Value – MSB	0xFF
0x112F	Receive STM-1 Section – LOS Threshold Value – LSB	0xFF
0x1130	Reserved	0x00
0x1131	Receive STM-1 Section – SF Set Monitor Interval – Byte 2	0x00
0x1132	Receive STM-1 Section – SF Set Monitor Interval – Byte 1	0x00
0x1133	Receive STM-1 Section – SF Set Monitor Interval – Byte 0	0x00
0x1134 – 0x1135	Reserved	0x00
0x1136	Receive STM-1 Section – SF Set Threshold – Byte 1	0x00
0x1137	Receive STM-1 Section – SF Set Threshold – Byte 0	0x00
0x1138, 0x1139	Reserved	0x00
0x113A	Receive STM-1 Section – SF Clear Threshold – Byte 1	0x00
0x113B	Receive STM-1 Section – SF Clear Threshold – Byte 0	0x00
0x113C	Reserved	0x00
0x113D	Receive STM-1 Section - SD Set Monitor Interval – Byte 2	0x00
0x113E	Receive STM-1 Section – SD Set Monitor Interval – Byte 1	0x00
0x113F	Receive STM-1 Section – SD Set Monitor Interval – Byte 0	0x00
0x1140, 0x1141	Reserved	0x00
0x1142	Receive STM-1 Section - SD Set Threshold - Byte 1	0x00
0x1143	Receive STM-1 Section – SD Set Threshold – Byte 0	0x00
0x1144, 0x1145	Reserved	0x00
0x1146	Receive STM-1 Section – SD Clear Threshold – Byte 1	0x00
0x1147	Receive STM-1 Section – SD Clear Threshold – Byte 0	0x00
0x1148 – 0x114A	Reserved	0x00
0x114B	Receive STM-1 Section – Force SEF Condition	0x00
0x114C, 0x114E	Reserved	0x00
0x114F	Receive STM-1 Section – Receive Section Trace Message Buffer Control Register	0x00
0x1150, 0x1151	Reserved	0x00
0x1152	Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 1	0x00
0x1153	Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 0	0x00



Address Location	REGISTER NAME	DEFAULT VALUES
0x1154, 0x1155	Reserved	0x00
0x1156	Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 1	0x00
0x1157	Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 0	0x00
0x1158	Reserved	0x00
0x1159	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x115A	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x115B	Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x115C	Reserved	0x00
0x115D	Receive STM-1 Section – Receive SF Clear Monitor Interval Byte 2	0xFF
0x115E	Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x115F	Receive STM-1 Section – Receive SF Clear Monitor Byte 0	0xFF
0x1160 – 0x1162	Reserved	0x00
0x1163	Receive STM-1 Section – Auto AIS Control Register	0x00
0x1164 – 0x1166	Reserved	0x00
0x1167	Receive STM-1 Section – Serial Port Control Register	0x00
0x1168 – 0x116A	Reserved	0x00
0x116B	Receive STM-1 Section - Auto AIS (in Downstream STM-0s) Control Register	0x000
0x116C – 0x1179	Reserved	
0x117A	Receive STM-1 Section - SOH Capture Indirect Address	0x00
0x117B	Receive STM-1 Section – SOH Capture Indirect Address	0x00
0x117C	Receive STM-1 Section SOH Capture Indirect Data	0x00
0x117D	Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x117E	Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x117F	Receive STM- Section – SOH Capture Indirect Data	0x00
0x1180 – 0x11FF	Reserved	0x00



1.4.1 RECEIVE STM-1 SOH PROCESSOR BLOCK REGISTER DESCRIPTION

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-N OH Extract	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble Disable	SDH/ SONET*	MS-REI Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Table 63: Receive STM-1 Section Control Register – Byte 0 (Address Location= 0x1103)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	STS-N OH	R/W	STS-N Overhead Extract (Revision C Silicon Only):
	Extract		This READ/WRITE bit-field permits the user to configure the RxSOH output port to output the SOH for all lower tributary STM-0s within the incoming STM-1 signal.
			0 – Disables this feature. In this mode, the RxSOH output port will only output the SOH for the first STM-0 within the incoming STM-1 signal.
			1 – Enables this feature.
6	SF Defect	R/W	Signal Failure (SF) Defect Condition Detect Enable:
	Condition Detect Enable		This READWRITE bit-field permits the user to enable or disable SF Defect Declaration and Clearance by the Receive STM-1 SOH Processor Block, as described below.
			0 – Configures the Receive STM-1 SOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified" SF defect declaration and clearance criteria.
		U.S.	1 – Configures the Receive STM-1 SOH Processor block to declare and clear the SF defect condition per the "user-specified" SF defect declaration and clearance" criteria.
			NOTE: The user must set this bit-field to "1" in order to permit the Receive STM-1 SOH Processor block to declare and clear the SF defect condition.
5	SD Defect	R/W	Signal Degrade (SD) Defect Condition Detect Enable:
	Condition Detect Enable	a m	This READ/WRITE bit-field permits the user to enable or disable SD Declaration and Clearance by the Receive STM-1 SOH Processor Block as described below.
		0	0 – Configures the Receive STM-1 SOH Processor blolck to NOT declare nor clear the SD defect condition per the "user-specified" SD defect declaration and clearance criteria.
			1 – Configures the Receive STM-1 SOH Processor block to declare and clear the SD defect condition per the "user-specified SD defect declaration and clearance" critieria.
			NOTE: The user must set this bit-field to "1" in order to permit the Receive STM-1 SOH Processor block to declare and clear the SD defect condition.
4	Descramble	R/W	De-Scramble Disable:
	Disable		This READ/WRITE bit-field permits the user to either enable or disable de- scrambling by the Receive STM-1 SOH Processor block.
			0 – De-Scrambling is enabled.



			1 – De-Scrambling is disabled.
3	SDH/SONET*	R/W	SDH/SONET Select:
			This READ/WRITE bit-field permits the user to configure the XRT94L33 device to operate in either the SONET or SDH Mode.
			0 – Configures the XRT94L33 device to operate in the SONET Mode.
			1 – Configures the XRT94L33 device to operate in the SDH Mode.
2	MS-REI Error	R/W	MS-REI (Line – Remote Error Indicator) Error Type:
	Туре		This READ/WRITE bit-field permits the user to specify how the Receive STM-1 SOH Processor block will count (or tally) MS-REI events, for Performance Monitoring purposes. The user can configure the Receive STM-1 SOH Processor block to increment MS-REI events on either a "perbit" or "per-frame" basis. If the user configures the Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Receive STM-1 Section MS-REI Event Count" register by the contents within the M1 byte of the incoming STM-1 data-stream.
			If the user configures the Receive STM-1 SOH Processor block to increment MS-REI events on a "per frame" basis, then it will increment the "Receive STM-1 Section MS-REI Event Count" register each time it receives an STM-1 frame, in which the M1 byte is set to a "non-zero" value. 0 – Configures the Receive STM-1 SOH Processor block to count or tally
			MS-REI events on a per-bit basis.
			1 – Configures the Receive STM-1 SOH Processor block to count or tally MS-REI events on a per-frame basis.
1	B2 Error Type	R/W	B2 Error type: This READ/WRITE bit-field permits the user to specify how the "Receive STM-1 SOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-1 SOH Processor block to increment B2 byte errors on either a "per- bit" or a "per-frame" basis. If the user configures the Receive STM-1 SOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the Receive STM-1 Section - B2 Byte Error Count" register by the number of bits (within each of the three B2 byte values) that is in error.
	The	or sr	If the user configures the Receive STM-1 SOH Processor block to increment B2 byte errors on a "per-frame" basis, then it will increment the "Receive STM-1 Section - B2 Byte Error Count" Register, each time it receives an STM-1 frame that contains at least one erred B2 byte.
		31	0 – Configures the Receive STM-1 SOH Processor block to count B2 byte errors on a "per-bit" basis.
			1 – Configures the Receive STM-1 SOH Processor block to count B2 byte errors on a "per-frame" basis.
0	B1 Error Type	R/W	B1 Error Type:
			This READ/WRITE bit-field permits the user to specify how the Receive STM-1 SOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-1 SOH Processor block to increment B1 byte errors on either a "perbit" or "per-frame" basis. If the user configures the Receive STM-1 SOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Receive Section B1 Error Count" register by the number of bits (within the B1 byte value) that is in error.
			If the user configures the Receive STM-1 SOH Processor block to increment B1 byte errors on a "per-frame" basis, then it will increment the



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"Receive STM-1 Section - B1 Byte Error Count" Register each time it receives an STM-1 frame that contains an erred B1 byte.
0 – Configures the Receive STM-1 SOH Processor block to count B1 byte errors on a "per-bit" basis.
1 – Configures the Receive STM-1 SOH Processor block to count B1 byte errors on a "per-frame" basis.

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Віт 7	Віт 6	Віт 6 Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
		Unused	MS-TIM Mismatch Defect Declared	Section Trace Message Unstable Defect Declared	MS-AIS Defect Declared		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Table 64: Receive STM-1 Section Status Register – Byte 1 (Address Location= 0x1106)

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 3	Unused	R/O	is d
2	MS-TIM Defect Declared	R/O	 MS-TIM Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the MS-TIM defect condition within the incoming STM-1 data-stream. The Receive STM-1 SOH Processor block will declare the MS-TIM defect condition, whenever it accepts a Section Trace Message (via the 00 byte, within the incoming STM-1 data-stream) that differs from the "Expected Section Trace Message". 0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the MS-TIM Defect Condition. 1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the MS-TIM Defect Condition.
1	Section Trace Message Unstable Defect Declared	R/O	 Section Trace Message Unstable Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STM-1 SOH Processor block will declare the Section Trace Message Unstable defect condition, whenever the "Section Trace Message Unstable" counter reaches the value 8. The Receive STM-1 SOH Processor block will increment the "Section Trace Message Unstable" counter reaches the value 8. The Receive STM-1 SOH Processor block will increment the "Section Trace Message Unstable" counter each time that it receives a Section Trace Message Unstable" counter to "Deviously received a given Section Trace Message 3 (or 5) consecutive times. Note: The Receive STM-1 SOH Processor block will also clear the "Section Trace Message Unstable" defect condition" once it has received a given Section Trace Message 3 (or 5) consecutive times. 0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the Section Trace Message Unstable defect condition. 1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the Section Trace Message Unstable defect condition.
0	MS-AIS Defect Declared	R/O	MS-AIS Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the MS-AIS (Line AIS) defect condition within the incoming STM-1 data stream. The Receive STM-1 SOH Processor block will declare the MS-AIS defect condition within the incoming STM-1 data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STM-1 frames.



0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the MS-AIS defect condition.
1 – Indicates that the Receive STM-1 SOH Processor block currently declaring the MS-AIS defect condition.

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Table 65: Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
MS-RDI Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	MS-RDI	R/O	MS-RDI (Line Remote Defect Indicator) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the MS-RDI defect condition within the incoming STM-1 signal. The Receive STM-1 SOH Processor block will declare the MS-RDI defect condition whenever it determines that bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive incoming STM-1 frames 0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the MS-RDI defect condition 1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the MS-RDI defect condition
	e + =		the MS-RDI defect condition?
6	S1 Byte Unstable Defect Declared	R/O	 S1 Byte Unstable Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Receive STM-1 SOH Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The Receive STM-1 SOH Processor block will increment the "S1 Byte Unstable Counter" each time that it receives an STM-1 frame that contains an S1 byte that differs from the previously received S1 byte. The Receive STM-1 SOH Processor block will clear the contents of the "S1 Byte Unstable Counter" to "0" whenever it receives the same S1 byte for 8 consecutive STM-1 frames. 0 - Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the "S1 Byte Unstable Defect Condition. 1 - Indicates that the Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable Defect Condition.
		1 20	"St Byte Unstable Defect Condition.
5	K1, K2 Byte	R/O	K1, K2 Byte Unstable Defect Declared:
	Unstable Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Receive STM-1 SOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever it fails to receive the same set of K1, K2 bytes, in 12 consecutive STM-1 frames. The Receive STM-1 SOH Processor block will clear the "K1, K2 Byte Unstable" defect condition whenever it receives a given set of K1, K2 byte values within three consecutive STM-1 frames.
			0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the K1, K2 Byte Unstable Defect Condition.
			1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the K1, K2 Byte Unstable Defect Condition.
4	SF Defect Declared	R/O	SF (Signal Failure) Defect Declared:



	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the LOS (Loss of Signal) defect condition.
0	LOS	R/O	LOS (Loss of Signal) Defect Declared:
			1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the SEF defect condition.
			0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the SEF defect condition.
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the SEF defect condition. The Receive STM-1 SOH Processor block will declare the SEF defect condition if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Receive STM-1 Section – In-Sync Threshold Value Register (Address Location= 0x112B) are met.
1	SEF Defect	RÍO	SEF (Severely Errored Frame) Defect Declared:
	the		 O – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the LOF defect condition. O – Indicates that the Receive STM-1 SOH Processor block is currently declaring the LOF defect condition.
	Declared	odu	This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the LOF defect condition. The Receive STM-1 SOH Processor block will declare the LOF defect condition, if it has been declaring the SEF (Severely Errored Frame) defect condition for 3ms (or 24 SONET frame periods).
2	LOF Defect	R/O	LOF (Loss of Frame) Defect Declared:
			 1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the SD Defect condition. This bit is set to '1" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
			This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SD Defect Declaration" threshold.
			 0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the SD Defect condition.
-	Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the SD defect condition. The Receive STM-1 SOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold.
3	SD Defect	R/O	given interval of time) does exceed the "SF Defect Declaration" threshold. SD (Signal Degrade) Defect Declared:
			the SF Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a
			This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold. 1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring
			0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the SF Defect condition.
			This READ-ONLY bit-field indicates whether or not the Receive STM-1 SOH Processor block is currently declaring the SF defect condition. The Receive STM-1 SOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold.



The Receive STM-1 SOH Processor block will declare the LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STM-1 data stream.
Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STM-1 Section – LOS Threshold Value" Register (Address Location= 0x112E and 0x112F).
0 – Indicates that the Receive STM-1 SOH Processor block is NOT currently declaring the LOS defect condition.
1 – Indicates that the Receive STM-1 SOH Processor block is currently declaring the LOS defect condition.

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Table 66: Receive STM-1 Section Interrupt Status Register – Byte 2 (Address Location= 0x1109)

Віт 7	Віт 6	BIT 5 BIT 4 BIT 3 BIT 2		Віт 1	Віт 0		
		Change of MS- AIS	Change of MS- RDI				
		Defect Condition Interrupt Status	Defect Condition Interrupt Status				
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of MS- AIS Defect Condition	RUR	Change of MS-AIS (Line AIS) Defect Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of
	Interrupt Status		MS-AIS Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			Whenever the Receive STM-1 SOH Processor block declares the MS-AIS defect condition.
			Whenever the Receive STM-1 SOH Processor block clears the MS-AIS defect condition.
			0 – Indicates that the "Change of MS-AIS Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of MS-AIS Defect Condition" interrupt has occurred since the last read of this register.
		AUC	Note: The user can determine if the Receive STM-1 SOH Processor block is currently declaring the MS-AIS defect condition by reading the contents of Bit 0 (MS-AIS Defect Declared) within the "Receive STM-1 Section Status Register – Byte 1" (Address Location = 0x1106).
0	Change of MS-RDI Defect	RUR	Change of MS-RDI (Line - Remote Defect Indicator) Defect Condition
	Condition Interrupt Status	andma	This RESET-upon-READ bit-field indicates whether or not the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			• Whenever the Receive STM-1 SOH Processor block declares the MS-RDI defect condition.
			• Whenever the Receive STM-1 SOH Processor block clears the MS-RDI defect condition.
			0 – Indicate that the "Change of MS-RDI Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine if the Receive STM-1 SOH Processor block is currently declaring the MS-RDI defect condition by reading out the state of Bit 7 (MS-RDI Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0" (Address Location = 0x1107).

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Table 67: Receive STM-1 Section Interrupt Status Register – Byte 1 (Address Location = 0x110A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status	Change in Section Trace Message Unstable Defect Condition Interrupt Status	New Section Trace Message Interrupt Status	Change in MS-TIM Defect Condition Interrupt Status	Receive SOH CAP DONE Interrupt Status	Change in K1, K2 Bytes Unstable Defect Condition Interrupt Status	NEW K1K2 Byte Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

			is d
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	New S1 Byte	RUR	New S1 Byte Value Interrupt Status:
	Value Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate the "New S1 Byte Value" Interrupt, anytime it has "accepted" a new S1 byte, from the incoming STM-1 data-stream
			0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register.
			Note The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STM-1 Section S1 Byte Value" register (Address Location= 0x1127).
6	Change in S1	RUR	Change in \$1 Byte Unstable Defect Condition Interrupt Status:
Defect Cor Interrupt S	Byte Unstable Defect Condition Interrupt Status	ect Condition	This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
	ne P.	S N	Whenever the Receive STM-1 SOH Processor block declares the "S1 Byte Unstable" defect condition.
	1,93	nd	• Whenever the Receive STM-1 SOH Processor block clears the "S1 Byte Unstable" defect condition.
		C	0 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine if the Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable" Defect condition by reading the contents of Bit 6 (S1 Byte Unstable Condition Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0" (Address Location = 0x1107).
5	Change in Section Trace	RUR	Change in Section Trace Message Unstable Defect condition Interrupt Status:
	Message Unstable Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Message Unstable" defect condition interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor



	Interrupt Statue		block will concrete this interrupt in reapones to either of the following events
	Interrupt Status		block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-1 SOH Processor block declares the "Section Trace Message Unstable" defect condition.
			• Whenever the Receive STM-1 SOH Processsor block clears the "Section Trace Message Unstable" defect condition.
			0 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has occurred since the last read of this register.
4	New Section	RUR	New Section Trace Message Interrupt Status:
	Trace Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New Section Trace Message" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it has accepted a new "Section Trace" Message within the incoming STM-1 data-stream.
			0 – Indicates that the "New Section Frace Message Interrupt" has not occurred since the last read of this register.
			1 – Indicates that the "New Section Trace Message Interrupt" has occurred since the last read of this register.
			Note: The user can read out the contents of the "Receive Section Trace Message Buffer", which is located at Address location 0x1300 through 0x133F
3	Change in MS-	RUR	Change in MS-TIM Defect Condition Interrupt Status:
	TIM Defect Condition Interrupt Status		This RESET upon READ bit-field indicates whether or not the "Change in MS-TIM Detect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-1 SOH Processor block declares the "MS-TUM" defect condition.
		N	 Whenever the Receive STM-1 SOH Processor block clears the "MS-TIM" defect condition.
		orocx	9 Indicates that the "Change in MS-TIM Defect Condition" interrupt has not occurred since the last read of this register.
	the	20	Indicates that the "Change in MS-TIM Defect Condition" interrupt has occurred since the last read of this register.
		or she	Note: The user can determine whether the Receive STM-1 SOH Processor block is currently declaring the "Section Trace Message Mismatch" defect condition by reading the state of Bit 2 (MS-TIM Defect Declared) within the "Receive STM-1 Section Status Register – Byte 1 (Address Location = 0x1106).
2	Receive SOH	RUR	Receive SOH Capture DONE – Interrupt Status:
	CAP DONE Interrupt Status		This RESET-upon-READ bit-field indicates whether the "Receive SOH Data Capture" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-1 SOH Processor block will generate an interrupt anytime it has captured the last SOH byte into the Capture Buffer.
			Note: Once the SOH (of a given STM-1 frame) has been captured and loaded into the "Receive SOH Capture" buffer, it will remain there for one SONET frame period.
			0 - Indicates that the "Receive SOH Data Capture" Interrupt has NOT



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			occurred since the last read of this register.
			-
			1 – Indicates that the "Receive SOH Data Capture" Interrupt has occurred since the last read of this register.
1	1 Change in K1, K2 Byte Unstable Defect Condition Interrupt Status	RUR	Change of K1, K2 Byte Unstable Defect Condition Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-1 SOH Processor block declares the "K1, K2 Byte Unstable Defect" condition.
			• Whenever the Receive STM-1 SOH Processor block clears the "K1, K2 Byte Unstable Defect" condition.
			0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine if the Receive STM-1 SOH Processor block is currently declaring the "K1, K2 Byte Unstable Defect Condition" by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Receive STM-1 Section Status Register – Byte 0" (Address Location = 0x1107).
0	New K1, K2 Byte Value Interrupt Status	RUR	New K1, K2 Byte Value Interrupt Status: This RESET upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt whenever it has "accepted" a new set of K1, K2 byte values from the incoming STM-1 data-stream. 0 Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
		. Jot	1 Undicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
	thepr	anna	Note: The user can obtain the contents of the new K1 byte by reading out the contents of the "Receive STM-1 Section K1 Byte Value" Register (Address Location= 0x111F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STM-1 Section K2 Byte Value" Register (Address Location= 0x1123).
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Table 68: Receive STM-1 Section Interrupt Status Register – Byte 0 (Address Location= 0x110B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in SF Defect Condition Interrupt Status	Change in SD Defect Condition Interrupt Status	Detection of MS-REI Event Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Condition Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7	Change in SF	RUR	Change of Signal Failure (SF) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			Whenever the Receive STM-TSOH Processor block declares the SF Defect Condition.
			Whenever the Receive STM-1 SOH Processor block clears the SF Defect Condition.
			0 – Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-1 SOH Processor block is currently declaring the "SF" defect condition by reading out the state of Bit 4 (SF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107).
6	Change of SD	RUR	Change of Signal Degrade (SD) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status	Prost	This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
		diand	• Whenever the Receive STM-1 SOH Processor block declares the SD Defect Condition.
			• Whenever the Receive STM-1 SOH Processor block clears the SD Defect Condition.
			0 - Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-1 SOH Processor block is declaring the "SD" defect condition by reading out the state of Bit 3 (SD Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107).
5	Detection of MS- REI Event Interrupt Status	RUR	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt Status:



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3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 2 Change of LOF Interrupt Status RUR Byte Error Interrupt Status RUR Byte Error Interrupt Status 2 Change of LOF Defect Condition Interrupt Status RUR Change of LOF Defect Condition Interrupt Status RUR Change of LOF Defect Condition Interrupt As occurred since the last read of this register. I = Indicates that the "Change of LOF Defect Condition Interrupt Has occurred since the last read of this register. I = Indicates that the "Change of LOF Defect Condition Interrupt Has occurred since the last read		Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of
2 Change of LOF Defect Condition Interrupt Status RUR RUR RUR Byte Error Interrupt Status RUR RUR RUR RUR RUR RUR RUR RUR RUR RUR				MS-REI Event" Interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it detects an MS-REI event within the incoming STM-1 data-
4 Detection of B2 Byte Error Interrupt Status RUR Byte Error Interrupt Status Detection of B2 Byte Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STM-1 data-stream. 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status Detection of B1 Byte Error Interrupt Mas occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR Change of LOS of Frame (LOF) Defect Condition Interrupt Mas NOT occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR Change of LOS of Frame (LOF) Defect Condition Interrupt Mas NOT occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status Change of LOS of Frame (LOF) Defect Condition Interrupt Mas NOT occurred since the last read of this register. 1 Indicates that the "Change of LOF Defect Condition" interrupt Mas NOT occurred since the last read of this register. 2 Change of LOF Defect Condition In Receviee STM-1 SOH Processor block declares the LOF defect condition				
Byte Error Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt as the "Detection of B2 Byte Error Interrupt" has not occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Mas occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status RUR RUR Cocurred Since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status RUR RUR RUR RUR Change of LOF Defect Condition Interrupt Status Detection of B1 Byte Error Interrupt Mas not occurred Since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR RUR Change of LOS Sof Frame (LOF) Defect Condition Interrupt Mas NOT occurred Since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR RUR RUR RUR RUR RUR RUR RUR RUR RUR				
Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STM-1 data-stream. 3 Detection of B1 Byte Error RUR Detection of B1 Byte Error Interrupt Status: 3 Detection of B1 Byte Error RUR Detection of B1 Byte Error Interrupt Status: 1 Interrupt Status RUR Detection of B1 Byte Error Interrupt Status: 1 This RESET-upon READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt Status: This RESET-upon READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 3 Detection of B1 Byte Error Interrupt "has occurred since the last read of this register. 4 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status: The RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Has occurred since the last read of this register. I - Indicates that the "Change of LOF Def	4		RUR	Detection of B2 Byte Error Interrupt Status:
3 Detection of B1 Byte Error Interrupt Status RUR Detection of B1 Byte Error Interrupt Status: This RESET-upon READ of Field indicates whether or not the "Detection of B1 Byte Error Interrupt Status 3 Detection of B1 Byte Error Interrupt Status RUR Detection of B1 Byte Error Interrupt Status: This RESET-upon READ of Field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive S1M-1 SDH Processor block will generate this interrupt anytime it detects as B1 byte error within the incoming S1M-1 data-stream. 0 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 1 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR Figstel 0 Figstel This RESET-upon READ bit-field indicates whether or not the "Change of UPF Defect Condition" interrupt has occurred since the last read of this register. 1 Change of LOF Defect Condition. Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. 0 - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 Change of SEF Defect Condition Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. 1 Change of SEF Defect Condition Note				B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt
3 Detection of B1 Byte Error Interrupt Status RUR Byte Error Interrupt Status Petection of B1 Byte Error Interrupt Status: This RESET-upon READ Dicfield indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B1 bre error within the incoming STM-1 data-stream. 0 - Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status RUR Figster Change of LOF Defect Condition Interrupt Status 4 Change of LOF Defect Condition Interrupt Status RUR Figster Change of LOS Defect Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 4 Whenever the Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events. 6 Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. 7 - Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 8 Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. 9 - Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 1 - Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the				
Byte Error Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B1 byte error within the incoming STM-1 data-stream. 2 Change of LOF Defect Condition Interrupt Status RUR Change of toes of Frame (LOF) Defect Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition Interrupt Status 4 Change of LOF Defect Condition RUR 6 Henever the Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • <td< td=""><td></td><td></td><td></td><td></td></td<>				
Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 0 - Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status: 1 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status: 1 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status: 1 - Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. 2 Change of LOF Defect Condition Interrupt Status: 1 - Indicates that the "Change of LOF Defect Condition Interrupt Status: 1 - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of th	3		RUR	Detection of B1 Byte Error Interrupt Status:
2 Change of LOF Defect Condition Interrupt Status: 2 Change of LOF Defect Condition Interrupt Status: 1 Interrupt Status 2 Change of LOF Defect Condition Interrupt Status: 1 This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 1 This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 1 Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. 0 - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 Change of SEF Defect Condition 1 Change of SEF Defect Condition Interrupt Status:				B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt
2 Change of LOF Defect Condition Interrupt Status RUR Change of Loss of Frame (LOF) Defect Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. • O - Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. • Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. 1 - Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. Note: The user can determine whether or not the Receive STM-1 SOH Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107). 1 Change of SEF Defect Condition RUR Change of SEF Defect Condition Interrupt Status:				
1 Change of SEF Defect Condition				
Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events. Interrupt Status Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. Interrupt in response to either of the following events. Whenever the Receive STM-1 SOH Processor block declares the LOF defect condition. Interrupt in response to either of the following events. Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition. Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. Note: The user can determine whether or not the Receive STM-1 SOH Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107). 1 Change of SEF Defect Condition Interrupt Status:	2		RUR	Change of Loss of Frame (LOF) Defect Condition Interrupt Status:
1 Change of SEF Defect Condition 1 Change of SEF Defect Condition			duct (C	LOF Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this
1 Change of SEF RUR Change of SEF Defect Condition Interrupt Status: 1 Change of SEF RUR Change of SEF Defect Condition Interrupt Status:		or or	shee	
1 Change of SEF RUR Change of SEF Defect Condition Interrupt Status: 1 Change of SEF RUR Change of SEF Defect Condition Interrupt Status:		theat	o Tuio	 Whenever the Receive STM-1 SOH Processor block clears the LOF defect condition.
1 Change of SEF Defect Condition 1 Change of SEF Defect Condition			ant	e marcade marche enange er zer bereet eenander maerreprinde reer
Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107). 1 Change of SEF Defect Condition RUR Change of SEF Defect Condition Interrupt Status:				
Defect Condition				Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address
Detect Condition	1		RUR	Change of SEF Defect Condition Interrupt Status:
Interrupt Status SEF" Defect Condition Interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.				register. The Receive STM-1 SOH Processor block will generate this
Whenever the Receive STM-1 SOH Processor block declares the SEF				

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			defect condition.
			• Whenever the Receive STM-1 SOH Processor block clears the SEF defect condition.
			0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-1 SOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107).
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-1 SOH Processor block declares the LOS defect condition.
			• Whenever the Receive STM-1 SOH Processor block clears the LOS defect condition.
			0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-1 SOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1107).

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Table 69: Receive STM-1 Section Interrupt Enable Register – Byte 2 (Address Location= 0x110D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of MS- AIS	Change of MS- RDI				
		Defect Condition Interrupt Enable	Defect Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	.5 .0
1	Change of MS-	R/W	Change of MS-AIS (Line AIS) Defect Condition Interrupt Enable:
	AIS Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of MS-AIS Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			Whenever the Receive STM-1 SOH Processor block declares the "MS- AIS" defect condition.
			Whenever the Receive STM-1 SOH Processor block clears the "MS-AIS" defect condition.
			0 – Disables the "Change of MS-AIS Defect Condition" Interrupt.
			1 – Enables the "Change of MS-AIS Defect Condition" Interrupt.
			Note: The user can determine if the Receive STM-1 SOH Processor block is currently declaring the MS-AIS defect condition by reading out the state of Bit 0 (MS-AIS Defect Declared) within the "Receive STM-1 Section Status Register – Byte 1" (Address Location= 0x1106).
0	Change of MS- RDI	R/W	Change of MS-RDI (Line Remote Defect Indicator) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable	she	This READ/WRITE bit-field permits the user to either enable or disable the "Change of MS-RDI Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
	0,0	n	• Whenever the Receive STM-1 SOH Processor block declares the "MS-RDI" defect condition.
			• Whenever the Receive STM-1 SOH Processor block clears the "MS-RDI" defect condition.
			0 – Disables the "Change of MS-RDI Defect Condition" Interrupt.
			1 – Enables the "Change of MS-RDI Defect Condition" Interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 70: Receive STM-1 Section Interrupt Enable Register – Byte 1 (Address Location= 0x110E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Change in Section Trace Message Unstable State Interrupt Enable	New Section Trace Message Interrupt Enable	Change in MS-TIM Defect Condition Interrupt Enable	Receive SOH CAP DONE Interrupt Enable	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	NEW K1K2 Byte Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	 New S1 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STM-1 SOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STM-1 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in	R/W	Change in S1 Byte Unstable Defect Condition Interrupt Enable:
	S1 Unstable Defect Condition Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Receive STM-1 SOH Processor block will generate an interrupt in response to either of the following conditions.
	Enable		Whenever the Receive STM-1 SOH Processor block declares the "S1 Byte Unstable defect condition.
			• Whenever the Receive STM-1 SOH Processor block clears the "S1 Byte Unstable" defect condition.
			0 – Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	17 Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5	Change in	R/W	Change in Section Trace Message Unstable defect condition Interrupt Enable:
	Section Trace Message Unstable Defect		This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Message Unstable Defect Condition" Interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate an interrupt in response to either of the following conditions.
	Condition Interrupt Enable		Whenever the Receive STM-1 SOH Processor block declares the "Section Trace Message Unstable" defect condition.
	Enable		Whenever the Receive STM-1 SOH Processor block clears the "Section Trace Message Unstable" defect condition.
			0 – Disables the "Change in Section Trace Message Unstable Defect Condition" Interrupt.
			1 – Enables the "Change in Section Trace Message Unstable Defect Condition" Interrupt.
4	New	R/W	New Section Trace Message Interrupt Enable:
	Section Trace		This READ/WRITE bit-field permits the user to enable or disable the "New Section



	Message Interrupt Enable		Trace Message" interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message. The Receive STM-1 SOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times via the J0 byte within the incoming STM-1 data-stream.
			0 – Disables the "New Section Trace Message" Interrupt.
			1 – Enables the "New Section Trace Message" Interrupt.
3	Change in MS-TIM	R/W	Change in "MS-TIM Defect Condition" interrupt enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in MS-TIM Defect condition" interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate an interrupt in response to either of the following events.
			<ul> <li>Whenever the Receive STM-1 SOH Processor block declares the "MS-TIM" defect condition.</li> </ul>
			Whenever the Receive STM-1 SOH Processor block clears the "MS-TIM" defect condition.      Note: The user can determine whether or not the Receive STM-1 SOH Processor
			block is currently declaring the "Section Trace Message Mismatch" defect condition by reading the state of Bit 2 (MS-TIM Defect Declared) within the "Receive STM-1 Section Status Register – Byte 1 (Address Location= 0x1106).
2	Receive	R/W	Receive SOH Capture DONE Interrupt Enable:
	SOH CAP DONE Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the "Receive SOH Data Capture Interrupt, within the Receive STM-1 SOH Processor Block.
	Enable		If this interrupt is enabled, then the Receive STM-1 SOH Processor block will generate an interrupt anytime it has captured the last SOH byte into the Capture Buffer.
			<b>Note:</b> Once the SOH (of a given STM-1 frame) has been captured and loaded into the Receive SOH Capture" buffer, it will remain there for one SONET frame period.
			0 - Disables the "Receive SOH Capture" Interrupt.
		S S	1 - Enables the "Receive SOH Capture" Interrupt.
1	Change in	R/W	Change of K1, K2 Byte Unstable Defect Condition Interrupt Enable:
	K1, K2 Byte Unstable Defect Condition	932	This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate an Interrupt in response to either of the following events.
	Interrupt Enable		<ul> <li>Whenever the Receive STM-1 SOH Processor block declares the "K1, K2 Byte Unstable defect" condition.</li> </ul>
			• Whenever the Receive STM-1 SOH Processor block clears the "K1, K2 Byte Unstable defect" condition.
			0 – Disables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
			1 – Enables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
0	New K1K2	R/W	New K1, K2 Byte Value Interrupt Enable:
	Byte Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STM-1 SOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STM-1 SOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STM-1 frames.



0 – Disables the "New K1, K2 Byte Value" Interrupt.	
1 – Enables the "New K1, K2 Byte Value" Interrupt.	

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# Table 71: Receive STM-1 Section Interrupt Status Register – Byte 0 (Address Location= 0x110F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of MS-REI Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Change of SF	R/W	Change of Signal Failure (SF) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events.
			• Whenever the Receive STN-1 SOH Processor block declares the SF defect condition.
			Whenever the Receive STM-1 SOH Processor block clears the SF defect condition.
			0 – Disables the "Change of SF Defect Condition Interrupt".
			1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD	R/W	Change of Signal Degrade (SD) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events.
		AUCE	• Whenever the Receive STM-1 SOH Processor block declares the SD defect condition.
	of	ochec	Whenever the Receive STM-1 SOH Processor block clears the SD defect condition.
		2 0	O – Disables the "Change of SD Defect Condition Interrupt".
	1. No		1 – Enables the "Change of SD Defect Condition Interrupt".
5	Detection of MS- REI Event	R/W	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of MS-REI Event interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STM-1 SOH Processor block detects an "MS-REI" event, within the incoming STM-1 data- stream.
			0 – Disables the "Detection of MS-REI Event" Interrupt.
			1 – Enables the "Detection of MS-REI Event" Interrupt.
4	Detection of B2	R/W	Detection of B2 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-



0 – Disables the "Detection of B2 Byte Error Interrupt".         1 – Enables the "Detection of B2 Byte Error Interrupt".         3       Detection of B1 Byte Error Interrupt Enable:         Byte Error Interrupt Enable       R/W         Detection of B1 Byte Error Interrupt Enable       This READ/WRITE bit-field permits the user to either enable	
3 Detection of B1 R/W Detection of B1 Byte Error Interrupt Enable: Byte Error Interrupt Enable This READ/WRITE bit-field permits the user to either enable	
Byte Error Interrupt Enable This READ/WRITE bit-field permits the user to either enable	
Interrupt Enable   This READ/WRITE bit-field permits the user to either enable	
"Detection of B1 Byte Error" Interrupt. If the user enables this the XRT94L33 will generate an interrupt anytime the Receiv Processor block detects a B1 byte error within the incomin stream.	s interrupt, then ve STM-1 SOH
0 – Disables the "Detection of B1 Byte Error Interrupt".	
1 – Enables the "Detection of B1 Byte Error Interrupt".	
2 Change of LOF R/W Change of Loss of Frame (LOF) Defect Condition Interrupt	t Enable:
Defect Condition Interrupt Enable "Change of LOF Defect Condition" interrupt. If the use interrupt, then the XRT94L33 will generate an interrupt in res of the following conditions.	er enables this
Whenever the Receive STM1 SOH Processor block decl defect condition.	ares the "LOF"
Whenever the Receive STM 1 SOH Processor clears the condition.	e "LOF" defect
0 – Disables the "Change of LOF Defect Condition Interrupt.	
1 – Enables the "Change of LOF Defect Condition" Interrupt.	
1         Change of SEF         Defect Condition           1         Defect Condition         R/W         Change of SEF Defect Condition Interrupt Enable:           This READ/WRITE bit field permits the user to either enable         "Change of SEF Defect Condition" Interrupt. If the use interrupt, then the XRT94L33 will generate an interrupt in res of the following conditions.	er enables this
Whenever the Receive STM-1 SOH Processor block decl     defect condition.	lares the "SEF"
• Whenever the Receive STM-1 SOH Processor block	ck clears the
0 - Disables the "Change of SEF Defect Condition Interrupt".	
Enables the "Change of SEF Defect Condition Interrupt".	
0 Change of LOS R/W Change of Loss of Signal (LOS) Defect Condition Interrupt	t Enable:
Defect Condition Interrupt Enable This READ/WRITE bit-field permits the user to either enable "Change of LOF Defect Condition" interrupt. If the use interrupt, then the XRT94L33 will generate an interrupt in res of the following conditions.	e or disable the er enables this
Whenever the Receive STM-1 SOH Processor block decl defect condition.	lares the "LOF"
Whenever the Receive STM-1 SOH Processor block cle defect condition.	ears the "LOF"
0 – Disables the "Change of LOF Defect Condition Interrupt.	



### Table 72: Receive STM-1 Section – B1 Byte Error Count Register – Byte 3 (Address Location= 0x1110)

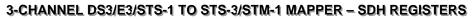
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	B1 Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

Bit Number	NAME	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_ Count[31:24]	RUR	<ul> <li>B1 Byte Error Count – MSB:</li> <li>This RESET-upon-READ register, along with "Receive STM-1 Section – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B1 byte error within the STM-1 data-stream.</li> <li>Note:</li> <li>1.If the Receive STM-1 SOH Processor block is configured to count B1 Byte Errors on a "per-bit" basis then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.</li> <li>2.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter by the that are in error.</li> </ul>

## Table 73: Receive STM-1 Section – B1 Byte Error Count Register – Byte 2 (Address Location= 0x1111)

	r				1	r		
Віт 7	Віт 6	Віт 5	Brt 4	Віт 3	Віт 2	Віт 1	Віт 0	
B1_Byte_Error_Count[23:16]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	00	8 8	0	0	0	0	
	av et ot							

BIT NUMBER		TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [23:16]	RUR	<ul> <li>B1 Byte Error Count (Bits 23 through 16): This RESET-upon-READ register, along with "Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B1 byte error.</li> <li>Note:</li> <li>1.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.</li> <li>2.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains an erred B1 byte.</li> </ul>





## Table 74: Receive STM-1 Section – B1 Byte Error Count Register – Byte 1 (Address Location= 0x1112)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B1_Byte_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_	RUR	B1 Byte Error Count – (Bits 15 through 8)
	Count [15:8]		<ul> <li>This RESET-upon-READ register, along with "Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B1 byte error.</li> <li><i>Note:</i></li> <li>1.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.</li> <li>2.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains an erred B1 byte.</li> </ul>
			*5 0° 83'

## Table 75: Receive STM-1 Section – B1 Byte Error Count Register – Byte 0 (Address Location= 0x1113)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0	
B1_Byte _Error Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	8	0	0	0	0	
	AUCT AT DO							

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [7:0]	RUR	<b>B1 Byte Error Count – LSB:</b> This RESET-upon-READ register, along with "Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.
			2.If the Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains an erred B1 byte.



#### Table 76: Receive STM-1 Section - B2 Byte Error Count Register - Byte 3 (Address Location= 0x1114)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
B2_Byte_Error_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_	RUR	B2 Byte Error Count – MSB:
	Count [31:24]		This RESET-upon-READ register, along with "Receive STM-1 Section – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream.
			Note:
			1.If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.
			2.If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains at least one erred B2 byte.
	thepr	duct le	time that it receives an STM-1 frame that contains at least one erred B2 byte.



	Table 77. Receive STM-T Section – BZ Byte Error Count Register – Byte Z Address Location= 0x1115)								
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
			B2_Byte_Erro	or_Count[23:16]					
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

### Table 77: Receive STM-1 Section – B2 Byte Error Count Register – Byte 2 Address Location= 0x1115)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte	RUR	B2 Byte Error Count (Bits 23 through 16):
	Error_Count [23:16]		This RESET-upon-READ register, along with "Receive STM-1 Section – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B2 byte error.
			Note:
			1.If the Receive STM-1 SOH Processor block is configured to count B2 Byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes of each incoming STM-1 frame) that are in error.
			2.If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains at least one erred B2 byte.
	the	Produ datand	byte.



#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

#### Table 78: Receive STM-1 Section - B2 Byte Error Count Register - Byte 1 (Address Location= 0x1116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B2_Byte_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte	RUR	B2 Byte Error Count – (Bits 15 through 8)
	Error_Count [15:8]		This RESET-upon-READ register, along with "Receive STM-1 Section – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream. <b>Note:</b>
			1. If the Receive STM-1 SOH Processor block is configured to count B2 byte
			errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.
			2. If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains at least one erred B2 byte.
	thedat	andma	time that it receives an STM-1 frame that contains at least one erred B2 byte.

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	Table 19. Receive STM-1 Section - Dz Dyte Lifor Count Register - Dyte o (Address Location= 0x1117)										
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	B2_Byte_Error_Count[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

### Table 79: Receive STM-1 Section – B2 Byte Error Count Register – Byte 0 (Address Location= 0x1117)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte	RUR	B2 Byte Error Count – LSB:
	Error_Count[7:0]		This RESET-upon-READ register, along with "Receive STM-1 Section – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime, the Receive STM-1 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.
			2. If the Receive STM-1 SOH Processor block is configured to count B2 Byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that is receives an STM-1 frame that contains at least one erred B2 byte.
	the	and man	counter each time that is receives an STM-1 frame that contains at least one erred B2 byte.



#### Table 80: Receive STM-1 Section – MS-REI Event Count Register – Byte 3 (Address Location= 0x1118)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	MS-REI_Event_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	MS-REI_Event_Count [31:24]	RUR	<ul> <li>MS-REI Event Count – MSB:</li> <li>This RESET-upon-READ register, along with "Receive STM-1 Section – MS-REI Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-1 data-stream.</li> <li>Note: <ol> <li>If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame.</li> </ol> </li> <li>If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains a "non-zero" M1 byte value.</li> </ul>

ine Rec MS-RELever, bit counter ea "non-zero" MA hoto order the base from the order the order the order the base from the order the order the order the order the base from the order the order



Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 1	Віт 0				
	MS-REI_Event_Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

#### Table 81: Receive STM-1 Section – MS-REI Event Count Register – Byte 2 (Address Location= 0x1119)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	MS-REI_Event_Count	RUR	MS-REI Event Count (Bits 23 through 16):
	[23:16]		This RESET-upon-READ register, along with "Receive STM-1 Section – MS-REI Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-1 data-stream.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.
			2. If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame" baiss, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains a non-zero M1 byte value.
	The produces	teet n	this 32 bit counter each time that it receives an STM-1 frame that contains a non-zero M1 byte value.



## Table 82: Receive STM-1 Section – MS-REI Event Count Register – Byte 1 (Address Location= 0x111A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	MS-REI_Event_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	MS-	RUR	MS-REI Event Count – (Bits 15 through 8)
	REI_Event_Count[15:8]		This RESET-upon-READ register, along with "Receive STM-1 Section – MS-REI Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a Line –Remote Error Indicator event within the incoming STM-1 data-stream.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.
			2. If the Receive STM-1 SOH Processor block is configured to count MS-RELevents on a "per-bit" basis, then it will increment this 32 bit counter each that it receives an STM-1 frame that contains a non-zero M1 byte.
	The product	or proc	bondered s



					Dyic V (A		011- 0X111D)			
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	MS-REI_Event_Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

#### Table 83: Receive STM-1 Section – MS-REI Event Count Register – Byte 0 (Address Location= 0x111B)

BIT NUMBER	Nаме	ΤΥΡΕ	DESCRIPTION
7 - 0	MS-	RUR	MS-REI Event Count – LSB:
	REI_Event_Count[7:0]		This RESET-upon-READ register, along with "Receive STM-1 Section – MS-REI Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-1 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-1 data-stream.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.
			2. If the Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame" baiss, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains a "non-zero" M1 byte value.
	The prod	uct of	bit counter each time that it receives an STM-1 frame that contains a "non-zero" M1 byte value.



## Table 84: Receive STM-1 Section – Received K1 Byte Value Register (Address Location= 0x111F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0						
	Filtered_K1_Byte_Value[7:0]												
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O						
0	0	0	0	0	0	0	0						

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION					
7 – 0	Filtered_K1_Byte Value[7:0]	R/O	Filtered/Accepted K1 Byte Value: These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value that the Receive STM-1 SOH Processor block has received. The Receive STM-1 SOH Processor block will "accept" a given K1 byte, once it has received this particular K1 byte value within 3 consecutive STM-1 frames. This register should be polled by Software in order to determine various APS codes.					
	oneanth							

# Table 85: Receive STM-1 Section – Receive K2 Byte Value Register (Address Location= 0x1123)

Віт 7	Віт 6	Віт 5	Віт 4	BIT3	Віт 2	Віт 1	Віт 0					
	Filtered_K2_Byte_Value[7:0]											
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O					
0	0	0		Q	0	0	0					
	09,00,00											

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 – 0	Filtered_K2_Byte_Value[7:0]	R/O	Filtered/Accepted K2 Byte Value:
	the product the	not	These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 Byte value that the Receive STM-1 SOH Processor block has received. The Receive STM-1 SOH Processor block will "accept" a given K2 byte, once it has received this particular K2 byte value within 3 consecutive STM-1 frames. This register should be polled by Software in order to determine various APS codes.
	<u>, 43, 4</u> ,		

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



## Table 86: Receive STM-1 Section – Received S1 Byte Value Register (Address Location= 0x1127)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0						
	Filtered_S1_Byte_Value[7:0]												
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O						
0	0	0	0	0	0	0	0						

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION					
7 – 0	Filtered_S1_Byte_Value[7:0]	R/O	Filtered/Accepted S1 Byte Value:					
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Receive STM-1 SOH Processor block has received. The Receive STM-1 SOH Processor block will "accept" a given S1 byte, once it has received this particular S1 byte value within 8 consecutive STM-1 frames.					

# Table 87: Receive STM-1 Section – In-Sync Threshold Value (Address Location=0x112B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		FRPATOUT[1:0]		FRPAT	FIN[1:0]	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0
				2.0	5		

BIT NUMBER	ΝΑΜΕ	Түре	č	DESCRIPTION					
7 – 5	Unused	R/O	911	000					
4 – 3	FRPATOUT	R/W	Framing Pattern -	EF Declaration Criteria:					
	[1:0]		Declaration criteria for	RTE bit-fields permit the user to define the SEF Defect the Receive STM-1 SOH Processor block. The relationship of these bit-fields and the corresponding SEF Defect are presented below.					
			FRPATOUT[1:0]	FRPATOUT[1:0] SEF Defect Declaration Criteria					
		nepr	510 00 3 11 2 01	The Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.					
		N. 90		<ul> <li>If the last (of the 3) A1 bytes, in the STM-1 data stream is erred, or</li> </ul>					
			C ^r	<ul> <li>If the first (of the 3) A2 bytes, in the STM-1 data stream, is erred.</li> </ul>					
				Hence, for this selection, a total of 16 bits are evaluated for SEF defect declaration.					
			10	The Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.					
				<ul> <li>If the last two (of the 3) A1 bytes, in the STM-1 data stream, are erred, or</li> </ul>					
				• If the first two (of the 3) A2 bytes, in the STM-1 data stream, are erred.					
				Hence, for this selection, a total of 32 bits are evaluated for SEF defect declaration.					



	1		11
		11	The Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.
			• If the last three (of the 3) A1 bytes, in the STM-1 data stream, are erred, or
			• If the first three (of the 3) A2 bytes, in the STM-1 data stream, are erred.
			Hence, for this selection, a total of 48 bits are evaluated for SEF defect declaration.
2 - 1	FRPATIN R/	W Framing Pattern – S	SEF Defect Clearance Criteria:
	[1:0]	Clearance" criteria fo	/RITE bit-fields permit the user to define the "SEF Defect or the Receive STM-1 SOH Processor block. The relationship these bit-fields and the corresponding SEF Defect Clearance d below.
		FRPATIN[1:0]	SEF Defect Clearance Criteria
		00 01	The Receive STM-1 SOH Processor block will clear the SEF detect condition if both of the following conditions are true for two consecutive SONET frame periods.
			If the last (of the 3) A1 bytes, in the STM-1 data stream is un-erred, and
			• , If the first (of the 3) A2 bytes, in the STM-1 data stream, is un-erred.
		hucise	Hence, for this selection, a total of 16 bits/frame are evaluated for SEF defect clearance.
		duct are not be orde	SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
		loteneor	• If the last two (of the 3) A1 bytes, in the STM-1 data stream, are un-erred, and
		and the state	• If the first two (of the 3) A2 bytes, in the STM-1 data stream, are un-erred.
	P	S al	Hence, for this selection, a total of 32 bits/frame are evaluated for SEF defect clearance.
	1 Bat	and may 11	The Receive STM-1 SOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
			If the last three (of the 3) A1 bytes, in the STM-1     data-stream, are un-erred, and
			• If the first three (of the 3) A2 bytes, in the STM-1 data stream, are un-erred.
			Hence, for this selection, a total of 48 bits/frame are evaluated for SEF defect declaration.
0	Unused R/	0	
· · · · · · · · · · · · · · · · · · ·			

## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 88: Receive STM-1 Section – LOS Threshold Value - MSB (Address Location= 0x112E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0						
	LOS_THRESHOLD[15:8]												
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W						
1	1	1	1	1	1	1	1						

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-1 Section – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STM-1 SOH Processor block must detect before it can declare the LOS defect condition.

# Table 89: Receive STM-1 Section – LOS Threshold Value - LSB (Address Location= 0x112F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRE	SHOLD[7:0]	<u>o</u> .		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1		1	1	1
				5 00 8			

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
			These READWRITE bits, along the contents of the "Receive STM-1
		10	Section – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STM-1 SOH Processor
			block must detect before it can declare the LOS defect condition.

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# Table 90: Receive STM-1 Section – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1131)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_SET_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_	R/W	SF_SET_MONITOR_INTERVAL – MSB:
	WINDOW [23:16]		These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.
			When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block will declare the SF defect condition. NOTES:
		oroc	The value that the user writes into these three (3) "SF Set Monitor Window" registers specifies the duration of the "SF Defect Declaration Monitoring Period", in terms of ms.
	C.	ot n	<ul> <li>This particular register byte contains the "MSB" (most significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring Period".</li> </ul>
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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 91: Receive STM-1 Section – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0x1132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

7 - 0       SF_SET_MONITOR_WINDOW [15:8]       R/W       SF_SET_MONITOR_INTERVAL (Bits 15 through 8): These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration         When the Receive STM-1 SOH Processor block is checking the incoming STM-Usignal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period" the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block will declare the SF defect condition.         NOTE: One value that the user writes into these three (3) "SF Set Monitor Window" Registers specifies the duration of the "SF Defect Declaration" Monitoring Period.	Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
	7 - 0		R/W	These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration When the Receive STM 1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user specified "SF Defect Declaration Monitoring Period". (In during this "SF Defect Declaration Monitoring Period" the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the SF defect condition.

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Table 92: Receive STM-1 Section – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1133)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_SET_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	SF_SET_MONITOR_INTERVAL - LSB:
			These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.
	N	tsine	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accomulate B2 byte errors throughout the user- specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block within the "Receive STM-1 SOH Processor block will declare the SF defect condition.
	, 0 ⁰	(1) e	NOTES:
	The product or product	ordei	<ol> <li>The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.</li> </ol>
	e producet not		2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".
	The and h		



# Table 93: Receive STM-1 Section – Receive SF SET Threshold – Byte 1 (Address Location= 0x1136)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_TH				ESHOLD[15:8]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	SF_SET_THRESHOLD – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to declare the SF (Signal Failure) Defect condition.
		jor jor	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STM-1 Section SF SET Threshold – Byte 0" register, then the Receive STM-1 SOH Processor block will declare the SF defect condition. <b>NOTE:</b> This particular register functions as the MSB (Most Significant byte) of the "16-bit" expression for the "SF Defect Declaration B2 Byte Error" Threshold.
	The product the pr	aren	



#### Table 94: Receive STM-1 Section – Receive SF SET Threshold – Byte 0 Address Location= 0x1137)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:	R/W	SF_SET_THRESHOLD – LSB:
	0]		These READ/WRITE bits, along the contents of the "Receive STM- 1 Section – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to declare the SF (Signal Failure) defect condition.
			When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STM-1 Section SF SET Threshold – Byte 1" register, then the Receive STM-1 SOH Processor block will declare the SF defect condition. <b>NOTE:</b> This particular register functions as the LSB (Least Significant byte) of the "16-bit" expression for the "SF Defect Declaration B2 Byte Error" Threshold.
	The product the pr	are to	

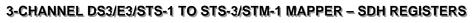




Table 95: Receive STM-1 Section – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0x113A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [15:8]	R/W	<ul> <li>SF_CLEAR_THRESHOLD – MSB:</li> <li>These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to clear the SF (Signal Failure) defect condition.</li> <li>When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-1 Section SF CLEAR Threshold – Byte 0" register, then the Receive STM-1 SOH Processor block will clear the SF defect condition.</li> <li>NOTE: This particular register functions as the MSB (Most Significant Byte) of the "16-bit" expression for the "SF Defect Clearance B2 Byte Error" Threshold.</li> </ul>
	The product in the product is the pr	or Pine	



Table 96: Receive STM-1 Section – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x113B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [7:0]	R/W	SF_CLEAR_THRESHOLD – LSB: These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STM-1 SOH Processor block to clear the SF (Signal Failure) defect condition. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 Signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that
	The product of and the	en lo	programmed into this and the "Receive STM-1 Section SF CLEAR Threshold – Byte 1" register, then the Receive STM-1 SOH Processor block will clear the SF defect condition. NOTE: This particular register functions as the LSB (Least Significant Byte) of the "16-bit" expression for the "SF Defect Clearance B2 Byte Error" Threshold.
	The prospective and may		

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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 97: Receive STM-1	Section - Receive SD	) Set Monitor Interval – I	Byte 2 (Address Location=
0x113D)			

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SD_SET_MONITOR_INTERVAL – MSB:
	[23:16]		These READ/WRITE bits, along the contents of the "Receive STM-1 Section SD SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration.
		ducts	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal, in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user- specified "SD Defect Declaration monitoring period". If, ouring this "SD Defect Declaration Monitoring period", the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block will declare the SD defect condition. NOTES:
	duct of pi	The product are be of the product of the prod	<ol> <li>The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration Monitoring Period", in terms of ms.</li> </ol>
	The presheaver		<ol> <li>This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Declaration Monitoring Period".</li> </ol>



#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Table 98: Receive STM-1 Section – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x113E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	SD_SET_MONITOR_INTERVAL – Bits 15 through 8:
7-0	SD_SET_MONITOR_WINDOW[15:8]	RINV	SD_SET_MONITOR_INTERVAL – Bits 15 through 8: These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user- specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 SOH Processor block will declare the SD defect condition.
		0	<b>NOTE:</b> The value that the user writes into these three
	lot no	ordere	<ul> <li>(3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.</li> </ul>

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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 99: Receive STM-1 Section – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0x113F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[	R/W	SD_SET_MONITOR_INTERVAL – LSB:
	7:0]		These READ/WRITE bits, along the contents of the "Receive STM-1 Section - SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration.
		duct	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period", the Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-1 Section SD SET Threshold" register, then the Receive STM-1 SOH Processor block will declare the SD defect condition.
		(°, 0)	NOTES:
	ict ar	no o	<ol> <li>The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.</li> </ol>
	The product lor pr	o ^t	<ol> <li>This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring period".</li> </ol>
	Theatender	1	



## Table 100: Receive STM-1 Section – Receive SD SET Threshold – Byte 1 (Address Location= 0x1142)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	SD_SET_THRESHOLD – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to declare the SD (Signal Degrade) defect condition. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 Signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoring Period" (If the number of accumulate B2 byte errors exceeds that value, which is programmed into this and the "Receive STM-1 SOH Processor block will declare the SD defect condition.

# Table 101: Receive STM-1 Section – Receive SD SET Threshold – Byte 0 (Address Location= 0x1143)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1 .		1	1	1	1	
		du	et ot					

BIT NUMBER	NAME	Түре	DESCRIPTION
ВІТ <b>NUMBER</b> 7 - 0	SD_SET_THRESHOLD[7:0]	R/W	<ul> <li>SD_SET_THRESHOLD – LSB:</li> <li>These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to declare the SD (Signal Degrade) defect condition.</li> <li>When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STM-1 Section SD SET Threshold – Byte 1" register, then the Receive STM-1</li> </ul>
			(Signal Degrade) defect condition. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STM-1 Section

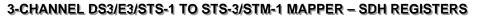




Table 102: Receive STM-1 Section – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1146)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		S	D_CLEAR_TH	RESHOLD[15:8	3]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	SD_CLEAR_THRESHOLD – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-1 Section SD CLEAR Threshold – Byte 0" register, then the Receive STM-1 SOH Processor block will clear the SD defect condition.
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Table 103: Receive STM-1	Section – Receive SE	OCLEAR Threshold -	Byte 1 (Address Location=
0x1147)			

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		:	SD_CLEAR_TH	IRESHOLD[7:0]	]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

ΝΑΜΕ	Түре	DESCRIPTION
SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD – LSB:
		These READ/WRITE bits, along the contents of the "Receive STM-1 Section – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-1 SOH Processor block to clear the SD (Signal Degrade) defect condition.
		When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors, throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-1 Section SD CLEAR Threshold – Byte 1" register, then the Receive STM-1 SOH Processor block will clear the SD defect condition.
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	SD_CLEAR_THRESHOLD[7:0]	

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 104: Receive STM-1 Section – Force SEF Condition Register (Address Location= 0x114B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	SEF FORCE						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	SEF Force:
			This READ/WRITE bit-field permits the user to force the Receive STM-1 SOH Processor block to declare the SEF detect condition. The Receive STM-1 SOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Receive STM-1 SOH Processor block to declare the SEF detect condition. The Receive STM-1 SOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STM-1 frames with the correct A1 and A2 bytes).

the correct A1 and A2 bytes.

# Table 105: Receive STM-1 Section – Receive Section Trace Message Buffer Control Register (Address Location= 0x114F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Lengt	Trace Message h[1:0]
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	1	1	5 0
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 5	Unused	R/O	in ctu
4	Receive Section Trace Message Buffer Read Select	R/W	<ul> <li>Receive Section Trace Message Buffer Read Selection:</li> <li>This READ/WRITE bit-field permits the user to specify which of the following Receive Section Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Section Trace Message Buffer address space.</li> <li>a. The "Actual" Receive Section Trace Message Buffer. The "Actual" Receive Section Trace Message Buffer contains the contents of the most recently received (and accepted) Section Trace Message via the incoming STM-1 data-stream.</li> <li>b. The "Expected" Receive Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer is usually specified by the user.</li> <li>0 — Executing a READ operation to the Receive Section Trace Message Buffer.</li> <li>1 — Executing a READ operation to the Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive</li> </ul>
	the de	suga	Section Trace Message Buffer". <b>Note:</b> In the case of the Receive STM-1 SOH Processor block, the "Receive Section Trace Message Buffer" is located at Address location 0x1300 through 0x133F.
3	Receive Section Trace Message	R/W	Receive Section Trace Message Accept Threshold:
	Accept Threshold	Accept	This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STM-1 SOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given "Section Trace Message" has been accepted then it can be read out of the "Actual Receive Section Trace Message" Buffer.
			0 – Configures the Receive STM-1 SOH Processor block to accept the incoming Section Trace Message after it has received it the third time in succession.
			1 – Configures the Receive STM-1 SOH Processor block to accept the incoming Section Trace Message after it has received it the fifth time in succession.



### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

		1			
2	Section Trace	R/W	Section Trace Mes	sage Alignment Type:	
	Message Alignment Type		SOH Processor blo	bit-field permits a user to specify how the Receive STM ck will locate the boundary of the incoming Section Tra incoming STM-1 data-stream, as indicated below.	
				e Receive STM-1 SOH Processor block to expect t age boundary to be denoted by a "Line Feed" character.	
			Section Trace Mest the MSB (most sign Trace Message). In	e Receive STM-1 SOH Processor block to expect t sage boundary to be denoted by the presence of a "1" ificant bit) of the very first byte (within the incoming Secti n this case, all of the remaining bytes (within the incomi sage) will each have a "0" within their MSBs.	in on
1 - 0	Receive Section	R/W	Receive Section T	race Message Length[1:0]:	
	Trace Message Length[1:0]		Section Trace Mes accept and load into relationship betwee	E bit-fields permit the user to specify the length of t sage that the Receive STM1 SOH Processor block w to the "Actual" Receive Section Trace Message Buffer. T en the content of these bit-fields and the correspondi ace Message Length is presented below.	will he
			Receive Section Trace Message Length[1:0]	Resulting Section Trace Message Length (in terms of bytes)	
			00	1 Byte	
			01	16 Bytes	
			10/11	64 Bytes	
	4th	o a a a a a a a a a a a a a a a a a a a		berec	



Table 106: Receive STM-1 Section – Receive SD Burst Error Tolerance – Byte 1 (Address Location	n=
_0x1152)	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

7-0	SD_BURST_TOLERANCE [15:8]	R/W	<ul> <li>SD_BURST_TOLERANCE – MSB:</li> <li>These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.</li> <li>Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-1 SOH</li> </ul>
	the product of	produ produ not be	Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
	The product of	he be	orde

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 107: Receive STM-1 Section – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1153)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [7:0]	R/W	<b>SD_BURST_TOLERANCE – LSB:</b> These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.
			<b>Note:</b> The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
	The bata and the	los pro-	po ordereo to ordereo



Table 108: Receive STM-1 Section – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1156)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	SF_BURST_TOLERANCE – MSB:
			These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.
		ut's	Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM- 1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.
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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 109: Receive STM-1 Section – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	SF_BURST_TOLERANCE – LSB:
			<ul> <li>These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.</li> <li>Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM-1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.</li> </ul>
	The product the pr	are h	



Table 110: Receive STM-1	Section – Receive	<b>SD Clear Monito</b>	or Interval – Byte 2	(Address Location=
0x1159)			-	-

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_CLEAR_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_	R/W	SD_CLEAR_MONITOR_INTERVAL – MSB:
	WINDOW[23:16]		These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
		oduct	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD detect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 SoH Processor block will clear the SD defect condition. NOTES:
	t lor		<ol> <li>The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.</li> </ol>
	roupet of	ot	<ol> <li>This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.</li> </ol>
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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Table 111: Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x115A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:
			These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
		ct of	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user- specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period" the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 Section SD Clear Threshold" register, then the Receive STM-1
	00	oner	SOH Processor block will clear the SD defect condition.
	ict are to	e der	<b>NOTE:</b> The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.
	The product are pr		

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Table 112: Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0 (Address Location=	;
0x115B)	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB:
	7:0]	icts of the second seco	These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance Monitoring" period. If, during this "SD Defect Clearance Monitoring" period, the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 Section SD Clear





Table 113: Receive STM-1 Section - Receive SF Clear Monitor Interval - Byte 2 (Address Location=	:
0x115D)	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDO	R/W	SF_CLEAR_MONITOR_INTERVAL – MSB:
	W [23:16]		These READ/WRITE bits, along with the contents of the "Receive STM-1 Section SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance
		odu	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 Soction SF Clear Threshold" register, then the Receive STM-1 SOH Processor block will clear the SF defect condition.
	t lot		The value that the user writes into these three (3) "SF Clear Monitor Window Registers", specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.
	The product los	noto	<ol> <li>This particular register byte contains the "MSB" (most significant byte) value fo the three registers that specify the "SF Defect Clearance Monitoring" period.</li> </ol>
	The atand mo		



Table 114: Receive STM-1 Section - Receive SF Clear Monitor Interval - Byte 1 (Addr	ess Location=
0x115E)	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	SF_CLEAR_MONITOR_WINDOW[15:8]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

ΝΑΜΕ	Түре	DESCRIPTION
SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	<ul> <li>SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:</li> <li>These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance.</li> <li>When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the userspecified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 SOH Processor block will clear the SF defect condition.</li> <li>NOTES: The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.</li> </ul>
The producet not		
	SF_CLEAR_MONITOR_WINDOW [15:8]	SF_CLEAR_MONITOR_WINDOW R/W



Table 115: Receive STM-1 Section - Receive SF Clear Monitor Interval - Byte 0 (Address Location=	:
0x115F)	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	SF_CLEAR_MONITOR_WINDOW[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL – LSB:
	[7:0]		These READ/WRITE bits, along with the contents of the "Receive STM-1 Section – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance.
		ducts)	When the Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user- specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance Monitoring" period, the Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-1 Section SF Clear Threshold" register, then the Receive STM-1 SOH Processor block will clear the SF defect condition.
	A CONTRACTOR OF		NOTES:
	The product of pro	lo trà	<ol> <li>The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring" period, in terms of ms.</li> </ol>
	e producet not		<ol> <li>This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.</li> </ol>
	Theatendry	1	



#### Table 116: Receive STM-1 Section – Auto AIS Control Register (Address Location= 0x1163)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AU-AIS (Down- stream) Upon Section Trace Message Unstable	Transmit AU-AIS (Down- stream) Upon Section Trace Message Mismatch	Transmit AU-AIS (Down- stream) Upon SF	Transmit AU-AIS (Down- stream) Upon SD	Transmit AU-AIS (Down- stream) upon Loss of Optical Carrier AIS	Transmit AU-AIS (Down- stream) upon LOF	Transmit AU-AIS (Down- stream) upon LOS	Transmit AU-AIS (Down- stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
	nis ed						

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Transmit AU-AIS (Down-stream)	R/W	Transmit Path AIS upon Declaration of the Section Trace Message Unstable Defect Condition:
	upon Section Trace Message Unstable		This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU- AIS) Indicator via the 'downstream' traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Unstable defect condition within the "incoming" STM-1 data- stream
			0 Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition.
	8		Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition.
	Transmit AU-AIS(	may	<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
6	Transmit AU-AIS (Down-stream)	R/W	Transmit Path AIS (AU-AIS) upon Declaration of the Section Trace Message Mismatch Defect Condition:
	Upon Section Trace Message Mismatch		This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks), anytime it declares the Section Trace Message Mismatch defect condition within the "incoming" STM-1 data stream.
			0 – Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Mismatch" defect condition.
			1 – Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the



			"Section Trace Message Mismatch" defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
5	Transmit AU-AIS (Down-stream) upon	R/W	Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition:
	SF		This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks), anytime it declares the SF defect condition.
			0 – Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the SF defect condition.
			1 – Configures the Receive STM1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the SF defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
4	Transmit AU-AIS (Down-stream) upon	R/W	Transmit Path AIS upon declaration of the Signal Degrade (SD) defect condition:
	SD	(	This READ/WRITE bit-field permits the user to configure the Receive STM1 SOH Processor block to automatically transmit the Path AIS (AU- AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks), anytime it declares the SD defect condition.
		duct	0 Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the SD defect condition.
	theat	e she	1 Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the SD defect condition.
		311	<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
3	Transmit AU-AIS	R/W	Transmit Path AIS upon Loss of Optical Carrier condition:
	(Down-stream) upon Loss of Optical Carrier		This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks), anytime it detects the "Loss of Optical Carrier" defect condition.
			0 – Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Loss of Optical Carrier" defect condition.
			1 - Configures the Receive STM-1 SOH Processor block to



			automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the "Loss of Optical Carrier" defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
2	Transmit AU-AIS (Down-stream) upon LOF	R/W	Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect condition:
	LOF		This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor block), anytime it declares the LOF defect condition.
			0 – Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the LOF defect condition.
			1 – Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the LOF defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
1	Transmit AU-AIS	R/W	Transmit Path AIS upon Loss of Signal (LOS):
	(Down-stream) upon LOS	U ST	This READ/WRITE bit-field permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor block), anytime it declares the LOS defect condition.
	neprog	neet	O – Does not configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the LOS defect condition.
	theatan		1 – Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) it declares the LOS defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS Enable) to "1" to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator, in response to this defect condition.
0	Transmit AU-AIS	R/W	Automatic Transmission of AU-AIS Enable:
	(Down-stream) Enable		This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit the Path AIS (AU-AIS) indicator, via the down-stream traffic (e.g., towards each of the three Receive TUG-3/AU- 3 Mapper VC-3 POH Processor blocks), upon declaration of either the SF, SD, Section Trace Message Mismatch, Section Trace Message



Unstable, LOF, LOS or Loss of Optical Carrier defect conditions.
It also permits the user to configure the Receive STM-1 SOH Processor block to automatically transmit a Path AIS (AU-AIS) Indicator via the "downstream" traffic (e.g., towards each of the three Receive TUG-3/AU- 3 Mapper VC-3 POH Processor blocks) anytime (and for the duration that) it declares the MS-AIS defect condition within the "incoming " STM- 1 data-stream.
0 – Configures the Receive STM-1 SOH Processor block to NOT automatically transmit the AU-AIS indicator (via the "downstream" traffic) whenever the Receive STM-1 SOH Processor block declares the MS-AIS or any other of the "above-mentioned" defect conditions.
1 – Configures the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator (via the "downstream" traffic towards each of the three Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks) whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the MS-AIS, SD, SF, LOF, LOS, Section Trace Message Mismatch, Section Trace Message Unstable or Loss of Optical Carrier defect condition).
<b>Note:</b> The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STM-1 SOH Processor block to automatically transmit the AU-AIS indicator upon detection of a given alarm/defect condition.

Processor block to and upon detection of a giv



#### Table 117: Receive STM-1 Section – Serial Port Control Register (Address Location= 0x1167)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed			RxSOH_	CLOCK_SPE	ED[3:0]
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxSOH_CLOCK_SPEED[7:0]	R/W	RxSOHClk Output Clock Signal Speed:         These READ/WRITE bit-fields permit the user to specify the frequency of the "RxSOHClk output clock signal.         The formula that relates the contents of these register bits to the "RxSOHClk" frequency is presented below.         FREQ = 19.44 /[2 * (RxSOH_CLOCK_SPEED + 1)         Note:       For STS-3/STM-1 applications, the frequency of the RxSOHClk output signal must be in the range of 0.6075MHz to 9.72MHz

Note: For STS-RXSOHC 0:6075M

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



## Table 118: Receive STM-1 Section – Auto AIS (in Downstream STM-0s) Control Register (Address Location= 0x116B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	Transmit AU-AIS/AIS (via Downstream STM-0s/ DS3s) upon LOS	Transmit AU-AIS/AIS (via Downstream STM-0s/ DS3s) upon LOF	Transmit AU-AIS/AIS (via Downstream STM-0s/ DS3s) upon SD	Transmit AU-AIS/AIS (via Downstream STM-0s/ DS3s) upon SF	MS-AIS Output Enable	Transmit AU-AIS/AIS (via Downstream STM-0s/ DS3s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
					inis re	ò	

Dim	N	There	
BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Unused	R/O	neonito
5	Transmit AU-AIS/AIS (via Downstream STM- 0s/DS3s) upon LOS	R/W	Transmit AU-AIS (via Downstream STM-0s) upon declaration of the LOS (Loss of Signal) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the LOS Defect condition:
			The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STM-0 or DS3 signals, on the "low-speed" side of the chip, as described below.
			For those channels that are configured to operate in the STM-0 Mode:
		duct	This READ/WRITE bit-field permits the user to configure all of the active Transmit STM-0 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition.
	thept	e no	0 Does not configure all "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS Indicator via the downstream" STM-0 signals, anytime the Receive STM-1 SOH Processor block declares the LOS defect condition.
	. 90	ano	1 – Configures all "activated" Transmit STM-0POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AU-AIS Down-stream – Upon LOS), within the Receive STM-1 Section – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STM-0 POH Processor blocks to IMMEDIATELY begin to transmit the AU-AIS condition whenever the Receive STM-1 SOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AU-AIS indicator downstream within 125us of the NE declaring the LOS defect.
			2. In the case of Bit 1 (Transmit AU-AIS Downstream – Upon LOS), several SONET frame periods are required (after the Receive STM-1



SOH Processor block has declared the LOS defect), before the Transmit STM-0 POH Processor blocks will begin the process of transmitting the AU-AIS indicators. 3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS via Downstream STM-0s Enable) within this register, in order enable this feature. For those channels that are configured to operate in the DS3 Mode: This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via their "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition. 0 - Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime the Receive STM-1 SOH Processor block declares the LOS defect condition. 1 - Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS Indicator via their "downstream" DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition. **NOTE:** In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS/AIS via Downstream STM-0s/DS3s Enable) within this register, in order to enable this feature. Transmit AU-AIS/AIS R/W Transmit AU-AIS via Downstream STM-0s) upon declaration of the 4 (via Downstream STM-LOF (Loss of Frame) defect condition/Transmit DS3 AIS (via 0s/DS3s) upon LOF Downstream DS3s) upon declaration of the LOF defect condition: The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STM-0 or DS3 signals, on the "low-speed" side of the chip, as described below. The product the pr For those channels that are configured to operate in the STM-0 Mode This READ/WRITE bit-field permits the user to configure all of the active Transmit STM-0 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOF defect condition. 0 - Does not configures all "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime the Receive STM-1 SOH Processor block declares the LOF defect condition. 1 - Configures all "activated" Transmit STM-0POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOF defect condition. Note: 1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AU-AIS Down-stream – Upon LOF), within the Receive STM-1 Section – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STM-0 POH Processor blocks to IMMEDIATELY begin to transmit the AU-AIS condition whenever the Receive STM-1 SOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AU-AIS indicator downstream within 125us of the NE

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declaring the LOF defect.

order enable this feature.

LOF defect condition.

block declares the LOF defect condition.

AU-AIS indicators.

2. In the case of Bit 2 (Transmit AU-AIS Downstream - Upon LOF), several SONET frame periods are required (after the Receive STM-1 SOH Processor block has declared the LOS defect), before the Transmit STM-0 POH Processor blocks will begin the process of transmitting the

3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS via Downstream STM-0s Enable) within this register, in

For those channels that are configured to operate in the DS3 Mode: This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive

0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AS indicator via the "downstream" DS3 signals, anytime the Receive STM-1(SOH Processor block declares the

1 - Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 Alsondicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor

NOTE: In addition to setting this bit-field to "1", the user must also set Bit

STM-1 SOH Processor block declares the LOF defect condition.

		0 (Transmit AU-AIS/AIS via Downstream STM-0s/DS3s Enable) within this register, in order to enable this feature.
Transmit AU-AIS/AIS (via Downstream STM- 0s/DS3s) upon SD	R/W	Transmit AU-AIS (via Downstream STM-0s) upon declaration of the SD (Signal Degrade) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the SD defect condition:
	. c't	The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STM-0 or DS3 signals, on the "low-speed" side of the chip, as described below.
S.	dure	For those channels that are configured to operate in the STM-0 Modes:
The pr	andn	This READ/WRITE bit-field permits the user to configure all of the active Transmit STM-0 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SD defect condition.
		0 – Does not configures all "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime the Receive STM-1 SOH Processor block declares the SD defect condition.
		1 – Configures all "activated" Transmit STM-0POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SD defect condition.
		Note:
		1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AU-AIS Down-stream – Upon SD), within the Receive STM-1 Section – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STM-0 POH Processor blocks to IMMEDIATELY
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			begin to transmit the AU-AIS condition whenever the Receive STM-1 SOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AU-AIS indicator downstream within 125us of the NE declaring the LOS defect.
			2. In the case of Bit 1 (Transmit AU-AIS Downstream – Upon LOF), several SONET frame periods are required (after the Receive STM-1 SOH Processor block has declared the SD defect), before the Transmit STM-0 POH Processor blocks will begin the process of transmitting the AU-AIS indicators.
			3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS via Downstream STM-0s Enable) within this register, in order enable this feature.
			For those channels that are configured to operate in the DS3 Mode:
			This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SD defect condition.
			0 – Does not configure all "active" DS3/E3 Framer block s to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime the Receive STM-1 SOH Processor block declares the SD defect condition.
			1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS Indicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SD defect condition.
			<b>NOTE:</b> In addition to setting this bit-field to "1" the user must also set Bit O Transmit AU-AIS/AIS via Downstream STM-0s/DS3s Enable) within this register in order to enable this feature.
2	Transmit AU-AIS/AIS (via Downstream STM- 0s/DS3s) upon SF	R/W	Transmit AU-AIS (via Downstream STM-0s) upon declaration of the Signal Failure (SF) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the SF defect condition:
	produ		The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STM-0 or DS3 signals, on the "low-speed" side of the chip, as described below.
	The aton	no	For those channels that are configured to operate in the STM-0 Mode:
	311		This READ/WRITE bit-field permits the user to configure all of the active Transmit STM-0 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SF defect condition.
			0 – Does not configures all "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime the Receive STM-1 SOH Processor block declares the SF defect condition.
			1 – Configures all "activated" Transmit STM-0POH Processor blocks to automatically transmit the AU-AIS Indicator via the "downstream" STM-0 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SF defect condition.
			NOTES:
			1. In the "long-run" the function of this bit-field is exactly the same as that



			of Bit 5 (Transmit AU-AIS Down-stream – Upon SF), within the Receive STM-1 Section – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STM-0 POH Processor blocks to IMMEDIATELY begin transmit the AU-AIS condition whenever the Receive STM-1 SOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AU-AIS indicator downstream within 125us of the NE declaring the SF defect.
			2. In the case of Bit 5 (Transmit AU-AIS Downstream – Upon SF), several SONET frame periods are required (after the Receive STM-1 SOH Processor block has declared the SF defect), before the Transmit STM-0 POH Processor blocks will begin the process of transmitting the AU-AIS indicators.
			3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS via Downstream STM-0s Enable) within this register, in order enable this feature.
			For those channels that are configured to operate in the DS3 Mode:
			This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SF defect condition.
			0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime the Receive STM-1 SOH Processor block declares the SF defect condition
			1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the SF defect condition.
		درگ	<b>NOTE:</b> In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AU-AIS/AIS via Downstream STM-0s/DS3s Enable) within this register, in order to enable this feature.
1	MS-AIS Output Enable	R/W	MS-AIS Output Enable:
	thept		This READ/WRITE bit-field, along with Bits 7 (8kHz or STUFF Out Enable) within the "Operation Output Control Register – Byte 1" (Address Location= 0x0150) permit the user to configure the "MS-AIS" indicator to be output via the "LOF" output pin (pin AD11).
	. 90	ano	If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "1" configures pin AD11 to function as the MS-AIS output indicator.
			If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "0" configures pin AD11 to function as the LOF output indicator.
			If Bit 7 (within the "Operation Output Control Register – Byte 1) is set to "1", then this register bit is ignored.
0	Transmit AU-AIS/AIS (via Downstream STM- 0s/	R/W	Automatic Transmission of AU-AIS/AIS (via the downstream STM-0s or DS3s) Enable:
	DS3s) Enable		The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STM-0 or DS3 signals, on the "low-speed" side of the chip, as described below.
			For those channels that are configured to operate in the STM-0



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	Mode:
	This READ/WRITE bit-field permits the user to configure all "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS indicator, via its "outbound" STM-0 signals, upon detection of an SF, SD, LOS, LOF and MS-AIS defect conditions.
	0 – Does not configure the "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares either the LOS, LOF, SD, SF or AIS defect condition.
	1 – Configures the "activated" Transmit STM-0 POH Processor blocks to automatically transmit the AU-AIS indicator (via their downstream signal paths), whenever (and for the duration that) the Receive STM-1 SOH Processor block declares either the LOS, LOF, SD, SF or MS-AIS defect conditions.
	NOTES: 1. The user must also set the corresponding bit-fields (within this register) to "1" in order to configure all "active" Transmit STM-0 SOH Processor blocks to automatically transmit the AU-AIS indicator (downstream) whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS, LOF, SD or SF defect conditions.
	<ol> <li>Setting this particular bit-field to "1" will also configure all "active" Transmit STM-0 SOH Processor blocks to automatically transmit the AU-AIS indicator (downstream) whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the MS-AIS defect condition.</li> <li>For those channels that are configured to operate in the DS3 Mode:</li> </ol>
	This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS, LOF, SD, SF or MS-AIS defect conditions.
orodu ² eet	0. Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime the Receive STM-1 SOH Processor block declares either the LOS, LOF, SD, SF or MS-AIS defect conditions.
The ata and max	1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime (and for the duration that) the Receive STM-1 SOH Processor block declares either the LOS, LOF, SD, SF or MS-AIS defect conditions.
Ŭ	NOTES:
	<ol> <li>The user must also set the corresponding bit-fields (within this register) to "1" in order to configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator (downstream) whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS, LOF, SD or SF defect conditions.</li> </ol>
	<ol> <li>Setting this particular bit-field to "1" will also configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator (downstream) whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the MS-AIS defect condition.</li> </ol>

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

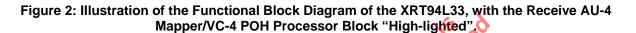


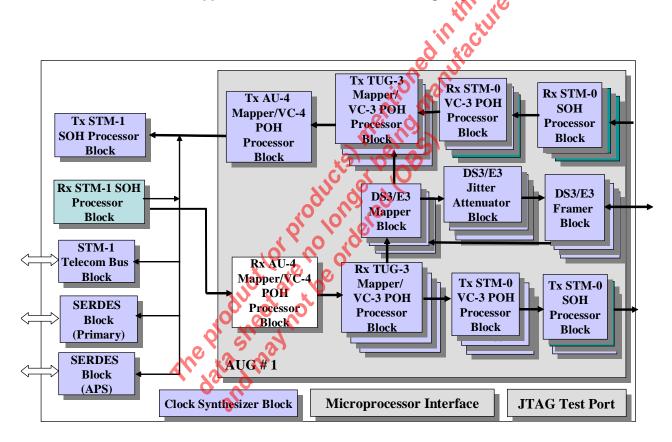
#### 1.5 RECEIVE AU-4 MAPPER/VC-4 POH PROCESSOR BLOCK

The register map for the Receive AU-4 Mapper/VC-4 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive AU-4 Mapper/VC-4 POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive AU-4 Mapper/VC-4 POH Processor Block "highlighted" is presented below in Figure 2.

It should be noted that for Mapper Aggregation Applications, the Receive AU-4 Mapper/VC-4 POH Processor block is only active if the user has configured the chip to operate in the SDH/TUG-3 Mapper. This functional block is not available if the user configures the chip to operate in the SDH/AU-3 Mode.







#### 1.5.1 RECEIVE AU-4 MAPPER/VC-4 POH PROCESSOR BLOCK REGISTER

#### Table 119: Receive AU-4 Mapper/VC-4 POH Processor Block Register - Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x1000 – 0x1181	Reserved	0x00
0x1182	Receive AU-4 Mapper/VC-4 Path – Control Register – Byte 1	0x00
0x1183	Receive AU-4 Mapper/VC-4 Path – Control Register – Byte 0	0x00
0x1184, 0x1185	Reserved	0x00
0x1186	Receive AU-4 Mapper/VC-4 Path – Status Register – Byte 1	0x00
0x1187	Receive AU-4 Mapper/VC-4 Path – Status Register – Byte 0	0x00
0x1188	Reserved	0x00
0x1189	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 2	0x00
0x118A	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 1	0x00
0x118B	Receive AU-4 Mapper/VC-4 Path – Interrupt Status Register – Byte 0	0x00
0x118C	Reserved	0x00
0x118D	Receive AU-4 Mapper/VC-4 Path - Interrupt Enable Register - Byte 2	0x00
0x118E	Receive AU-4 Mapper/VC-4 Path - Interrupt Enable Register - Byte 1	0x00
0x118F	Receive AU-4 Mapper/VC Path Interrupt Enable Register – Byte 0	0x00
0x1190 - 0x1192	Reserved	0x00
0x1193	Receive AU-4 Mapper/VC-4 Path SONET Receive HP-RDI Register	0x00
0x1194, 0x1195	Reserved	0x00
0x1196	Receive AU-4 Mapper/VC-4 Path – Received Path Label Byte (C2) Register	0x00
0x1197	Receive AU-4-Mapper/VC-4 Path – Expected Path Label Byte (C2) Register	0x00
0x1198	Receive AU-4 Mapper/VC-4 Path – B3 Error Count Register – Byte 3	0x00
0x1199	Receive AU-4 Mapper/VC-4 Path – B3 Error Count Register – Byte 2	0x00
0x119A	Receive AV-4 Mapper/VC-4 Path – B3 Error Count Register – Byte 1	0x00
0x119B	Receive AU-4 Mapper/VC-4 Path – B3 Error Count Register – Byte 0	0x00
0x119C	Receive AU-4 Mapper/VC-4 Path – HP-REI Error Count Register – Byte 3	0x00
0x119D	Receive AU-4 Mapper/VC-4 Path – HP-REI Error Count Register – Byte 2	0x00
0x119E	Receive AU-4 Mapper/VC-4 Path – HP-REI Error Count Register – Byte 1	0x00
0x119F	Receive AU-4 Mapper/VC-4 Path – HP-REI Error Count Register – Byte 0	0x00
0x11A0 - 0x11A2	Reserved	0x00
0x11A3	Receive AU-4 Mapper/VC-4 Path – Receive J1 Byte Control Register	0x00
0x11A4, 0x11A5	Reserved	0x00



Address Location	REGISTER NAME	DEFAULT VALUES
0x11A6	Receive AU-4 Mapper/VC-4 Path – Pointer Value Register – Byte 1	0x00
0x11A7	Receive AU-4 Mapper/VC-4 Path – Pointer Value Register – Byte 0	0x00
0x11A8 – 0x11AA	Reserved	0x00
0x11AB	Receive AU-4 Mapper/VC-4 Path – Loss of Pointer – Concatenation Status Register	0x00
0x11AC - 0x11B2	Reserved	0x00
0x11B3	Receive AU-4 Mapper/VC-4 Path – AIS - Concatenation Status Register	0x00
0x11B4 – 0x11BA	Reserved	0x00
0x11BB	Receive AU-4 Mapper/VC-4 Path – AUTO AIS Control Register	0x00
0x11BC - 0x11BE	Reserved	0x00
0x11BF	Receive AU-4 Mapper/VC-4 Path – Serial Port Control Register	0x00
0x11C0 - 0x11C2	Reserved	0x00
0x11C3	Receive AU-4 Mapper/VC-4 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0x11C4 - 0x11D2	Reserved	0x00
0x11D3	Receive AU-4 Mapper/VC-4 Path Receive J1Byte Capture Register	0x00
0x11D4 - 0x11D6	Reserved	0x00
0x11D7	Receive AU-4 Mapper/VC-4 Path Receive B3 Byte Capture Register	0x00
0x11D8 – 0x11DA	Reserved 0 10 01	0x00
0x11DB	Receive AU-4 Mapper/VC 4 Path Receive C2 Byte Capture Register	0x00
0x11DC - 0x11DE	Reserved	0x00
0x11DF	Receive AU-4 Mapper/VC-4 Path – Receive G1 Byte Capture Register	0x00
0x11E0 - 0x11E2	Reserved	0x00
0x11E3	Receive A0-4 Mapper/VC-4 Path – Receive F2 Byte Capture Register	0x00
0x11E4 - 0x11E6	Reserved	0x00
0x11E7	Receive AU-4 Mapper/VC-4 Path – Receive H4 Byte Capture Register	0x00
0x11E8 – 0x11EA	Reserved	0x00
0x11EB	Receive AU-4 Mapper/VC-4 Path – Receive Z3 Byte Capture Register	0x00
0x11EC - 0x11EE	Reserved	0x00
0x11EF	Receive AU-4 Mapper/VC-4 Path – Receive Z4 (K3) Byte Capture Register	0x00
0x11F0-0x11F2	Reserved	0x00
0x11F3	Receive AU-4 Mapper/VC-4 Path – Receive Z5 Byte Capture Register	0x00
0x11F4 – 0x11FF	Reserved	

#### 1.5.2 RECEIVE AU-4 MAPPER/VC-4 POH PROCESSOR BLOCK REGISTER DESCRIPTION

#### Table 120: Receive AU-4 Mapper/VC-4 Path – Control Register – Byte 0 (Address Location= 0x1183)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Check	HP-RDI	REI-P	B3 Error Type
				Stuff	Туре	Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.
			0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.
			1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation will be ignored.
2	HP-RDI Type	R/W	Path – Remote Defect Indicator Type Select:
		duct (C	This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4-POH Processor block to support either the "Single-Bit" or the "Enhanced" HP-RDI form of signaling, as described below. 0 - Configures the Receive AU-4 Mapper/VC-4 POH Processor block to support the Single-Bit HP-RDI. In this mode, the Receive AU-4 Mapper//C-4 POH Processor block will only monitor Bit 5, within the G1 byte (of incoming SPE data), in order to declare and clear the HP-RDI defect condition.
	thep	oducit osheet	Configures the Receive AU-4 Mapper/VC-4 POH Processor block to support the Enhanced HP-RDI (ERDI-P). In this mode, the Receive AU-4 Mapper/VC-4 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the HP-RDI defect condition.
1	REI-P Error	R/W	REI-P Error Type:
	Туре	<b>?</b>	This READ/WRITE bit-field permits the user to specify how the "Receive AU-4 Mapper/VC-4 POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive AU-4 Mapper/VC-4 POH Processor block to increment REI-P events on either a "per-bit" or "per-frame" basis. If the user configures the Receive AU-4 Mapper/VC-4 POH Processor block to increment REI-P events on a "per-bit" basis, then it will increment the Receive AU-4 Mapper/VC-4 Path REI-P Error Count" register by the value of the lower nibble within the G1 byte of the incoming AU-4 Mapper/VC-4 data-stream.
			If the user configure the Receive AU-4 Mapper/VC-4 POH Processor block to increment REI-P events on a "per-frame" basis, then it will increment the "Receive AU-4 Mapper/VC-4 Path – REI-P Error Count" register each time it receives an STS-3c SPE, in which the lower-nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value.
			0 - Configures the Receive AU-4 Mapper/VC-4 POH Processor block to

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			count or tally REI-P events on a per-bit basis. 1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to count or tally REI-P events on a "per-frame" basis.
0	B3 Error Type	R/W	B3 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive AU-4 Mapper/VC-4 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive AU-4 Mapper/VC-4 POH Processor block to increment B3 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive AU-4 Mapper/VC-4 POH Processor block to increment B3 byte errors on a "per-bit" basis, then it will increment the "Receive AU-4 Mapper/VC-4 PAth - B3 Byte Error Count" register by the number of bits (within the B3 byte value of the incoming AU-4/VC-4 data-stream) that is in error.
			If the user configures the Receive AU-4 Mapper/VC-4 POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count" Register each time that it receives an STS-3c SPE that contains an erred B3 byte.
			0 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to count B3 byte errors on a "per-bit" basis.
			1 – Configures the Receive AU4 Mapper/VC-4 POH Processor block to count B3 byte errors on a "per-frame" basis.

- Configures the Receive AU count B3 byte errors on a "perstrand"



## Table 121: Receive AU-4 Mapper/VC-4 Path – Receive Status Register – Byte 1 (Address Location= 0x1186)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused				Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 1 U	Jnused	R/O	while rock
M Uu [	Path Trace lessage Instable Defect Declared	R/O	<ul> <li>Path Trace Message Unstable Defect Declared:</li> <li>This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive AU-4 Mapper/VC-4 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The "Path Trace Message Unstable" counter will be incremented for each time that it receives a Path Trace Message Unstable" counter is cleared to "0" whenever the Receive AU-4 Mapper/VC-4 POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times.</li> <li>Note: Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to "0".</li> <li>0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the Path Trace Message Unstable defect condition.</li> <li>1 Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the Path Trace Message Unstable defect condition.</li> </ul>

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 122: Receive AU-4 Mapper/VC-4 Path – SONET Receive Status Register – Byte 0 (Address Location= 0x1187)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	UNEQ-P Defect Declared	PLM-P Defect Declared	HP-RDI Defect Declared	HP-RDI Unstable Condition	LOP-P Defect Declared	AU-AIS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	TIM-P Defect	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition.
			The Receive AU-4 Mapper/VC-4POH Processor block will declare the "TIM-P" defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STS-3c data-stream) matches the expected 1, 16 or 64-byte message.
			The Receive AU-4 Mapper/VC4 POH Processor block will clear the "TIM-P" defect condition, when 80% of the received 1, 16 or 64-byte string (received via the J1 byte) matches the expected 1, 16 or 64-byte message.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the TIM-P defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Defect Declared:
	Unstable Defect Declared	6	This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the "Path Signal Label Byte" Unstable defect condition.
	~	nepro	The Receive AU-4 Mapper/VC-4 POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the "C2 Byte Unstable" counter reaches the value "5". The "C2 Byte Unstable" counter will be incremented for each time that it receives an STS-3c SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Byte Unstable" counter is cleared to "0" whenever the Receive AU-4 Mapper/VC-4 POH Processor block has received 3 (or 5) consecutive STS-3c SPEs that each contain the same C2 byte value.
			<b>Note:</b> Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	UNEQ-P	R/O	Path – Unequipped Indicator (UNEQ-P) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the UNEQ-P defect condition.
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the UNEQ-



			P defect condition anytime that it receives at least five (5) consecutive AU- 4/VC-4 frames, in which the C2 byte was set to 0x00 (which indicates that the STS-3c SPE is "Unequipped").
			The Receive AU-4 Mapper/VC-4 POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive AU-4/VC-4 frames, in which the C2 byte was set to a value other than 0x00.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently NOT declaring the UNEQ-P defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the UNEQ-P defect condition.
			Note:
			1. The Receive AU-4 Mapper/VC-4 POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive AU-4/VC-4 frames with C2 bytes being set to "0x00" (e.g., if the "Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register is set to "0x00").
			2. The Address Locations of the "Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register is 0x1197
4	PLM-P	R/O	Path Payload Mismatch Indicator (PLM-P) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the PLM-P defect condition.
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive AU-4/VC-4 frames, in which the C2 byte was set to a value other than that which it is expecting to receive.
			Whenever the Receive AU-4 Mapper/VC-4 POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers.
			• The "Receive AU-4 Mapper/VC-4 Path – Received Path Label Value" Register (Address Location = 0x1196)
		AUC	• The "Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register (Address Location = 0x1197)
	0	proshe	The "Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive AU-4 Mapper/VC-4 POH Processor blocks expects to receive.
	The	atandr	The "Receive AU-4 Mapper/VC-4 Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive AU-4 Mapper/VC-4 POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive SONET frames).
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the PLM-P defect condition if the contents of these two register do not match. The Receive AU-4 Mapper/VC-4 POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently NOT declaring the PLM-P defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the PLM-P defect condition.
			<b>Note:</b> The Receive AU-4 Mapper/VC-4 POH Processor block will clear the PLM-P defect, upon declaring the UNEQ-P defect condition.
3	HP-RDI	R/O	Path Remote Defect Indicator (HP-RDI) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4



			Mapper/VC-4 POH Processor block is currently declaring the HP-RDI defect condition.
			If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to support the "Single-bit HP-RDI" function, then it will declare the HP-RDI defect condition if Bit 5 (within the G1 byte of the incoming AU-4/VC-4 frame) is set to "1" for "HP-RDI_THRD" number of incoming consecutive STS-3c SPEs.
			If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to support the Enhanced HP-RDI" (EHP-RDI) function, then it will declare the HP-RDI defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming AU-4/VC-4 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "HP-RDI_THRD" number of consecutive STS-3c SPEs.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the HP-RDI defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the HP-RDI defect condition.
			Note:
			1. The user can specify the value for "HP-RDI_THRD" by writing the appropriate data into Bits 3 through 0 (HP-RDI THRD) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Register.
			2. The Address Location of the "Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Registers is 0x1193
2	HP-RDI	R/O	HP-RDI (Path – Remote Defect Indicator) Unstable Defect Declared:
	Unstable Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the "HP-RDI Unstable" defect condition. The Receive AU-4 Mapper/VC-4 POH Processor block will declare a "HP-RDI Unstable" defect condition whenever the "HP-RDI Unstable Counter" reaches the value "HP-RDI THRD". The "HP-RDI Unstable" counter is incremented for each time that the Receive AU-4 Mapper/VC-4 POH Processor block receives an HP-RDI value that differs from that of the previous AU-4/VC-4 frame. The "HP-RDI Unstable" counter is cleared to "0" whenever the same HP-RDI value is received in "HP-RDI_THRD" consecutive AU-4/VC-4 frames.
		Ś	Note: Receiving a given HP-RDI value, in "HP-RDI_THRD" consecutive
		Pro	Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the "HP-RDI Unstable" defect condition.
	K	ne ata	1 Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is purrently declaring the "HP-RDI Unstable" defect condition.
		2	Note:
			1. The user can specify the value for "HP-RDI_THRD" by writing the appropriate data into Bits 3 through 0 (HP-RDI THRD) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Register.
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Registers is 0x1193
1	LOP-P	R/O	Loss of Pointer Indicator (LOP-P) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition.
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive AU-4 Mapper/VC-4 POH Processor block will declare the LOP-P defect condition, if



			it detects 8 to 10 consecutive NDF events.
			The Receive AU-4 Mapper/VC-4 POH Processor block will clear the LOP-P defect condition, whenever the Receive AU-4 Mapper/VC-4 POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming AU-4/VC-4 frames.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the LOP-P defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the LOP-P defect condition.
0	AU-AIS	R/O	Path AIS (AU-AIS) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AU-AIS defect condition. The Receive AU-4 Mapper/VC-4 POH Processor block will declare the AU-AIS defect condition if it detects all of the following conditions within three consecutive incoming AU-4/VC-4 frames.
			a. The H1, H2 and H3 bytes are set to an "All Ones" pattern.
			b. The entire SPE is set to an "All Ones" pattern.
			The Receive AU-4 Mapper/VC-4 POH Processor block will clear the AU-AIS defect condition when it detects a valid AU-4/VC-4 pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive AU-4/VC-4 frames.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the AU-AIS defect condition.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AU-AIS defect condition.
			<b>Note:</b> The Receive AU-4 Mapper/VC-4 POH Processor block will NOT declare the LOP-P defect condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AU-AIS defect condition.

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## Table 123: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0x1189)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in AIS-C Defect Condition Interrupt Status	Change in LOP-C Defect Condition Interrupt Status	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
					wils re	ò	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	6 K3C
6	Change in AIS-C Defect Condition Interrupt Status	RUR	Change in AIS (AIS) Concatenation) Defect Condition
			This RESET-upon-READ bit-field permits indicates whether or not the "Change in AIS-C Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then an interrupt will be generated in response to either of the following events.
		, pr	a Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the AIS-C defect condition with one of the STM-0 time-slots"; within the incoming AU-4/VC-4 signal.
	The product	ole	Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the AIS-C defect condition with one of the "STM-0 time-slots"; within the incoming AU- 4/VC-4 signal.
	orothe	er no	0 – Indicates that the "Change in AIS-C Defect Condition" Interrupt has NOT occurred since the last read of this register.
	the tak	3	1 – Indicates that the "Change in AIS-C Defect Condition" Interrupt has occurred since the last read of this register.
	1. 9s nd		<b>Note:</b> The user can determine the current state of AIS-C by reading out the contents of the "Receive AU-4 Mapper/VC-4 Path – AIS-C Status" Register (Address Locations: 0x11B3).
5	Change in LOP-C Defect Condition Interrupt Status	RUR	Change in LOP-C (Loss of Pointer - Concatenation) Defect Condition Interrupt Status:
			This RESET-upon-READ bit-field permits indicates whether or not the "Change in LOP-C Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then an interrupt will be generated in response to either of the following events.
			<ul> <li>a. Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the LOP-C defect condition with one of the "STM-0 time-slots"; within the incoming AU-4/VC-4 signal.</li> </ul>



	Γ	1	
			<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the LOP-C defect condition with one of the "STM-0 timeslots"; within the incoming AU- 4/VC-4 signal.</li> </ul>
			0 – Indicates that the "Change in LOP-C Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in LOP-C Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine the current state of the LOP-C defect by reading out the contents of the "Receive AU-4 Mapper/VC-4 Path – LOP-C Status" Register (Address Locations: 0x11AB).
4	Detection of AIS Pointer	RUR	Detection of AIS Pointer Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming AU-4/VC-4 data stream.
			<b>Note:</b> An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the SOH) are each set to an "All Ones" pattern.
			0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register.
		NU	1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change	RUR	Detection of Pointer Change Interrupt Status:
	Interrupt Status	6,00	This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the ast read of this register.
	Detection of Pointer Change Interrupt Status	not be	If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the SOH bytes).
	the to not		0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register.
	1 9's 10		1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	i on ouptaio interiupt	RUR	Path Overhead Data Capture Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "POH Capture" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data, for the next SPE will be loaded into the "POH Capture" buffer.
			0 – Indicates that the "POH Capture" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "POH Capture" Interrupt has occurred



			since the last read of this register.
			<i>Note:</i> The user can obtain the contents of the POH, within the most recently received SPE by reading out the contents of address locations "0xN0D3" through "0xN0F3").
1	Change in TIM-P Defect Condition Interrupt Status	RUR	Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.
			This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
			Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares theTIM-P detect condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the TIM-P defect condition.
			0 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.
0	Change in Path Trace Message Unstable Defect	RUR	Change in Path Trace Identification Message Unstable Defect Condition," Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.
		orpri	If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate this interrupt in response to either of the following events.
	e product	20	• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declare the "Path Trace Message Unstable" Defect Condition.
	e proshe	atro	• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "Path Trace Message Unstable" defect condition.
	The atand		0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.



## Table 124: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0x118A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in HP-RDI Unstable Defect Condition Interrupt Status	New HP-RDI Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

	1	1	<u> </u>
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	New Path Trace	RUR	New Path Trace Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.
			0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the ast read of this register.
			1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of REI-P	RUR	Detection of REI-P Event Interrupt Status:
	Event Interrupt Status		This RESET upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
	NOIN		If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming AU-4/VC-4 data-stream.
			Indicates that the "Detection of REI-P Event" Interrupt has NOT securred since the last read of this register.
	the to	SINA	1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ- P Defecft	RUR	Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Status:
	P Defectt Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following conditions.
			Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the UNEQ-P Defect Condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the UNEQ-P Defect Condition.
			0 – Indicates that the "Change in UNEQ-P Defecft Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has



			occurred since the last read of this register.
			Note:
			<ol> <li>The user can determine the current state of the UNEQ-P defect condition by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register.</li> </ol>
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Registers is 0x1187
4	Change in PLM-P Defect Condition	RUR	Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit indicates whether or not the "Change in PLM- P Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive AU-4 Mapper/VC-4 POH Processor block declares the "PLM-P" Defect Condition
			When the Receive AU 4 Mapper/VC-4 POH Processor block clears the "PLM-P" Defect Condition.
			0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register.
3	-	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon READ bit-field indicates whether or not the "New C2 Byte Onterrupt has occurred since the last read of this register.
		, U	If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
		odu	0 - Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
	ine (	S, S,	14 Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2 Byte	RUR	Change in C2 Byte Unstable Defect Condition Interrupt Status:
	Unstable Defect Condition Interrupt Status	an	This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
			• When the Receive AU-4 Mapper/VC-4 POH Processor block declares the "C2 Byte Unstable" defect condition.
			• When the Receive AU-4 Mapper/VC-4 POH Processor block clears the "C2 Byte Unstable" defect condition.
			0 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.



			Note:
			1. The user can determine the current state of "C2 Byte Unstable Defect Condition" by reading out the state of Bit 6 (C2 Byte Unstable Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register.
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register is 0x1187
1	Change in HP-RDI	RUR	Change in HP-RDI Unstable Defect Condition Interrupt Status:
	Unstable Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in HP-RDI Unstable Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following conditions.
			<ul> <li>When the Receive AU-4 Mapper/VC-4 POH Processor block declares an "HP-RDI Unstable" defect condition.</li> </ul>
			<ul> <li>When the Receive AU-4 Mapper/VC-4 POH Processor block clears the "HP-RDI Unstable" defect condition.</li> </ul>
			0 – Indicates that the "Change in HP-RDI Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in HP-RDI Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> 1. The user can determine the current state of "HP-RDI Unstable Defectg condition" by reading out the state of Bit 2 (HP-RDI Unstable Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register.
		Ó	<ol> <li>The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register is 0x1187</li> </ol>
0	New HP-RDI Value Interrupt Status	RUR	New HP-RDI Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New HP- RDI Value" interrupt has occurred since the last read of this register.
	ine the	sheat	If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate this interrupt anytime it receives and "validates" a new HP-RDI value.
	1. 93	0	0 – Indicates that the "New HP-RDI Value" Interrupt has NOT occurred since the last read of this register.
	0		1 – Indicates that the "New HP-RDI Value" Interrupt has occurred since the last read of this register.
			Note:
			1. The user can obtain the "New HP-RDI Value" by reading out the contents of the "HP-RDI ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Register".
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register is 0x1193



## Table 125: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0x118B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte	Detection of New Pointer	Detection of Unknown	Detection of Pointer	Detection of Pointer	Detection of NDF Pointer	Change of LOP-P	Change of AU-AIS
Error Interrupt Status	Interrupt Status	Pointer Interrupt Status	Decrement Interrupt Status	Increment Interrupt Status	Interrupt Status	Defect Condition Interrupt Status	Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Detection of B3	RUR	Detection of B3 Byte Error Interrupt Status:
	Byte Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming AU-4/VC-4 data stream.
			0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt.
			1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of	RUR	Detection of New Pointer Interrupt Status:
	New Pointer Interrupt Status		This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register.
		رة	fo the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POL Processor block will generate an interrupt anytime it detects a new pointer value in the incoming AU-4/VC-4 frame.
		90	Note Pointer Adjustments with NDF will not generate this interrupt.
		pr she	0 - Indicates that the "Detection of New Pointer" Interrupt has NOT
	44	data dr	1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of	RUR	Detection of Unknown Pointer Interrupt Status:
	Unknown Pointer Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories.
			An Increment Pointer
			A Decrement Pointer
			An NDF Pointer
			An AIS (e.g., All Ones) Pointer
			New Pointer
			0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT



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			occurred since the last read of this register.
			_
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of	RUR	Detection of Pointer Decrement Interrupt Status:
	Pointer Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of	RUR	Detection of Pointer Increment Interrupt Status:
	Pointer Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of	RUR	Detection of NDF Pointer Interrupt Status:
	NDF Pointer Interrupt Status	AUCT 2	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
	0	othery	Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
	the	3 113	1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP	RUR	Change of LOP-P Defect Condition Interrupt Status:
	P Defect Condition	0	This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
			a. Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the "LOP-P" defect condition.
			<ul> <li>Whenever the Receive "AU-4 Mapper/VC-4 POH Processor" block clears the LOP-P defect condition.</li> </ul>
			0 – Indicates that the "Change in LOP-P Defect Condition" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change in LOP-P Defect Condition" interrupt has



			occurred since the last read of this register.	
			Note:	
			1. The user can determine if the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the LOP-P defect condition by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register.	
			2. The Address Location of the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register is 0x1187	
0	Change of AU-	RUR	Change of AU-AIS Defect Condition Interrupt Status:	
	AIS Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AU-AIS Defect Condition" Interrupt has occurred since the last read of this register.	
		If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.		
			<ul> <li>Whenever the Receive AU-4, Mapper/VC-4 POH Processor block declares the AU-AIS defect condition.</li> </ul>	
			Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the AU-AIS defect condition.	
			0 – Indicates that the "Change of AU-AIS Defect Condition" Interrupt has NOT occurred since the last read of this register.	
			1 – Indicates that the "Change of AU-AIS Defect Condition" Interrupt has occurred since the last read of this register.	
		Note: 1. The user can determine if the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AU-AIS defect condition by reading out the state of Bit 0 (AU-AIS Defect Declared) within the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte		
		duct	0" Register 2.0 The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Registers is 0x1187	
2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Registers is 0x1187				



# Table 126: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location= 0x118D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New K3 Byte Interrupt Enable	Change in AIS-C Defect Condition Interrupt Enable	Change in LOP-C Defect Condition Interrupt Enable	Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	POH Capture Interrupt Enable	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
					is od		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	New K3 Byte Interrupt Enable	R/W	New K3 Byte Interrupt Enable:
	Lhable		This READ/WRITE bit-field permits the user to either enable or disable the "New K3 Byte" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new K3 Byte.
			0 – Disables the "New K3 Byte" Interrupt.
			1 - Enables the "New K3 Byte" Interrupt.
6	Change in AIS-C Defect Condition Interrupt Enable	R/W	Change in AIS-C (AIS Concatenation) Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS-C Defect Condition" Interrupt.
	ڻ		If this interrupt is enabled, then an interrupt will generated in response to either of the following events.
	orothe	et no	<ul> <li>a. Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the AIS-C defect condition within one of the STM-0 time-slots; within the incoming AU-4/VC-4 signal.</li> </ul>
	The product	13.7	<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the AIS-C defect condition with one of the STM- 0 time-slots; within the incoming AU-4/VC-4 signal.</li> </ul>
	21		0 – Disables the "Change in AIS-C Defect Condition" Interrupt.
			1 – Enables the "Change in AIS-C Defect Condition" Interrupt
			Note:
			This bit-field is only valid if the XRT94L33 is receiving an AU-4/VC-4 signal.
			This bit-field is only valid for the following Address Locations: "0x118D" (for AU-4/VC-4)
5	Change in LOP-C Condition Interrupt	R/W	Change in LOP-C (Loss of Pointer - Concatenation) Condition Interrupt Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP-C Defect Condition" Interrupt.
			If this interrupt is enabled, then an interrupt will generated in response to either of the following events.

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			<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the LOP-C defect condition with one of the STM-0 timeslots; within the incoming AU-4/VC-4 signal.</li> </ul>
			<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the LOP-C defect condition with one of the STM-0 timeslots; within the incoming AU-4/VC-4 signal.</li> </ul>
			0 – Disables the "Change in LOP-C Defect Condition" Interrupt.
			1 – Enables the "Change in LOP-C Defect Condition" Interrupt
			Note:
			This bit-field is only valid if the XRT94L33 is receiving an AU-4/VC-4 signal.
			This bit-field is only valid for the following Address Locations: "0x118D" (for AU-4/VC-4)
4	Detection of AIS Pointer	R/W	Detection of AIS Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt.
			If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming AU-4/VC-4 data stream.
			<b>Note:</b> An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the SOH) are each set to an "All Ones" Pattern.
			0 – Disables the "Detection of AIS Pointer" Interrupt.
			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:
	Change Interrupt Enable		This READWRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.
	<b>x</b>	JCL * 2	this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.
	,0	0	Disables the "Detection of Pointer Change" Interrupt.
	9	N 2	1 – Enables the "Detection of Pointer Change" Interrupt.
2	POH Capture Interrupt	R/W	Path Overhead Data Capture Interrupt Enable:
	Enable	0	This READ/WRITE bit-field permits the user to either enable or disable the "POH Capture" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data for the next SPE will be loaded into the "POH Capture" Buffer.
			0 – Disables the "POH Capture" Interrupt
			1 – Enables the "POH Capture" Interrupt.
1	Condition Interrupt		Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH



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			Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the TIM-P defect condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the TIM-P defect condition.
			0 – Disables the "Change in TIM-P Condition" Interrupt.
			1 – Enables the "Change in TIM-P Condition" Interrupt.
0	Change in Path Trace Message Unstable	R/W	Change in "Path Trace Message Unstable Defect Condition" Interrupt Status:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in Path Trace Message Unstable Defect Condition" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the "Path Frace Message Unstable" defect Condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "Path Trace Message Unstable" defect Condition.
			0 – Disables the "Change in Path Trace Message Unstable Defect Condition" interrupt
			1 - Enables the "Change in Path Trace Message Unstable Defect Condition" interrupt.
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## Table 127: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0x118E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in HP-RDI Unstable Defect Condition Interrupt Enable	New HP-RDI Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	Γ		<u> </u>
BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7	New Path Trace	R/W	New Path Trace Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.
			0 – Disables the "New Path Trace Message" Interrupt.
			1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of	R/W	Detection of REI-R Event Interrupt Enable:
	REI-P Event Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt.
		k	If this interrupt is enabled, then he Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects an REI-P event within the coming AU-4/VC-4 data-stream.
		C C	0 Disables the "Detection of REI-P Event" Interrupt.
		.00	— Enables the "Detection of REI-P Event" Interrupt.
5	Change in UNEQ-P Defect	R/W	Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt
	Condition Interrupt Enable	9310 d	This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Defect Condition" interrupt.
		<b>3</b>	If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the UNEQ-P Defect Condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the UNEQ-P Defect Condition.
			0 – Disables the "Change in UNEQ-P Defect Condition" Interrupt.
			1 – Enables the "Change in UNEQ-P Defect Condition" Interrupt.
4	Change in PLM- P Defect	R/W	Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt.



			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the
			following conditions.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the "PLM-P" Defect Condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "PLM-P" Defect Condition.
			0 – Disables the "Change in PLM-P Defect Condition" Interrupt.
			1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte	R/W	New C2 Byte Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New C2 Byte" Interrupt.
			Note:
			<ol> <li>The user can obtain the value of this "New C2" byte by reading the contents of the "Receive AU-4 Mapper/VC-4 Path – Received Path Label Value" Register.</li> </ol>
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – Received Path Label Value" Register is 0x1196
2	Change in C2 Byte Unstable	R/W	Change in C2 Byte Unstable Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Defect Condition" Interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
		obleet	Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the "C2 Byte Unstable" defect condition.
	e P	ashay	• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "C2 Byte Unstable" defect condition.
			0 – Disables the "Change in C2 Byte Unstable Condition" Interrupt.
		an -	1 – Enables the "Change in C2 Byte Unstable Condition" Interrupt.
1	Change in HP-	R/W	Change in HP-RDI Unstable Defect Condition Interrupt Enable:
	RDI Unstable Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in HP-RDI Unstable Defect Condition" interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares an "HP-RDI Unstable defect" condition.
			• Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "HP-RDI Unstable defect" condition.
			0 – Disables the "Change in HP-RDI Unstable Defect Condition" Interrupt.
			1 – Enables the "Change in HP-RDI Unstable Defect Condition" Interrupt.



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0	New HP-RDI Value Interrupt Enable	R/W	<b>New HP-RDI Value Interrupt Enable</b> : This READ/WRITE bit-field permits the user to either enable or disable the "New HP-RDI Value" interrupt.
			If this interrupt is enabled, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate this interrupt anytime it receives and "validates" a new HP-RDI value.
			0 – Disables the "New HP-RDI Value" Interrupt.
			1 – Enable the "New HP-RDI Value" Interrupt.

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## Table 128: Receive AU-4 Mapper/VC-4 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0x118F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte	Detection of New Pointer	Detection of Unknown	Detection of Pointer	Detection of Pointer	Detection of NDF Pointer	Change of LOP-P	Change of AU-AIS
Error Interrupt Enable	Interrupt Enable	Pointer Interrupt Enable	Decrement Interrupt Enable	Increment Interrupt Enable	Interrupt Enable	Defect Condition Interrupt Enable	Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of B3	R/W	Detection of B3 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		<ul> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming AU-4/VC-4 data-stream.</li> <li>0 – Disables the "Detection of B3 Byte Error" interrupt.</li> <li>1 – Enables the "Detection of B3 Byte Error" interrupt.</li> </ul>
6	Detection of New Pointer Interrupt Enable	R/W	<ul> <li>Detection of New Pointer Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming AU-4/VC-4 frame.</li> <li>Note: Pointer Adjustments with NDF will not generate this interrupt.</li> <li>0 _ Disables the "Detection of New Pointer" Interrupt.</li> </ul>
		d'et	C Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	and may	Detection of Unknown Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories.
			An Increment Pointer.
			A Decrement Pointer
			An NDF Pointer
			AIS Pointer
			New Pointer.
			0 – Disables the "Detection of Unknown Pointer" Interrupt.
			1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of	R/W	Detection of Pointer Decrement Interrupt Enable:
	Pointer Decrement Interrunt Enable		This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this



	Interrupt Enable		interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event.
			0 – Disables the "Detection of Pointer Decrement" Interrupt.
			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of	R/W	Detection of Pointer Increment Interrupt Enable:
	Pointer Increment Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Disables the "Detection of Pointer Increment" Interrupt.
			1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF	R/W	Detection of NDF Pointer Interrupt Enable
	Pointer Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
			0 – Disables the "Detection of NDF Pointer" interrupt.
			1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-	R/W	Change of LOP-P Defect Condition Interrupt Enable:
	P Defect Condition Interrupt Enable		This READ/WRITE bit field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Defect Condition interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor will generate an interrupt in response to either of the following events.
			<ul> <li>a. Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the LOP-P defect condition.</li> <li>b. Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the LOP-P defect condition.</li> </ul>
		ి	0 Disable the "Change of LOP-P Defect Condition" Interrupt.
		AND A	– Enables the "Change of LOP-P Defect Condition" Interrupt.
		NO NO	Note:
	The	data ndr	The user can determine if the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the LOP-P defect condition by reading out the contents of Bit 1 (LOP-P Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0".
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status Byte 0" Register is 0x1187
0	Change of AU- AIS Defect	R/W	Change of AU-AIS Defect Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of AU-AIS (Path AIS) Defect Condition" interrupt. If the user enables this interrupt, then the Receive AU-4 Mapper/VC-4 POH Processor block will generate an interrupt in response to either of the following events.
			<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block declares the "AU-AIS" defect condition.</li> </ul>
			<ul> <li>Whenever the Receive AU-4 Mapper/VC-4 POH Processor block clears the "AU-AIS" defect condition.</li> </ul>



<ul> <li>0 – Disables the "Change of AU-AIS Defect Condition" Interrupt.</li> <li>1 – Enables the "Change of AU-AIS Defect Condition" Interrupt.</li> <li>Note:</li> </ul>
1. The user can determine if the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AU-AIS defect condition by reading out the contents of Bit 0 (AU-AIS Defect Declared) within the "Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register.
2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – SONET Receive POH Status – Byte 0" Register is 0x1187



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## Table 129: Receive AU-4 Mapper/VC-4 Path – SONET Receive HP-RDI Register (Address Location= 0x1193)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused	HP-RDI_ACCEPT[2:0]			HP-RDI THRESHOLD[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	
6 – 4	HP- RDI_ACCEPT[2:0]	R/O	Accepted HP-RDI Value: These READ-ONLY bit-fields contain the value of the most recently "accepted" HP-RDI (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive AU-4 Mapper/VC-4 POH Processor block. Note: A given HP-RDI value will be "accepted" by the Receive AU-4 Mapper/VC-4 POH Processor block, if this HP-RDI value has been consistently received in "HP-RDI THRESHOLD[3:0]" number of SONET frames.
3 - 0	HP-RDI THRESHOLD[3:0]	R/W	HP-RDI Threshold[3:0]: These READ/WRITE bit-fields permit the user to defined the "HP-RDI Acceptance Threshold" for the Receive AU-4 Mapper/VC-4 POH Processor Block. The "HP-RDI Acceptance Threshold" is the number of consecutive SONET frames, in which the Receive AU-4 Mapper/VC-4 POH Processor block must receive a given HP-RDI value, before it "accepts" or "validates" it. The most recently "accepted" HP-RDI value is written into the "HP-RDI ACCEPT[2:0]" bit-fields, within this register.

ACCEPT[20]"



#### Table 130: Receive AU-4 Mapper/VC-4 Path – Received Path Label Value (Address Location= 0x1196)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Received_C2_Byte_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Received C2 Byte	R/O	Received "Filtered" C2 Byte Value:
	Value[7:0]		These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive AU-4 Mapper/VC-4 POH Processor block.
			The Receive AU-4 Mapper/VC-4 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive SONET frames.
			Note:
			1. The Receive AU-4 Mapper/VC-4 POH Processor block uses this register, along the "Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register, when declaring or clearing the UNEQ-P and PLM-P defect conditions.
			2. The Address Location of the Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value" Register is 0x1197

#### Table 131: Receive AU-4 Mapper/VC-4 Path – Expected Path Label Value (Address Location= 0x1197)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Expected_C2_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	10		1	1	1	1			
		d'e	0							

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value:
	Th'dated h		These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive AU-4 Mapper/VC-4 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions.
			If the contents of the "Received C2 Byte Value[7:0]" (see "Receive AU-4 Mapper/VC-4 Path – Received Path Label Value" register) matches the contents in these register, then the Receive AU-4 Mapper/VC-4 POH will not declare any defect conditions.
			<b>NOTE:</b> The Receive AU-4 Mapper/VC-4 POH Processor block uses this register, along with the "Receive AU-4 Mapper/VC-4 Path – Receive Path Label Value" Register (Address Location = 0x1196), when declaring or clearing the UNEQ-P and PLM-P defect conditions.

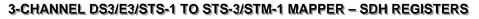




Table 132: Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Byte 3 (Address Location= 0x1198)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	B3_Byte_Error_Count[31:24]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	B3_Byte_Error_Count[31:24]	RUR	B3 Byte Error Count – MSB:
			<ul> <li>This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a B3 byte error.</li> <li><i>Note:</i> <ol> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.</li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.</li> </ol> </li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.</li> </ul>

# Table 133: Receive AU-4 Mapper/VC-4 Path B3 Byte Error Count Register – Byte 2 (Address Location= 0x1199)

Віт 7	Віт 6	Віт 5	Вл 4	Віт 3	Віт 2	Віт 1	Віт 0			
B32Byte_Brror_Count[23:16]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0 0 0 0 0 0 0									

BIT NUMBER	NAME V	Түре	DESCRIPTION			
7 – 0	B3_Byte_Error_Count[23:16]	RUR	B3 Byte Error Count (Bits 23 through 16):			
			This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a B3 byte error.			
			Note:			
			1. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.			
			2. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.			



## Table 134: Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Byte 1 (Address Location= 0x119A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	B3_Byte_Error_Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	B3_Byte_ Error_Count[15:8]	RUR	<ul> <li>B3 Byte Error Count – (Bits 15 through 8):</li> <li>This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a B3 byte error.</li> <li>Note: <ol> <li>If the Receive AU 4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.</li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.</li> </ol> </li> </ul>

# Table 135: Receive AU-4 Mapper/VC-4 Path Bit 7 Bit 6 Bit 5 Bit 6 Bit 7<

Віт 7	Віт 6	Віт 5	С Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	B3 Byte_Error_Count[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0		0	0	0	0	0				

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	B3_Byte_Error_Count[7:0]	RUR	B3 Byte Error Count – LSB:
			This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (or each incoming STS-3c SPE) that are in error.
			2. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 136: Receive AU-4 Mapper/VC-4 Path - REI-P Event Count Register - Byte 3 (Address Location= 0x119C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	REI-P_Event_Count[31:24]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	REI-P_Event_Count[31:24]	RUR	REI-P Event Count – MSB:
			<ul> <li>This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream.</li> <li><i>Note:</i> <ol> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-3c SPE.</li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-3c SPE.</li> </ol> </li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a "non-zero" REI-P value.</li> </ul>

#### Table 137: Receive AU-4 Mapper/VC-4 Path – REI-PEvent Error Count Register – Byte 2 (Address Location= 0x119D) 0 1 ୍ଷ ୦

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Віт 7	Віт 6	Віт 5	Вл 4	Віт 3	Віт 2	Віт 1	Віт 0
		, C	REI-P_Event	_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0		0	0	0	0	0

	× 5		
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P_Event_Count[23:16]	RUR	REI-P Event Count (Bits 23 through 16):
	9 ¹ 1		This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream.
			Note:
			1. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming AU-4/VC-4 frame.
			2. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an



STS-3c SPE that contains a "non-zero" REI-P value.
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 138: Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Byte 1 (Address Location=0x119E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			REI-P_Event	_Count[15:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	REI-P_Event_Count[15:8]	RUR	REI-P Event Count – (Bits 15 through 8)
			<ul> <li>This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a Path –Remote Error Indicator event within the incoming STS-3c SPE data-stream.</li> <li>Note:</li> <li>1. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within the incoming STS-3c SPE.</li> <li>2. If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a non-zero REI-P value.</li> </ul>

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Table 139: Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Byte 0 (Address Location=
0x119F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	REI-P_Event_Count[7:0]	RUR	REI-P Event Count – LSB:
		6	<ul> <li>This RESET-upon-READ register, along with "Receive AU-4 Mapper/VC-4 Path – REI-P Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive AU-4 Mapper/VC-4 POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream.</li> <li>Note: <ol> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte.</li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte.</li> </ol> </li> <li>If the Receive AU-4 Mapper/VC-4 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS 3c SPE that contains a "non-zero" REI-P value.</li> </ul>
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## Table 140: Receive AU-4 Mapper/VC-4 Path – Receive Path Trace Message Buffer Control Register (Address Location=0x11A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		New Message Ready	Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Message Type		Path Trace _ength[1:0]
R/O	R/O	R/O	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 5	Unused	R/O	nis eo
5	New Message Ready	R/O	<ul> <li>New Message Ready:</li> <li>This READ/WRITE bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block has (1) accepted a new Receive Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register.</li> <li>0 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block has (1) NOT accepted a new Path Trace Message, nor (2) has the Receive AU-4 Mapper/VC-4 POH Processor block loaded any new messages into the Receive Path Trace Message buffer, since the last read of this register.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block has (1) accepted a new Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register.</li> </ul>
4	Received Path Trace Message Buffer Read Select	R/W	<ul> <li>Receive Path Trace Message Buffer Read Selection:</li> <li>This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will ead out, whenever it reads out the contents of the Receive Path Trace Message Buffer.</li> <li>a. The "Actual" Receive Path Trace Message Buffer Contains the contents of the most recently received (and accepted) Path Trace Message via the incoming AU-4/VC-4 data-stream.</li> <li>b. The "Expected" Receive Path Trace Message Buffer Contains the contents of the Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message Buffer contains the contents of the Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message Buffer, will return contents of the Path Trace Message Buffer are usually specified by the user.</li> <li>0 – Executing a READ to the Receive Path Trace Message Buffer, will return contents within the "Actual" Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer will return contents within the "Expected" Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> <li>1 – Executing a READ to the Receive Path Trace Message Buffer.</li> </ul>
3	Path Trace Message Accept Threshold	R/W	Path Trace Message Accept Threshold: This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive AU-4 Mapper/VC-4 POH Processor block must receive



			a given Receive Path Trace Message, before it is accepted and loaded into the "Actual" Receive Path Trace Message Buffer, as described below.
			0 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to accept the incoming Path Trace Message after it has received it the third time in succession.
			1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to accept the incoming Path Trace Message after it has received in the fifth time in succession.
2	Path Trace	R/O	Path Trace Message Alignment Type:
	Message Alignment Type		This READ/WRITE bit-field permits a user to specify how the Receive AU-4 Mapper/VC-4 POH Processor block will locate the boundary of the incoming Path Trace Message (within the incoming AU-4/VC-4 data-stream), as indicated below.
			0 – Configures the Receive AU-4, Mapper/VC-4 POH Processor block to expect the Path Trace Message boundary to be denoted by a "Line Feed" character.
			1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to except the Path Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the first byte (within the incoming Path Trace Message). In this case, all of the remaining bytes (within the incoming Path Trace Message) will each have a "0" within their MSBs.
1 – 0	Path Trace Message Length[1:0]	R/W	Path Trace Message Length[1:0]: These READ/WRITE bit-fields permit the user to specify the length of the Receive Path Trace Message that the Receive AU-4 Mapper/VC-4 POH Processor block will accept and load into the "Actual" Receive Path Trace Message Buffer The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.
			MSG Resulting Path Trace Message Length
		, C	1 Byte
	الم	000	01 16 Bytes
	6	SU	10/11 64 Bytes
	11000	andn	

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 141: Receive AU-4 Mapper/VC-4 Path – Pointer Value – Byte 1 (Address Location= 0x11A6)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						Value MSB[9:8]
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[1:0]	R/O	Current Pointer Value – MSB:
			These READ-ONLY bit-fields, along with that from the "Receive AU-4 Mapper/VC-4 Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive AU-4 Mapper/VC-4 POH Processor" block is using to locate the STS 3c SPE within the incoming AU- 4/VC-4 data stream. <b>Note:</b> These register bits comprise the two-most significant bits of the Pointer Value.

#### Table 142: Receive AU-4 Mapper/VC-4 Path – Pointer Value Byte 0 (Address Location=0x11A7)

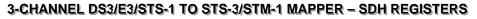
Віт 7	Віт 6	Віт 5	Віт 4 💋 Віт 3 🗸	Віт 2	Віт 1	Віт 0		
		C	Current_Pointer_Value_LSB[7:0	)]				
R/O	R/O	R/O	R/O R/O	R/O	R/O	R/O		
0	0	0		0	0	0		
	1 10 10 10 10 10 10 10 10 10 10 10 10 10							

BIT NUMBER		DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	Current Pointer Value – LSB:
	The prosteet not	These READ-ONLY bit-fields, along with that from the "Receive AU-4 Mapper/VC-4 Path – Pointer Value – Byte 1 Register combine to reflect the current value of the pointe that the "Receive AU-4 Mapper/VC-4 POH Processor" block is using to locate the STS-3c SPE within the incoming AU 4/VC-4 data stream.
	311	<b>Note:</b> These register bits comprise the Lower Byte value of the Pointer Value.

#### Table 143: Receive AU-4 Mapper/VC-4 Path – LOP-C Status Register (Address Location=0x11AB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	LOP-C Defect Declared STM- 0 time-slot # 3	LOP-C Defect Declared STM- 0 time-slot # 2	Unused		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 3	Unused	R/O	
2	LOP-C Defect Declared – STM-0 Time-Slot # 3	R/O	Loss of Pointer – Concatenation Defect Declared – STM-0 Time-Slot # 3:
			This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) defect condition with STM-0 time-slot # 3 (within the incoming AU-4/VC-4 signal).
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the LOP-C defect condition, with STM-0 time-slot # 3; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STM-0 time-slot # 3) for 8 consecutive AU-4/VC-4 frames.
		du	0 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the LOP-C defect condition with STM-0 time-slot # 3 within the incoming AU-4/VC- 4 data-stream.
		Pro no	<ul> <li>Mindicates that the Receive AU-4 Mapper/VC-4 POH</li> <li>Processor block is currently declaring the LOP-C defect</li> <li>condition with STM-0 time-slot # 3 within the incoming AU-4/VC-</li> <li>4 data-stream.</li> </ul>
	duct	st, pe	<b>Note:</b> This bit-field is only valid if the XRT94L33 is receiving and processing an AU-4/VC-4 signal.
1	LOP-C Defect Declared STM-0 Time Slot # 2	R/O	Loss of Pointer – Concatenation Defect Declared – STM-0 Time-Slot # 2:
	STM-0 Time-Slot # 2		This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) defect condition with STM-0 time-slot # 2 (within the incoming AU-4/VC-4 signal).
			The Receive AU-4 Mapper/VC-4 POH Processor block will declare the LOP-C defect condition, with STM-0 time-slot # 2; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STM-0 time-slot # 2) for 8 consecutive AU-4/VC-4 frames.
			0 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the LOP-C defect condition with STM-0 time-slot # 2 within the incoming AU-4/VC-4 data-stream.
			1 – Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the LOP-C defect condition with STM-0 time-slot # 2 within the incoming AU-4/VC-4 data-stream.
			Note: This bit-field is only valid if the XRT94L33 is receiving



			and processing an AU-4/VC-4 signal.
0	Unused	R/O	





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#### Table 144: Receive AU-4 Mapper/VC-4 Path – AIS-C Status Register (Address Location=0x11B3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	AIS-C Defect Declared STM- 0 time-slot # 3	AIS-C Defect Declared STM- 0 time-slot # 2	Unused		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 3	Unused	R/O	
2	AIS-C Defect Declared – STM-0 Time-Slot # 3	R/O	<ul> <li>AIS - Concatenation Defect Declared - STM-0 Time-Slot # 3: This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is declaring the AIS-C (AIS - Concatenation) defect condition with STM-0 time- slot # 3 (within the incoming AU-4/VC-4 signal).</li> <li>The Receive AU-4 Mapper/VC-4 POH Processor block will declare the AIS-C defect condition, with STM-0 time-slot # 3; if it receives an "All Ones" string; in the H1, H2 bytes (associated with STM-0 time-slot # 3) for 3 consecutive AU-4/VC-4 frames.</li> <li>0 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the AIS-C defect condition with STM-0 time-slot # 3.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AIS-C defect condition with STM-0 time-slot # 3.</li> <li>Note: This bit-field is only valid if the XRT94L33 is receiving and processing an AU-4/VC-4 signal.</li> </ul>
1	AIS-C Defect Declared STM-0 Time-Slot # 2 he produce the produce	at B/O	<ul> <li>AIS - Concatenation Defect Declared - STM-0 Time-Slot # 2</li> <li>This READ-ONLY bit-field indicates whether or not the Receive AU-4 Mapper/VC-4 POH Processor block is declaring the AIS-C (Loss of Pointer - Concatenation) defect condition with STM-0 time-slot # 2 (within the incoming AU-4/VC-4 signal).</li> <li>The Receive AU-4 Mapper/VC-4 POH Processor block will declare the AIS-C defect condition, with STM-0 time-slot # 2; if it receives an "All Ones" string in the H1, H2 bytes (associated with STM-0 time-slot # 2) for 3 consecutive AU-4/VC-4 frames.</li> <li>0 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is NOT currently declaring the AIS-C defect condition with STM-0 time-slot # 2.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AIS-C defect condition with STM-0 time-slot # 2.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AIS-C defect condition with STM-0 time-slot # 2.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AIS-C defect condition with STM-0 time-slot # 2.</li> <li>1 - Indicates that the Receive AU-4 Mapper/VC-4 POH Processor block is currently declaring the AIS-C defect condition with STM-0 time-slot # 2.</li> </ul>
0	Unused	R/O	

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 145: Receive AU-4 Mapper/VC-4 Path – AUTO AIS Control Register (Address Location= 0x11BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit TU-AIS (Down- stream) Upon C2 Byte Unstable	Transmit TU-AIS (Down- stream) Upon UNEQ-P	Transmit TU-AIS (Down- stream) Upon PLM- P	Transmit TU-AIS (Down- stream) Upon Path Trace Message Unstable	Transmit TU-AIS (Down- stream) Upon TIM-P	Transmit TU-AIS (Down- stream) upon LOP-P	Transmit TU-AIS (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

1-

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Unused	R/O	in trut
6	Transmit TU-AIS (Downstream) upon C2 Byte Unstable	R/W	Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the Unstable C2 Byte Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) Indicator via the "downstream" AU-4/VC-4 traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares Unstable C2 Byte defect condition within the "incoming" AU-4/VC-4 data-stream.
			0 - Does not configure the Receive AU-4 Mapper/VC-4 POH Processon block to automatically transmit the TU-AIS indicator (via the "downstream" traffic) whenever it declares "Unstable C2 Byte" defect condition.
	<u>د</u>		1 Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Unstable C2 Byte" defect condition.
	theptol	heet	<b>Wrote:</b> The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
5	Transmit TU-AIS (Downstream) upon UNEQ-P	CR/W	Transmit Path AIS (Downstream, towards the Receive STS- 1/STM-0 Telecom Bus Interface # 0) upon Declaration of the UNEQ-P (Path-Unequipped) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the UNEQ-P defect condition.
			0 – Does not configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the UNEQ-P defect condition.
			1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the UNEQ-P defect condition.



			<b>Note:</b> The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
4	Transmit TU-AIS (Downstream) upon PLM-P	R/W	Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the PLM-P (Path- Payload Label Mismatch) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the PLM-P defect condition.
			0 – Does not configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the PLM-P defect condition.
			1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the PLM-P defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
3	Transmit TU-AIS (Downstream) upon Path Trace Message	R/W	Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the Path-Trace Message Unstable Defect Condition:
	Unstable		This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" AU-4/VC-4 data- stream.
	The atand	is no	0 – Does not configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the "Path Trace Message Unstable" defect condition.
	C and		1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the "Path Trace Message Unstable" defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
2	Transmit TU-AIS (Downstream) upon TIM-P	R/W	Transmit Path AIS (Downstream towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Detection of the TIM-P (Path- Trace Identification Message Mismatch Defect) defect condition:
			This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit a Path AIS (TU-AIS) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime

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			(and for the duration that) it declares the TIM-P defect condition, within the incoming AU-4/VC-4 data-stream.
			0 – Does not configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the TIM-P defect condition.
			1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the TIM-P defect condition, within the incoming AU-4/VC-4 data-stream.
			<b>Note:</b> The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
1	Transmit TU-AIS (Downstream) upon LOP-P	R/W	Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Detection of Loss of Pointer (LOP-P) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) Indicator via the "downstream" traffic (e.g., towards Receive STS-3/STM-1 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming AU-4/VC-4 data-stream.
			0 – Does not configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the LOP-P defect condition. 1 Configures the Receive AU-4 Mapper/VC-4 POH Processor block
		, lot	to automatically transmit the TU-AIS indicator (via the "downstream" traffic towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the LOP-P defect condition.
	oroč	the s	Note The user must also set Bit 0 (Transmit TU-AIS Enable) to "1" to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator, in response to this defect condition.
0	Transmit TU-AIS (Downstream) Enable	R/W	Automatic Transmission of TU-AIS Enable:
	80	0	This READ/WRITE bit-field serves two purposes.
	<i>∕</i> ∕		It permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the Path AIS (TU-AIS) indicator, via the down-stream traffic (e.g., towards Receive STS- 1/STM-0 Telecom Bus Interface # 0), whenever (and for the duration that) it declares either the UNEQ-P, PLM-P, TIM-P, LOP-P, or Path Trace Message Unstable defect conditions.
			It also permits the user to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the TU-AIS defect condition, within the incoming AU-4/VC-4 data-stream.
			0 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to NOT automatically transmit the TU-AIS indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" defect conditions.



1 – Configures the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares any of the "above- mentioned" defect condition.
<b>Note:</b> The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive AU-4 Mapper/VC-4 POH Processor block to automatically transmit the TU-AIS indicator upon detection of a given alarm/defect condition.

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 146: Receive AU-4 Mapper/VC-4 Path – Serial Port Control Register (Address Location= 0x11BF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused				RxPOH_CLOCK_SPEED[7:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxPOH_CLOCK_SPEED[7:0]	R/W	RxPOHClk Output Clock Signal Speed:         These READ/WRITE bit-fields permit the user to specify the frequency of the "RxPOHClk output clock signal.         The formula that relates the contents of these register bits to the "RxPOHClk" frequency is presented below.         FREQ = 19.44 /[20 (RxPOH_CLOCK_SPEED)         Note:       For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz

Note: For STS-3/ST/ RAPOHONE OL 0-304MHz to S



## Table 147: Receive AU-4 Mapper/VC-4 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0x11C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P (via Downstream STS-3c) upon LOP-P	Unused	Transmit AIS-P (via Downstream STS-3cs) upon PLM-P	Unused	Transmit AIS-P (via Downstream STS-3c) upon UNEQ-P	Transmit AIS-P (via Downstream STS-3c) upon TIM-P	Transmit AIS-P (via Downstream STS-3c) upon AIS-P	Unused
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	
7	Transmit AIS-P (via Downstream STS-3c) upon LOP-P	R/W	<ul> <li>Transmit AIS-P (via Downstream STS-3c) upon LOP-P</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit STS-3c. POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-3c signal, anytime the Receive STS-3c POH Processor block declares the LOP-P defect.</li> <li>0 - Does not configure the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect.</li> <li>1 Configures the corresponding Transmit STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect.</li> </ul>
6	Unused	R/O	5
5	Transmit AIS-P (via Downstream STM-05) upon PLM-P	RAW	<ul> <li>Transmit AIS-P (via Downstream STM-0s) upon PLM-P:</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.</li> <li>0 – Does not configure the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.</li> <li>1 – Configures the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.</li> <li>1 – Configures the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.</li> </ul>
4	Unused	R/O	
3	Transmit AIS-P (via Downstream STM-0s) upon UNEQ-P	R/W	Transmit AIS-P (via Downstream STM-0s) upon UNEQ-P: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, anytime the Receive STS- 3c POH Processor block declares the UNEQ-P defect.



			<ul> <li>0 – Does not configure the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.</li> <li>1 – Configures the corresponding Transmit STM-0 POH</li> </ul>
			Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.
2	Transmit AIS-P (via Downstream STM-0s) upon TIM-P	R/W	<b>Transmit AIS-P (via Downstream STM-0s) upon TIM-P:</b> This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, anytime the Receive STS- 3c POH Processor block declares the TIM-P defect.
			0 – Does not configure the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
			1 – Configures the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
1	Transmit AU-AIS (via Downstream STM-0s) upon AU-AIS	R/W	Transmit AU-AIS (via Downstream STM-0s) upon AU-AIS: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, anytime the Receive STS- 3c POH Processor block declares the AIS-P defect.
		orpro	0 Does not configure the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
	roduct	at not	P Configures the corresponding Transmit STM-0 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
0	Unused	R/O	
L	The date of the	>	1



## Table 148: Receive AU-4 Mapper/VC-4 Path – Receive J1 Byte Value Capture Register (Address Location= 0x11D3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	J1_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION		
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	Receive J1 Byte Captured Value[7:0]		
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received AU-4/VC-4 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new J1 byte value.		

## Table 149: Receive AU-4 Mapper/VC-4 Path – Receive B3 Byte Value Capture Register (Address Location= 0x11D7)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0		
			B3_Byte_Capture	ed_Value[7:0]					
R/O	R/O	R/O	R/O	R/0	R/O	R/O	R/O		
0	0	0		0	0	0	0		
	100 10 e0								

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	Receive B3 Byte Captured Value[7:0]
	AUCT OF	NO NO	These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received AU-4/VC-4 frame.
	e prosheet	0	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new B3 byte value.
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Table 150: Receive AU-4 Mapper/VC-4 Path – Receive C2 Byte Value Capture Register (Address Location= 0x11DB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
C2_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION					
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	Received C2 Byte Captured Value[7:0]					
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received AU-4/VC-4 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new C2 byte value.					

## Table 151: Receive AU-4 Mapper/VC-4 Path – Receive GOByte Value Capture Register (Address Location= 0x11DF)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0			
			G1_Byte_Captu	ired_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	<u> </u>	0	0	0			

BIT NUMBER	ΝΑΜΕ	TYPE	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	Receive G1 Byte Captured Value[7:0]
	e product	are	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new G1 byte value.
	Theatandn	*	



## Table 152: Receive AU-4 Mapper/VC-4 Path – Receive F2 Byte Value Capture Register (Address Location=0x11E3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	Receive F2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received AU-4/VC-4 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new F2 byte value.

## Table 153: Receive AU-4 Mapper/VC-4 Path – Receive H4 Byte Value Capture Register (Address Location=0x11E7)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0			
	H4_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/0	R/O	R/O	R/O			
0	0	0	000	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[70]	R/O	Receive H4 Byte Captured Value[7:0]
	uct at		These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received AU-4/VC-4 frame.
	prosheet	0	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new H4 byte value.
	The stand me		

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 154: Receive AU-4 Mapper/VC-4 Path - Receive Z3 Byte Value Capture Register (Address Location=0x11EB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Z3_Byte_Captu	red_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION					
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Receive Z3 Byte Captured Value[7:0]					
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received AU-4/VC-4 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z3 byte value.					
	and it a							

#### Table 155: Receive AU-4 Mapper/VC-4 Path – Receive Z4 (K3) Byte Value Capture Register (Address Location= 0x11EF)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0				
Z4(K3)_Byte_Captured_Value[7:0]											
R/O	R/O	R/O	R/O 🎽	7 R/0	R/O	R/O	R/O				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	T	YPE	8	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[7:0]		8 0 8	Th (K3 fra Th fra	ceive Z4 (K3) Byte Value Captured Value[7:0] ese READ-ONLY bit-fields contain the value of the Z4 3) byte, within the most recently received AU-4/VC-4 me. is particular value is stored in this register for one SONET me period. During the next SONET frame period, this lue will be overridden with a new Z4 (K3) byte value.
	J. 93 19.				



Table 156: Receive AU-4 Mapper/VC-4 Path – Receive Z5 Byte Value Capture Register (Address Location= 0x11F3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Receive Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received AU-4/VC-4 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.

Lang Las particular value is frame period. During the will be overridden with a the ove



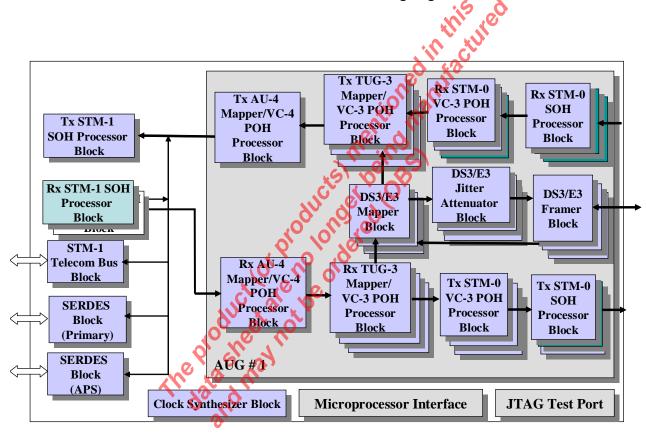
#### 1.6 REDUNDANT RECEIVE STM-1 SOH PROCESSOR BLOCK

The register map for the Redundant Receive STM-1 SOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Redundant Receive STM-1 SOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Redundant Receive STM-1 SOH Processor Block "highlighted" is presented below in Figure 3.

**NOTE:** The Redundant Receive STM-1 SOH Processor block is only active if the user has configured the XRT94L33 device to support Line APS Applications.

## Figure 3: Illustration of the Functional Block Diagram of the XRT94L33, with the Redundant Receive STM-1 SOH Processor Block "High-lighted".





#### 1.6.1 REDUNDANT RECEIVE STM-1 SOH PROCESSOR BLOCK REGISTER

#### Table 157: Redundant Receive STM-1 SOH Processor Block Control Register – Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x1600 - 0x1702	Reserved	
0x1703	Redundant Receive STM-1 Section Control Register – Byte 0	0x00
0x1704 – 0x1705	Reserved	0x00
0x1706	Redundant Receive STM-1 Section Status Register – Byte 1	0x00
0x1707	Redundant Receive STM-1 Section Status Register – Byte	0x02
0x1708	Reserved	0x00
0x1709	Redundant Receive STM-1 Section Interrupt Status Register – Byte 2	0x00
0x170A	Redundant Receive STM Section Interrupt Status Register – Byte 1	0x00
0x170B	Redundant Receive STM-1 Section Interrupt Status Register – Byte 0	0x00
0x170C	Reserved	0x00
0x170D	Redundant Receive STM-1 Section Interrupt Enable Register – Byte 2	0x00
0x170E	Redundant Receive STM-1 Section Interrupt Enable Register – Byte 1	0x00
0x170F	Redundant Receive STM-1 Section Interrupt Enable Register – Byte 0	0x00
0x1710	Redundant Receive STM-1 Section B1 Error Count – Byte 3	0x00
0x1711	Redundant Receive STM-1 Section B1 Error Count – Byte 2	0x00
0x1712	Redundant Receive STM-1 Section B1 Error Count – Byte 1	0x00
0x1713	Redundant Receive STM-1 Section B1 Error Count – Byte 0	0x00
0x1714 🔗	Redundant Receive STM-1 Section B2 Error Count – Byte 3	0x00
0x1715	Redundant Receive STM-1 Section B2 Error Count – Byte 2	0x00
0x1716	Redundant Receive STM-1 Section B2 Error Count – Byte 1	0x00
0x1717	Redundant Receive STM-1 Section B2 Error Count – Byte 0	0x00
0x1718	Redundant Receive STM-1 Section MS-REI Error Count – Byte 3	0x00
0x1719	Redundant Receive STM-1 Section MS-REI Error Count – Byte 2	0x00
0x171A	Redundant Receive STM-1 Section MS-REI Error Count – Byte 1	0x00



ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x171B	Redundant Receive STM-1 Section MS-REI Error Count – Byte 0	0x00
0x171C	Reserved	0x00
0x171D - 0x171E	Reserved	0x00
0x171F	Redundant Receive STM-1 Section K1 Byte Value	0x00
0x1720 – 0x1722	Reserved	0x00
0x1723	Redundant Receive STM-1 Section K2 Byte Value	0x00
0x1724 – 0x1726	Reserved	0x00
0x1727	Redundant Receive STM-1 Section S1 Byte Value	0x00
0x1728 – 0x172A	Reserved	0x00
0x172B	Redundant Receive STM-1 Section In-Sync Threshold	0x00
0x172C, 0x172D	Reserved	0x00
0x172E	Redundant Receive STM-1 Section - LOS Threshold Value - MSB	0xFF
0x172F	Redundant Receive STM-1 Section - LOS Threshold Value - LSB	0xFF
0x1730	Reserved a contract of the con	0x00
0x1731	Redundant Receive STM-1 Section – SF Set Monitor Interval – Byte 2	0x00
0x1732	Redundant Receive STM-1 Section – SF Set Monitor Interval – Byte 1	0x00
0x1733	Redundant Receive STM-1 Section – SF Set Monitor	0x00
0x1734 – 0x1735	Reserved	0x00
0x1736	Redundant Receive STM-1 Section – SF Set Threshold – Byte 1	0x00
0x1737	Redundant Receive STM-1 Section – SF Set Threshold – Byte 0	0x00
0x1738, 0x1739	Reserved	0x00
0x173A	Redundant Receive STM-1 Section – SF Clear Threshold – Byte 1	0x00
0x173B	Redundant Receive STM-1 Section – SF Clear Threshold – Byte 0	0x00
0x173C	Reserved	0x00
0x173D	Redundant Receive STM-1 Section – SD Set Monitor Interval – Byte 2	0x00
0x173E	Redundant Receive STM-1 Section – SD Set Monitor Interval – Byte 1	0x00



### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Address Location	REGISTER NAME	DEFAULT VALUES
0x173F	Redundant Receive STM-1 Section – SD Set Monitor Interval – Byte 0	0x00
0x1740, 0x1741	Reserved	0x00
0x1742	Redundant Receive STM-1 Section – SD Set Threshold – Byte 1	0x00
0x1743	Redundant Receive STM-1 Section – SD Set Threshold – Byte 0	0x00
0x1744, 0x1745	Reserved	0x00
0x1746	Redundant Receive STM-1 Section – SD Clear Threshold – Byte 1	0x00
0x1747	Redundant Receive STM-1 Section - SD Clear Threshold - Byte 0	0x00
0x1748 – 0x174A	Reserved	0x00
0x174B	Redundant Receive STM-1 Section Force SEF Condition	0x00
0x174C, 0x174E	Reserved	0x00
0x174F	Redundant Receive STM-to Section – Receive J0 Trace Buffer Control	0x00
0x1750, 0x1751	Reserved	0x00
0x1752	Redundant Receive STM-1 Section – SD Burst Error Count Tolerance Byte 1	0x00
0x1753	Redundant Receive STM-1 Section – SD Burst Error Count Tolerance – Byte 0	0x00
0x1754, 0x1755	Reserved	0x00
0x1756	Redundant Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 1	0x00
0x1757	Redundant Receive STM-1 Section – SF Burst Error Count Tolerance – Byte 0	0x00
0x1758	Reserved	0x00
0x1759	Redundant Receive STM-1 Section –Receive SD Clear Monitor Interval – Byte 2	0xFF
0x175A	Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x175B	Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x175C	Reserved	0x00
0x175D	Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x175E	Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 1	0xFF

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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Address Location	REGISTER NAME	DEFAULT VALUE
0x5F 0x175F	Redundant Receive STM-1 Section – Receive SF Clear Monitor – Byte 0	0xFF
0x60 – 0x62 0x1760 – 0x1762	Reserved	0x00
0x63 0x1763	Redundant Receive STM-1 Section – Auto AIS Control Register	0x00
0x64 – 0x66 0x1764 – 0x1766	Reserved	0x00
0x67 0x1767	Redundant Receive STM-1 Section – Serial Port Control Register	0x00
0x68 – 0x6A 0x1768 – 0x176A	Reserved	0x00
0x6B 0x176B	Redundant Receive STM-1 Section Auto AIS (in Downstream STM-0s) Control Register	0x000
0x6C – 0x79 0x176C – 0x1779	Reserved	
0x7A 0x117A	Redundant Receive STM-1 Section SOH Capture Indirect Address	0x00
0x7B 0x117B	Redundant Receive STM-1 Section SOH Capture Indirect Address	0x00
0x7C 0x117C	Redundant Receive STM-1 Section – SOH Capture Indirect Data	0x00
0x7D 0x117D	Redundant Receive STM-7 Section – SOH Capture Indirect Data	0x00
0x7E 0x117E	Redundant Receive STM-1 Section – SOH Capture Indirect	0x00
0x7F 0x117F	Redundant Receive STM-1 Section – SOH Capture Indirect	0x00
0x80 – 0xFF 🛛 🚺	Reserved	0x00



### 1.6.2 REDUNDANT RECEIVE STM-1 SOH PROCESSOR BLOCK REGISTER DESCRIPTION

### Table 158: Redundant Receive STM-1 Section Control Register – Byte 0 (Address Location= 0x1703)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-N OH Extract	SF Detect Condition Detect Enable	SD Detect Condition Defect Enable	Descramble Disable	Unused	MS-REI Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	STS-N OH	R/W	STS-N Overhead Extract (Revision C Silicon Only):
	Extract		This READ/WRITE bit-field permits the user to configure the RxSOH output port to output the SOH for all lower tributary STM-0s within the incoming STM-1 signal.
			0 – Disables this feature. In this mode, the RxSOH output port will only output the SOH for the first STM-0 within the incoming STM-1 signal.
			1 – Enables this feature.
6	SF Defect	R/W	Signal Failure (SF) Defect Condition Detect Enable:
	Condition Detect Enable		This READ/WRITE bit-field permits the user to enable or disable SF Defect Declaration and Clearance by the Redundant Receive STM-1 SOH Processor Block, as described below.
			0 – Configures the Redundant Receive STM-1 SOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified" SF defect declaration and clearance criteria.
			1 – Configures the Redundant Receive STM-1 SOH Processor block to declare and clear the SF defect condition per the "user-specified" SF defect declaration and clearance" critieria.
	or	duret	<b>NOTE:</b> The user must set this bit-field to "1" in order to permit the Redundant Receive STM-1 SOH Processor block to declare and clear the SF defect condition.
5	SD Defect	R/W	Signal Degrade (SD) Defect Condition Detect Enable:
	Condition Detect Enable	andli	This READ/WRITE bit-field permits the user to enable or disable SD Defect Declaration and Clearance by the Redundant Receive STM-1 SOH Processor Block as described below.
			0 – Configures the Redundant Receive STM-1 SOH Processro block to NOT declare nor clear the SD defect condition per the "user-specified" SD defect declaration and clearance criteria.
			1 – Configures the Receive STM-1 SOH Processor block to declare and clear the SD defect condition per the "user-specified" SD defect declaration and clearance" criteria.
			<b>NOTE:</b> The user must set this bit-field to "1" in order to permit the Redundant Receive STM-1 SOH Processro block to declare and clear the SD defect condition,
4	Descramble	R/W	De-Scramble Disable:
	Disable		This READ/WRITE bit-field permits the user to either enable or disable de- scrambling by the Redundant Receive STM-1 SOH Processor block.

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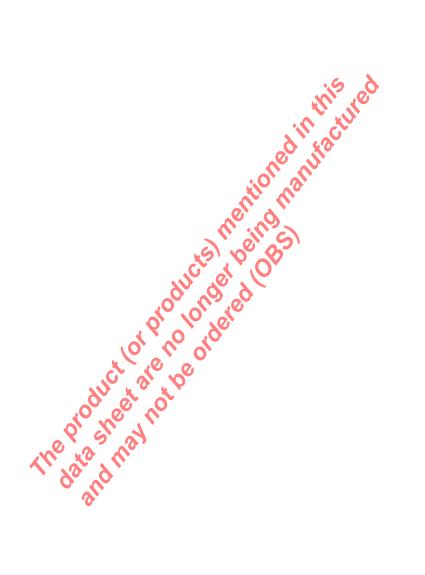
			0 – De-Scrambling is enabled.
			1 – De-Scrambling is disabled.
3	Unused	R/O	
2	MS-REI Error Type	R/W	MS-REI (Line – Remote Error Indicator) Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STM-1 SOH Processor block will count (or tally) MS-REI events, for Performance Monitoring purposes. The user can configure the Redundant Receive STM-1 SOH Processor block to increment MS-REI events on either a "per-bit" or "per-frame" basis. If the user configures the Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment the "Redundant Receive STM-1 SOH Processor block to increment MS-REI event Count" registers by the contents within the M1 byte of the incoming STM-1 data-stream
			If the user configures the Redundant Receive STM-1 SOH Processor block to increment MS-REI events on a "per-frame" basis, then it will increment the "Redundant Receive STM-1 Section MS-REI Event Count" register each time it receives an STM-1 frame, in which the M1 byte is set to a "non-zero" value.
			0 – Configures the Redundant Receive STM-1 SOH Processor block to count or tally MS-REI events on a per-bit basis.
			1 – Configures the Redundant Receive STM-1 SOH Processor block to count or tally MS-RELevents on a per-frame basis.
1	B2 Error Type	R/W	B2 Error Type:
		, c	This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STM-1 SOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Redundant Receive STM-1 SOH Processor block to increment B2 byte errors on either a "per-bit" of "per-frame" basis. If the user configures the Redundant Receive STM-1 SOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the Redundant Receive STM-1 SOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the Redundant Receive STM-1 Section - B2 Byte Error Count" register by the number of bits (within each of the three B2 byte values) that is in error.
	a the	produ	If the user configures the Redundant Receive STM-1 SOH Processor block to increment B2 byte errors on a "per-frame" basis, then it will increment the "Redundant Receive STM-1 Section – B2 Byte Error Count" Register, each time it receives an STM-1 frame that contains at least one erred B2 byte.
		93,49	0 – Configures the Redundant Receive STM-1 SOH Processor block to count B2 byte errors on a "per-bit" basis.
		.0	1 – Configures the Redundant Receive STM-1 SOH Processor block to count B2 byte errors on a "per-frame" basis.
0	B1 Error Type	R/W	B1 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STM-1 SOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Redundant Receive STM-1 SOH Processor block to increment B1 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Redundant Receive STM-1 SOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 SOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 Sot Processor block to increment B1 byte errors on a byte errors on a "per-bit" basis, then it will increment the "Redundant Receive STM-1 Section - B1 Byte Error Count" register by the number of bits (within the B1 byte value) that is in error.
			If the user configures the Redundant Receive STM-1 SOH Processor block to increment B1 byte errors on a "per-frame" basis, then it will increment the "Redundant Receive STM-1 Section – B1 Byte Error Count" Register



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each time it receives an STM-1 frame that contains an erred B1 byte.
0 – Configures the Redundant Receive STM-1 SOH Processor block to count B1 byte errors on a "per-bit" basis.
1 – Configures the Redundant Receive STM-1 SOH Processor block to count B2 byte errors on a "per-frame" basis.



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### Table 159: Redundant Receive STM-1 Section Status Register – Byte 1 (Address Location= 0x1706)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unused							
							Declared	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	MS-AIS	R/O	MS-AIS Defect Declared:
Defect Declared		This READ-ONLY bit-field indicates whether of not the Redundant Receive STM-1 SOH Processor block is currently declaring the MS-AIS (Line AIS) defect condition within the incoming STM-1 data stream. The Redundant Receive STM-1 SOH Processon block will declare the MS-AIS defect condition within the incoming STM-1 data-stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STM-1 frames.	
			0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the MS-AIS defect condition.
			1 – Indicates that the Redundant Receive STM-1 SOH Processor block is currently declaring the MS-AIS defect condition.
	the	or of use	currently declaring the MS-AIS defect condition.



### Table 160: Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
MS-RDI Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	MS-RDI	R/O	MS-RDI (Line Remote Defect Indicator) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STM- 1 SOH Processor block is currently declaring the MS-RDI defect condition within the incoming STM-1 signal. The Redundant Receive STM-1 SOH Processor block will declare the MS-RDI defect condition whenever it determines that bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern within 5 consecutive incoming STM-1 frames. 0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT
			currently declaring the MS RDI defect condition. 1 – Indicates that the Redundant Receive STM-1 SOH Processor block is
			currently declaring the MS RDI defect condition.
6	S1 Byte Unstable Defect Declared	R/O	<ul> <li>S1 Byte Unstable Defect Declared:</li> <li>This READ-ONLY bit-field indicates whether or not the Redundant Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Redundant Receive STM-1 SOH Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable" defect Counter" reaches the value 32. The Redundant Receive STM-1 SOH Processor block will increment the "S1 Byte Unstable Counter" each time that it receives an STM-1 frame that contains an S1 byte that differs from the previously received S1 byte. The Redundant Receive STM-1 SOH Processor block will clear the contents of the "S1 Byte Unstable Counter" is cleared to "0" whenever it receives the same S1 byte for 8 consecutive STM-1 frames.</li> <li>Ø – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the "S1 Byte Unstable" Defect Condition.</li> <li>Ø – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the "S1 Byte Unstable" Defect Condition.</li> </ul>
5	K1, K2 Byte	R/O	K1, K2 Byte Unstable Defect Declared:
	Unstable Defect Declared	<i>.</i>	This READ-ONLY bit-field indicates whether or not the Redundant Receive STM- 1 SOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Redundant Receive STM-1 SOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever it fails to receive the same set of K1, K2 bytes, in 12 consecutive STM-1 frames. The Redundant Receive STM-1 SOH Processor block will clear the "K1, K2 Byte Unstable" defect condition whenever it receives a given set of K1, K2 byte values within three consecutive STM-1 frames.
			0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the K1, K2 Unstable Defect Condition.
			1 – Indicates that the Redundant Receive STM-1 SOH Processor block is currently declaring the K1, K2 Unstable Defect Condition.
4	SF Defect	R/O	SF (Signal Failure) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STM-

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



			<ol> <li>SOH Processor block is currently declaring the SF defect condition. The Redundant Receive STM-1 SOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified" B2 Byte Error" threshold.</li> <li>Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the SF Defect condition.</li> <li>This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold.</li> <li>Indicates that the Redundant Receive STM-1 SOH Processor block is</li> </ol>
			currently declaring the SF Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a
			given interval of time) does exceed the "SF Defect Declaration" threshold.
3	SD Defect	R/O	SD (Signal Degrade) Defect Declared: 🏑 👌
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STM- 1 SOH Processor block is currently declaring the SD defect condition. The Redundant Receive STM-1 SOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a "user-specified" period of time) exceeds a certain "user-specified" B2 Byte Error" threshold.
			0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the SD Defect condition.
			This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SD Defect Declaration" threshold.
			<ol> <li>Indicates that the Redundant Receive STM-1 SOH Processor block is currently declaring the SD Detect condition.</li> </ol>
			This bit is set to "d" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Defect Declared:
	Defect Declared	oro	This READ ONLY bit-field indicates whether or not the Redundant Receive STM- 1 SOH Processor block is currently declaring the LOF defect condition. The Redundant Receive STM-1 SOH Processor block will declare the LOF defect condition, if it has been declaring the SEF (Severely Errored Frame) defect condition for 3ms (or 24 SONET frame periods).
		0 7	9 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the LOF defect condition.
	K	. 931	1 – Indicates that the Redundant Receive STM-1 SOH Processor block is currently declaring the LOF defect condition.
1	SEF	R/O	SEF (Severely Errored Frame) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STM- 1 SOH Processor block is currently declaring the SEF defect condition. The Redundant Receive STM-1 SOH Processor block will declare the SEF defect condition, if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Redundant Receive STM-1 Section – In-Sync Threshold Value Register (Address Location= 0x172B) are met. 0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT
			currently declaring the SEF defect condition. 1 – Indicates that the Redundant Receive STM-1 SOH Processor block is
			currently declaring the SEF defect condition.
0	LOS Defect	R/O	LOS (Loss of Signal) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STM-



Declared	1 SOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Redundant Receive STM-1 SOH Processor block will declare the LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STM-1 data stream.
	<b>Note:</b> The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Redundant Receive STM-1 Section – LOS Threshold Value" Register (Address Location= 0x172E and 0x172F).
	0 – Indicates that the Redundant Receive STM-1 SOH Processor block is NOT currently declaring the LOS defect condition.
	1 – Indicates that the Redundant Receive STM-1 SOH Processor block is currently declaring the LOS defect condition.

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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 161: Redundant Receive STM-1 Section Interrupt Status Register – Byte 2 (Address Location= 0x1709)

Віт 7	Віт 6	Віт 5	BIT 5 BIT 4 BIT 3 BIT 2		Віт 1	Віт 0	
		Change of MS- AIS	Change of MS- RDI				
		Defect Condition Interrupt Status	Defect Condition Interrupt Status				
R/O	R/O R/O R/O R/O R/O				RUR	RUR	
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	is so
1	Change of MS-	RUR	Change of MS-AIS (Line AIS) Defect Condition Interrupt Status:
	AIS Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of MS-AIS Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			Whenever the Redundant Receive STM-1 SOH Processor block declares the MS-AIS defect condition
			Whenever the Redundant Receive STM-1 SOH Processor block clears the MS-AIS defect condition
			0 – Indicates that the "Change of MS-AIS Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of MS-AIS Defect Condition" interrupt has occurred since the last read of this register.
		du	Note: The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the MS-AIS defect condition by reading the contents of Bit 0 (MS-AIS Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 1" (Address Location= 0x1706).
0	Change of MS-RDI Defect	RUR	Change of MS-RDI (Line - Remote Defect Indicator) Defect Condition Interrupt Status:
	Condition Interrupt Status	M re	This RESET-upon-READ bit-field indicates whether or not the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			• Whenever the Redundant Receive STM-1 SOH Processor block declares the MS-RDI defect condition.
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the MS-RDI defect condition
			0 – Indicates that the "Change of MS-RDI Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the MS-RDI defect condition by reading out the state of Bit 7 (MS-RDI Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 0" (Address Location = 0x1707).



# Table 162: Redundant Receive STM-1 Section Interrupt Status Register – Byte 1 (Address Location = 0x170A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status		Unused		Receive SOH CAP DONE Interrupt Status	Change in K1, K2 Bytes Unstable Defect Condition Interrupt Status	NEW K1K2 Byte Value Interrupt Status	
RUR	RUR	R/O	R/O	R/O	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	
	inis ed							

1			
BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	<ul> <li>New S1 Byte Value Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate the "New S1 Byte Value" Interrupt anytime it has "accepted" a new S1 byte, from the incoming STM-1 data-stream.</li> <li>0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register.</li> <li>1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register.</li> <li>Note: The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Redundant Receive STM-1 Section S1 Value" register (Address Location= 0x1727).</li> </ul>
6	Change in S1 Byte Unstable Defect Condition Interrupt Status	RUR	<ul> <li>Change in S1 Byte Unstable Defect Condition Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block declares the "S1 Byte Unstable" defect condition.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block clears the "S1 Byte Unstable" defect condition.</li> <li>Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>I – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has not occurred since the last read of this register.</li> <li>Note: The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable" defect condition the "Redundant Receive STM-1 SOH Processor block is currently declaring the "S1 Byte Unstable" defect condition.</li> </ul>
5 – 3		R/O	
2	Receive SOH CAP DONE	RUR	Receive SOH Capture DONE – Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether the "Receive SOH Data



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			Capture" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Redundant Receive STM-1 SOH Processor block will generate an interrupt anytime it has captured the last SOH byte into the Capture Buffer.
			<b>Note:</b> Once the SOH (of a given STM-1 frame) has been captured and loaded into the "Receive SOH Capture" buffer, it will remain there for one SONET frame period.
			0 – Indicates that the "Receive SOH Data Capture" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Receive SOH Data Capture" Interrupt has occurred since the last read of this register.
1	Change in K1,	RUR	Change of K1, K2 Byte Unstable Defect Condition Interrupt Status:
	K2 Byte Unstable Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Redundant Receive STM-1 SOH Processor block declares the "K1, K2 Byte Unstable Defect" condition.
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the "K1, K2 Byte Unstable" defect condition.
			0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the "K1, K2 Unstable Defect Condition" by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Redundant Receive STM-1 Section Status Register – Byte 0" (Address Location = 0x1707).
0	NEW K1, K2	RUR	New K1, K2 Byte Value Interrupt Status:
	Byte Value Interrupt Status	produ	This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt whenever it has "accepted" a new set of K1, K2 byte values from the incoming STM-1 data-stream.
		00° 2	number of the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
		ð`	1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can obtain the contents of the new K1 byte by reading out the contents of the "Redundant Receive STM-1 Section K1 Byte Value" Register (Address Location= 0x171F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Redundant Receive STM-1 Section K2 Byte Value" Register (Address Location= 0x1723).



# Table 163: Redundant Receive STM-1 Section Interrupt Status Register – Byte 0 (Address Location= 0x170B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in SF Defect Condition Interrupt Status	Change in SD Defect Condition Interrupt Status	Detection of MS-REI Event Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Condition Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION		
7	Change in SF	RUR	Change of Signal Failure (SF) Defect Condition Interrupt Status:		
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.		
			• Whenever the Redundant Receive STM-1 SOH Processor block declares the SF defect condition.		
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the SF defect condition.		
			0 – Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register.		
			1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register.		
		AUC'S	Note: The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the "SF" defect condition by reading out the state of Bit 4 (SF Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707).		
6	Change of SD	RUR	Change of Signal Degrade (SD) Defect Condition Interrupt Status:		
	Defect Condition Interrupt Status	ashra	ana	adma	This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
		311-	• Whenever the Redundant Receive STM-1 SOH Processor block declares the SD Defect condition.		
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the SD Defect condition.		
		0 – Indicates that the "Change of SD Defect occurred since the last read of this register.	0 – Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register.		
			1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register.		
			<b>Note:</b> The user can determine the whether or not the Redundant Receive STM-1 SOH Processor block is currently declaring the SD defect condition by reading out the state of Bit 3 (SD Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707).		
5	Detection of MS-	RUR	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt		

**REI Event** 

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Status:

	Interrupt Status		<ul> <li>This RESET-upon-READ bit-field indicates whether or not the "Declaration of MS-REI Event" Interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt anytime it detects an MS-REI event within the incoming STM-1 data-stream.</li> <li>0 - Indicates that the "Detection of MS-REI Event" Interrupt has NOT occurred since the last read of this register.</li> <li>1 - Indicates that the "Detection of MS-REI Event" Interrupt has occurred</li> </ul>
		0.10	since the last read of this register.
4	Detection of B2 Byte Error Interrupt Status	RUR	<ul> <li>Detection of B2 Byte Error Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.</li> <li>The Redundant Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STM-1 datastream.</li> <li>0 – Indicates that the "Detection of B2 Byte Error Interrupt" has NOT occurred since the last read of this register.</li> </ul>
			1 – Indicates that the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.
3	Detection of B1 Byte Error Interrupt Status	RUR	<ul> <li>Detection of B1 Byte Error Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt anytime it detects a B1 byte within the incoming STM-1 datastream.</li> <li>0 - Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register.</li> <li>1 Indicates that the "Detection of B1 Byte Error Interrupt" has occurred</li> </ul>
2	Change of LOF	RUR	Since the last lead of this register Change of Loss of Frame (LOF) Defect Condition Interrupt Status:
L	Defect Condition Interrupt Status	or star	<ul> <li>This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block declares the LOF defect condition.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block clears the LOF defect condition.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block clears the LOF defect condition.</li> <li>O – Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register.</li> </ul>
			<ul> <li>1 – Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register.</li> </ul>
			Note: The user can determine whether the Redundant Receive STM-1 SOH Processor block is currenly declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707).
1	Change of SEF Defect Condition	RUR	Change of SEF Defect Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF" Defect Condition Interrupt has occurred since the last read of this



			register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Redundant Receive STM-1 SOH Processor block declares the SEF defect condition.
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the SEF defect condition.
			0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine whether or not the Redundant Receive STM-1 SOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707).
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STM-1 SOH Processor block will generate this interrupt in response to either of the following events.
			Whenever the Redundant Receive STM-1 SOH Processor block declares the LOS defect condition.
			Whenever the Redundant Receive STM-1 SOH Processor block clears the LOS defect condition
			0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register.
		duct	Note: The user can determine whether the Redundant Receive STM-1 SOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Redundant Receive STM-1 Section Status Register – Byte 0 (Address Location= 0x1707).
	Thela	andma	<b>Y</b>

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 164: Redundant Receive STM-1 Section Interrupt Enable Register – Byte 2 (Address Location= 0x170D)

Віт 7	Віт 6	Віт 5	Віт 5 Віт 4 Віт 3 Віт 2		Віт 1	Віт 0	
		Change of MS- AIS Defect Condition Interrupt Enable	Change of MS- RDI Defect Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 2	Unused	R/O	this ted
1	Change of MS- AIS Defect Condition Interrupt Enable	R/W	<ul> <li>Change of MS-AIS (Line AIS) Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change of MS-AIS Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block declares the "MS-AIS" defect condition.</li> </ul>
			<ul> <li>Whenever the Redundant Receive STM-1 SOH Processor block clears the "MS-AIS" defect condition?</li> <li>0 – Disables the "Change of MS-AIS Defect Condition" Interrupt.</li> <li>1 – Enables the "Change of MS-AIS Defect Condition" Interrupt.</li> <li>Note: The user can determine if the Redundant Receive STM-1 SOH Processor block is currently declaring the MS-AIS defect condition by reading out the state of Bit 0 (MS-AIS Defect Condition Status Register – Byte 1" (Address Location= 0x1706).</li> </ul>
0	Change of MS- RDI Defect Condition Interrupt Enable	Rai and	<ul> <li>Change of MS-RDI (Line Remote Defect Indicator) Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the Change of MS-RDI Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block declares the "MS-RDI" defect condition.</li> <li>Whenever the Redundant Receive STM-1 SOH Processor block clears the "MS-RDI" defect condition.</li> <li>O – Disables the "Change of MS-RDI Defect Condition" Interrupt.</li> <li>1 – Enables the "Change of MS-RDI Defect Condition" Interrupt.</li> </ul>



# Table 165: Redundant Receive STM-1 Section Interrupt Enable Register – Byte 1 (Address Location= 0x170E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Unused			Receive SOH CAP DONE Interrupt Enable	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	NEW K1K2 Byte Value Interrupt Enable
R/W	R/W	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7	New S1 Byte	R/W	New S1 Byte Value Interrupt Enable
	Value Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Redundant Receive STM-1 SOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Redundant Receive STM-1 SOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STM-1 frames.
			0 – Disables the "New \$1 Byte Value" Interrupt.
			1 – Enables the "New S1-Byte Value" Interrupt.
6	Change in S1	R/W	Change in S1 Byte Unstable Defect Condition Interrupt Enable:
	Unstable State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Redundant Receive STM-1 SOH Processor block will generate an interrupt in response to either of the following conditions.
		JUC'	• Whenever the Redundant Receive STM-1 SOH Processor block declares the "S1 Byte Unstable" defect condition.
	<i>.</i>	10 ne	Whenever the Redundant Receive STM-1 SOH Processor block clears the "S1 Byte Unstable" defect condition.
	O C	5	Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
			1 – Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5 - 3	Unused	R/O	
2	Receive SOH	R/W	Receive SOH Capture DONE – Interrupt Enable:
	CAP DONE Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive SOH Data Capture" interrupt, within the Redundant Receive STM-1 SOH Processor Block.
			If this interrupt is enabled, then the Redundant Receive STM-1 SOH Processor block will generate an interrupt anytime it has captured the last SOH byte into the Capture Buffer.
			<b>Note:</b> Once the SOH (of a given STM-1 frame) has been captured and loaded into the "Receive SOH Capture" buffer, it will remain there for one SONET frame period.
			0 – Disables the "Receive SOH Capture" Interrupt.
			1 – Enables the "Receive SOH Capture" Interrupt.



	r		
1	Change in K1,	R/W	Change of K1, K2 Byte Unstable Defect Condition Interrupt Enable:
	K2 Byte Unstable Defect Condition Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Redundant Receive STM-1 SOH Processor block will generate an Interrupt in response to either of the following events.
	Enable		• Whenever the Redundant Receive STM-1 SOH Processor block declares the "K1, K2 Byte Unstable defect" condition.
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the "K1, K2 Byte Unstable defect" condition.
			0 – Disables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
			1 – Enables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
0	New K1K2 Byte Interrupt Enable	R/W	New K1, K2 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Redundant Receive STM-1 SOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Redundant Receive STM-1 SOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STM-1 frames. 0 – Disables the "New K1, K2 Byte Value" Interrupt. 1 – Enables the "New K1, K2 Byte Value" Interrupt.



# Table 166: Redundant Receive STM-1 Section Interrupt Status Register – Byte 0 (Address Location= 0x170F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of MS-REI Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Change of SF	R/W	Change of Signal Failure (SF) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events.
			<ul> <li>Whenever the Redundant Receive STM-1 SOH Processor block declares the SF defect condition.</li> </ul>
			Whenever the Redundant Receive STM-1 SOH Processor block clears the SF defect condition.
			0 – Disables the "Change of SF Defect Condition Interrupt".
			1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD	R/W	Charge of Signal Degrade (SD) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable	, ch	This READ/WRITE bit-field permits the user to either enable or disable the Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events.
		due	• Whenever the Redundant Receive STM-1 SOH Processor block declares the SD defect condition.
	P	She	Whenever the Redundant Receive STM-1 SOH Processor block clears the SD defect condition.
		6.4	0 – Disables the "Change of SD Defect Condition Interrupt".
	. 9.0	no	1 – Enables the "Change of SD Defect Condition Interrupt".
5	Detection of MS- REI Event	R/W	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Line – MS-REI Event" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STM-1 SOH Processor block detects an "MS-REI" event, within the incoming STM-1 data-stream.
			0 – Disables the "Detection of MS-REI Event" Interrupt.
			1 – Enables the "Detection of MS-REI Event" Interrupt.
4	Detection of B2	R/W	Detection of B2 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive



			STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream.
			0 – Disables the "Detection of B2 Byte Error Interrupt".
			1 – Enables the "Detection of B2 Byte Error Interrupt".
3	Detection of B1	R/W	Detection of B1 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STM-1 SOH Processor block detects a B1 byte error within the incoming STM-1 data-stream.
			0 – Disables the "Detection of B1 Byte Error Interrupt".
			1 – Enables the "Detection of B1 Byte Error Interrupt".
2	Change of LOF	R/W	Change of Loss of Frame (LOF) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			Whenever the Redundant Receive STM-1 SOH Processor block declares the "LOF" defect condition
			Whenever the Redundant Receive STM-1 SOH Processor clears the     "LOF" defect condition.
			0 – Disables the "Change of LOF Defect Condition Interrupt.
			1 – Enables the "Change of LOF Defect Condition" Interrupt.
1	Change of SEF Defect Condition Interrupt Enable	R/W	Change of SEF Defect Condition Interrupt Enable: This READ/WRITE bit field permits the user to either enable or disable the "Change of SEF Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
		di	Whenever the Redundant Receive STM-1 SOH Processor block declares the "SEF" defect condition.
		Qr e	Whenever the Redundant Receive STM-1 SOH Processor block clears the "SEF" defect condition.
		xo.	PDisables the "Change of SEF Defect Condition Interrupt".
		3	1 – Enables the "Change of SEF Defect Condition Interrupt".
0	Change of LOS	R/W	Change of Loss of Signal (LOS) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			• Whenever the Redundant Receive STM-1 SOH Processor block declares the "LOF" defect condition.
			• Whenever the Redundant Receive STM-1 SOH Processor block clears the "LOF" defect condition.
			0 – Disables the "Change of LOF Defect Condition Interrupt.
			1 – Enables the "Change of LOF Defect Condition" Interrupt.
	1		



Table 167: Redundant Receive STM-1 Section – B1 Byte Error Count Register – Byte 3 (Address Location= 0x1710)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B1_Byte_Error_Count[31:24]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

Bit Number	NAME	Түре	DESCRIPTION				
7 - 0	B1_Byte_Error_	RUR	B1 Byte Error Count – MSB:				
	Count[31:24]		This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B1 byte error.				
			Note:				
		count B1 Byte Errors on a "per bit" basis, then it will increment th counter by the number of bits within the B1 byte (of each incoming frame) that are in error.	1. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 Byte Errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.				
			2. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte error on a "per-frame" basis, then it will increment this 32-bit counter each time that receives an STM-1 frame that contains an erred B1 byte.				



Table 168: Redundant Receive STM-1 Section – B1 Byte Error Count Register – Byte 2 (Address Location= 0x1711)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B1_Byte_Error_Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B1_Byte	RUR	B1 Byte Error Count (Bits 23 through 16):
	Error_Count [23:16]		This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits within the B1 byte (of each incoming STM-1 frame) that are in error.
			2. If the Redundant Receive STM-1 SOH Processro block is configured to count B1 byte errors on "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-1 frame that contains an erred B1 byte.
	the	Produ datand	counter each time that it receives an STM-1 frame that contains an erred B1 byte.
		or sur	



Table 169: Redundant Receive STM-1 Section – B1 Byte Error Count Register – Byte 1 (Address Location= 0x1712)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B1_Byte Error_Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [15:8]	RUR	B1 Byte Error Count – (Bits 15 through 8)
	Count [15.o]	This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B1 byte error	
			Note:
			1. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.
			2. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32-bit counter by the number of trames that contain erred B1 bytes.
	thedat	andma	counter by the number of frames that contain erred B1 bytes.

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Table 170: Redundant Receive STM-1 Section – B1 Byte Error Count Register – Byte 0 (Address Location= 0x1713)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B1_Byte Error_Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_	RUR	B1 Byte Error Count – LSB:
	Count [7:0]		This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STM-1 frame) that are in error.
			2. If the Redundant Receive STM-1 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-1 frame that contains an erred B1 byte.
	the	Produ datand	counter each time that it receives an STM-1 frame that contains an erred B1 byte.

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Table 171: Redundant Receive STM-1	Section - B2 Byte	Error Count Regi	ister – Byte 3 (Address
Location= 0x1714)	-	-	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
ВIТ <b>N</b> UMBER 7 - 0	NAME B2_Byte_Error_ Count [31:24]	TYPE RUR	DESCRIPTION         B2 Byte Error Count – MSB:         This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream.         Note:         1. If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.         2. If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-1 frame that contains at least one erred B2 byte.

errors on a sper-fit time that it receive byte.



Table 172: Redundant Receive STM-1 Section – B2 Byte Error Count Register – Byte 2 Address Location= 0x1715)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_	RUR	B2 Byte Error Count (Bits 23 through 16):
	Count [23:16]		This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis then it will increment this 32-bit counter by the number of bits, within the B2 byte (of each incoming STM-1 frame) that are in error.
			2. If the Redundant Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-1 frame that contains at least one erred B2 byte
	the	produ datand	counter each time that it receives an STM-1 frame that contains at least one erred B2 byte

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Table 173: Redundant Receive STM-1	Section – B2 Byte Error	Count Register – Byte 1 (Address
Location= 0x1716)	-	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
BIT NUMBER 7 - 0	NAME B2_Byte_Error_ Count [15:8]	TYPE RUR	<ul> <li>B2 Byte Error Count – (Bits 15 through 8)</li> <li>This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream.</li> <li>Note: <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.</li> </ol> </li> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.</li> </ul>
			counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.

count B2 byte error counter each time erred B2 byte of the transferred be of the transfe



Table 174: Redundant Receive STM-1 Section – B2 Byte Error Count Register – Byte 0 (Address Location= 0x1717)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Byte Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B2_Byte	RUR	B2 Byte Error Count – LSB:
	Error_Count[7:0]		<ul> <li>This RESET-upon-READ register, along with "Redundant STM-1 Receive Section – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a B2 byte error within the incoming STM-1 data-stream.</li> <li>Note: <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.</li> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STM-1 frame) that are in error.</li> </ol> </li> </ul>

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Table 175: Redundant Receive STM-1	Section - MS-REI Event	Count Register – Byte 3 (Address
Location= 0x1718)		2 2 .

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
MS-REI_Event_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	MS-REI_Event_Count	RUR	MS-REI Event Count – MSB:
	[31:24]		<ul> <li>This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – MS-REI Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-1 datastream.</li> <li>Note: <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within the each incoming STM-1 frame.</li> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within the each incoming STM-1 frame.</li> </ol> </li> </ul>

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Table 176: Redundant Receive STM-1 Section – MS-REI Event Count Register – Byte 2 (Address Location= 0x1719)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
MS-REI_Event_Count[23:16]									
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	MS-	RUR	MS-REI Event Count (Bits 23 through 16):
	REI_Event_Count [23:16]		<ul> <li>This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – MS-REI Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-1 data-stream.</li> <li><i>Note:</i> <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.</li> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.</li> </ol> </li> </ul>

to count MS REi 32 bit counter ea non-zero M1 byte



Table 177: Redundant Receive STM-	I Section – MS-REI Event	Count Register – Byte 1 (Address
Location= 0x171A)		

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
MS-REI_Event_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	MS-REI	RUR	MS-REI Event Count – (Bits 15 through 8)
	Event_Count[15:8]		<ul> <li>This RESET-upon-READ register along with "Redundant Receive STM-1 Section – MS-REI Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-1 datastream.</li> <li>Note: <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 SOH Processor block is configured to count MS-REI events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-1 frame that contains a non-zero M1 byte value.</li> </ol> </li> </ul>

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Table 178: Redundant Receive STM-1 Section – MS-REI Event Count Register – Byte 0 (Address Location= 0x171B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
MS-REI_Event_Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	MS- REI_Event_Count [7:0]	RUR	<ul> <li>MS-REI Event Count – LSB:</li> <li>This RESET-upon-READ register, along with "Redundant Receive STM-1 Section – MS-REI Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STM-1 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-1 data-stream.</li> <li>Note: <ol> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.</li> </ol> </li> <li>If the Redundant Receive STM-1 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the MS-REI fields of the M1 byte within each incoming STM-1 frame.</li> </ul>

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Table 179: Redundant Receive STM-1 Section – Received K1 Byte Value Register (Address Location= 0x171F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Filtered_K1_Byte_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7 – 0	Filtered_K1_Byte_Value[7:0]	R/O	Filtered/Accepted K1 Byte Value:				
			These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value, that the Redundant Receive STM-1 SOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STM-1 frames. This register should be polled by Software in order to determine various APS codes.				
	ONCAN						

### Table 180: Redundant Receive STM-1 Section – Receive K2 Byte Value Register (Address Location= 0x1723)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
			Filtered_K2_B	/te_Value[7:0]					
R/O	R/O	R/O	RO	R/O	R/O	R/O	R/O		
0	0	0		0	0	0	0		

BIT NUMBER	Nаме		
7 – 0	Filtered_K2_Byte_Val	RO Filtered/Accepted K2 Byte Value:	
		These READ-ONLY bit-fields contain the value of the most tiltered" K2 Byte value, that the Redundant Receive STM Processor block has received. These bit-fields are valid if the pair (to which it belongs) has been received for 3 consecutive frames.	-1 SOH e K1/K2
	Theatad	This register should be polled by Software in order to determine APS codes.	e various
	2		



# Table 181: Redundant Receive STM-1 Section – Received S1 Byte Value Register (Address Location= 0x1727)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Filtered_S1_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	Filtered/Accepted S1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Redundant Receive STM-1 SOH Processor block has received. These bit fields are valid if it has been received for 8 consecutive STM-1 frames.

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# Table 182: Redundant Receive STM-1 Section – In-Sync Threshold Value (Address Location=0x172B) Drag Drag Drag Drag

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		FRPATO	OUT[1:0]	FRPAT	⁻ IN[1:0]	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION
7 – 5	Unused	R/O		
4 – 3	FRPATOUT[1:0]	R/W	Framing Pattern – S	EF Declaration Criteria:
			Declaration criteria fo The relationship betw	RITE bit-fields permit the user to define the SEF Defect r the Redundant Receive STM-1 SOH Processor block. /een the state of these bit-fields and the corresponding on Criteria are presented below.
			00	The Redundant Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.
			(15) p	• Fthe last (of the 3) A1 bytes, in the STM-1 data stream is erred, or
			dundend	If the first (of the 3) A2 bytes, in the STM-1 data stream, is erred.
			pro lo dere	Hence, for this selection, a total of 16 bits are evaluated for SEF defect declaration.
		duct	are belondered	The Redundant Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.
	Q	she		<ul> <li>If the last two (of the 3) A1 bytes, in the STM-1 data stream, are erred, or</li> </ul>
	These	3 (1		• If the first two (of the 3) A2 bytes, in the STM-1 data stream, are erred.
	•	311		Hence, for this selection, a total of 32 bits are evaluated for SEF defect declaration.
			11	The Redundant Receive STM-1 SOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods.
				<ul> <li>If the last three (of the 3) A1 bytes, in the STM- 1 data stream, are erred, or</li> </ul>
				• If the first three (of the 3) A2 bytes, in the STM- 1 data stream, are erred.
				Hence, for this selection, a total of 48 bits are evaluated for SEF defect declaration.
2 - 1	FRPATIN[1:0]	R/W	Framing Pattern – S	EF Defect Clearance Criteria:
			These two READ/WR	RITE bit-fields permit the user to define the "SEF Defect



		FRPATIN[1:0]	SEF Defect Clearance Criteria
		00 01	The Redundant Receive STM-1 SOH Processon block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
			If the last (of the 3) A1 bytes, in the STM-1 data stream is un-erred, and
			• If the first (of the 3) A2 bytes, in the STM-1 data stream, is un-erred.
			Hence, for this selection, a total of 16 bits/frame are evaluated for SEF defect clearance.
		10	The Redundant Receive STM-1 SOH Processo block will clear the SEF defect condition if both o the following conditions are true for two consecutive SONET frame periods.
			If the last two (of the 3) A1 bytes, in the STM-1     data stream, are un-erred, and
			If the first two (of the 3) A2 bytes, in the STM-1
		CLS .	Hence for this selection, a total of 32 bits/frame are evaluated for SEF defect clearance.
		eet not be	The Redundant Receive STM-1 SOH Processo block will clear the SEF defect condition if both o the following conditions are true for two consecutive SONET frame periods.
			If the last three (of the 3) A1 bytes, in the STM     1 data-stream, are un-erred, and
	6	e o	• If the first three (of the 3) A2 bytes, in the STM 1 data stream, are un-erred.
	Qr 2		Hence, for this selection, a total of 48 bits/frame are evaluated for SEF defect declaration.



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Table 183: Redundant Receive STM-1 Section - LOS Threshold Value - MSB (Address Location= 0x172E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	LOS_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
			These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STM-1 SOH Processor block must detect before it can declare the LOS defect condition.

## 6.9 Table 184: Redundant Receive STM-1 Section – LOS Threshold Value - LSB (Address Location= 0x172F) A?

Віт 7	Віт 6	Віт 5	Віт 4 🕜 Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRESHOLD[7:0]			
R/W	R/W	R/W	R/W S R/W	R/W	R/W	R/W
1	1	1		1	1	1
			0° 0° 0 -			

BIT NUMBER	ΝΑΜΕ	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
	oroche	et	These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STM-1 SOH Processor block must detect before it can declare the LOS defect condition.
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 185: Redundant Receive STM-1 Section –Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1731)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
<b>Віт Number</b> 7 - 0	NAME SF_SET_MONITOR_ WINDOW [23:16]	Type R/W	<ul> <li>SF_SET_MONITOR_INTERVAL – MSB:</li> <li>These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.</li> <li>When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 SOH Processor block will declare the SF defect condition.</li> <li>NOTES:         <ul> <li>The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF</li> </ul> </li> </ul>
		or	Monitor Window" registers, specifies the duration of the "SF Defect Declaration Monitoring Period, in terms of ms. 2. This particular register byte contains the "MSB" (most
	The production of the producti	neet n	"SF Defect Declaration Monitoring Period".

Table 186: Redundant Receive STM-1	Section – Receive SF S	SET Monitor Interval	- Byte 1 (Address
Location= 0x1732)			

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

Bit Number	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW [15:8]	R/W	<ul> <li>SF_SET_MONITOR_INTERVAL (Bits 15 through 8):</li> <li>These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.</li> <li>When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period" the Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 SOH Processor block will declare the SF defect condition.</li> <li>NOTE: The value that the user writes into these three (3) "SF Set Monitor Window" Registers, specifies the duration of the "SF Defect Declaration.</li> </ul>
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 187: Redundant Receive STM-1 Section – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1733)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	SF_SET_MONITOR_INTERVAL – LSB:
		ducts	These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Falure) Defect Declaration. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user- specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 Section SF SET Threshold" register, then the Redundant Receive STM-1 SOH Processor block will declare the SF defect condition. <b>NOTES:</b>
	The product of product of the produc	o rd	<ol> <li>The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.</li> </ol>
	e producet not		<ol> <li>This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".</li> </ol>
	Theatendin		,

Table 188: Redundant Receive STM-1 Section – Receive SF SET Threshold – Byte 1 (Address Location= 0x1736)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	SF_SET_THRESHOLD – MSB:
		AUCT	These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to declare the SF (Signal Failure) Defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal, in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is of programmed into this and the "Redundant Receive STM-1 Section SF SET Threshold – Byte 0" register, then the Redundant Receive STM-1 SOH Processor block will declare the SF defect condition.
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 189: Redundant Receive STM-1 Section – Receive SF SET Threshold – Byte 0 Address Location= 0x1737)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:	R/W	SF_SET_THRESHOLD – LSB:
	0]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to declare the SF (Signal Failure) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Redundant Receive STM-1 Section SF SET Threshold – Byte 1" register, then the Redundant Receive STM-1 SOH Processor block will declares the SF defect condition.

Table 190: Redundant Receive STM-1 Section – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0x173A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_CLEAR_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
BIT NUMBER 7 - 0	NAME SF_CLEAR_THRESHOLD [15:8]	R/W	SF_CLEAR_THRESHOLD – MSB: These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to clear the SF (Signal Failure) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive
	The preshead	•	



Table 191: Redundant Receive STM-1 Section – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x173B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD – LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant Receive STM-1 SOH Processor block to clear the SF (Signal Failure) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STM-1 Section SF CLEAR Threshold – Byte 1" register, then the Redundant Receive STM-1 SOH Processor block will clear the SF defect condition.

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Table 192: Redundant Receive STM-1 Section -	Receive SD Set Monitor Interval -	Byte 2 (Address
Location= 0x173D)		

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	SD_SET_MONITOR_INTERVAL – MSB:
	[23.10]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Redundant Receive STM-1 SOH Processor
			block is checking the incoming STM-1 signal, in order to determine if it should declare SD defect condition, it will
			accumulate B2 byte errors throughout the user- specified "SD Defect Declaration monitoring period". If,
		me	during this "SD Defect Declaration Monitoring period", the Redundant Receive STM-1 SOH Processor block
		SX	accumulates more B2 byte errors than that specified
	811	del l	Threshold" register, then the Redundant Receive STM- 1 SOH Processor block will declare the SD defect
	NO.	of se	condition.
		6,	NOTES:
	duct are the	0`	<ol> <li>The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration Monitoring Period", in terms of ms.</li> </ol>
	the product or product or product of the product of		<ol> <li>This particular register byte contains the "MSB" (Most Signficant Byte) value of the three registers that specify the "SD Defect Declaration Monitoring Period".</li> </ol>
	, 90° 3110		



Table 193: Redundant Receive STM-1 Section – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x173E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	SD_SET_MONITOR_INTERVAL – Bits 15 through 8:
	The producet not	ducts ducts	<ul> <li>These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration.</li> <li>When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the userspecified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 Section SD SET Threshold" register, then the Redundant Receive STM-1 SOH Processor block will declare the SD defect condition.</li> <li>NOTE: The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.</li> </ul>

Table 194: Redundant Receive STM-1 Section	- Receive SD Set Monitor Interval -	- Byte 0 (Address
Location= 0x173F)		

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SD_SET_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[	R/W	SD_SET_MONITOR_INTERVAL – LSB:
	7:0]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration.
	Mod	ucts	When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user- specified "SD Defect Declaration Monitoring Period". If, during the "SD Defect Declaration Monitoring Period", the Redundant Receive STM-1 SOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STM-1 Section SD SET Threshold" register, then the Redundant Receive STM-1 SOH Processor block will declare the SD defect condition. <b>NOTES:</b>
	ict are no	eorde	<ol> <li>The value that the user writes into these three (3) "SD Set Monitor Window" Registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.</li> </ol>
	The product or product		<ol> <li>This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring period".</li> </ol>
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 195: Redundant Receive STM-1 Section – Receive SD SET Threshold – Byte 1 (Address Location= 0x1742)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_SET_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	SD_SET_THRESHOLD – MSB:
			These READ/WRITE bits along the contents of the "Redundant Receive STM-1 Section – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to declare the SD (Signal Degrade) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoirng Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Redundant Receive STM-1 Section SD SET Threshold – Byte 0" register, then the Redundant Receive STM-1 SOH Processor block will declare the SD defect condition.

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Table 196: Redundant	<b>Receive STM-</b>	1 Section -	Receive SD	) SET	Threshold -	Byte 0 (	Address
Location= 0x1743)							

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SD_SET_THRESHOLD[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD – LSB:
			These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to declare the SD (Signal Degrade) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Redundant Receive STM-1 Section SD SET Threshold – Byte 1" register, then the Redundant Receive STM-1 SOH Processor block will declare the SD defect condition.
	The product of and the		indered t

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 197: Redundant Receive STM-1 Section – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1746)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SD_CLEAR_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	Nаме	Түре	DESCRIPTION					
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	SD_CLEAR_THRESHOLD – MSB:					
These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD CLEA Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block clear the SD (Signal Degrade) defect condition. When the Redundant Receive STM-1 SOH Processor block clear the SD (Signal Degrade) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determin if it should Clear the SD defect condition, it will accumula B2 byte errors throughout the "SD Defect Clearant Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Peduadating Period". STM-1 Section SD CLEAR Threebook								
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Table 198: Redundant Receive STM-1	Section – Receive	SD CLEAR Three	shold – Byte 1 (Address
Location= 0x1747)			

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_CLEAR_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD – LSB:
		uct.	These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STM-1 SOH Processor block to clear the SD (Signal Degrade) defect condition. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors, throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STM-1 Section SD CLEAR Threshold – Byte 1" register, then the Redundant Receive STM-1 SOH Processor block will clear the SD defect condition.
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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Table 199: Redundant Receive STM-1 Section – Force SEF Condition Register (Address Location= 0x174B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SEF FORCE							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	SEF Force:
			This READ/WRITE bit-field permits the user to force the Redundant Receive STM-1 SOH Processor block to declare the SEF defect condition. The Redundant Receive STM-1 SOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Redundant Receive STM-1 SOH Processor block to declare the SEF defect. The Redundant Receive STM-1 SOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STM-1 frames with the correct A1 and A2 bytes).



## Table 200: Redundant Receive STM-1 Section – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0x1752)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	SD_BURST_TOLERANCE[15:8]										
R/W	R/W R/W R/W R/W R/W R/W R/W										
1	1	1	1	1	1	1	1				

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_BURST_	R/W	SD_BURST_TOLERANCE – MSB:
	TOLERANCE [15:8]		<ul> <li>These READ/WRITE bits, along with the contents of the "Redundant Receive STM-1 Section – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.</li> <li>Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STM-1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.</li> </ul>



Table 201: Redundant Receive STM-1 Section – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1753)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	SD_BURST_TOLERANCE[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
1	1	1	1	1	1	1	1				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7 - 0       SD_BURST_ TOLERANCE [7:0]       R/W       SD_BURST_TOLERANCE - LSB:         These READ/WRITE bits, along with the contents of the "Redundant Receive STM-1 Section – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.         Note:       The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STM-1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.							
	×	le proc	Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.				



Table 202: Redundant Receive STM-1 Section – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1756)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0					
	SF_BURST_TOLERANCE[15:8]											
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
1	1	1	1	1	1	1	1					

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_BURST_ TOLERANCE [15:8]	R/W	<ul> <li>SF_BURST_TOLERANCE – MSB:</li> <li>These READ/WRITE bits, along with the contents of the "Redundant Receive STM-1 Section – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SF (Signal Failure) detect condition.</li> <li>Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STM-1 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.</li> </ul>

Table 203: Redundant Receive STM-1 Section – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1757)

BIT 7	Віт 6	Віт 5	BIT4	Віт 3	Віт 2	Віт 1	Віт 0				
57	Birv	Biro		-		0	Birt				
		1	SF_BURST_TO	DLERANCE[7:0]							
R/W	R/W	R/W	Ø R/₩	R/W	R/W	R/W	R/W				
1	1		\$ <b>`</b> \$	1	1	1	1				

BIT NUMBER		Түре	DESCRIPTION
7 - 0	SF_BURST TOLERANCE [7:0]	Brw C	<ul> <li>SF_BURST_TOLERANCE – LSB:</li> <li>These READ/WRITE bits, along with the contents of the "Redundant Received STM-1 Section – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Received STM-1 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-1 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition.</li> <li>Note: The purpose of this feature is to permit the user to provide some leve of B2 byte error burst filtering, when the Redundant Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STM-1 SOH Processor block is accumulating B2 byte errors in order to block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.</li> </ul>

Table 204: Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0x1759)

## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
SD_CLEAR_MONITOR_WINDOW[23:16]											
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
1	1	1	1	1	1	1	1				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[23:	R/W	SD_CLEAR_MONITOR_INTERVAL – MSB:
	16]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
			When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user- specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Redundant Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SD Clear Threshold" register, then the Redundant Receive STM- 1 SOH Processor block will clear the SD defect
		JUL S	Condition NOTES:
	otoro		<ol> <li>The value that the user writes into these three</li> <li>(3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period" in terms of ms.</li> </ol>
	oductare	¢e	<ol> <li>This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.</li> </ol>
	The product or product are not		



Table 205: Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x175A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
	The lata not not be not be	bered	When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period" the Redundant Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SD Clear Threshold" register, then the Redundant Receive STM-1 SOH Processor block will clear the SD defect condition.
	roduct are be		<b>NOTE:</b> The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.
	The Past nav		<u>.</u>

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 206: Redundant Receive STM-1 Section – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0x175B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB:
	7:0]		These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SD Clear Monitor Interval – Byte 2 and Byte 1 th registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
	The ata nav	When the block is determin accumu "SD Def "SD Def Receive B2 byte Receive then the will clear	When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Redundant Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SD Clear Threshold" register, then the Redundant Receive STM-1 SOH Processor block will clear the SD defect condition. NOTES:
			1000
	product at	t pe	<ol> <li>This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.</li> </ol>
	The atand ma		·

Table 207: Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte	2 (Address
Location= 0x175D)	-

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDO W [23:16]	R/W	SF_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Pailure) defect clearance.
		ducts	When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during the "SF Defect Clearance" Monitoring period, the Redundant Receive STM- 1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SE Clear Threshold" register then the Redundant
	nct or b	o', c	<ol> <li>The value that the user writes into these three (3) "SF Clear Monitor Window Registers", specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.</li> </ol>
	The product of pro-		<ol> <li>This particular register byte contains the "MSB" (most significant byte) value fo the three registers that specify the "SF Defect Clearance Monitoring" period.</li> </ol>
L	The Jate of the	1	۱J

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 208: Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0x175E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user- specified "SF Defect Clearance" Monitoring period. If,
	60	ctsin	during this "SF Defect Clearance" Monitoring period, the Redundant Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SF Clear Threshold" register, then the Redundant Receive STM- SOH Processor block will clear the SF defect condition.
	ct or pho	eordei	<b>NOTES:</b> The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.
	The product are point to the product are point to the product are point to the product of the pr		

Table 209: Redundant Receive STM-1 Section – Receive SF Clear Monitor Interval – Byte 0 (Address
Location= 0x175F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL - LSB:
	[7:0]	ts) me	These READ/WRITE bits, along the contents of the "Redundant Receive STM-1 Section – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Redundant Receive STM-1 SOH Processor block is checking the incoming STM-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user- specified "SF Defect Clearance" Monitoring period, the Redundant Receive STM-1 SOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STM-1 Section SF Clear Threshold" register, then the Redundant Receive STM-1 SOH Processor block will clear the SF defect condition. NOTES:
	huct are be	oru	<ol> <li>The value that the user writes into these three</li> <li>(3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring" period, in terms of ms.</li> </ol>
	the ta may not		<ol> <li>This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.</li> </ol>
	desto		

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 210: Redundant Receive STM-1 Section – Serial Port Control Register (Address Location= 0x1767)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Unused				RxSOH_CLOCK_SPEED[7:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxSOH_CLOCK_SPEED[7:0]	R/W	RxSOHClk Output Clock Signal Speed:These READ/WRITE bit fields permit the user to specify thefrequency of the "RxSOHClk output clock signal.The formula that relates the contents of these register bits tothe "RxSOHClk" frequency is presented below.FREQ = 19.44 /2* (RxSOH_CLOCK_SPEED + 1)Note: For STS 3/STM-1 applications, the frequency of theRxSOHClk output signal must be in the range of0.6076MHz to 9.72MHz

Note: For STS 3 RXSOHGH 0.6075MH



#### 1.7 TRANSMIT STM-1 SOH PROCESSOR BLOCK

The register map for the Transmit STM-1 SOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit STM-1 SOH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 whenever it has been configured to operate in the SDH/TUG-3 and the SDH/AU-3 Modes, with the "Transmit STM-1 SOH Processor Block "highlighted" is presented below in Figure 4 and 5.

# Figure 4: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the SDH/TUG-3 Mode), with the Transmit STM-1 SOH Processor Block "High-lighted".

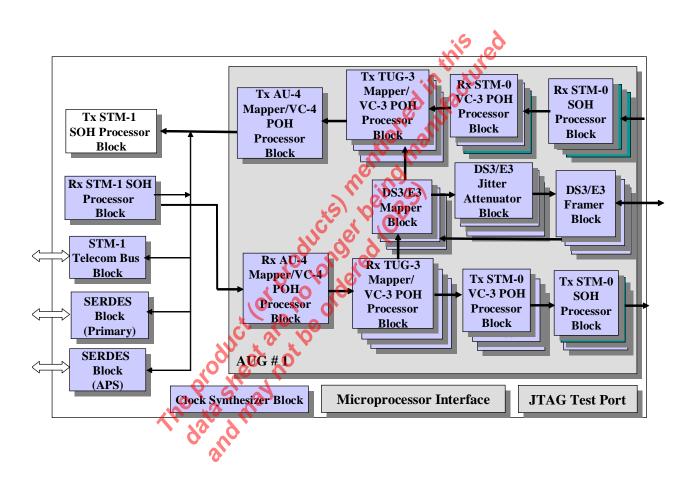
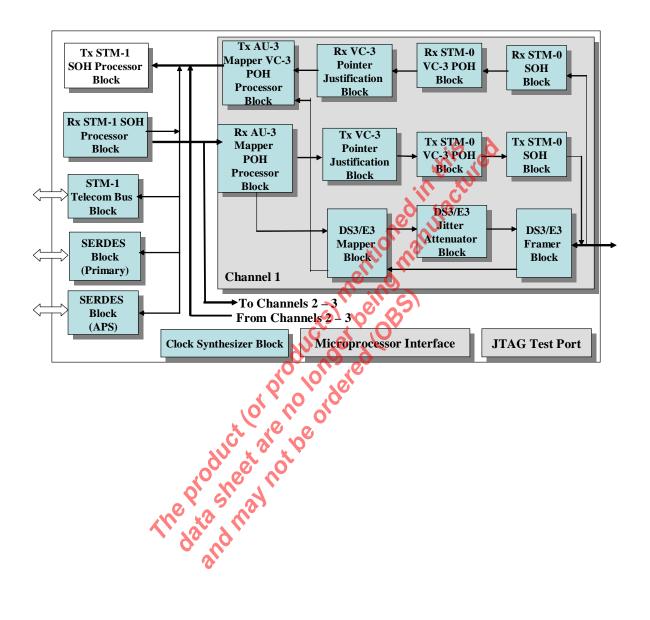




Figure 5, Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the SDH/AU-3 Mode) with the Transmit STM-1 SOH Processor Block "highlighted"





#### TRANSMIT STM-1 SOH PROCESSOR BLOCK REGISTER

### Table 211: Transmit STM-1 SOH Processor Block Registers – Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x1800 - 0x1901	Reserved	0x00
0x1902	Transmit STM-1 Section – SONET Transmit Control Register – Byte 1	0x00
0x1903	Transmit STM-1 Section – SONET Transmit Control Register – Byte 0	0x00
0x1904 – 0x1915	Reserved	0x00
0x1916	Reserved	0x00
0x1917	Transmit STM-1 Section – Transmit A1 Byte Error Mask – Low Register – Byte 0	0x00
0x1918 – 0x191E	Reserved	0x00
0x191F	Transmit STM-1 Section – Transmit A2 Byte Erro Mask Low Register – Byte 0	0x00
0x1920 - 0x1921	Reserved	0x00
0x1923	Transmit STM-1 Section – B1 Byte Error Mask Register	0x00
0x1924 - 0x1926	Reserved	0x00
0x1927	Transmit STM-1 Section – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0x1928 – 0x192A	Reserved	0x00
0x192B	Transmit STM-1 Section - Transmit B2 Byte - Bit Error Mask Register - Byte 0	0x00
0x192C - 0x192D	Reserved	0x00
0x192E	Transmit STM-1 Section – K1K2 Byte (APS) Value Register – Byte 1	0x00
0x192F	Transmit STM-1 Section - K1K2 Byte (APS) Value Register – Byte 0	0x00
0x1930 - 0x1931	Reserved	0x00
0x1933	Transmit STM-1 Section – MS-RDI Control Register	0x00
0x1934 – 0x1936	Reserved	0x00
0x1937	Transmit STM-1 Section – M1 Byte Value Register	0x00
0x1938 – 0x193A	Reserved	0x00
0x193B	Transmit STM-1 Section – S1 Byte Value Register	0x00
0x193C – 0x193E	Reserved	0x00
0x193F	Transmit STM-1 Section – F1 Byte Value Register	0x00
0x40 – 0x42 0x1940 – 0x1942	Reserved	0x00
0x1943	Transmit STM-1 Section – E1 Byte Value Register	0x00
0x1944	Transmit STM-1 Section – E2 Byte Control Register	0x00
0x1945	Reserved	0x00

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



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Address Location	REGISTER NAME	DEFAULT VALUES
0x1946	Transmit STM-1 Section – E2 Byte Pointer Register	0x00
0x1947	Transmit STM-1 Section – E2 Byte Value Register	0x00
0x1948 – 0x194A	Reserved	0x00
0x194B	Transmit STM-1 Section – Transmit J0 Byte Value Register	0x00
0x194C – 0x194E	Reserved	0x00
0x194F	Transmit STM-1 Section – Transmit J0 Byte Control Register	0x00
0x1950 – 0x1952	Reserved	0x00
0x1953	Transmit STM-1 Section – Serial Port Control Register	0x00
0x1954 –0x19FF	Reserved	0x00

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#### 1.7.1 TRANSMIT STM-1 SOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 212: Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	STS-N Overhead Insert	E2 Byte Insert Method	E1 Byte Insert Method	F1 Byte Insert Method	S1 Byte Insert Method	K1K2 Byte Insert Method	M1 Byte Insert Method[1]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	niseo
6	STS-N Overhead Insert	R/W	<ul> <li>STS-N Overhead Insert:</li> <li>This READ/WRITE bit-field permits the user to configure the TxSOH input port to insert the SOH for all lower-tributary STM-0s within the outbound STM-1 signal.</li> <li>0 – Disables this feature. In this mode, the TxSOH input port will only accept the SOH for the first STM-0 within the outbound STM-1 signal.</li> <li>1 – Enables this feature.</li> </ul>
5	E2 Byte Insert Method	R/W	<ul> <li>E2 Byte Insert Method:</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to use either the contents within the "Transmit STM-1 SOH Processor block to use either the contents within the "transmit STM-1 Section – E2 Byte Value" Register or the TxSOH input port as the source for the E2 byte, within the outbound STM-1 data-stream, as described below.</li> <li>Configures the Transmit STM-1 SOH Processor block to accept externally supplied data (via the "TxSOH serial input port) and to insert this data into the E2 byte position within each outbound STM-1 frame.</li> <li>Configures the Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 Section – E2 Byte Value" register (Address Location = 0x1947) into the E2 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the E2 byte within the "Transmit Output" STM-1 data-stream.</li> </ul>
4		R/W	E1 Byte Insert Method:
	Method		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to use either the contents within the "Transmit STM-1 Section – E1 Byte Value" Register or the TxSOH Input port as the source for the E1 byte, within the outbound STM-1 data-stream, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to accept externally supplied data (via the "TxSOH serial input port) and to insert this data into the E1 byte position within each outbound STM-1 frame.
			1 – Configures the Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 Section – E1 Byte Value" register (Address Location = 0x1943) into the E1 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the E1 byte within the "Transmit Output" STM-1 data-stream.



## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

3	F1 Byte Insert	R/W	F1 Byte Insert Method:
	Method		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to use either the contents within the "Transmit STM-1 Section – F1 Byte Value" Register or the TxSOH Input port as the source for the F1 byte, within the outbound STM-1 data-stream, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the F1 Byte position within each outbound STM-1 frame.
			1 – Configures the Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 Section – F1 Byte Value" register (Address Location = 0x193F) into the F1 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the F1 byte within the "Transmit Output" STM-1 data-stream.
2	S1 Byte Insert	R/W	S1 Byte Insert Method:
	Method		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to use either the contents within the "Transmit STM-1 Section – S1 Byte Value" Register or the TxSOH Input port as the source for the E1 byte, within the outbound STM-1 data-stream, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the S1 Byte position within each outbound STM-1 frame.
			1 – Configures the Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 Section – S1 Byte Value" register (Address Location = 0x193B). This configuration selection permits the user to have software control over the value of the S1 byte within the "Transmit Output" STM-1 data-stream.
1	K1K2 Byte Insert Method	R/W	<ul> <li>K1K2 Byte Insert Method:</li> <li>This READWRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to use either the contents within the "Transmit STM-1 Section – K1 Byte Value" and "Transmit STM-1 Section – K2 Byte Value" registers or the "TxSOH Input port as the source for the K1 and K2 bytes, within the outbound STM-1 data-stream, as described below.</li> <li>O – Configures the Transmit STM-1 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the K1 and K2 Byte positions within each outbound STM-1 frame.</li> </ul>
		<b>'0</b> '	1 – Configures the Transmit STM-1 SOH Processor block to insert the contents within the "Transmit STM-1 Section – K1 Byte Value" Register (Address Location = $0x192E$ ) and the "Transmit STM-1 Section – K2 Byte Value" register (Address Location = $0x192F$ ) into the K1 and K2 byte-positions, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the K1 and K2 bytes within the "Transmit Output" STM-1 data-stream.
0	M1 Byte Insert	R/W	M1 Byte Insert Method – Bit 1:
	Method[1]		This READ/WRITE bit-field, along with the "M1 Insert Method[0]" bit-field (located in the "Transmit STM-1 Section – SONET Control Register – Byte 0") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STM-1 data stream.
			The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STM-1 frame) is presented



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M1 Byte Metho		Source of M1 Byte
0	0	Functions as the MS-REI indicator (based upon the number of B2 byte errors that have been detected by the Receive STM-1 SOF Processor block)
0	1	The M1 byte value is obtained from the contents of the "Transmit STM-1 Section – M1 Byte Value" register (Address Location = 0x1937).
		<b>NOTE:</b> This configuration selection permit the user to exercise software control over the contents within the M1 byte, of each outbound STM-1 frame
1	0	The M1 byte value is obtained from the TXSOH" Serial Input Port.
1	1 nion	Functions as the MS-REI bit-field (based upo the number of B2 byte errors that have bee detected by the Receive STM-1 SO Processor block).

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# Table 213: Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
M1 Byte Insert Method[0]	Unused	Force Transmission of MS-RDI	Force Transmission of MS-AIS	Force Tranmission of LOS Patttern	Scrambler Enable	B2 Byte Error Insert	A1A2 Byte Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	M1 Byte Insert Method[0]	R/W	M1 Byte Insert Method – Bit 0:         This READ/WRITE bit-field, along with the "M1 Insert Method[1]" bit-field (located in the "Transmit STM-1 Section – SONET Control Register – Byte 1") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STM-1 data stream.         The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STM-1 frame) is presented below.         M1 Insert       Source of M1 Byte         0       0       Functions as the MS-REI indicator (based upon the number of B2 byte errors that have been detected by the Receive STM-1 SOH Processor block)         0       0       Functions as the M2-REI indicator selection – M1 Byte Value" register (Address Location= 0x1937).         NOTE:       This configuration selection permits the user to exercise software control over the contents within the M1 byte of each outbound STM-1 frame.         1       0       The M1 byte value is obtained from the "TxSOH" Serial Input Port.         1       1       Functions as the M3-REI bit-field (based upon the number of B2 byte errors that have been detected by the Receive STM-1 Serial Input Port.
6	Unused	R/O	
5	Force Transmission of MS-RDI	R/W	<ul> <li>Force Transmission of MS-RDI (Line - Remote Defect Indicator):</li> <li>This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-1 SOH Processor block to generate and transmit the MS-RDI indicator to the remote terminal equipment as described below.</li> <li>0 – Does not configure the Transmit STM-1 SOH Processor block to generate and transmit the MS-RDI indicator. In this setting, the Transmit STM-1 SOH Processor block will only generate and transmit the MS-RDI indicator whenever the Receive STM-1 SOH Processor</li> </ul>



			block is declaring a defect condition.
			1 – Configures the Transmit STM-1 SOH Processor block to generate and transmit the MS-RDI indicator to the remote terminal equipment. In this case, the STM-1 Transmitter will force bits 6, 7 and 8 (of the K2 byte) to the value "1, 1, 0".
			<b>Note:</b> This bit-field is ignored if the Transmit STM-1 SOH Processor block is transmitting the Line AIS (MS-AIS) indicator or the LOS pattern.
4		R/W	Force Transmission of MS-AIS (Line AIS) Indicator:
	of MS-AIS		This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-1 SOH Processor block to generate and transmit the MS-AIS indicator to the remote terminal equipment, as described below.
			0 – Does not configure the Transmit STM-1 SOH Processor block to generate and transmit the MS AlS indicator. In this case, the Transmit STM-1 SOH Processor block will continue to transmit normal traffic to the remote terminal equipment.
			1 – Configures the Transmit STM-1 SOH Processor block to generate and transmit the MS-AIS indicator to the remote terminal equipment. In this case, the Transmit STM-1 SOH Processor block will force all bits (within the "outbound" STM-1 frame) with the exception of the Section Overhead Bytes to an "All Ones" pattern.
			<b>Note:</b> This bit-field is ignored if the Transmit STM-1 SOH Processor block is transmitting the LOS pattern.
3		R/W	Force Transmission of LOS Pattern:
	of LOS Pattern	.4	This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-1 SOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment, as described below.
	NUC	0	<ul> <li>Does not configure the Transmit STM-1 SOH Processor block to generate and transmit the LOS pattern. In this case, the Transmit STM-1 SOH Processor block will continue to transmit "normal" traffic to the remote terminal equipment.</li> </ul>
	the to the	hay r	- Configures the Transmit STM-1 SOH Processor block to transmit the LOS pattern to the remote terminal equipment. In this case, the Transmit STM-1 SOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern.
2	Scrambler Enable	R/W	Scrambler Enable:
	<u>v</u>		This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STM-1 SOH Processor block circuitry
			0 – Disables the Scrambler.
			1 – Enables the Scrambler.
1	B2 Byte Error Insert	R/W	Transmit B2 Byte Error Insert Enable:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STM-1 Section – Transmit B2 Byte Error Mask Registers" as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT insert errors into the B2 bytes, within the outbound STM-1 signal.
			1 - Configures the Transmit STM-1 SOH Processor block to insert

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			errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers").
0	A1A2 Byte Error Insert	R/W	Transmit A1A2 Byte Error Insert Enable:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STM-1 Section – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STM-1 data-stream.
			1 – Configures the Transmit STM-1 SOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit A1 Byte Error Mask" and "Transmit A2 Byte Error Mask" Registers.

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Table 214: Transmit STM-1 Section – Transmit A1 Byte Error Mask – Low Register – Byte 0 (Address Location= 0x1917)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3		Віт 2	Віт 1	Віт 0
Unused					A1 Byte Error in STM-0 # 2	A1 Byte Error in STM-0 # 1	A1 Byte Error in STM-0 # 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-3	Unused	R/O	
2	A1 Byte Error in STM-0 # 2	R/W	A1 Byte Error in STM-0 # 2, within outbound STM-1 signal:
	3110-0 # 2		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0 # 2 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A1 byte, within STM-0 Channel 2.
			1 – Configures the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0 Channel 2. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred.
			Note: This pit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
1	A1 Byte Error in	R/W	A Byte Erroin STM-0 # 1, within outbound STM-1 signal:
	STM-0 # 1	lot p	This READWRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0, # 1 within the outbound STM-1 signal, as described below.
		ct ste	0 Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A1 byte, within STM-0 Channel 1.
	A1 Byte Error in	neet n	1 – Configures the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0 Channel 1. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred.
	th data		<b>Note:</b> This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	AT Dyte Litor in	R/W	A1 Byte Error in STM-0 # 0, within outbound STM-1 signal:
	STM-0 # 0		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0 # 0 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A1 byte, within STM-0 Channel 0.
			1 – Configures the Transmit STM-1 SOH Processor block to transmit an erred A1 byte, within STM-0 Channel 0. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence, all 8-bits within this particular A1 byte will be erred.
			<b>Note:</b> This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".



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Table 215: Transmit STM-1 Section – Transmit A2 Byte Error Mask – Low Register – Byte 0 (Address Location= 0x191F)

Віт 7	Віт 6	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
		Unused	A2 Byte Error in STM-0 # 2	A2 Byte Error in STM-0 # 1	A2 Byte Error in STM-0 # 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-3	Unused	R/O	
2	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 2, within outbound STM-1 signal:
	STM-0 # 2		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM-0 # 2 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 2.
			1 – Configures the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM 0 Channel 2. In this configuration settting, the state of bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred.
			Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
1	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 1, within outbound STM-1 signal:
	STM-0 # 1		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM-0 # 1 within the outbound STM-1 signal, as described below.
		AUCE	0 Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 1.
	nepr		1 - configures the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM-0 Channel 1. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred.
	11.93	and	<b>Note:</b> This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 0, within the outbound STM-1 signal:
	STM-0 # 0		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM-0 # 0 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 0.
			1 – Configures the Transmit STM-1 SOH Processor block to transmit an erred A2 byte, within STM-0 Channel 0. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence, all 8-bits within this particular A2 byte will be erred.
			<b>Note:</b> This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register –

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		Byte 0 (Address Location= 0x1903) to "1".





#### Table 216: Transmit STM-1 Section – B1 Byte Error Mask Register (Address Location= 0x1923)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B1_Byte_Error_Mask[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	B1_Byte_Error_Mask [7:0]	R/W	B1 Byte Error Mask[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound STM-1 data stream.
			The Transmit STM-1 SOH Processor block will perform an XOR operation with the contents of the B1 byte (within each outbound STM-1 frame), and the contents within this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" STM-1 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. <b>Note:</b> For normal operation, the user should set this register to 0x00.

Note: For normal to 0x00.



Table 217: Transmit STM-1	Section – Trans	smit B2 Byte Error	Mask Register -	Byte 0 (Address
Location= 0x1927)		-	-	

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	B2 Byte Error in STM-0 Channel 2	B2 Byte Error in STM-0 Channel 1	B2 Byte Error in STM-0 Channel 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-3	Unused	R/O	this rec
2	B2 Byte Error in	R/W	B2 Byte Error in STM-0 Channel # 2
	STM-0 Channel # 2		<ul> <li>This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred B2 byte, within STM-0 Channel 2.</li> <li>If the user enables this feature, then the Transmit STM-1 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within STM-0 Channel 2) and the contents of the "Transmit STM-1 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B) The results of this calculation will be written back into the "B2 byte" position, within STM-0 Channel 2, prior to transmission to the remote terminal</li> <li>0 – Configures the Transmit STM-1 SOH Processor block to NOT insert errors into this particular B2 byte, within STM-0 Channel 2.</li> <li>1 – Configures the Transmit STM-1 SOH Processor block to insert</li> </ul>
		JUC ^t	errors into the B2 byte, within STM-0 Channel 2. Note: This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address = 0x1903) to "1".
4	DO Duto Error in		
1	B2 Byte Error in STM-0 Channel # 1	RAW	<b>B2 Byte Error in STM-0 Channel # 1:</b> This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred B2 byte, within STM-0 Channel 1.
		21	If the user enables this feature, then the Transmit STM-1 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within STM-0 Channel 1) and the contents of the "Transmit STM-1 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STM-0 Channel 1, prior to transmission to the remote terminal.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT insert errors into this particular B2 byte, within STM-0 Channel 1.
			1 – Configures the Transmit STM-1 SOH Processor block to insert errors into the B2 byte, within STM-0 Channel 1.
			<b>Note:</b> This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	B2 Byte Error in STM-0 Channel # 0	R/W	B2 Byte Error in STM-0 Channel # 0:



STM-0 Channel # 0	This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to transmit an erred B2 byte, within STM-0 Channel 0.
	If the user enables this feature, then the Transmit STM-1 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within STM-0 Channel 0) and the contents of the "Transmit STM-1 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STM-0 Channel 0, prior to transmission to the remote terminal.
	0 – Configures the Transmit STM-1 SOH Processor block to NOT insert errors into the B2 byte, within STM-0 Channel 0.
	1 – Configures the Transmit STM-1 SOH Processor block to insert errors into this particular B2 byte, within STM-0 Channel 0.
	<b>Note:</b> This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".

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## Table 218: Transmit STM-1 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
Transmit_B2_Error_Mask[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Transmit_B2_Error_Mask[7:0]	R/W	Transmit B2 Error Mask Byte:
			These READ/WRITE bit-fields permit the user to specify exact which bits, within the "selected" B2 byte (within the outbound STM-1 signal) will be erred
			If the user configures the Transmit STM-1 SOH Processor block to transmit one or more erred B2 bytes, then the Transmit STM-1 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within the "selected" STM-0 Channel) and the contents of this register. The results of this calculation will be written back into the "B2 byte" position within the "selected" STM-0 Channel, (within the outbound STM-1 signal) prior to transmission to the remote terminal.
			The user can select which STM-0 channels (within the outbound STM-1 signal) will contain the "erred" B2 byte, by writing the appropriate data into the "Transmit STM-1 Section – Transmit B2 Byte Error Mask Register – Bytes 1 and 0 (Address Location= 0x1927).
		orpri	Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
	The product	et no	



#### Table 219: Transmit STM-1 Section – K1K2 (APS) Value Register – Byte 1 (Address Location= 0x192E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_K2_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit_K2_Byte_Value[7:0]	R/W	Transmit K2 Byte Value:
			If the user has configured the Transmit STM-1 SOH Processor Block to use the contents of the "Transmit K2 Byte Value" Register as the source for the K2 byte value (within the outbound STM-1 data-stream), then these READ/WRITE bit- fields will permit the user to specify the contents of the K2 byte, within the "outbound" STM-1 signal. If Bit 1 (K1K2 Byte Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "K2" byte-field, within each outbound STM-1 frame. <b>Note:</b> These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".

"K2" byte-field, with Note: These reg Method) i



	Table 220. Transmit STM-T Section - KTK2 (AFS) value Register - Dyte 0 (Address Location= 0x1921)										
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
			Transmit_K1_E	Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				

#### Table 220: Transmit STM-1 Section – K1K2 (APS) Value Register – Byte 0 (Address Location= 0x192F)

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Transmit_K1_Byte_Value[7:0]	R/W	Transmit K1 Byte Value:
			If the user has configured the Transmit STM-1 SOH Processor block to use the contents of the "Transmit K1 Byte Value" Register as the source for the K1 byte value (within the outbound STM-1 data-stream), then these READ/WRITE bit-fields will permit the user to specify the contents of the K1 byte, within the "outbound" STM-1 signal.
			If Bit 1 (K1K2 Byte Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "K1" byte-field, within each outbound STM-1 frame.
			Note: These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".
	The product	or pro-	poly noteed no ordered be

#### Table 221: Transmit STM-1 Section – MS-RDI Control Register (Address Location= 0x1933)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		External	Transmit	Transmit	Transmit
			MS-RDI Enable	MS-RDI upon MS-AIS	MS-RDI upon LOF	MS-RDI upon LOS	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3	External MS-RDI Enable	R/W	External MS-RDI Insertion Enable:
			This READ/WRITE bit field permits the user to configure the Transmit STM-1 SOH Processor to accept data via the "TxSOH" input pin, when transmitting the MS-RDI indicator to the remote terminal equipment.
			0 – Configures the Transmit STM-1 SOH Processor block to internally generate the MS-RDI indicator based upon defect conditions that are being declared by the Receive STM-1 SOH Processor block.
			1 – Configure the Transmit STM-1 SOH Processor block accept external data via the "TxSOH" input port and to load this value into Bits 6, 7 and 8 (within the K2 byte) within each outbound STM-1 data-stream.
2	Transmit MS-RDI upon MS- AIS	R/W	Transmit Line Remote Defect Indicator (MS-RDI) upon Declaration of the MS-AIS defect condition:
	AIS AIS the product of the ata that	le pe	This READ/WRITE bit-field permits the user to configure the ransmit STM-1 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor is declaring the Line AIS (MS-AIS) defect condition as described below.
	ne prosheet	not	0 – Configures the Transmit STM-1 SOH Processor block to NOT automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block is declares the MS-AIS defect condition.
	1. 93 upt		1 – Configures the Transmit STM-1 SOH Processor block to automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the MS-AIS defect condition.
1	Transmit MS-RDI upon LOF	R/W	Transmit Line Remote Defect Indicator (MS-RDI) upon Declaration of the LOF defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor block is declaring the LOF defect condition as described below.
			0 – Configures the Transmit STM-1 SOH Processor to NOT automatically transmit the MS-RDI indicator, whenever the Receive STM-1 SOH Processor block declares the LOF defect condition.
			1 – Configures the Transmit STM-1 SOH Processor block to automatically transmit the MS-RDI indicator, whenever (and for

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			the duration that) the Receive STM-1 SOH Processor block declares the LOF defect condition.
0	Transmit MS-RDI upon LOS	R/W	Transmit Line Remote Defect Indicator (MS-RDI) upon Declaration of the LOS defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-1 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor block declares the LOS defect condition.
			0 – Configures the Transmit STM-1 SOH Processor block to NOT automatically transmit the MS-RDI indicator, whenever the Receive STM-1 SOH Processor block declares the LOS defect condition.
			1 – Configures the Transmit STM-1 SOH Processor block to automatically transmit the MS RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition.

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#### Table 222: Transmit STM-1 Section – M1 Byte Value Register (Address Location= 0x1937)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit_M1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
<b>Віт Number</b> 7 — 0	NAME Transmit_M1_Byte_Value [7:0]	Type R/W	Transmit M1 Byte Value: If the appropriate "M1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the M1 byte, within the "outbound" STM-1 signal. If Bit 0 (M1 Byte Insert Method – Bit 1) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1002) and Bit 7 (M1 Byte Insert Method
			<ul> <li>Bit 0) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 0 (Address Location = 0x1903) is set to "[0, 1]", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "M1" byte-field, within each outbound STM-1 frame.</li> <li>Note: These register bits are ignored if the M1 Byte Insert Method[1:0] bits are set to any value other than "[0, 1]".</li> </ul>

# Table 223: Transmit STM-1 Section – S1 Byte Value Register (Address Location= 0x193B)

Віт 7	Віт 6	Віт 5	BIT 4	Bit 3	Віт 2	Віт 1	Віт 0	
Transmit_S1_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	<b>0</b> 0	0	0	0	0	
	O C C NO							

BIT NUMBER	NAME 6	Түре	DESCRIPTION
7 – 0	Transmit_S1_Byte_Value[7:0]	R/W	<ul> <li>Transmit S1 Byte Value:</li> <li>If the appropriate "S1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the S1 byte, within the "outbound" STM-1 signal.</li> <li>If Bit 2 (S1 Byte Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "S1" byte-field, within each outbound STM-1 frame.</li> <li>Note: These register bits are ignored if Bit 2 (S1 Byte Insert Method) is set to "0".</li> </ul>

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			-						
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_F1_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

#### Table 224: Transmit STM-1 Section – F1 Byte Value Register (Address Location= 0x193F)

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	Transmit_F1_Byte_Value[7:0]	R/W	Transmit F1 Byte Value:
			<ul> <li>If the appropriate "F1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the F1 byte, within the "outbound" STM-1 signal.</li> <li>If Bit 3 (F1 Byte Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "F1" byte-field, within each outbound STM-1 frame.</li> <li>Note: These register bits are ignored if Bit 3 (F1 Byte Insert Method) is set to "0".</li> </ul>
			e d

### Table 225: Transmit STM-1 Section – E1 Byte Value Register (Address Location= 0x1943)

Transmit_E1_Byte_Value[7:0]								
R/W I	R/W R/W	R/W	R/W	R/W	R/W	R/W		
0	0 0	<b>6</b>	0	0	0	0		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E1_Byte_Value[7:0]	R/W	Transmit E1 Byte Value:
	me prosher	an an	If the appropriate "E1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E1 byte, within the "outbound" STM-1 signal.
	Ti dat di		If Bit 4 (E1 Byte Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "E1" byte-field, within each outbound STM-1 frame.
			<b>Note:</b> These register bits are ignored if Bit 4 (E1 Byte Insert Method) is set to "0".



#### Table 226: Transmit STM-1 Section – E2 Byte Control Register (Address Location= 0x1944)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Enable All STM-0s				Unused			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Enable All STM-	R/W	Enable All STM-0s:
	Os		This READ/WRITE bit-field permits the user to implement either of the following configurations options for software control of the E2 byte value, within the outbound STM-1 signal.
			0 – Configures the Transmit STM-1 SOH Processor block to read out the contents of the "Transmit STM-1 Section – E2 Byte Value" register and load that value into the E2 byte (within STM-0 # 1) within the outbound STM-1 signal.
			1 – Configures the Transmit STM-1 SOH Processor block to read out the contents of the 3 "shadow" registers, and to load these values into the E2 byte positions, within each corresponding STM-0 signal; within the outbound STM-1 signal.
			<b>Note:</b> This register bit is ignored if Bit 5 (E2 Byte Insert Method) within the "Transmit STM-1 Section – SONET Transmit Control Register Byte 1" (Address Location= 0x1902) is set to "0".
6 - 0	Unused	R/O	a no a

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#### Table 227: Transmit STM-1 Section – E2 Pointer Register (Address Location= 0x1946)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused						E2_Poir	nter[1:0]
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	E2_Pointer[1:0]	R/W	<ul> <li>E2 Pointer[3:0]: These READ/WRITE bit-fields permit the user to uniquely identify one of the 3 STM-0 E2 byte "shadow" registers, when performing read or write operations to these registers.</li> <li>If the user has set Bit 7 (Enable All STM-0s), within this register to "1", then the contents of these four register bits, act as a pointer to a given "shadow" register. Once the user specifies this pointer value; then he/she completes the read or write operation (to or from the "shadow" register) by performing a read or write to the "Transmit STM-1 Section – E2 Byte Value" register (Address Location= 0x1947).</li> <li>Valid "shadow" pointer values range from "0x00" to "0x02" (where the pointer value of "0x00" corresponds to the E2 "shadow" register, corresponding to STM-0 # () and so on).</li> <li>Note: This register bit is ignored if Bit 7 (Enable All STM-0s) is set to "1"; or if Bit 5 (E2 Byte Insert Method) within the "Transmit STM- 1 Section – SONET Transmit Control Register – Byte 1" (Address Location= 0x1902) is set to "0".</li> </ul>

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#### Table 228: Transmit STM-1 Section – E2 Byte Value Register (Address Location=0x1947)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_E2_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Transmit_E2_Byte_Value[7:0]	R/W	Transmit E2 Byte Value:
			The exact function of these register bits depends upon whether Bit 7 (Enable All STM-0s) within the "Transmit STM-1 Section – E2 Byte Control" Register (Address Location= 0x1944) has been set to "0" or "1"; as described below.
			If "Enable All STM 0s" is set to "0"
			If the appropriate "E2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E2 byte, within the "outbound" STM-1 signal. More specifically, this value will be loaded into the E2 byte position, within STM-0 # 1 (within the outbound STM-1 signal).
			If Bit 5 (E2 Insert Method) within the Transmit STM-1 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STM-1 SOH Processor block will load the contents of this register into the "E2" byte-field, within each outbound STM-1 frame.
		. 20	definition of the set to "1"
	Ś		In this mode, these register bit permit the user to have direct READ/WRITE access of the "STM-0 E2 Byte shadow" register; that is being pointed at by the "E2 Pointer[1:0]" value.
		t e	These register bits are ignored if Bit 5 (E2 Byte Insert Method) is set to "0".
	The product ar	Ŏ.	

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#### Table 229: Transmit STM-1 Section – J0 Byte Value Register (Address Location= 0x194B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_J0_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Transmit_J0_Value[7:0]	R/W	Transmit J0 Byte Value[7:0]:
			If the user has configured the Transmit STM-1 SOH Processor block to use the "Transmit J0 Byte Value" Register as the "source" of the "outbound" Section Trace Message, then these READ/WRITE bits will permit the user to specify the contents within the J0 byte of each outbound STM-1 frame. <b>Note:</b> This register is only valid if the Transmit STM-1 SOH Processor block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STM-1 frame. The user accomplishes this by setting the "Transmit Section Trace Message Source[1:0]" bit-fields (within the Transmit STM-1 Section – Transmit Section Trace Message Control Register Address = 0x194F) to "1, 0"

this by setting Source[1:0] Section – Tra Register - Add



Table 230: Transmit STM-1 Section – Transmit Section Trace Message Control Register (Address Location= 0x194F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Transmit Section Trace Messsage Length[1:0]		Transmit Section Trace Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION
7 – 4	Unused	R/O		
3-2	Transmit Section Trace Message Length[1:0]	R/W	These two READ/M the Section Trace block will repeated between the conter	Trace Message Length[1:0]: /RITE bit-fields permit the user to specify the length of message that the Transmit STM-1 SOH Processor dly transmit to the remote LTE. The relationship its of these bit-fields and the corresponding Transmit sage Length is presented below.
			Transmit Section Trace Message Length[1:0]	
			00	1 Byte
			01	16 Bytes
			10 or 11	64 Bytes
1 – 0	Transmit Section Trace Message Source[1:0]	R/W	These two READ/V	<b>Frace Message Source[1:0]:</b> VRITE bit-fields permit the user to specify the source Section Trace message that will be Sectioned via the ithin the outbound STM-1 data-stream, as depicted
	The prod	neet	Transmit Section Trace Message Source[1:0]	Resulting Source of the Section Trace Message.
	1.93.	6	00	Fixed Value:
	3			The Transmit STM-1 SOH Processor block will automatically set the J0 Byte, in each "outbound" STM-1 frame to the value "0x01".
			01	The "Transmit Section Trace Message Buffer".
				The Transmit STM-1 SOH Processor block will read out the contents within the Transmit Section Trace Message Buffer, and will transmit this message to the remote LTE.
				The "Transmit STM-1 SOH Processor block - Transmit Section Trace Message Buffer" Memory is located at Address Location 0x1B00 through 0x1B3F.
			10	From the "Transmit J0 Value[7:0]" Register.

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		11	From the "TxSOH" Input pin (pin F8).
			In this configuration setting, the Transmit STM-1 SOH Processor block will externally accept the contents of the "Section Trace Message" via the "TxSOH Input Port" and it will Section this message (via the J0 byte-channel) to the remote LTE.

## Table 231: Transmit STM-1 Section – Serial Port Control Register (Address Location= 0x1953)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		TxSOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
endn							

The formula that relates the contents of these register b	BIT NUMBER	NAME	Түре	DESCRIPTION
These READ/WRITE bit-fields permits the user to specify frequency of the "TxSOHCIk output clock signal. The formula that relates the contents of these register b	7 - 4	Unused	R/O	CALL COLOR
FREQ = 19.44 /[2 * (TxSOH_CLOCK_SPEED + 1) Note: For STM-1/STM-1 applications, the frequency of	3 - 0	TxSOH_CLOCK_SPEED[7:0]	R/W of of of are the	<ul> <li>These READ/WRITE bit-fields permits the user to specify the requency of the "TxSOHCIk output clock signal.</li> <li>The formula that relates the contents of these register bits to the "TxSOHCIk" frequency is presented below.</li> <li>FREQ = 19.44 /[2 * (TxSOH_CLOCK_SPEED + 1)</li> <li>Note: For STM-1/STM-1 applications, the frequency of the TxSOHCIk output signal must be in the range of</li> </ul>



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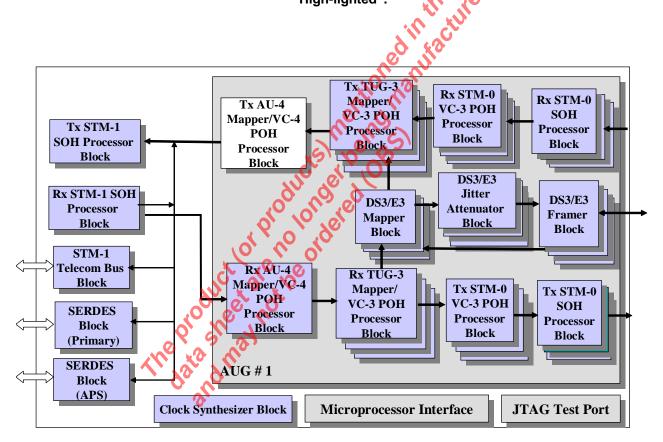
#### 1.8 TRANSMIT AU-4/VC-4 POH PROCESSOR BLOCK REGISTERS

The register map for the Transmit AU-4/VC-4 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit AU-4/VC-4 POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 whenever it has been configured to operate in the SDH/TUG-3 and the SDH/AU-3 modes, with the "Transmit AU-4/VC-4 POH Processor Block "highlighted" is presented below in Figure 5.

It should be noted that for Mapper Aggregation Applications, the Transmit AU-4 Mapper/VC-4 POH Processor block is only active if the user has configured the chip to operate in the SDH/TUG-3 Mapper Mode. This functional block is not active if the user configures the chip to operate in the SDH/AU-3 Mode.

# Figure 5: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the SDH/TUG-3 Mode), with the Transmit AU-4/VC-4 POH Processor Block "High-lighted".



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#### TRANSMIT AU-4/VC-4 POH PROCESSOR BLOCK REGISTERS

#### Table 232: Transmit AU-4/VC-4 POH Processor Block - Register Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0x1900 – 0x1981	Reserved	0x00
0x1982	Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1	0x00
0x1983	Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0	0x00
0x1984 – 0x1992	Reserved	0x00
0x1993	Transmit AU-4/VC-4 Path – Transmit J1 Byte Value Register	0x00
0x1994 – 0x1996	Reserved	0x00
0x1997	Transmit AU-4/VC-4 Path – B3 Byte Mask Register	0x00
0x1998 – 0x199A	Reserved	0x00
0x199B	Transmit AU-4/VC-4 Path – Transmit C2 Byte Value Register	0x00
0x199C – 0x199E	Reserved	0x00
0x199F	Transmit AU-4/VC-4 Path – Transmit G1 Byte Value Register	0x00
0x19A0 – 0x19A2	Reserved	0x00
0x19A3	Transmit AU-4/VC-4 Path – Transmit P2 Byte Value Register	0x00
0x19A4 – 0x19A6	Reserved	0x00
0x19A7	Transmit AU-4/VC-4 Path – Transmit H4 Byte Value Register	0x00
0x19A8 – 0x19AA	Reserved	0x00
0x19AB	Transmit AU-4/VC-4 Rath – Transmit Z3 Byte Value Register	0x00
0x19AC – 0x19AE	Reserved	0x00
0x19AF	Transmit AU-4/VC-4 Path – Transmit Z4 Byte Value Register	0x00
0x19B0 – 0x19B2	Reserved	0x00
0x19B3	Transmit AU-4AVC-4 Path – Transmit Z5 Byte Value Register	0x00
0x19B4 – 0x19B6	Reserved	0x00
0x19B7	Transmit AU-4/VC-4 Path – Transmit Path Control Register – Byte 0	0x00
0x19B8 – 0x19BA	Reserved	0x00
0x19BB	Transmit AU-4/VC-4 Path – Transmit J1 Control Register	0x00
0x19BC – 0x19BE	Reserved	0x00
0x19BF	Transmit AU-4/VC-4 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0x19C0 - 0x19C2	Reserved	0x00
0x19C3	Transmit AU-4/VC-4 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0x19C4 – 0x19C5	Reserved	0x00
0x19C6	Transmit AU-4/VC-4 Path – Transmit Pointer Byte Register – Byte 1	0x02



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Address Location	REGISTER NAME	DEFAULT VALUES
0x19C7	Transmit AU-4/VC-4 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0x19C8	Reserved	0x00
0x19C9	Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 2	0x40
0x19CA	Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 1	0xC0
0x19CB	Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 0	0xA0
0x19CC - 0x19CE	Reserved	0x00
0x19CF	Transmit AU-4/VC-4 Path – Transmit Path Serial Port Control Register	0x00
0x19D0 – 0x19FF	Reserved	0x00

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### 1.8.1 TRANSMIT AU-4/VC-4 POH PROCESSOR BLOCK REGISTER DESCRIPTION

#### Table 233: Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1 (Address Location= 0x1982)

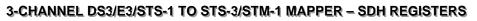
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 4	Unused	R/O	.6 2
3	Z5 Byte	R/W	Z5 Byte Insertion Type:
	Insertion Type		<ul> <li>This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to use either the contents within the "Transmit AU-4/VC-4 Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte, in the outbound VC-4 data-stream, as described below.</li> <li>0 – Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound VC-4.</li> </ul>
			1 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z5 byte position within each outbound VC-4.
			<b>Note:</b> The Address Location of the Transmit AU-4/VC-4 POH Processor Block - Transmit Z5 Byte Value Register is 0x19B3
2	Z4 Byte Insertion Type	R/W	<ul> <li>Z4 Byte Insertion Type:</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to use either the contents within the "Transmit AU-4/VC-4 Path – Transmit Z4 Byte Value" Register or the TxPOH input pin as the source for the Z4 byte, in the outbound VC-4 data-stream, as described below.</li> <li>Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit Z4 Byte Value" Register into the Z4 byte position within each outbound VC-4.</li> <li>Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the "TxPOH" input port) and to insert this data into the Z4 byte position within each outbound VC-4.</li> <li>Note: The address location of the Transmit AU-4/VC-4 POH Processor block -Transmit Z4 Byte Value Register is 0x19AF</li> </ul>
1	Z3 Byte	R/W	Z3 Byte Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit AU- 4/VC-4 POH Processor block to use either the contents within the "Transmit AU-4/VC-4 Path – Transmit Z3 Byte Value" Register or the TxPOH input pin as the source for the Z3 byte, in the outbound VC-4 data-stream, as described below.
			0 – Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound VC-4.
			1 - Configures the Transmit AU-4/VC-4 POH Processor block to accept



			<ul> <li>externally supplied data (via the "TxPOH" input port) and to insert this data into the Z3 byte position within each outbound VC-4.</li> <li>Note: The Address Location of the Transmit AU-4/VC-4 POH Processor block - Transmit Z3 Byte Value Register is 0x19AB</li> </ul>
0	H4 Byte Insertion Type	R/W	H4 Byte Insertion Type: This READ/WRITE bit-field permits the user to configure the Transmit AU- 4/VC-4 POH Processor block to use either the contents within the "Transmit AU-4/VC-4 Path – Transmit H4 Byte Value" Register or the TxPOH input pin as the source for the H4 byte, in the outbound VC-4 data-stream, as described below.
			0 – Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound VC-4.
			1 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound VC-4.
			<b>Note:</b> The Address Location of the Transmit AU-4/VC-4 POH Processor block -Transmit H4 Byte Value Register is 0x19A7

The Address Location of block - Transmit H4 Byte





#### Table 234: Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0 (Address Location= 0x1983)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F2 Byte Insertion Type		Insertion a[1:0]		Insertion e[1:0]	C2 Byte Insertion Type	Unused	Force Transmission of AU-AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	F2 Byte	R/W	F2 Byte Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to use either the contents within the "Transmit AU-4/VC-4 Path – Transmit F2 Byte Value" Register or the TxPOH input pin as the source for the F2 byte, in the outbound VC-4 data-stream, as described below.
			0 – Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit F2 Byte Value" Register into the F2 byte position within each outbound VC-4.
			1 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound VC-4.
			<b>Note:</b> The Address Location of the Transmit AU-4/VC-4 POH Processor block -Transmit F2 Byte Value Register is 0x19A3
6 - 5	HP-REI	R/W	HP-REI Insertion Type[1:0]:
	Insertion Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit AU-4/VC-4 POH Processor block to use one of the three following sources for the HP-REI bit-fields (e.g., bits 1 through 4, within the G1 byte) within each outbound VC-4.
		The pro	• From the Receive AU-4/VC-4 POH Processor block (e.g., the Transmit AU- 4/VC-4 POH Processor block will set the HP-REI bit-fields to the appropriate value, based upon the number of B3 byte errors that the Receive AU-4/VC-4 POH Processor block detects and flags, within its incoming VC-4 data-stream).
			From the "Transmit G1 Byte Value" Register. In this case, the Transmit AU- 4/VC-4 POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit AU-4/VC-4 POH Processor block – Transmit G1 Byte Value" Register into the HP-REI bit-fields within each outbound VC-4.
		0	From the "TPOH" input pin. In this case, the Transmit AU-4/VC-4 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the HP-REI bit-fields within each outbound VC-4.
			00/11 – Configures the Transmit AU-4/VC-4 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the Receive AU-4/VC-4 POH Processor block detects and flags within the incoming STS-3c data-stream.
			01 – Configures the Transmit AU-4/VC-4 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit AU-4/VC-4 POH Processor block - Transmit G1 Byte Value" register.
			10 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the HP-REI bit-positions within each outbound VC-4.
			Note: The address location of the Transmit AU-4/VC-4 POH Processor block



			- Transmit G1 Byte Value Register is 0x199F
4 - 3	HP-RDI Insertion Type[1:0]	R/W	<b>HP-RDI Insertion Type[1:0]:</b> These two READ/WRITE bit-fields permit the user to configure the Transmit AU-4/VC-4 POH Processor block to use one of the three following sources for the HP-RDI bit-fields (e.g., bits 5 through 7, within the G1 byte) within each outbound VC-4.
			• From the corresponding Receive AU-4/VC-4 POH Processor block (e.g., the Transmit AU-4/VC-4 POH Processor block will set the HP-RDI bit-fields to the appropriate value, based upon which defect conditions are being declared by the Receive AU-4/VC-4 POH Processor block, within its incoming VC-4 data-stream).
			• From the "Transmit G1 Byte Value" Register. In this case, the Transmit AU- 4/VC-4 POH Processor block will insert the content of bits 2 through 0 within the "Transmit AU-4/VC-4 POH Processor block – Transmit G1 Byte Value" Register into the HP-RDI bit-fields within each outbound VC-4.
			• From the "TPOH" input pin. In this case, the Transmit AU-4/VC-4 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the HP-RDI bit-fields within each outbound VC-4.
			00/11 – Configures the Transmit AU-4/VC-4 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the defects conditions that the Receive AU-4/VC-4 POH Processor block is currently declaring within the incoming STS-3c data-stream.
			01 – Configures the Transmit-AU-4/VC-4 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit AU-4/VC-4 POH Processor block - Transmit G1 Byte Value" register.
			10 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the HP-RDI bit-positions within each outbound VC-4.
			<b>Note:</b> The address location of the Transmit AU-4/VC-4 POH Processor block - Transmit G1 Byte Value Register is 0x199F
2	C2 Byte	R/W	C2 Byte Insertion Type:
	Insertion Type	logy r	This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC- 4 POH Processor block to use either the contents within the "Transmit AU- 4/VC-4 Path – Transmit C2 Byte Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound VC-4 data-stream, as described below.
	The	and	O – Configures the Transmit AU-4/VC-4 POH Processor block to insert the contents within the "Transmit AU-4/VC-4 Path – Transmit C2 Byte Value" Register into the C2 byte-position within each outbound VC-4.
		•	1 – Configures the Transmit AU-4/VC-4 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the C2 byte position within each outbound VC-4.
			<b>Note:</b> The address location of the Transmit AU-4/VC-4 POH Processor block - Transmit C2 Byte Value Register is 0x199B
1	Unused	R/O	
0	Force	R/W	Force Transmission of AU-AIS:
	Transmission of AU-AIS		This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to (via software control) transmit the AU-AIS indicator to the remote PTE.
			If this feature is enabled, then the Transmit AU-4/VC-4 POH Processor block will automatically set the H1, H2, H3 and all the "outbound" VC-4 bytes to an "All Ones" pattern, prior to routing this data to the Transmit STM-1SOH



Processor block.
0 – Configures the Transmit AU-4/VC-4 POH Processor block to NOT transmit the AU-AIS indicator to the remote PTE. In this case, the Transmit AU-4/VC-4 POH Processor block will transmit "normal" traffic to the remote PTE.
1 – Configures the Transmit AU-4/VC-4 POH Processor block to transmit the AU-AIS indicator to the remote PTE.

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

#### Table 235: Transmit AU-4/VC-4 Path – Transmitter J1 Byte Value Register (Address Location= 0x1993)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_J1_Byte[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit J1 Byte	R/W	Transmit J1 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound VC-4.
			If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte tocation, within each "outbound" VC-4. This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Transmit Path Trace Message Source[1:0]) within the "Transmit AU-4/VC-4 Path – SONET Path Trace Message Control Register" register. <b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – SONET J1 Byte Control Register is 0x19BB

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



## Table 236: Transmit AU-4/VC-4 Path – Transmitter B3 Byte Error Mask Register (Address Location= 0x1997)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit B3 Byte Error_Mask[7:0]	R/W	Transmit B3 Byte Error Mask[7:0]:
			This READ/WRITE bit-field permits the user to insert errors into the B3 byte within each "outbound" VC-4, prior to transmission to the Transmit STM-1SOH Processor block.
			The Transmit AU-4/VC-4 POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte-position within each "outbound" VC-4.
			If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error.
			<b>Note:</b> For normal operation, the user should set this register to 0x00.

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#### Table 237: Transmit AU-4/VC-4 Path – Transmit C2 Byte Value Register (Address Location= 0x199B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_C2_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit C2 Byte	R/W	Transmit C2 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound VC-4.
			If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" VC-4. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Byte Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" register. <b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – SONET Control Control Register – Byte 0" Register is 0x1983

## Table 238: Transmit AU-4/VC-4 Path – Transmit G1 Byte Value Register (Address Location= 0x199F)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0
			Transmit_G1_By	te_Value[7:0]			
R/W	R/W	R/W	R/W	V R/W	R/W	R/W	R/W
0	0	0	8.0.8	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	de la companya de la	Transmit G1 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the contents of the HP-RDI and HP-REI bit-fields, within each G1 byte in the "outbound" VC-4. If the users sets "HP-REI_Insertion_Type[1:0]" and "HP- RDI_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the HP- REI and the HP-RDI bit-fields (within each G1 byte of the "outbound" VC-4) will be dictated by the contents of this register.
			Note:
			1. The "HP-REI_Insertion_Type[1:0]" and "HP-RDI_Insertion_Type[1:0]" bit- fields are located in the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" Register.
			2. The Address Location of the Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" Register is 0x1983

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 239: Transmit AU-4/VC-4 Path – Transmit F2 Byte Value Register (Address Location= 0x19A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_F2_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit F2 Byte	R/W	Transmit F2 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound VC-4.
			If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" VC-4. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" register. <b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – SONET Control Control Register is 0x1983

#### Table 240: Transmit AU-4/VC-4 Path – Transmit H4 Byte Value Register (Address Location= 0x19A7)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0		0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	Rav	<ul> <li>Transmit H4 Byte Value:</li> <li>These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound VC-4.</li> <li>If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" VC-4.</li> <li>This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1" register.</li> <li>Note: The Address Location for the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1" register is 0x1982</li> </ul>



#### Table 241: Transmit AU-4/VC-4 Path – Transmit Z3 Byte Value Register (Address Location= 0x19AB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	0 Transmit Z3 Byte R/W Value[7:0]		Transmit Z3 Byte Value:
			These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound VC-4.
			If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" VC-4. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1" register. <b>Note:</b> The Address Location for the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 1" register is 0x1982

#### Table 242: Transmit AU-4/VC-4 Path – Transmit Z4 Byte Value Register (Address Location= 0x19AF)

Віт 7	Віт 6	Віт 5	BIT 4	Вт 3	Віт 2	Віт 1	Віт 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0 0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	TYPE	DESCRIPTION
7 - 0	Transmit Z4 Byte R/W		Transmit Z4 Byte Value:
	Value[7:0]	8 . N?	hese READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound VC-4.
	1.93		If the user configures the Transmit AU-4/VC-4 POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" VC-4.
			This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" register.
			<b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" Register is 0x1982

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#### Table 243: Transmit AU-4/VC-4 Path – Transmit Z5 Byte Value Register (Address Location= 0x19B3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit Z5 Byte	R/W	Transmit Z5 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound VC-4.
			If the user configures the Transmit AU-4//C-4 POH Processor block to this register as the source of the Z5 byte then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" VC-4. This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit AU-4/VC-4 Path – SONET Control Register – Byte 0" register. <b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – SONET Control Control Register – Byte 0" register is 0x1982

#### Table 244: Transmit AU-4/VC-4 Path – Transmit Path Control Register (Address Location= 0x19B7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	Pointer Force:
			This READ/WRITE bit-field permits the user to load the values contained within the "Transmit AU-4/VC-4 POH Arbitrary H1 Pointer Byte" and "Transmit AU-4/VC-4 POH Arbitrary H2 Pointer Byte" registers into the H1 and H2 bytes (within the outbound STS-3c data stream).
			<b>Note:</b> The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition.
			0 – Configures the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks to transmit STS-3c/STM-1data with normal and correct H1 and H2 bytes.
			1 – Configures the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-3c/STM-1 data-stream) with the values in the "Transmit AU-4/VC-4 POH Arbitrary H1 and H2 Pointer Byte" registers.
			Note: The Address Location of the Transmit AU-4/VC-4 Arbitrary H1 Pointer Byte register is 0x19BF
		duc	2. The Address Location of the Transmit AU-4/VC-4 Arbitrary H2 Pointer Byte register is 0x19C3
4	Check Stuff	R/W	Check Stuff Monitoring:
	The d	310	This READ/WRITE bit-field permits the user to configure the Transmit AU- 4/VC-4 POH and Transmit STM-1 SOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods.
			0 – Disables this feature.
			In this mode, the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods.
			1 – Enables this feature.
			In this mode, the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.
3 Insert Negative R/W Insert Negative Stuff:		Insert Negative Stuff:	
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit AU-

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			4/VC-4 POH and Transmit STM-1 SOH Processor blocks to insert a negative- stuff into the outbound STS-3c/STM-1 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STM-0/STM-1 data stream).
			• The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on.
			<b>Note:</b> Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2	Insert Positive	R/W	Insert Positive Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit AU- 4/VC-4 POH and Transmit STM-1 SOH Processor blocks to insert a positive- stuff into the outbound STS-3c/STM-1 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-3c/STM-1 data-stream, immediately after the H3 byte position within the outbound STS-3c/STM-1 data stream).
			• The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on.
			<b>Note:</b> Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
1	Insert Continuous	R/W	Insert Continuous NDF Events:
	NDF Events	e proc	This READ/WRITE bit-field permits the user configure the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STM-1 data stream.
	~*	93.0	As the Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor blocks insert the NDF event into the STM-0/STM-1 data stream, it will proceed to load in the contents of the "Transmit AU- 4/VC-4 POH Arbitrary H1 Pointer" and "Transmit AU-4/VC-4 POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STS-3c/STM-1 data stream).
			0 – Configures the "Transmit AU-4/VC-4 SOH and Transmit STM-1 POH Processor" blocks to not continuously insert NDF events into the "outbound" STS-3c/STM-1 data stream.
			1- Configures the "Transmit AU-4/VC-4 POH and Transmit STM-1 SOH Processor" blocks to continuously insert NDF events into the "outbound" STS-3c/STM-1 data stream.
0	Insert Single	R/W	Insert Single NDF Event:
	NDF Event		This READ/WRITE bit-field permits the user to configure the Transmit AU- 4/VC-4 POH and Transmit STM-1 SOH Processor blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STM-1 data stream.



Writing a "0" to "1" transition into this bit-field causes the following to happen.
• The "N" bits, within the H1 byte will set to the value "1001"
• The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit AU-4/VC-4 POH – Arbitrary H1 Pointer" and "Transmit AU-4/VC-4 POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3).
• Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on.
Note:
1. Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2. The Address Location of the Transmit AU-4/VC-4 Arbitrary H1 Pointer Byte register is 0x19BF
3. The Address Location of the Transmit AU-4/VC-4 Arbitrary H2 Pointer Byte register is 0x19C3
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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 245: Transmit AU-4/VC-4 Path – Transmit Path Trace Message Control Register (Address Location= 0x19BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Path Trace Length[1:0]	Transmit Path Trace Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION			
7 – 4	Unused	R/O					
3 - 2	Transmit Path Trace Message_Length[1:0]	R/W	These READ/WRITE It Path Trace Message, will repeatedly transmi content of these bit-fi Length is presented be	Message Length[1:0]: bit-fields permit the user to specify the ler that the Transmit AU-4/VC-4 POH Proce- it to the remote PTE. The relationship be ields and the corresponding Path Trace elow	ssor block etween the		
			00	1 Byte			
			01	16 Bytes			
			10/11	64 Bytes			
1 - 0	Transmit Path Trace Message Source[1:0]				These READ/WRITE to Coutbound" Path Trace channel within the outb	Message Source[1:0]: bit-fields permit the user to specify the sou e Message that will be transported via th bound STS-3c data-stream, as depicted be Resulting Source of the Path Tra Message Fixed Value: The Transmit AU-4/VC-4 POH Pro	ne J1 byte elow. Ice
	. 90			block will automatically set the J1 byte, each outbound VC-4 to the value "0x00			
		01	The Transmit Path Trace Message Be The Transmit AU-4/VC-4 POH Pro block will read out the contents with Transmit Path Trace Message buffer, a transmit this message to the remote PT The Transmit AU-4/VC-4 POH Pro block – Transmit Path Trace Message Memory is located at Address Loc 0x1D00 through 0x1D3F.	icessor hin the and will E. icessor Buffer			
			10	From the "Transmit J1 Byte Value Register:			
				In this setting, the Transmit AU-4/VC-4 Processor block will read out the conte			



	the "Transmit AU-4/VC-4 Path – Transmit J1 Byte Value Register, and will insert this value into the J1 byte-position within each outbound VC-4.
11	From the "TxPOH" Input pin: In this configuration setting, the Transmit AU- 4/VC-4 POH Processor block will externally accept the contents of the "Path Trace Message" via the "TxPOH Input Port" and it will transport this message (via the J1 byte- channel) to the remote PTE.

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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 246: Transmit AU-4/VC-4 Path – Transmit Arbitrary H1 Byte Pointer Register (Address Location= 0x19BF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
NDF Bits				SS	Bits	H1 Pointer Value		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	NDF Bits	R/W	NDF (New Data Flag) Bits:
			These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit AU-4/VC-4 Path – Transmit Path Control" Register.
			<b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – Transmit Path Control register is 0x19B7
3 - 2	SS Bits	R/W	<ul> <li>SS Bits</li> <li>These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit AU-4/VC-4 Path – Transmit Path Control" Register</li> <li><i>Note:</i></li> <li>1. For SONET Applications, the "SS" bits have no functional value, within the H1 byte.</li> <li>2. The Address Location of the Transmit AU-4/VC-4 Path – Transmit Path Control register is 0x19B7</li> </ul>
1 - 0	H1 Pointer Value[1:0]	R/W	<ul> <li>H1 Pointer Value[1:0]: These two READ/WRITE bit-fields, along with the constants of the "Transmit AU-4/VC-4 Rath – Transmit Arbitrary H2 Byte Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the 10-bit Pointer Word.</li> <li>These two READ/WRITE bit-fields permit the user to define the value of the two most significant bits within the Pointer word.</li> <li>Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit AU-4/VC-4 Path – Transmit Path Control" Register, the values of these two bits will be loaded into the two most significant bits within the Pointer Word.</li> <li>Note: The Address Location of the Transmit AU-4/VC-4 Path – Transmit Path Control register is 0x19B7</li> </ul>



Table 247: Transmit AU-4/VC-4 Path – Transmit Arbitrary H2 Byte Pointer Register (Address Location= 0x19C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	H2 Pointer	R/W	H2 Pointer Value[1:0]:
	Value[7:0]		These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit AU-4/VC-4 Path – Transmit Arbitrary H1 Pointer" Register permit the user to provide the contents of the 10-bit Pointer Word.
			These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word.
			Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit AU-4/VC-4 Path – Transmit Path Control" Register, the values of these eight bits will be loaded into the H2 byte, within the outbound STS-
			3c/STM-1 data stream.
			1. The Address Location of the Transmit AU-4/VC-4 Path – Transmit Arbitrary H1 Pointer" register is 0x19C3
			2. The Address Location of the Transmit AU-4/VC-4 Path – Transmit Path Control register is 0x1987

Table 248: Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte Register – Byte 1 (Address Location= 0x19C6)

Віт 7	Віт 6	Віт 5 Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
		Tx_Pointer	r_High[1:0]				
R/O	R/O	R/O R/O	R/O	R/O	R/O	R/O	
0	0	e e e	0	0	1	0	

BIT NUMBER	NAME 0	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	Tx_Pointer_ High[1:0]	RO	<ul> <li>Transmit Pointer Word – High[1:0]:</li> <li>These two READ-ONLY bits, along with the contents of the "Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte Register – Byte 0" reflect the current value of the pointer (or offset of the VC-4 within the outbound STS-3c frame).</li> <li>These two bits contain the two most significant bits within the "10-bit pointer" word.</li> <li>Note: The Address Location of the Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C7</li> </ul>

## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 249: Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0x19C7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	1	0	1	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Tx_Pointer_ Low[7:0]	R/O	DESCRIPTION         Transmit Pointer Word – Low[7:0]:         These two READ-ONLY bits, along with the contents of the "Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte Register – Byte 1" reflect the current value of the pointer (or offset of the VC-4 within the output STS-3c frame).         These two bits contain the eight least significant bits within the "10-bit pointer"
			word. <b>Note:</b> The Address Location of the Transmit AU-4/VC-4 Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C6

Address Location of the second second



## Table 250: Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 2 (Address Location= 0x19C9)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		PLM-I	PLM-P HP-RDI Code[2:0]		Transmit HP-RDI upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 - 1	PLM-P HP-RDI	R/W	PLM-P (Path – Payload Mismatch) Defect – HP-RDI Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit AU-4/VC-4 POH Processor block will transmit, within the HP-RDI bit fields of the G1 byte (within each "outbound" VC-4), whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block detects and declares the PLM-P defect condition. <b>Note:</b> In order to enable this feature, the user must set Bit 0 (Transmit HP-RDI upon PLM-P) within this register to "1".
0	Transmit HP-RDI upon PLM-P	R/W	Transmit the HP-RDI Indicator upon declaration of the PLM-P defect condition:
	the produce	eet not	This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the PLM-P defect condition.





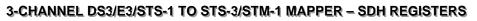
## Table 251: Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 1 (Address Location= 0x19CA)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2 Віт 1		Віт 0		
TIM-P	HP-RDI Coo	de[2:0]	Transmit HP-RDI upon TIM-P			Transmit HP-RDI upon UNEQ-P		
R/W	R/W	R/W	R/W	R/W R/W R/W		R/W		
1	1	0	0	0	0	0	0	

7 - 5       TIM-P HP-RDI Code[2:0]       R/W       TIM-P (Path - Trace Identification Mismatch) Det Code:         These three READ/WRITE bit-fields permit the user value that the Transmit AU-4/VC-4/POH Process	to specify the
transmit, within the HP-RDL bit-fields of the G1 byt "outbound" VC-4), whenever (and for the duration the AU-4/VC-4 POH Processor block detects and decla defect condition.	te (within each at) the Receive
<b>Note:</b> In order to enable this feature, the user in (Transmit HP-RDI upon TIM-P) within this re	
4 Transmit HP-RDI upon R/W Transmit the HP-RD Indicator upon declaration defect condition:	of the TIM-P
This READ/WRITE bit-field permits the user to configure AU-4/VC-4 POH Processor block to automatically transport of the configured in Bits 7 through 5 – within towards the remote PTE whenever (and for the due Receive AU-4/VC-4 POH Processor block declares the condition.	ansmit the HP- in this register) ration that) the
0 - Configures the Transmit AU-4/VC-4 POH Processor automatically transmit the HP-RDI indicator wheneve duration that) the Receive AU-4/VC-4 POH Processor the TIM-P defect condition.	er (and for the
duration that) the Receive AU-4/VC-4 POH Processor the TIM-P defect condition. O- Configures the Transmit AU-4/VC-4 POH Processor automatically transmit the HP-RDI indicator whenever duration that) the Receive AU-4/VC-4 POH Processor the TIM-P defect condition. NOTE: The Transmit AU-4/VC-4 POH Processor blo the HP-RDI indicator (in response to the Receive A Processor block declaring the TIM-P defect condition) HP-RDI bit-fields (within each outbound VC-4) to the	er (and for the
<b>NOTE:</b> The Transmit AU-4/VC-4 POH Processor blo the HP-RDI indicator (in response to the Receive A Processor block declaring the TIM-P defect condition) HP-RDI bit-fields (within each outbound VC-4) to the the "TIM-P HP-RDI Code[2:0]" bit-fields within this regi	U-4/VC-4 POH ) by setting the contents within
3 - 1 UNEQ-P HP-RDI R/W UNEQ-P (Path – Unequipped) Defect – HP-RDI Cod	e:
Code[2:0] These three READ/WRITE bit-fields permit the user value that the Transmit AU-4/VC-4 POH Proces transmit, within the HP-RDI bit-fields of the G1 byt "outbound" VC-4), whenever (and for the duration tha AU-4/VC-4 POH Processor block detects and declare defect condition.	sor block will te (within each at) the Receive
<b>Note:</b> In order to enable this feature, the user in (Transmit HP-RDI upon UNEQ-P) within this	
0     Transmit HP-RDI upon UNEQ-P     R/W     Transmit the HP-RDI indicator upon declaration of defect condition:	of the UNEQ-P



This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the UNEQ-P defect condition.
0 – Configures the Transmit AU-4/VC-4 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the UNEQ-P defect condition.
1 – Configures the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the UNEQ-P defect condition.
<b>NOTE:</b> The Transmit AU-4/VC-4 POH Processor block will transmit the HP-RDI indicator (in response to the Receive AU-4/VC-4 POH Processor block declaring the UNEQ-P defect condition) by setting the HP-RDI bit-fields (within each outbound VC-4) to the contents within the "UNEQ-P HP-RDI Code[2:0]" bit-fields within this register.





## Table 252: Transmit AU-4/VC-4 Path – HP-RDI Control Register – Byte 1 (Address Location= 0x19CB)

Віт 7	Віт 6	Віт 5	BIT 4 BIT 3 BIT 2 BIT 1		Віт 0		
AU-LC	P HP-RDI Co	de[2:0]	Transmit HP- RDI upon AU-LOP	AU-A	Transmit HP-RDI upon AU-AIS		
R/W	R/W	R/W	R/W	R/W R/W R/W		R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	AU-LOP HP-RDI	R/W	AU-LOP (Path – Loss of Pointer) Defect – HP-RDI Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit AU-4/VC-4 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within each "outbound" VC-4), whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block detects and declares the AU-LOP defect condition.
			<b>Note:</b> In order to enable this feature, the user must set Bit 4 (Transmit HP-RD) upon AU-LOP) within this register to "1".
4	Transmit HP-RDI upon AU-LOP	R/W	Transmit the HR-RDI indicator upon declaration of the AU-LOP defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-LOP defect condition.
		uct of	0 – Configures the Transmit AU-4/VC-4 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-LOP defect condition.
	PIC	d'reet	1 Configures the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-LOP defect condition.
	The pro	nome	<b>NOTE:</b> The Transmit AU-4/VC-4 POH Processor block will transmit the HP-RDI indicator (in response to the Receive AU-4/VC-4 POH Processor block declaring the AU-LOP defect condition) by setting the HP-RDI bit-fields (within each outbound VC-4) to the contents within the "AU-LOP HP-RDI Code[2:0]" bit-fields within this register.
3 - 1	AU-AIS HP-RDI	R/W	AU-AIS (Path – AIS) Defect – HP-RDI Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit AU-4/VC-4 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within the "outbound" VC-4), whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block detects and declares the AU-AIS defect condition.
			<b>Note:</b> In order to enable this feature, the user must set Bit 0 (Transmit HP-RDI upon AU-AIS) within this register to "1".
0	Transmit HP-RDI upon AU-AIS	R/W	Transmit the HP-RDI Indicator upon declaration of the AU-AIS defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit



AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-AIS defect condition.

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0 – Configures the Transmit AU-4/VC-4 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-AIS defect condition.

1 – Configures the Transmit AU-4/VC-4 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive AU-4/VC-4 POH Processor block declares the AU-AIS defect condition.

**NOTE:** The Transmit AU-4/VC-4 POH Processor block will transmit the HP-RDI indicator (in response to the Receive AU-4/VC-4 POH Processor block declaring the AU-AIS defect condition) by setting the HP-RDI bit-field (within each outbound VC-4) to the contents within the "AU-AIS HP-RDI Code[2:0]" bit-fields within this register.

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## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 253: Transmit AU-4/VC-4 Path – Serial Port Control Register (Address Location= 0x19CF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			TxPOH Clock Speed [3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 - 0	TxPOH Clock Speed [3:0]	R/W	TxPOHClk Output Clock Signal Speed:         These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHClk output clock signal. The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below.         FREQ = 19.44/[2 * (TxPOH_CLOCK_SPEED + 1)         Note: For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHZ

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#### 1.9 RECEIVE TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK

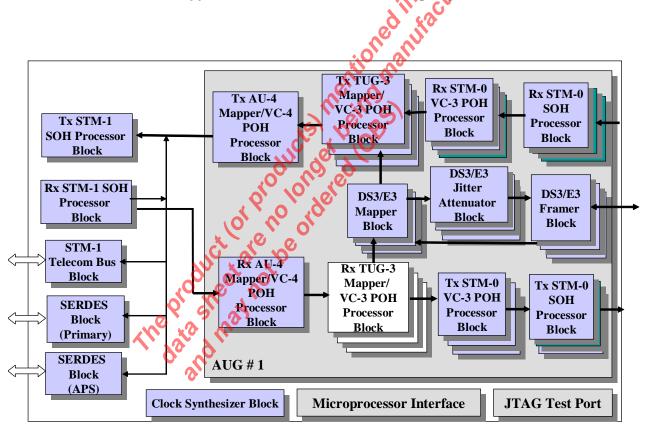
The register map for the Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor" block registers is presented below.

Throughout the XRT94L33 documentation, this particular functional block is actually represented by the following two functional blocks.

- The Receive TUG-3 Mapper/VC-3 POH Processor Block (for SDH/TUG-3 Applications)
- The Receive AU-3 Mapper/VC-3 POH Processor Block (for SDH/AU-3 Applications)

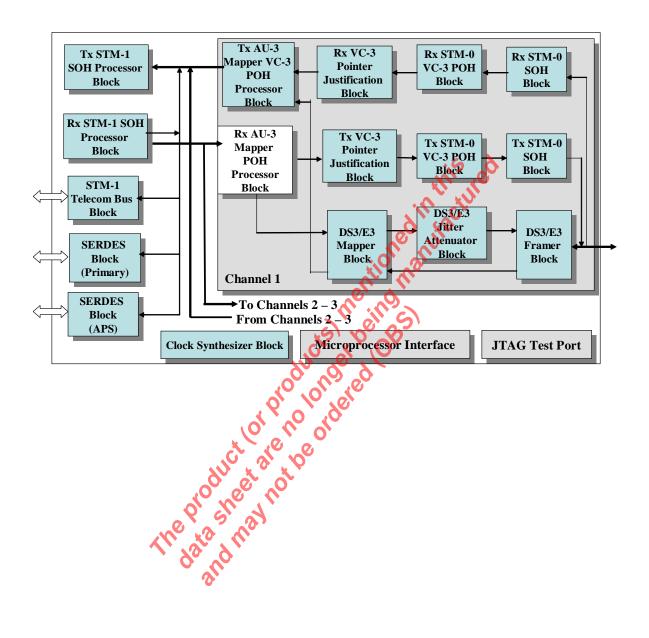
In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 (whenever it has been configured to operate in the SDH/TUG-3 Mode), with the "Receive TUG-3/Mapper VC-3 POH Processor Block "highlighted" is presented below in Figure 6.

Figure 6: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block "High-lighted".





#### Figure 3, Illustration of the Functional Block Diagram of the XRT94L33, with the Receive AU-3 Mapper/VC-3 POH Processor Block "Highlighted"

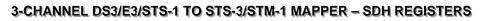




## Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Register

## Table 254: Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block Register - Address Map

Address Location	REGISTER NAME	DEFAULT VALUE
0xN000 – 0xN181	Reserved	0x00
0xN182	Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 1	0x00
0xN183	Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 0	0x00
0xN184, 0xN185	Reserved	0x00
0xN186	Receive TUG-3/AU-3 Mapper VC-3 Path – Status Register – Byte 1	0x00
0xN187	Receive TUG-3/AU-3 Mapper VC-3 Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte	0x00
0xN18B	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Status Register – Byte	0x00
0xN18C	Reserved	0x00
0xN18D	Receive TUG-3/AU-3 Mapper VC-3 Path - Interrupt Enable Register - Byte 2	0x00
0xN18E	Receive TUG-3/AU-3 Mapper VC 3 Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive TUG-3/AU-3 Mapper VC-3 Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive TUG 3/AU 3 Mapper VC-3 Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Byte (C2) Register	0x00
0xN197	Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Byte (C2) Register	0x00
0xN198	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 3	0x00
0xN199	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 2	0x00
0xN19A	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 1	0x00
0xN19B	Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 0	0x00





Address Location	REGISTER NAME	DEFAULT VALUES
0xN19C	Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 3	0x00
0xN19D	Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 2	0x00
0xN19E	Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 1	0x00
0xN19F	Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 0	0x00
0xN1A0 - 0xN1A2	Reserved	0x00
0xN1A3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receiver J1 Byte Control Register	0x00
0xN1A4, 0xN1A5	Reserved	
0xN1A6	Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value Register– Byte 1	0x00
0xN1A7	Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value Register – Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive TUG-3/AU-3 Mapper VC-3 Pather AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive TUG-3/AU-3 Mapper VC-3 Path – Serial Port Control Register	0x00
0xN1C0 - 0xN1C2	Reserved	0x00
0xN1C3	Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 - 0xN1D2	Reserved	0x00
0xN1D3	Receive TUG 3/AU 3 Mapper VC-3 Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved of	0x00
0xN1DB	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive C2 Byte Capture Register	0x00
0xN1DC - 0xN1DE	Reserved	0x00
0xN1DF	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive G1 Byte Capture Register	0x00
0xN1E0 - 0xN1E2	Reserved	0x00
0xN1E3	Receive TUG-3/AU-3 Mapper VC-3 Path - Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00



#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Address Location	REGISTER NAME	DEFAULT VALUES
0xN1E7	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN1FF	Reserved	0x00

---- Receiv



### 1.9.1 RECEIVE TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 255: Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 1 (Address Location= 0xN182, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unused							
							Async PDI-P or	
							AU-AIS/TU-AIS	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W	
0	0	0	0	0	0	0	0	

7-1       Unused       R/O         0       DS3 AIS upon Async PDI-P or AU-AISTU-AIS:         PDI-P or AU-AIS/TU-AIS       This READ/WRITE bit-field permits the user to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer Block to transmit the DS3 AIS indicator (to downstream circuitry) whenever (and for the ouration that) it (the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block) declares the Async PDI-P or AU-AIS/TU-AIS defect condition within the inoming VC-3 adta-stream.         0       Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the DS3 AIS indicator (via the Egress Direction) upon declaration of either the AU-AIS/TU-AIS or the Async PDI-P defect conditions.         1       Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the DS3 AIS indicator whenever (and for the duration that) it declares either the AU-AIS/TU-AIS or the Async PDI-P defect conditions.         1       Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the DS3 AIS indicator whenever (and for the duration that) it declares either the AU-AIS/TU-AIS or the Async PDI-P defect condition.         Nore:       This register bit is only valid if the incoming VC-3 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "Low-Speed" Side of the chip) is configured to operate in the DS3 Mode. Whenever a VC-3 signal is transporting an asynchronous/Mapped DS3 signal, then a given PTE will recognize and declare the PDI-P defect condition whenever it "accepts" the C2 byte to the value "WFC".	BIT NUMBER	NAME	Түре	DESCRIPTION
upon Async PDI-P or AU-AIS/TU- AIS       This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer Block to transmit the DS3 AIS indicator (to downstream circuitry) whenever (and for the duration that) it (the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block) declares the Async PDI-P or AU-AIS/TU- AIS defect condition within the incoming VC-3 data-stream.         0 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator (via the Bgress Direction) upon declaration of either the AU-AIS/TU-AIS or the Async PDI-P defect conditions.         1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator whenever (and for the duration that) it declares either the AU- AIS/TU-AIS on the PDI-P defect condition.         Note:       This register bit is only valid if the incoming VC-3 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "Low-Speed" Side of the chip) is configured to operate in the DS3 Wode. Whenever a VC-3 signal is transporting an asynchronous proped DS3 signal, then a given PTE will recognize and declare the PDI-P defect condition whenever it "accepts" the C2 byte to the value	7 – 1	Unused	R/O	this rec
× 8° × 0	0	upon Async PDI-P or AU-AIS/TU-	R/W	<ul> <li>This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer Block to transmit the DS3 AIS indicator (to downstream circuitry) whenever (and for the duration that) it (the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block) declares the Async PDI-P or AU-AIS/TU-AIS defect condition within the incoming VC-3 data-stream.</li> <li>0 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator (via the Egress Direction) upon declaration of either the AU-AIS/TU-AIS or the Async PDI-P defect conditions.</li> <li>1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator (via the Egress Direction) upon declaration of either the AU-AIS/TU-AIS or the Async PDI-P defect conditions.</li> <li>1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator whenever (and for the duration that) it declares either the AU-AIS/TU-AIS or the PDI-P defect condition.</li> <li>Note: This register bit is only valid if the incoming VC-3 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "Low-Speed" Side of the chip) is configured to operate in the DS3 Mode. Whenever a VC-3 signal is transporting an asynchronously-mapped DS3 signal, then a given PTE will recognize and declare the PDI-P defect condition whenever it "accepts" the C2 byte to the value</li> </ul>



Table 256: Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 0 (Address Location= 0xN183, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Check	RDI-P	HP-REI/	B3 Error Type
				Stuff	Туре	LP-REI	
						Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 4	Unused	R/O	.6 2
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.
			0 – Disables this SONET standard implementation. In this mode, all pointer- adjustment operations that are detected will be accepted.
			1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation, will be ignored.
2	RDI-P Type	R/W	Path – Remote Defect Indicator Type Select:
			This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P form of signaling, as described below.
		duct	0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will only monitor Bit 5, within the G1 byte (of incoming SPE data), in order to declare and clear the RDI-P defect condition.
	thep	s he	Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block support the Enhanced RDI-P (ERDI-P). In this mode, the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.
1	HP-REI/LP-RE	R/W	HP-REI/LP-REI Error Type:
	Error Type	<b>V</b>	This READ/WRITE bit-field permits the user to specify how the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will count (or tally) HP-REI/LP-REI events, for Performance Monitoring purposes. The user can configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment HP-REI/LP-REI events on either a "per-bit" or "per-frame" basis. If the user configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment HP-REI/LP-REI events on a "per-bit" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment HP-REI/LP-REI events on a "per-bit" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 Path HP-REI/LP-REI Event Count" register by the value of the lower nibble within the G1 byte of the incoming STM-0 data-stream.
			If the user configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment HP-REI/LP-REI events on a "per-frame" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 Path HP-REI/LP-REI Event Count" Register each time it receives an STM-0 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value.

		0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to count or tally HP-REI/LP-REI events on a per-bit basis.
		1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to count or tally HP-REI/LP-REI events on a per-bit basis.
0 B3 Erro	or Type R/V	B3 Error Type:
		<ul> <li>This READ/WRITE bit-field permits the user to specify how the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-bit" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-bit" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 PAth B3 Byte Error Count" register by the number of bits (within the B3 byte value of the incoming VC-3 data-stream) that is in error.</li> <li>If the user configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to increment B3 byte errors on a "per-frame" basis.</li> <li>0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to count B3 byte errors on a "per-bit" basis.</li> <li>1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to count B3 byte errors on a "per-frame" basis.</li> </ul>

Configures the Receive TUG to count B3 byte errors on a "per-



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Table 257: Receive TUG-3/AU-3 Mapper VC-3 Path – Control Register – Byte 0 (Address Location= 0xN186, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 6 Віт 5 Віт 4 Віт 3 Віт 2				Віт 1	Віт 0
		DS3 Async PDI-P Defect Declared	Path Trace Message Unstable Defect Declared				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 2	Unused	R/O	thisnet
1	DS3 Async PDI-P Defect Declared	R/O	Asynchronously-Mapped DS3 PDI-P (Payload Defect Indicator) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processon block is currently declaring the "Asynchronous DS3 PDI-P defect condition. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor will declare the "Asynchronous DS3 PDI-P" defect condition for the duration that it has "accepted" the C2 byte value of "0xFC". 0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the "Asynchronous DS3 PDI-P" defect condition. 1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the "Asynchronous DS3 PDI-P" defect condition. 1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the "Asynchronous DS3 PDI-P" defect condition. Notes: This register bit is only valid if the incoming VC-3 signal is transporting an asynchronously-mapped DS3 signal; and if the corresponding channel (on the "low-speed" side of the chip) is configured to operate in the DS3 Mode.
0	Path Trace Message Unstable Defect Declared	RO	<ul> <li>Path Trace Message Unstable Defect Declared:</li> <li>This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will increment the "Path Trace Message Unstable" counter each time that it receives a Path Trace message that differs from the previously received message. The Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block will clear the "Path Trace Message Unstable" counter whenever it has received a given Path Trace Message 3 (or 5) consecutive times.</li> <li>0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the "Path Trace Message Unstable" defect condition.</li> <li>1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the Path Trace Message Unstable defect condition.</li> </ul>



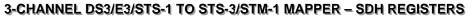
Table 258: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	AU-LOP/TU- LOP Defect Declared	AU- AIS/TU- AIS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7	TIM-P Defect	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition.
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the "TIM-P" defect condition, when none of the Path Trace Message bytes within the most recently Path Trace Message (received via the incoming VC-3 data- stream) matches the contents of the "expected" Path Trace message.
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the "TIM-P" defect condition, when at least 80% of the received Path Trace Message bytes (within the most recently received Path Trace Message) matches the contents of the "expected" Path Trace message.
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the TIM-P defect condition.
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Indicator:
	Unstable Defect Declared	NO	This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the "C2 Byte Unstable" defect condition.
	×	9313	The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the "C2 Byte Unstable" defect condition, whenever the "C2 Byte Unstable" counter reaches the value of "5". The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will increment the "C2 Unstable" counter each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the contents of the "C2 Unstable" counter to "0" whenever it has received 3 (or 5) consecutive SPEs of the same C2 byte value.
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the C2 (Path Signal Label Byte) Unstable defect condition is NOT declared.
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	UNEQ-P	R/O	Path – Unequipped (UNEQ-P) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the UNEQ-P defect condition.
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the



			UNEQ-P defect condition, anytime that it, unexpectedly receives at least five (5) consecutive VC-3 frames, in which the C2 byte was set to the value "0x00" (which indicates that the SPE is "Unequipped").								
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive VC-3 frames, in which the C2 byte was set to a value other than 0x00.								
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT declaring the UNEQ-P defect condition.								
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the UNEQ-P defect condition.								
			<b>Note:</b> The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive SONET frames with C2 bytes being set to "0x00" (e.g., if the "Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Value" Register –Address Location=0xN197) is set to "0x00".								
4	PLM-P	R/O	Path Payload Mismatch (PLM-P) Defect Declared:								
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the PLM-P defect condition.								
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive VC-3 frames, in which the C2 byte was set to a value other than that which it is expecting to receive.								
			Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is checking in order to determine whether or not it should declare the PLM-P defect, it will check the contents of the following two registers.								
			<ul> <li>The "Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Value" Register (Address Location= 0xN196).</li> </ul>								
			<ul> <li>The "Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Value" Register (Address Location= 0xN197).</li> </ul>								
		44	The "Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks expects to receive.								
	the	10 51 10 51	The "Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block has most recently "accepted" or "validated" (by receiving this same C2 byte in five consecutive SONET frames).								
	~ 8	3110	The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare a PLM-P defect condition; if the contents of these two register do not match. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match.								
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the PLM-P defect condition.								
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the PLM-P defect condition.								
			NOTES:								
											<ol> <li>The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the PLM-P defect condition, upon declaring the UNEQ-P defect condition.</li> </ol>
			<ol> <li>If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block unexpectedly accepts the C2 byte value of "0x00", then it will NOT declare the PLM-P defect condition. In this case, the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block will declare the UNEQ-P</li> </ol>								



			defect condition
3	RDI-P Defect	R/O	Path Remote Defect Indicator (RDI-P) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the RDI-P defect condition.
			If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare the RDI-P defect condition if Bit 5 (within the G1 byte of the incoming VC-3 frame) is set to "1" for "RDI-P_THRD" number of incoming consecutive VC-3s.
			If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming VC-3 frame) are set to either [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive VC-3 frames.
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT declaring the RDI-P defect condition.
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the RDI-P defect condition.
			<b>Note:</b> The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
2	RDI-P	R/O	RDI-P (Path – Remote Defect Indicator) Unstable Defect Declared:
	Unstable Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the "RDI-P Unstable" defect condition. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the "RDI-P Unstable" defect condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The Receive TUG-3/AU- 3 Mapper VC-3 POH Processor block will increment the "RDI-P Unstable" counter each time that it receives an RDI-P value that differs from that of the previous VC-3 frame. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the "RDI-P Unstable" counter to "0" whenever it has received the same RDI-P value is received in "RDI-P_THRD" consecutive VC-3 frames.
		NO	0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the RDI-P Unstable defect condition.
		e z	9- Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the RDI-P Unstable defect condition.
		80.00	<b>Note:</b> The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
1	AU-LOP/TU-	R/O	Loss of PointerDefect Indicator (AU-LOP/TU-LOP) Defect Declared:
	LOP Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-LOP/TU-LOP (Loss of Pointer) defect condition.
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the AU-LOP/TU-LOP defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the AU-LOP/TU-LOP defect condition, if it detects 8 to 10 consecutive NDF events.
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the AU-LOP/TU-LOP defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive



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			incoming SONET frames.			
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the AU-LOP/TU-LOP defect condition.			
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-LOP/TU-LOP defect condition.			
0	AU-AIS/TU-	R/O	Path AIS (AU-AIS/TU-AIS) Defect Declared:			
	AIS Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-AIS/TU-AIS defect condition. The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will declare the AU-AIS/TU-AIS defect condition if it detects all of the following conditions within three consecutive incoming VC-3 frames.			
			• The H1, H2 and H3 bytes are set to an "All Ones" pattern.			
			The entire SPE is set to an "All Ones" pattern.			
			The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will clear the AU- AIS/TU-AIS defect condition whenever it detects a valid VC-3 pointer (H1 and H2 bytes) and a "set" of "normal" NDF for three consecutive VC-3 frames.			
			0 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is NOT currently declaring the AU-AIS/TU-AIS defect condition.			
			1 – Indicates that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block s currently declaring the AU-AIS/TU-AIS defect condition.			
			<b>Note:</b> The Receive TUG 3/AU-3 Mapper VC-3 POH Processor block will NOT declare the AU-LOP/TU-LOP defect condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AU-AIS/TU-AIS defect condition.			
	NOT declare the AU-LOP/IO-LOP defect condition if it defects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AU-AIS/TU-AIS defect condition.					
The Prest and may						



Table 259: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in PDI-P Defect Condition Interrupt Status	Unı	ısed	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
RUR	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
					wils re	ò	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Change in PDI-P Defect Condition Interrupt Status:	RUR	<ul> <li>Description</li> <li>Change in PDI-P Defect Condition Interrupt Status:</li> <li>This RESET-upon-READ biddel indicates whether or not the "Change in PDI-P Defect Condition" Interrupt condition has occurred since the last read of this register.</li> <li>If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the DS3 Asynchronous PDI-P Defect Condition (e.g., whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block accepts" a C2 byte value of "0xFC").</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block accepts" a C2 byte value of "0xFC".</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block has "removed" the C2 byte value of "0xFC" by accepting a different C2 byte value).</li> <li>Indicates that the "Change in PDI-P Defect Condition" Interrupt has NOT occurred since the last read of this register.</li> <li>Indicates that the "Change in PDI-P Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>Indicates that the "Change in PDI-P Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>NOT ES: <ul> <li>This register bit is only valid if the incoming VC-3 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "low-speed" side of the XRT94L33 device) is configured to operate in the DS3 Mode.</li> </ul> </li> <li>The user can determine whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the PDI-P Defect condition by reading out the state of Bit 1 (DS3 Asynch PDI-P Defect condition by reading out the state of Bit 1 (DS3 Asynch PDI-P Defect Condition by reading out the state of Bit 1 (DS3 Asynch PDI-P Defect Condition by reading out the state of Bit 1 (DS3 Asynch PDI-P Defect Condition by reading out the state of Bit 1 (DS3 Asynch P</li></ul>
6 - 5	Unused	R/O	
4	Detection of AIS Pointer Interrupt Status	RUR	Detection of AIS Pointer Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.



			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming VC-3 data stream.
			<b>Note:</b> An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the SOH) are each set to an "All Ones" pattern.
			0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer	RUR	Detection of Pointer Change Interrupt Status:
	Change Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the SOH bytes).
			0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	POH Capture	RUR	Path Overhead Data Capture Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "POH Capture" Interrupt has occurred since the last read of this register.
		0	If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data, for the next SPE will be loaded into the "POH Capture" buffer.
	Ň		0 - Indicates that the "POH Capture" Interrupt has NOT occurred since the last read of this register.
	orot	<b>100</b>	P-Indicates that the "POH Capture" Interrupt has occurred since the last read of this register.
	Thelata	ma	<b>Note:</b> The user can obtain the contents of the POH, within the most recently received SPE by reading out the contents of address locations "0xN0D3" through "0xN0F3").
1	Change in TIM-P	RUR	Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the TIM-P defect condition.
			0 - Indicates that the "Change in TIM-P Defect Condition" Interrupt has

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		not occurred since the last read of this register.		
		1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.		
		<b>NOTE:</b> The user can determine whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the TIM-P defect condition by reading out the state of Bit 7 (TIM-P Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – Receive TUG-3/AU- 3 Mapper VC-3 POH Status Register – Byte 0 (Address = 0xN187).		
Change in Path Trace Message	RUR	Change in Path Trace Identification Message Unstable Defect Condition" Interrupt Status:		
Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Identification Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.		
		If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.		
		<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declare the "Path Trace Message Unstable" Defect Condition.</li> </ul>		
		<ul> <li>Whenever the Receive TUG 3/AU-3 Mapper VC-3 POH Processor block clears the "Path Trace Message Unstable" Defect condition.</li> </ul>		
		0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.		
		1 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.		
	Trace Message Unstable Defect Condition Interrupt Status	Trace Message Unstable Defect Condition Interrupt Status		



# Table 260: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Status	Detection of HP-REI/ LP-REI Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

		-	.6 2
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	New Path Trace	RUR	New Path Trace Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.
			0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of	RUR	Detection of HP-REI/LP-REI Event Interrupt Status:
	HP-REI/ LP-REI Event Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of HP-REI/LP-REI Event" Interrupt has occurred since the last read of this register.
		duct	If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects an HP-REI/LP- REI event within the incoming VC-3 data-stream.
	pr	she	OCIndicates that the "Detection of HP-REI/LP-REI Event" Interrupt has NOT occurred since the last read of this register.
	Theat	0 m	1 – Indicates that the "Detection of HP-REI/LP-REI Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ-P Defect	RUR	Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P Defect Condition.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the UNEQ-P Defect Condition.
			0 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has NOT occurred since the last read of this register.



			1 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the UNEQ-P defect condition by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
4	Change in PLM-P Defect	RUR	Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "PLM-P" Defect Condition.</li> </ul>
			<ul> <li>Whenever the Receive TUG 3/AU 3 Mapper VC-3 POH Processor block clears the "PLM-P" Defect Condition.</li> </ul>
			0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register.
			<b>NOTE:</b> The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the PLM-P defect condition by reading out the state of Bit 4 (PLM-P Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive POH Status – Byte 0" Register (Address Location = 0xN187).
3	New C2 Byte	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" interrupt has occurred since the last read of this register.
		NOON	If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
	a the	8.9	0 Ondicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
		90° no	1 – Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
		•	<b>NOTE:</b> Once the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block has "accepted" a new C2 byte value, it will load the value of this byte into the "Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Path Label Value" Register (Address = 0xN196).
2	Change in C2	RUR	Change in C2 Byte Unstable Defect Condition Interrupt Status:
	Byte Unstable Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "C2 Byte Unstable" defect condition.



1       Change in RDI-P       RUR       0 – Indicates that the "Change in C2 Byte Interrupt has NOT occurred since the last read of this and of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred since the last read of this interrupt has occurred sintered of the last read of th	f this register. Unstable Defect Condition" register. of the Receive TUG-3/AU-3 c currently declaring the "C2 eading out the state of Bit 6 within the "Receive TUG-
1       Change in RDI-P       RUR       RUR       Interrupt has occurred since the last read of this         Interrupt has occurred since the last read of this       Note:       The user can determine whether or mental mapper VC-3 POH Processor block is         Byte       Unstable       Defect       Condition" by reading the condition of the conditio	register. ot the Receive TUG-3/AU-3 c currently declaring the "C2 eading out the state of Bit 6 within the "Receive TUG-
Mapper VC-3 POH Processor block is         Byte Unstable Defect Condition" by re         (C2 Byte Unstable Defect Declared)         3/AU-3 Mapper VC-3 Path – SONET         0" Register (Address Location= 0xN18         1       Change in RDI-P         RUR       Change in RDI-P Unstable Defect Condition In	currently declaring the "C2 eading out the state of Bit 6 within the "Receive TUG-
	nterrupt Status:
Unstable Defect Condition Interrupt Status Unstable Defect Condition Interrupt Status	
If this interrupt is enabled, then the Receive TUC Processor block will generate an interrupt in following conditions.	
<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper declares the "RDI-P Unstable" defect condition.</li> </ul>	VC-3 POH Processor block
When the Receive TUG-3/AU-3 Mapper V clears the "RDI-P Unstable" defect condition.	C-3 POH Processor block
0 – Indicates that the "Change in RDI-P Unstable has NOT occurred since the last read of this regi	
1 – Indicates that the "Change in RDI-P Unstable has occurred since the last read of this register.	e Defect Condition" Interrupt
Note: The user can determine whether or no Mapper VC-3 POH Processor block (BDI-P Unstable Defect Condition" by (RDI-P Unstable Defect Condition) wit 3 Mapper VC-3 Path – SONET Rec Register (Address Location= 0xN187).	is currnelty declaring the reading out the state of Bit 2 hin the "Receive TUG-3/AU- eive POH Status – Byte 0"
0 New RDI-P Value Interrupt Status Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value Value V	
If this interrupt is enabled, then the Receive TUC Processor block will generate this interrupt "validates" a new RDI-P value.	
0 – Indicates that the "New RDI-P Value" Interru the last read of this register.	upt has NOT occurred since
1 – Indicates that the "New RDI-P Value" Inter last read of this register.	rupt has occurred since the
Note: The user can obtain the "New RDI-P contents of the "RDI-P ACCEPT[2:0] are located in Bits 6 through 4, within Mapper VC-3 Path – SONET Receive Location=0xN193).	" bit-fields. These bit-fields n the "Receive TUG-3/AU-3



# Table 261: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of AU- LOP/TU- LOP Defect Condition Interrupt Status	Change of AU-AIS/TU- AIS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
					nis e	Ò	

7 Detection of B3 RUR Detection of B3 Byte Error Interrupt Status: Byte Error	
Interrupt Status This RESET-upon-READ bit-field indicates whether B3 Byte Error" Interrupt has occurred since the last	
If this interrupt is enabled, then the Receive TUP POH Processor block will generate an interrupt any error in the incoming VC-3 data stream.	
0 – Indicates that the "Detection of B3 Byte Er occurred since the last read of this interrupt.	rror" Interrupt has NOT
1 – Indicates that the "Detection of B3 Byte Error since the last read of this interrupt.	" Interrupt has occurred
6 Detection of New RUR Detection of New Pointer Interrupt Status:	
Pointer Interrupt Status This RESET-upon-READ indicates whether the "Do interrupt has occurred since the last read of this reg	
VC-3 POH Processor block will generate an interr new pointer value in the incoming VC-3 frame.	ve TUG-3/AU-3 Mapper upt anytime it detects a
Note: Pointer Adjustments with NDF will not gen	erate this interrupt.
Indicates that the "Detection of New Point Coccurred since the last read of this register.	ter" Interrupt has NOT
1 – Indicates that the "Detection of New Pointer" since the last read of this register.	' Interrupt has occurred
5 Detection of RUR Detection of Unknown Pointer Interrupt Status:	
Unknown Pointer Interrupt Status Unknown Pointer" interrupt has occurred since the I	
If the user enables this interrupt, then the Receiv VC-3 POH Processor block will generate an interrup a "pointer" that does not fit into any of the following	pt anytime that it detects
An Increment Pointer	
A Decrement Pointer	
An NDF Pointer	
An AIS (e.g., All Ones) Pointer	
New Pointer	



			0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of	RUR	Detection of Pointer Decrement Interrupt Status:
	Pointer Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer	RUR	Detection of Pointer Increment Interrupt Status:
	Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF	RUR	Detection of NDF Pointer Interrupt Status:
	Pointer Interrupt Status	duct	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
	pro	she	0 – Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
	Theat	nd m	1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of AU-	RUR	Change of AU-LOP/TU-LOP Defect Condition Interrupt Status:
	LOP/TU-LOP Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in AU-LOP/TU-LOP Defect Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.
			Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition.
			Whenever the Receive "TUG-3/AU-3 Mapper VC-3 POH Processor" block clears the AU-LOP/TU-LOP defect condition.
			0 – Indicates that the "Change in AU-LOP/TU-LOP Defect Condition" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change in AU-LOP/TU-LOP Defect Condition"



			interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-LOP/TU-LOP defect condition by reading out the state of Bit 1 (AU-LOP/TU- LOP Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
0	Change of AU-	RUR	Change of AU-AIS/TU-AIS Defect Condition Interrupt Status:
	AIS/TU-AIS Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AU-AIS/TU-AIS Defect Condition" Interrupt has occurred since the last read of this register.
			<ul> <li>If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-AIS/TU-AIS defect condition.</li> </ul>
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the AU-AIS/TU-AIS defect condition.
			0 – Indicates that the "Change of AU-AIS/TU-AIS Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AU-AIS/TU-AIS Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-AIS/TU-AIS defect condition by reading out the state of Bit 0 (AU-AIS/TU-AIS Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).

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# Table 262: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location= 0xN18D, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in PDI-P Defect Condition Interrupt Enable	Unused		Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	POH Capture Interrupt Enable	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/W	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

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BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7	Change in PDI-P Defect Condition Interrupt Enable	R/W	<ul> <li>Change in PDI-P Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in PDI-P Defect Condition" Interrupt. If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the DS3 Asynchronous PDI-P defect condition (e.g., whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the DS3 Asynchronous PDI-P defect condition (e.g., whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the DS3 Asychronous PDI-P defect condition (e.g., whenever it accepts a C2 byte value of "0xFC").</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the DS3 Asychronous PDI-P defect condition (e.g., whenever it nas "removed" the C2 byte value of "0xFC" by accepting a different C2 byte value).</li> <li>D – Disables the "Change in PDI-P Defect Condition" Interrupt.</li> <li><i>1 Enables the "Change in PDI-P Defect Condition" Interrupt.</i></li> <li><i>1 This register bit is only valid if the incoming VC-3 signal is transporting an asynchronously-mapped DS3 signal; and if the corresponding channel (on the "low-speed" side of the XRT94L33 device) is configured to operate in the DS3 Mode.</i></li> <li><i>2. The user can determine whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the PDI-P defect condition by reading out the state of Bit 1 (DS3 Async PDI-P defect Declared) within the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is a currently declaring the PDI-P defect condition by reading out the state of Bit 1 (DS3 Async PDI-P Defect Declared) within the Receive TUG-3/AU-3 Mapper VC-3 PAH – Control Register – Byte 0 (Address = 0xN186).</i></li> </ul>
6 - 5	Unused	R/O	
4	Detection of AIS	R/W	Detection of AIS Pointer Interrupt Enable:
	Pointer Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt.
			If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming VC-3 data stream.
			<b>Note:</b> An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the SOH) are each set to an "All Ones" Pattern.

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			0 – Disables the "Detection of AIS Pointer" Interrupt.		
			1 – Enables the "Detection of AIS Pointer" Interrupt.		
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:		
	Change Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.		
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.		
			0 – Disables the "Detection of Pointer Change" Interrupt.		
			1 – Enables the "Detection of Pointer Change" Interrupt.		
2	POH Capture Interrupt Enable	R/W	Path Overhead Data Capture Interrupt Enable:		
			This READ/WRITE bit-field permits the user to either enable or disable the "POH Capture" Interrupt.		
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards the POH data for the next SPE will be loaded into the "POH Capture" Buffer.		
			0 – Disables the "POH Capture" Interrupt		
			1 – Enables the "POH Capture" Interrupt.		
1	Change in TIM-P Defect Condition Interrupt Enable	R/W	Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt: This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Defect Condition" interrupt.		
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor		
			block declares the TIM-P defect condition.		
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the TIM-P defect condition.</li> </ul>		
	1 he		O – Disables the "Change in TIM-P Defect Condition" Interrupt.		
	8		1 – Enables the "Change in TIM-P Defect Condition" Interrupt.		
			<b>NOTE:</b> The user can determine whether or not the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the TIM-P defect condition by reading out the state of Bit 7 (TIM-P Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – Receive TUG-3/AU- 3 Mapper VC-3 POH Status Register – Byte 0 (Address = 0xN187).		
0	Change in Path Trace Message	R/W	Change in "Path Trace Message Unstable Defect Condition" Interrupt Status:		
	Unstable Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in Path Trace Message Unstable Defect Condition" Interrupt.		
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.		
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "Path Trace Message Unstable" defect Condition.		



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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the "Path Trace Message Unstable" defect Condition.
0 – Disables the "Change in Path Trace Message Unstable Defect Condition" interrupt.
1 – Enables the "Change in Path Trace Message Unstable Defect Condition" interrupt.





# Table 263: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Enable	Detection of HP-REI/LP- REI Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7	NEW Path Trace	R/W	New Path Trace Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.
			0 – Disables the "New Path Trace Message" Interrupt.
			1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of HP-	R/W	Detection of HP-REI/LP-REI Event Interrupt Enable:
	REI/LP-REI Event Interrupt Enable		This READ/WRITE bit field permits the user to either enable or disable the "Detection of HP-REI/LP-REI Event" Interrupt.
		t.	If this interrupt is enabled, then he Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects an HP- REI/LP-REI event within the coming VC-3 data-stream.
		G	0 Disables the "Detection of HP-REI/LP-REI Event" Interrupt.
		.000	- Enables the "Detection of HP-REI/LP-REI Event" Interrupt.
5	Change in UNEQ-P Defect Condition	R/W	Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Defect Condition" interrupt.
		3	If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P Defect Condition.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the UNEQ-P Defect Condition.
			0 – Disables the "Change in UNEQ-P Defect Condition" Interrupt.
			1 – Enables the "Change in UNEQ-P Defect Condition" Interrupt.
4	Change in PLM-P Defect Condition	R/W	Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt.



			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "PLM-P" Defect Condition.</li> </ul>
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the "PLM-P" Defect Condition.
			0 – Disables the "Change in PLM-P Defect Condition" Interrupt.
			1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte	R/W	New C2 Byte Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New 2 Byte" Interrupt.
			<b>Note:</b> The user can obtain the value of this "New C2" byte by reading the contents of the "Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Value" Register (Address Location= 0xN196).
2	Change in C2 Byte Unstable Defect	R/W	Change in C2 Byte Unstable Defect Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Defect Condition" Interrupt.
		4	If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "C2 Byte Unstable" defect condition.
	6.	Jet (	• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the "C2 Byte Unstable" defect condition.
	pr.	Nº 1	0 – Disables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
	10 3	n'a	1 – Enables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
1	Change in RD4P Unstable Defect	R/W	Change in RDI-P Unstable Defect Condition Interrupt Enable:
	Condition Interrupto		This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Defect Condition" interrupt.
			If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "RDI-P Unstable" defect condition.
			• Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the "RDI-P Unstable" defect condition.
			0 – Disables the "Change in RDI-P Unstable Defect Condition" Interrupt.
			1 – Enables the "Change in RDI-P Unstable Defect Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	<b>New RDI-P Value Interrupt Enable:</b> This READ/WRITE bit-field permits the user to either enable or disable



the "New RDI-P Value" interrupt.
If this interrupt is enabled, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value.
0 – Disables the "New RDI-P Value" Interrupt.
1 – Enable the "New RDI-P Value" Interrupt.

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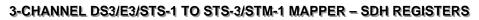


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# Table 264: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of AU- LOP/TU- LOP Defect Condition Interrupt Enable	Change of AU-AIS/TU- AIS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Detection of	R/W	Detection of B3 Byte Error Interrupt Enable:
	B3 Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming VC-3 data-stream.
			0 – Disables the "Detection of B3 Byte Error" interrupt.
			1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of New Pointer	R/W	Detection of New Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE out-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive TUG-3/AD-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming VC-3 frame.
			Note: Pointer Adjustments with NDF will not generate this interrupt.
			0 – Disables the "Detection of New Pointer" Interrupt.
		×	1 – Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	R	Detection of Unknown Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories.
		.0.	An Increment Pointer.
			A Decrement Pointer
			An NDF Pointer
			AIS Pointer
			New Pointer.
			0 – Disables the "Detection of Unknown Pointer" Interrupt.
			1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of	R/W	Detection of Pointer Decrement Interrupt Enable:
	Pointer Decrement Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a "Peinter Decrement" overt





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			detects a "Pointer-Decrement" event.
			0 – Disables the "Detection of Pointer Decrement" Interrupt.
			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Increment Interrupt Enable:
	Increment Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Disables the "Detection of Pointer Increment" Interrupt.
			1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of	R/W	Detection of NDF Pointer Interrupt Enable:
	NDF Pointer Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event
			0 – Disables the "Detection of NDF Pointer" interrupt.
			1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of	R/W	Change of AU-LOP/TU-LOP Defect Condition Interrupt Enable:
	AU-LOP/TU- LOP Defect Condition Interrupt Enable		<ul> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointe)" Defect Condition interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor will generate an interrupt in response to either of the following events.</li> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block</li> </ul>
			declares the AU-LOP/TU-LOP defect condition.
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the AU-LOP/TU-LOP defect condition.</li> </ul>
			0 – Disable the "Change of AU-LOP/TU-LOP Defect Condition" Interrupt.
			1 - Enables the "Change of AU-LOP/TU-LOP Defect Condition" Interrupt.
		nep	Note: The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-LOP/TU-LOP defect condition by reading out the contents of Bit 1 (AU-LOP/TU-LOP Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).
0	Change of	R/W	Change of AU-AIS/TU-AIS Defect Condition Interrupt Enable:
	AU-AIS/TU- AIS Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of AU-AIS/TU-AIS (Path AIS)" Defect Condition interrupt. If the user enables this interrupt, then the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will generate an interrupt in response to either of the following events.
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the "AU-AIS/TU-AIS" defect condition.</li> </ul>
			<ul> <li>Whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block clears the "AU-AIS/TU-AIS" defect condition.</li> </ul>
			0 – Disables the "Change of AU-AIS/TU-AIS Defect Condition" Interrupt.
			1 – Enables the "Change of AU-AIS/TU-AIS Defect Condition" Interrupt.
			<b>Note:</b> The user can determine if the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is currently declaring the AU-AIS/TU-AIS defect condition by reading out the contents of Bit 0 (AU-AIS/TU-AIS Defect Declared) within the "Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive



POH Status – Byte 0" (Address Location= 0xN187).
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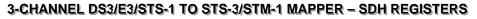




Table 265: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive RDI-P Register (Address Location= 0xN193, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused	RDI-P_ACCEPT[2:0]			T[2:0] RDI-P THRESHOLD[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Unused	R/O	
6 – 4	RDI-P_ACCEPT[2:0]	R/O	Accepted RDI-P Value:
			These READ-ONLY bit-fields contain the RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been most recently accepted by the Receive TUG-3/AU-3 Mapper VC-3 POH-Processor block.
			Note: A given RDI-P value will be "accepted" by the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of SONET frames.
3 – 0		R/W	RDI-P Threshold[3:0]:
	THRESHOLD[3:0]		These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive TUG-3/AU-3 Mapper VC-3 POH Processor Block.
			The "RDI-P Acceptance Threshold" is the number of consecutive SONET frames, in which the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it
			The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.

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Table 266: Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Value (Address Location= = 0xN196, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Received_C2_Byte_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Received C2 Byte	R/O	Received "Filtered" C2 Byte Value:
	Value[7:0]		<ul> <li>These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block.</li> <li>The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive SONET frames.</li> <li>Note: The Receive TUG-3/AU-3 Mapper VC-3 POH Processor block uses this register, along the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor block uses this register, along the "Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Value" Register (Address Location= 0xN197), when declaring or clearing the UNEQ-P and PLM-P defect conditions.</li> </ul>

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 267: Receive TUG-3/AU-3 Mapper VC-3 Path – Expected Path Label Value (Address Location= 0xN197, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0					
	Expected_C2_Byte_Value[7:0]											
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
1	1	1	1	1	1	1	1					

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value: These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions If the contents of the "Received C2 Byte Value[7:0]" (see "Receive TUG-3/AU-3 Mapper VC-3 Path – Received Path Label Value" register) matches the contents in these register, then the Receive TUG-3/AU-3 Mapper VC-3 POH will not declare the PLM-P nor the UNEQ-P defect conditions

Table 268: Receive TUG-3/AU-3 Mapper VC-3 Path - B3 Byte Error Count Register – Byte 3 (Address Location= 0xN198, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0					
B3_Byte Error Count[31:24]											
RUR	RUR	RUR	RUR	RUR	RUR	RUR					
0	0	0	0000	0	0	0					

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[31:24]	RUR	B3 Byte Error Count – MSB:
	The pland	27	This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a B3 byte error.
	<b>0</b> *		Note:
			1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming VC-3) that are in error.
			2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an VC-3 that contains an erred B3 byte.



# Table 269: Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 2 (Address Location= 0xN199, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B3_Byte_Error_Count[23:16]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	B3_Byte_Error_Count[23:16]	RUR	B3 Byte Error Count (Bits 23 through 16):
			This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive TUC-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming VC-3) that are in error.
			2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an VC-3 that contains an erred B3 byte.
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Table 270: Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 1 (Address Location= 0xN19A, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
B3_Byte_Error_Count[15:8]											
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	B3_Byte_Error_Count[15:8]	RUR	B3 Byte Error Count – (Bits 15 through 8):
			<ul> <li>This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a B3 byte error.</li> <li><i>Note:</i> <ol> <li>If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming VC-3) that are in error.</li> <li>If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming VC-3) that are in error.</li> </ol> </li> </ul>

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# Table 271: Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Byte 0 (Address Location= 0xN19B, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B3_Byte_Error_Count[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	B3_Byte_Error_Count[7:0]	RUR	B3 Byte Error Count – LSB:
			This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming VC-3) that are in error.
			2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an VC-3 that contains an error B3 byte.
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Table 272: Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 3 (Address Location= 0xN19C, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0				
HP-REI/LP-REI_Event_Count[31:24]											
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	HP-REI/LP-REI Event_Count[31:24]	RUR	HP-REI/LP-REI Event Count – MSB: This RESET-upon-READ register, along with "Receive TUG-3/AU- 3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register –
			Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a Path – Remote Error Indicator event within the incoming VC-3 data stream.
			Note: 1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within
			the HP-REVLP-REI field of the incoming G1 byte within each incoming VC-32 2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each time that it
			receives an VC-3 that contains a "non-zero" HP-REI/LP-REI value.



Table 273: Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 2 (Address Location= 0xN19D, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI/LP-REI_Event_Count[23:16]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
<b>Віт Number</b> 7 — 0	Nаме HP-REI/LP-REI Event_Count[23:16]	Type RUR	HP-REI/LP-REI Event Count (Bits 23 through 16): This RESET-upon-READ register along with "Receive TUG-3/AU- 3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a Path – Remote Error Indicator event within the incoming VC-3 data-stream. NOTES: 1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block
			is configured to count HP-REI/LP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the HP-REI/LP-REI field of the incoming G1 byte within each incoming VC-3.
		60.	2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each tiem that it receives an VC-3 that contains a "non-zero" HP-REI/LP-REI value.

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Table 274: Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 1 (Address Location=0xN19E, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI/LP-REI_Event_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 0	HP-REI/LP-REI	RUR	HP-REI/LP-REI Event Count – (Bits 15 through 8)
	Event_Count[15:8]		<ul> <li>This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP REI Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a Path – Remote Error Indicator event within the incoming VC-3 data-stream.</li> <li>Note:</li> <li>1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the HP-REI/LP-REI field of the incoming G1 byte within each incoming VC-3</li> <li>2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-frame" basis, then it will increment this 32-bit counter and "per-frame" basis, then it will increment this 32-bit counter each time that it receives an VC-3 that contains a non-zero HP-REI/LP-REI value.</li> </ul>

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# Table 275: Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Byte 0 (Address Location= 0xN19F, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI/LP-REI_Event_Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	HP-REI/LP-REI	RUR	HP-REI/LP-REI Event Count – LSB:
	Event_Count[7:0]		<ul> <li>This RESET-upon-READ register, along with "Receive TUG-3/AU-3 Mapper VC-3 Path – HP-REI/LP-REI Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects a Path – Remote Error Indicator event within the incoming VC-3 datastream.</li> <li>Note:</li> <li>1. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP REI/LP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the HP-REI/LP-REI field of the incoming G1 byte within each incoming VC-3.</li> <li>2. If the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block is configured to count HP-REI/LP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an VC-3 that contains a "non-zero" HP-REI/LP-REI value.</li> </ul>

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Table 276: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Path Trace Message Buffer Control Register (Address Location=0xN1A3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Receive Pa Message L			
R/O	R/O	R/O	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 5	Unused	R/O	th ure
4	Received Path Trace Message Buffer Read Select	R/W	Receive Path Trace Message Buffer Read Selection: This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Path Trace Message Buffer. <b>m.</b> The "Actual" Receive Path Trace Message Buffer. The
	The product	orpre	Actual" Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming VC-3 data-stream.
	rotuc	etno	user. – Executing a READ to the Receive Path Trace Message Buffer, will return the contents within the "Actual" Receive Path Trace Message" buffer.
	The start	131	1 – Executing a READ to the Receive Path Trace Message Buffer will return the contents within the "Expected Receive Path Trace Message Buffer".
	duano		<b>Note:</b> In the case of the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block, the "Receive Path Trace Message Buffer" is located at Address Location 0xN500 through 0xN53F, where N ranges in value from 0x02 to 0x04.
3	Path Trace Message Accept	R/W	Path Trace Message Accept Threshold:
	Threshold		This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block must receive a given Receive Path Trace Message, before it is accepted and loaded into the "Actual" Receive Path Trace Message buffer, as described below.
			0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to accept the incoming Path Trace Message after it has received it the third time in succession.
			1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to accept the Incoming Path Trace Message



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			after it has received	in the fifth time in succession.
2	Path Trace Message	R/O	Path Trace Messa	ge Alignment Type:
	Alignment Type		Receive TUG-3/AL locate the boundary	bit-field permits a user to specify how the J-3 Mapper VC-3 POH Processor block will y of the incoming Path Trace Message (within data-stream), as indicated below.
			Processor block to	e Receive TUG-3/AU-3 Mapper VC-3 POH expect the Path Trace Message boundary to ine Feed" character.
			Processor block to be denoted by the p byte) of the very Message). In this	e Receive TUG-3/AU-3 Mapper VC-3 POH expect the Path Trace Message boundary to presence of a "1" in the MSB (most significant first byte (within the incoming Path Trace caes, all of the remaining bytes (within the ce Message) will each have a "0" within their
1 – 0	1 – 0 Receive Path Trace Message Length[1:0]	R/W	These READ/WRI length of the Rec TUG-3/AU-3 Mapp load into the "Actua relationship betwee	<b>a Message Length[1:0]:</b> TE bit-fields permit the user to specify the eve Path Trace Message that the Receive or VC-3 POH Processor block will accept and al" Receive Path Trace Message Buffer. The en the content of these bit-fields and the eive Path Trace Message Length is presented
			Receive Path Trace Message Length[1:0]	Resulting Path Trace Message Length (in terms of bytes)
				00
		× ~ 0	01	16 Bytes
		ເຍີຼຍ	10/11	64 Bytes
	The product of	not		

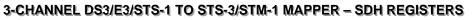




Table 277: Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value – Byte 1 (Address Location= 0xN1A6, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Current_Pointer	Value MSB[9:8]				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[1:0]	R/O	<ul> <li>Current Pointer Value – MSB:</li> <li>These READ-ONLY bit-fields, along with that from the "Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor" block is using to locate the SPE within the incoming SONET data stream.</li> <li>Note: These register bits comprise the two-most significant bits of the Pointer Value.</li> </ul>

# Table 278: Receive TUG-3/AU-3 Mapper VC-3 Path Pointer Value – Byte 0 (Address Location=0xN1A7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
		(	Current_Pointer	Value_LSB[7:0	)]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0		0	0	0	0

BIT NUMBER		Түре	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	<ul> <li>Current Pointer Value – LSB:</li> <li>These READ-ONLY bit-fields, along with that from the "Receive TUG-3/AU-3 Mapper VC-3 Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive TUG-3/AU-3 Mapper VC-3 POH Processor" block is using to locate the SPE within the incoming SONET data stream.</li> <li>Note: These register bits comprise the Lower Byte value of the Pointer Value.</li> </ul>



# Table 279: Receive TUG-3/AU-3 Mapper VC-3 Path – AUTO AIS Control Register (Address Location= 0xN1BB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AU-AIS/ TU-AIS (Down- stream) Upon C2 Byte Unstable	Transmit AU-AIS/ TU-AIS (Down- stream) Upon UNEQ-P	Transmit AU-AIS/ TU-AIS (Down- stream) Upon PLM- P	Transmit AU-AIS/ TU-AIS (Down- stream) Upon Path Trace Message Unstable	Transmit AU-AIS/ TU-AIS (Down- stream) Upon TIM-P	Transmit AU-AIS/ TU-AIS (Down- stream) upon AU- LOP/TU- LOP	Transmit AU-AIS/ TU-AIS (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0		0	0
		·			the rec		·

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	
6	Transmit AU- AIS/TU-AIS (Downstream) upon C2 Byte Unstable	R/W	<ul> <li>Transmit Path AIS (Downstream, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) upon Declaration of the Unstable C2 Byte Detect Condition:</li> <li>This READ/WRITE bit field permits the user to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU/AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the Unstable C2 Byte detect condition within the "incoming" STM-0 data-stream.</li> <li>0 - Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor DS3/E3 Mapper block) whenever it declares the "Unstable C2 Byte" defect condition.</li> <li>1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the "Unstable C2 Byte" defect condition.</li> <li>1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the "Unstable C2 Byte" defect condition.</li> <li>Note: The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "1" to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator, in response to this defect condition.</li> </ul>
5	Transmit AU- AIS/TU-AIS (Downstream) upon UNEQ-P	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper blocks) upon Declaration of the UNEQ-P (Path – Unequipped) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the UNEQ-P defect condition.
			0 – Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper Block) whenever it declares the UNEQ-P

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			defect condition.
			1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the UNEQ-P defect condition.
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "1" to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator, in response to this defect condition.
4	Transmit AU- AIS/TU-AIS (Downstream) upon	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) upon Declaration of PLM-P (Path – Payload Label Mismatch) Defect Condition:
	PLM-P		This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the PLM-P defect condition.
			0 – Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever it declares the PLM-P defect condition.
			1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the PLM-P defect condition.
			Note The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator, in response to this defect condition.
3	Transmit AU- AIS/TU-AIS (Downstream) upon	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) upon declaration of the Path Trace Message Unstable Defect Condition:
	Path Trace Message Unstable	at and	This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STM-0 data-stream.
			0 – Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STM-0 data-stream.
			1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the Path Trace Message Unstable defect condition.
			Note: The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "1" to configure the Receive TUG-3/AU-3 Mapper VC-3 POH



			Processor block to automatically transmit the AU-AIS/TU-AIS indicator, in response to this defect condition.							
2	Transmit AU- AIS/TU-AIS (Downstream) upon TIM-P	R/W	Transmit Path AIS (Downstream towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) upon declaration o the TIM-P (Path Trace Identification Message Mismatch) defect condition:							
			This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the TIM-P defect condition within the incoming VC-3 data-stream.							
			0 – Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever it declares the TIM-P defect condition.							
			1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the TIM-P defect condition.							
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "1" to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator in response to this defect condition.							
1	Transmit AU- AIS/TU-AIS (Downstream) upon	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) upon Declaration of the Loss of Pointer (AU-LOP/TU-LOP) Defect Condition:							
	AU-LOP/TU-LOP	in the second	uct (C	uct (C	uct (C	uct (	uct	uct	Jot C	This READ/WRITE bit-field permits the user to configure the Receive TUG- 3/AU3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the AU- LOP/TU-LOP defect condition within the incoming STM-0 data-stream.
	the ata		Does not configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever it declares the AU-LOP/TU- LOP defect condition.							
	~ ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		1 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block)) whenever (and for the duration that) it declares the AU-LOP/TU-LOP defect condition.							
			<b>Note:</b> The user must also set Bit 0 (Transmit AU-AIS/TU-AIS Enable) to "1" to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator, in response to this defect condition.							
0	Transmit AU-	R/W	Automatic Transmission of AU-AIS/TU-AIS Enable:							
	AIS/TU-AIS (Downstream)		This READ/WRITE bit-field serves two purposes.							
	Enable		It permits the user to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the Path AIS (AU-AIS/TU- AIS) indicator, via the down-stream traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block), upon							



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declaration of either the UNEQ-P, PLM-P, TIM-P, AU-LOP/TU-LOP or the Path Trace Message Unstable defect conditions.
It also permits the user to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit a Path (AU-AIS/TU-AIS) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) anytime (and for the duration that) it declares the AU-AIS/TU-AIS defect condition within the "incoming " STM-0 data-stream.
0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenever it declares any of the "above-mentioned" defect conditions.
<ul> <li>1 - Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the AU-AIS/TU-AIS indicator (via the "downstream" traffic, towards the corresponding Transmit STM-0 POH Processor or DS3/E3 Mapper block) whenver (and for the duration that) it declares any of the "above-mentioned" condition.</li> <li>Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive TUG-3/AU-3</li> </ul>
Mapper VC-3 POR Processor block to automatically transmit the AU-AIS/TU-AIS indicator upon detection of a given alarm/defect condition.

in ord apper VC-3 POH Pro AU-AIS/TU-AIS indicate condition.



# Table 280: Receive TUG-3/AU-3 Mapper VC-3 Path – Serial Port Control Register (Address Location= 0xN1BF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unu	ised		RxPOH_CLOCK_SPEED[7:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxPOH_CLOCK_SPEED[7:0]	R/W	RxPOHCIk Output Clock Signal Speed:
			These READ/WRITE bit-fields permit the user to specify the frequency of the "RxPOHCIk output clock signal.
			The formula that relates the contents of these register bits to the "RxPOHClk" frequency is presented below.
			FREQ = 19.44 /[2*(RxPOH_CLOCK_SPEED + 1)
			<b>Notes:</b> For STS 3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz

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Table 281: Receive TUG-3/AU-3 Mapper VC-3 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon AU- LOP/TU-LOP	Unused	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon PLM-P	Unused	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon UNEQ-P	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon TIM-P	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon AU-AIS/ TU-AIS	Transmit DS3 AIS (via Downstream DS3/E3) upon PDI-P
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0 🍤	0	0
L					th. I	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Transmit or DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon AU- LOP/TU-LOP	R/W	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3 signals) upon declaration of the AU-LOP/TU-LOP defect condition: The exact function of this register bit-field depends upon whether the
			channel has been configured to operate in the STM-0 or DS3/E3 Mode, as described below.
			If the Channel has been configured to operate in the STM-0 Mode: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AU-AIS (Path AIS) Indicator
		, lor	Via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block
	N	ن ^م	If the Channel has been configured to operate in the DS3/E3 Mode:
	The production of the producti	1124	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition.
	<u>&amp;</u>		0 – Does not configure the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition.
			1 – Configures the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition.
6	Unused	R/O	
5	Transmit AU-AIS or DS3/E3 AIS (via	R/W	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3 signals) upon declaration of the PLM-P defect



	Downstream STM-0s or		condition:
	DS3/E3s) upon PLM-P		The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STM-0 or DS3/E3 Mode, as described below.
			If the Channel has been configured to operate in the STM-0 Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition.
			If the Channel has been configured to operate in the DS3/E3 Mode:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition.
			0 – Does not configure the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signals, anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition.
		Pro	1 - Configures the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition.
4	Unused	R/O	
3	DS3/E3 AIS (via Downstream STM-0s or DS3/E3s) upon UNEOP	R/W	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3 signals) upon declaration of the UNEQ-P defect condition:
	Theatandman		The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STM-0 or DS3/E3 Mode, as described below.
	, 90° 110		If the Channel has been configured to operate in the STM-0 Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.
			If the Channel has been configured to operate in the DS3/E3 Mode:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.



			<ul> <li>0 – Does not configure the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.</li> <li>1 – Configures the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect</li> </ul>
			condition.
2	Transmit AU-AIS or DS3/E3 (via Downstream	R/W	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3 signals) upon declaration of the TIM-P defect condition:
	STM-0s) upon TIM-P		The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STM-0 or DS3/E3 Mode, as described below.
			If the Channel has been configured to operate in the STM-0 Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 PON Processor block (within the corresponding channel) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.
			If the Channel has been configured to operate in the DS3/E3 Mode:
		or	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.
	orodu		<ul> <li>Oees not configure the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signals, anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.</li> </ul>
	the atas	max	1 – Configures the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.
1	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or	R/W	Transmit AU-AIS or DS3/E3 AIS (via Downstream STM-0s or DS3/E3 signals) upon declaration of the AU-AIS/TU-AIS defect condition:
	DS3/E3s) upon AU-AIS/ TU-AIS		The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STM-0 or DS3/E3 Mode, as described below.
			If the Channel has been configured to operate in the STM-0 Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block (within the corresponding channel) to automatically transmit the AU-AIS (Path AIS) Indicator via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block



			declares the AU-AIS/TU-AIS defect condition.
			If the Channel has been configured to operate in the DS3/E3 Mode:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-AIS/TU-AIS defect condition.
			0 – Does not configure the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signals, anytime the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-AIS/TU-AIS defect condition.
			1 – Configures the corresponding Transmit STM-0 POH Processor (or DS3/E3 Framer) block to automatically transmit the AU-AIS (or DS3/E3 AIS) Indicator via the "downstream" STM-0 (or DS3/E3) signal, anytime (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-AIS/TU-AIS defect condition.
0	Transmit DS3 AIS (via	R/W	Transmit DS3 AIS upon PDI-P or AU-AIS:
	Downstream DS3s) upon PDI-P		This READ/WRITE bit-field permits the user to configure the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically command the DS3/E3 Framer block to transmit an AIS signal (to downstream circuitry) whenever it (the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block) detects an Async PDI-P or an AU-AIS condition, in the incoming VC-3 data-stream.
		s pro	0 – Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processof block to NOT command the DS3/E3 Framer block to automatically transmit an AIS signal upon detection of an AU-AIS or a PDI-P condition.
	duce	are	1 Configures the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to command the DS3/E3 Framer block to automatically transmit an AIS signal upon detection of an AU- AIS or PDI-P.
	orthe		Note:
	The product		<b>Note:</b> This register bit is only valid if the incoming STM-0 signal is transporting an asynchronous DS3 signal; and if the corresponding channel is configured to operate in the DS3 Mode. When an asynchronous DS3 signal is being transported by a SONET signal, the PDI-P condition is indicated by setting the C2 byte to the value "0xFC".

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 282: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	J1_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	J1 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received VC-3 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new J1 byte value.
			20 × 20

# Table 283: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0	
B3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O 📩	R/0	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	
00,19,00								

BIT NUMBER	Nаме	TYPE	
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	B3 Byte Captured Value[7:0]
	AUCT	arei	These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received VC-3 frame.
	proshe	A no	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new B3 byte value.
	Theatsda		



# Table 284: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive C2 Byte Capture Register (Address Location= 0xN1DB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	C2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION			
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	C2 Byte Captured Value[7:0]			
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received VC-3 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new C2 byte value.			
\$ \$0°						

# Table 285: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0	
G1_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0 0	0	0	0	0	
	0, 0, 0							

BIT NUMBER		Түре	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	e pe	These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received VC-3 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new G1 byte value.
	The stand may	<u> </u>	

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 286: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive F2 Byte Capture Register (Address Location=0xN1E3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	F2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	F2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received VC-3 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new F2 byte value.
			ed its

# Table 287: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0	
H4_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O 🎽	R/0	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	
	0,00,00,00							

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	H4 Byte Captured Value[7:0]
	UST.	30	These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received VC-3 frame.
	Proshee	t not	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new H4 byte value.
	Theatandn		



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# Table 288: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z3 Byte Capture Register (Address Location= 0xN1EB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Z3 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z3 byte value.

# Table 289: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0	
	Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/0	R/O	R/O	R/O	
0	0	0		0	0	0	0	

BIT NUMBER		Түре	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value [7:0]	R/O V	<b>Z4 (K3) Byte Captured Value[7:0]</b> These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z4 (K3) byte value.
	The and mas	<u> </u>	

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 290: Receive TUG-3/AU-3 Mapper VC-3 Path – Receive Z5 Capture Register (Address Location= 0xN1F3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received VC-3 frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.

include value is show in the overridden with a new in the overridden with a new

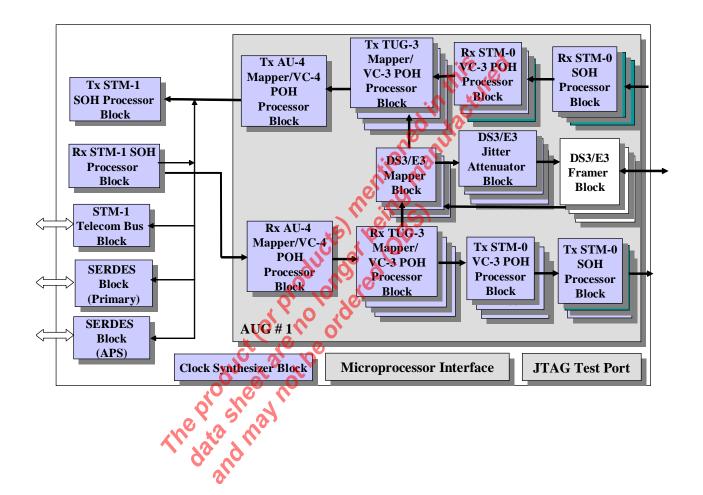


#### 1.10 DS3/E3 FRAMER BLOCK

The register map for the DS3/E3 Framer Block is presented in the Table below. Additionally, a detailed description of each of the "DS3/E3 Framer" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "DS3/E3 Framer Block "highlighted" is presented below in Figure 7.

# Figure 7: Illustration of the Functional Block Diagram of the XRT94L33, with the DS3/E3 Framer Block "High-lighted



#### 1.10.1 **DS3/E3 FRAMER BLOCK REGISTER**

#### Table 291: DS3/E3 Framer Block Control Register Map

Address Location	REGISTER NAME	DEFAULT VALUES
0xN300	Operating Mode Register	0x23
0xN301	I/O Control Register	0xA0
0xN302, 0xN303	Reserved	0x00
0xN304	Block Interrupt Enable Register	0x00
0xN305	Block Interrupt Status Register	0x00
0xN306 – 0xN30B	Reserved	0x00
0xN30C	Test Register	0x00
0xN30D – 0xN30F	Payload HDLC Control Register	0x00
0xN30E – 0xN30F	Reserved	0x00
0xN310	RxDS3 Configuration and Status Register RxE3 Configuration and Status Register # 1 – G.832 RxE3 Configuration and Status Register # 1 – G.751	0x02
0xN311	RxDS3 Status Register RxE3 Configuration and Status Register #2 - 6,832 RxE3 Configuration and Status Register # 2 - 6.751	0x67
0xN312	RxDS3 Interrupt Enable Register RxE3 Interrupt Enable Register # 1 - 6.832 RxE3 Interrupt Enable Register # 1 - 6.751	0x00
0xN313	RxDS3 Interrupt Status Register RxE3 Interrupt Enable Register # 2 – G.832 RxE3 Interrupt Enable Register # 2 – G.751	0x00
0xN314	RxDS3 Sync Detect Enable Register RxE3 Interrupt Status Register # 1 – G.832 RxE3 Interrupt Status Register # 1 – G.751	0x00
0xN315	RxE3 Interrupt Status Register # 2 – G.832 RxE3 Interrupt Status Register # 2 – G.751	0x00
0xN316	RxDS3 FEAC Register	0x7E
0xN317	RxDS3 FEAC Interrupt Enable/Status Register	0x00
0xN318	RxDS3 LAPD Control Register RxE3 LAPD Control Register	0x00
0xN319	RxDS3 LAPD Status Register RxE3 LAPD Status Register	0x00





### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Address Location	REGISTER NAME	DEFAULT VALUES
0xN31A	RxE3 NR Byte Register – G.832	0x00
	RxE3 Service Bit Register – G.751	
0xN31B	RxE3 GC Byte Register – G.832	0x00
0xN31C	RxE3 TTB-0 Register – G.832	0x00
0xN31D	RxE3 TTB-1 Register – G.832	0x00
0xN31E	RxE3 TTB-2 Register – G.832	0x00
0xN31F	RxE3 TTB-3 Register – G.832	0x00
0xN320	RxE3 TTB-4 Register – G.832	0x00
0xN321	RxE3 TTB-5 Register – G.832	0x00
0xN322	RxE3 TTB-6 Register – G.832	0x00
0xN323	RxE3 TTB-7 Register – G.832	0x00
0xN324	RxE3 TTB-8 Register – G.832	0x00
0xN325	RxE3 TTB-9 Register – G.832	0x00
0xN326	RxE3 TTB-10 Register – G.832	0x00
0xN327	RxE3 TTB-11 Register – G.832	0x00
0xN328	RxE3 TTB-12 Register – G832	0x00
0xN329	RxE3 TTB-13 Register G.832	0x00
0xN32A	RxE3 TTB-14 Register – G.832	0x00
0xN32B	RxE3 TTB-15 Register - G.832	0x00
0xN32C	RxE3 SSM Register – G 832	0x00
0xN32D – 0xN32E	Reserved	0x00
0xN32F	RxDS3 Pattern Register	0x0C
0xN330	TxDS3 Configuration Register	0x00
	TxE3 Configuration Register – G.832	
	TxE3 Configuration Register – G.751	
0xN331	TxDS3 FEAC Configuration and Status Register	0x00
0xN332	TxDS3 FEAC Register	0x7E
0xN333	TxDS3 LAPD Configuration Register	0x08
	TxE3 LAPD Configuration Register	
0xN334	TxDS3 LAPD Status/Interrupt Register	0x00
	TxE3 LAPD Status/Interrupt Register	
0xN335	TxDS3 M-Bit Mask Register	0x00
	TxE3 GC Byte Register – G.832	
	TxE3 Service Bits Register – G.751	

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Address Location	REGISTER NAME	DEFAULT VALUES
0xN336	TxDS3 F-Bit Mask # 1 Register	0x00
	TxE3 MA Byte Register – G.832	
0xN337	TxDS3 F-Bit Mask # 2 Register	0x00
	TxE3 NR Byte Register – G.832	
0xN338	TxDS3 F-Bit Mask # 3 Register	0x00
	TxE3 TTB-0 Register – G.832	
0xN339	TxDS3 F-Bit Mask # 4 Register	0x00
	TxE3 TTB-1 Register – G.832	
0xN33A	TxE3 TTB-2 Register – G.832	0x00
0xN33B	TxE3 TTB-3 Register – G.832	0x00
0xN33C	TxE3 TTB-4 Register – G.832	0x00
0xN33D	TxE3 TTB-5 Register – G.832	0x00
0xN33E	TxE3 TTB-6 Register – G.832	0x00
0xN33F	TxE3 TTB-7 Register – G.832	0x00
0xN340	TxE3 TTB-8 Register – G.832	0x00
0xN341	TxE3 TTB-9 Register – G.832	0x00
0xN342	TxE3 TTB-10 Register – G.832	0x00
0xN343	TxE3 TTB-11 Register – 6,832	0x00
0xN344	TxE3 TTB-12 Register - G.832	0x00
0xN345	TxE3 TTB-13 Register - G.832	0x00
0xN346	TxE3 TTB-14 Register – G-832	0x00
0xN347	TxE3 TTB-15 Register - G.832	0x00
0xN348	TxE3 FA1 Error Mask Register – G.832	0x00
	TxE3 FAS Error Mask Upper Register – G.751	
0xN349	TxE3 FA2 Enter Mask Register – G.832	0x00
	TxE3 FAS Error Mask Lower Register – G.751	
0xN34A	TxE3 BIP-8 Mask Register – G.832	0x00
	TxE3 BIP-4 Mask Register – G.751	
0xN34B	Tx SSM Register – G.832	0x00
0xN34C	TxDS3 Pattern Register	0x0C
0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0xN34F	PMON Excessive Zero Count Register - LSB	0x00
0xN350	PMON LCV Event Count Register - MSB	0x00



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Address Location	REGISTER NAME	DEFAULT VALUES
0xN351	PMON LCV Event Count Register - LSB	0x00
0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0xN354	PMON Parity Error Event Count Register - MSB	0x00
0xN355	PMON Parity Error Event Count Register - LSB	0x00
0xN356	PMON FEBE Event Count Register - MSB	0x00
0xN357	PMON FEBE Event Count Register - LSB	0x00
0xN358	PMON CP-Bit Error Count Register - MSB	0x00
0xN359	PMON CP-Bit Error Count Register - LSB	0x00
0xN35A – 0xN367	Reserved	0x00
0xN368	PMON PRBS Bit Error Count Register - MSBO	0x00
0xN369	PMON PRBS Bit Error Count Register - LSB	0x00
0xN36A – 0xN36B	Reserved	0x00
0xN36C	PMON Holding Register	0x00
0xN36D	One Second Error Status Register	0x00
0xN36E	One Second – LCV Count Accumulator Register - MSB	0x00
0xN36F	One Second – LCV Count Accumulator Register - LSB	0x00
0xN370	One Second – Parity Error Accumulator Register - MSB	0x00
0xN371	One Second - Parity Error Accumulator Register - LSB	0x00
0xN372	One Second – CP Bit Error Accumulator Register - MSB	0x00
0xN373	One Second - CP Bit Error Accumulator Register – LSB	0x00
0xN374 – 0xN37F	Reserved	0x00
0xN380	Line Interface Drive Register	0x00
0xN381 – 0xN382	Reserved	0x00
0xN383	TxLAPD Byte Count Register	0x00
0xN384	RxLAPD Byte Count Register	0x00
0xN385 – 0xN3AF	Reserved	0x00
0xN3B0	Transmit LAPD Memory Indirect Address Register	0x00
0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xN3B2	Receive LAPD Memory Indirect Address Register	0x00
0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xN3B4 – 0xN3EF	Reserved	0x00

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#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Address Location	REGISTER NAME	DEFAULT VALUES
0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xN3F1	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 0	0x10
0xN3F2	Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F3 – 0xN3F7	Reserved	0x00
0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00
0xN3FA – 0xN3FF	Reserved	0x00

The base of the of the

#### 1.10.2 DS3/E3 FRAMER BLOCK REGISTER DESCRIPTION

### Table 292: Operating Mode Register (Address Location= 0xN300, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Framer Local Loop Back	IsDS3	Internal LOS Enable	Software RESET	Unused	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	1	0	0	0	1	1

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION		
7	Framer Local	R/W	Framer Block L	.ocal Loop-back Mode:		
	Loop Back		<ul> <li>This READ/WRITE bit field configures the corresponding DS3/E3 Framer block to operate in the Framer Local Loop-back Mode. If the DS3/E3 Framer block has been configured to operate in the Framer Local Loop-back Mode, then the output of the Frame Generator block will be internally looped back into the input of the Primary Frame Synchronizer block.</li> <li>0 - Configures the DS3/E3 Framer block to to operate in the Normal Operating (e.g., Non-Framer Local Loop-back) Mode</li> </ul>			
				DS3/E3 Framer block to op		Loop-
6	IsDS3	R/W	to configure the F Secondary Frame format. The rela	E bit-field, along with Bit 2 ( Frame Generator, the Prima Synchronizer blocks to op tionship between the state ormat is presented below.	ary Frame Synchronizer ar erate in the appropriate fr	nd the aming
		X	Bit 6 (IsDS3)	Bit 2 (Frame Format)	Framing Format	
		NIC		0	E3, ITU-T G.751	
		lo re	0	1	E3, ITU-T G.832	
	e	ata due	1	0	DS3, C-bit Parity	
	1 × ×	<u>,                                    </u>	1	1	DS3, M13	
		3	Framer block (e.g	settings apply to all three ( g., the Primary Frame Syn eer block and the Frame Ger	chronizer block, the Seco	
5	Internal LOS	R/W	Internal LOS Er	nable:		
	Enable		LOS Detector", w blocks. If the us and/or Secondary incoming DS3/E3 and it will declare density and the n data-stream.	E bit-field permits the user t ithin both the Primary and ser enables the "Internal Lo Frame Synchronizer block signal for a sufficient numb and clear the LOS defect number of consecutive "0" to les the "Internal LOS Det	Secondary Frame Synchro OS Detector", then the Po- will be configured to check er of "consecutive" all-zero t condition based upon the bits within the incoming D	onizer rimary ck the os bits e "1s" S3/E3
			Secondary Frame	les the "Internal LOS Det Synchronizer block will N signal for a sufficient numb	OT be configured to chec	ck the

#### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

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			will NOT declar density and the data-stream.	re nor clear the LOS defect number of consecutive "0"	will NOT declare nor clear the LOS defect condition based upon the "1s" density and the number of consecutive "0" bits within the incoming DS3/E3 data-stream.			
			0 – Internal LOS	Detector is disabled.				
			1 – Internal LOS	Detector is enabled.				
			Note:					
			Char the C	nel is configured to opera	can only be enabled if the ate in the Dual-Rail Mode. If erate in the Single-Rail Mode, will be disabled.			
			Fram confi decla devic	e Synchronizer block (de gured to operate in the In re the LOS defect condi	izer block or the Secondary pending upon which block is gress Path) will automatically tion anytime an off-chip LIU ling "EXT_LOS_n" input pin, s register bit.			
4	RESET	R/W	Software RESET Input:					
			A "0" to "1" transition in this bit field commands a Software RESET to each of the following blocks within the Channel.					
			The Primary Frame Synchronizer Block					
			The Secondary Frame Synchronizer Block					
			_	Direction Mapper Block				
				irection Mapper Block				
		8	Once the user executes a Software reset to the Channel, all of the internal state machines (within each of these blocks) will be reset; and the Primary and Secondary Frame Synchronizer blocks will execute a "Reframe" operation. Note: For a Software Reset, the contents of the Command Registers within the corresponding DS3/E3 Framer block will not be reset to their default values.					
3	Unused	R/0	Les h					
2	Frame Format	RN	Frame Format: This READ/WRITE bit-field, along with Bit 6 (IsDS3), permits the user to configure the Frame Generator, the Primary Frame Synchronizer and the Secondary Frame Synchronizer blocks to operate in the appropriate framing format. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below.					
			Bit 6 (IsDS3	Bit 2 (Frame Format)	Framing Format			
			0	0	E3, ITU-T G.751			
			0	1	E3, ITU-T G.832			
			1	0	DS3, C-bit Parity			
			1	1	DS3, M13			
1 - 0	TimRefSel[1:0]	R/W	Time Referen	ce Select:	·			
					e user to define both the timing r the Frame Generator block, as			



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	presented below.		
	TimRefSel[1:0]	Timing Reference	Framing Reference
	00	Loop-Timing (Timing is taken from the Primary Frame Synchronizer block)	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).
	01	The clock source originating from traffic that is "up-stream" from the Frame Generator block. The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Framing Alignment Information from either the Primary or Secondary Frame Synchronizer block (The Frame Generator block will initialte the generation of a new DS3 or E3 Frame based upon Framing Alignment information originating from either the Primary Frame Synchronizer block or the Secondary Frame Synchronizer block, depending upon which block is upstream from the Frame Generator block).
oroduci	are pe	The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).
The stand	11	The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).
	configuratio from either Frame Syne	n, in which the Frame Ge the Primary Frame Synchi	Generator/Frame Synchronizer enerator block is down-stream ronizer block or the Secondary user is strongly advised to set

## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



### Table 293: I/O Control Register (Address Location= 0xN301, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Disable TxLOC	LOC	Disable RxLOC	AMI/Zero- Suppression	Primary Frame - Single Rail/Dual Rail* Select	Frame Generator Block - DS3/E3 Clock Output Invert:	DS3/E3 CLK_IN Invert:	Reframe
R/W	R/O	R/W	R/W	R/O	R/O	R/O	R/W
1	0	1	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Disable	R/W	Disable Transmit Loss of Clock Feature:
	TxLOC		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Loss of Clock" feature.
			If this feature is enabled, then the D\$3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a "Loss of Transmit (or Frame Generator) Clock Event were to occur.
			The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from "hanging" in the event of a "Loss of Clock" event.
			0 – Enables the "Transmit Loss of Clock" feature.
			1 - Disables the "Transmit Loss of Clock" feature.
6	LOC	R/O	Loss of Clock Indicator
			This READ-ONDY bit-field indicates that the Channel has experiences a Loss of Clock event.
5	Disable	R/W	Disable Receive Loss of Clock Feature
	RxLOC		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Loss of Clock" feature.
			If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a "Loss of Receiver (or Frame Synchronizer) Clock Event were to occur.
		100	The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from "hanging" in the event of a "Loss of Clock" event.
			Enables the "Receive Loss of Clock" feature.
			1 – Disables the "Receive Loss of Clock" feature.
4	AMI/Zero- Suppressi	R/W	AMI/Zero-Suppression Line Code Select - Primary Frame Synchronizer Block Input/ Frame Generator Block Output:
	on		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer Block (associated with channel N) to operate in either the AMI or B3ZS/HDB3 Line Code; as described below.
			0 – Configures the DS3/E3 Framer Channel to operate in the B3ZS/HDB3 Line Code.
			1- Configures the DS3/E3 Framer Channel to operate in the AMI Line Code.
3	Primary Frame - Single	R/W	Primary Frame Synchronizer Block Input/Frame Generator Block Output - Single-Rail/Dual-Rail Select:



	Rail/Dual	Th	s READ/WRITE bit-field permits the user to implement either of the following
	Rail Select		ions.
			1. To configure the Primary Frame Synchonizer block to accept the Ingress DS3/E3 data (from the DS3/E3 LIU IC) in either the Single-Rail or Dual-Rail Manner.
			<ol> <li>To configure the DS3/E3 Frame Generator block to output the Egress DS3/E3 data (to the DS3/E3 LIU IC) in either rthe Single-Rail or Dual-Rail Manner.</li> </ol>
		Fra	re specifically, if the user configures the Primary Frame Synchronizer and the me Generator blocks to operate in the Single-Rail Mode, then the following will open.
			The Primary Frame Synchronizer block will accept data (from the LIU IC) in a gle-Rail Manner.
			The Frame Generator block will output data (to the LIU IC) in a Single-Rail nner.
			ne user configures the Primary Frame Synchronizer and Frame Generator blocks operate in the Dual-Rail mode, then the following will happen.
			The Primary Frame Synchronizer block will accept data (from the LIU IC) in a al-Rail Manner.
		• 7	The Frame Generator block will output data (to the LIU IC) in a Dual-Rail Manner.
		0 – in t	Configures the Primary Frame Synchronizer/Frame Generator blocks to operate he Dual-Rail Mode.
			Configures the Primary Frame Synchronizer/Frame Generator blocks to operate he Single-Rail Mode.
		No	te: This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Direction, and if the Frame Generator block has been configured to operate in the Egress Direction.
2	Frame	Fra	me Generator Block - DS3/E3_CLK_OUT Invert:
	Generator Block - DS3/E3_ CLK_OUT Invert:	Ge	s READ/WRITE bit-field permits the user to configure the DS3/E3 Frame nerator block (of Channel n), within the XRT94L33, to update the "TxDS3POS_n" CTxDS3NEG_n" output pins (pin B18, G24, AG9) upon either the rising or falling e of TxDS3LineClk_n" (pin C17, E25, AF10)
	ANC.	"То	TxDS3POS_n/TxDS3NEG_n" is updated upon the rising edge of DS3LineClk_n". The user should insure that the LIU IC will sample DS3POS_n" upon the falling edge of "TxDS3LineClk_n".
			- "TxDS3POS_n/TxDS3NEG_n" is updated upon the falling edge of DS3LineClk_n". The user should insure that the LIU IC will sample DS3POS_n/TxDS3NEG_n" pins upon the rising edge of "TxDS3LineClk_n".
		No	<b>te:</b> This bit-field is only active if the Frame Generator block has been configured to operate in the Egress Path.
1		R/O DS	3/E3_Clock Input - Invert:
	Clock Input - Invert	Se ope "R	s READ/WRITE bit-field permits the user to configure either the Primary or condary Frame Synchronizer block (depending upon which Synchronizer block is erating in the Ingress Path), within the XRT94L33; to sample and latch the DS3POS_n" input pins (pin B14. C21. AG15)" upon either the rising or falling ge of "RxDS3LineClk_n" (pin D14, A24, AF14)
		"R>	<ul> <li>Configures the DS3/E3 Framer block circuitry to sample the DS3POS_n/RxDS3NEG_n" input pins upon the falling edge of the DS3LineClk_n" input signal.</li> </ul>
		1	- Configures the DS3/E3 Framer block circuitry to sample the



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			"RxDS3POS_n/RxDS3NEG_n" input pins upon the rising edge of "RxDS3LineClk_n".
			<b>NOTE:</b> This register bit-field applies to either the Primary or Secondary Frame Synchronizer block (depending upon which block is operating in the Ingress Path).
0	Reframe	R/W	Primary DS3/E3 Frame Synchronizer Block – Reframe Command:
			A "0" to "1" transition, within this bit-field commands the Primary DS3/E3 Frame Synchronizer block (within Channel n) to exit the Frame Maintenance Mode, and go back and enter the Frame Acquisition Mode.
			<b>Note:</b> The user should go back and set this bit-field to "0" following execution of the "Reframe" Command.





# Table 294: Block Interrupt Enable Register (Address Location= 0xN304, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Enable			Unused			DS3/E3 Frame Generator Block Interrupt Enable	One Second Interrupt
R/W	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

			is a
BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7	Primary and/or Secondary DS3/E3 Frame Synch Block Interrupt Enable	R/W	<ul> <li>Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to enable or disable both the Primary and Secondary Frame Synchronizer blocks for Interrupt Generation. If the user enables the Primary and Secondary Frame Synchronizer blocks (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the Source level, as well; in order for these interrupts to be enabled.</li> <li>However, up the user disables the Primary and Secondary Frame Synchronizer block (for Interrupt Generation) at the Block Level, then ALL Frame Synchronizer-related blocks are disabled.</li> <li>0 - Both the Primary and Secondary Frame Synchronizer blocks are Disabled for Interrupt Generation.</li> <li>1 - Both the Primary and Secondary Frame Synchronizer blocks are enabled (at the Block level) for Interrupt Generation.</li> </ul>
6 – 2	Unused	R/O	N N
1	DS3/E3 Frame Generator Block	RANG	<ul> <li>DS3/E3 Frame Generator Block Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to enable or disable the Frame Generator block for Interrupt Generation. If the user enables the Frame Generator block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the "Source" level, as well; in order for these interrupts to be enabled.</li> <li>However, if the user disables the Frame Generator block (for Interrupt Generation) at the Block Level, then ALL Frame Generator-related blocks are disabled.</li> <li>0 – Frame Generator block is Disabled for Interrupt Generation.</li> <li>1 – Frame Generator block is Enabled (at the Block Level) for Interrupt Generation.</li> </ul>
0	One Second Interrupt	R/W	<ul> <li>One Second Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to enable or disable the One-Second Interrupt, within Channel n. If the user enables this interrupt, then Channel n will generate an interrupt at one second intervals.</li> <li>0 – One Second Interrupt is disabled.</li> <li>1 – One Second Interrupt is enabled.</li> </ul>

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 295: Block Interrupt Status Register (Address Location= 0xN305, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Primary and/or Secondary DS3/E3 Frame Sync Block Interrupt Status			Unused			DS3/E3 Frame Generator Block Interrupt Status	One Second Interrupt		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR		
0	0	0	0	0	0	0	0		
	this rec								

BIT NUMBER	NAME	Түре	DESCRIPTION				
7	Primary and/or Secondary	R/O	Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Status:				
	DS3/E3 Frame Synch Block Interrupt Status		This READ-ONLY bit-field indicates whether or not a "Primary or Secondary DS3/E3 Frame Synchronizer Block"-related interrupt (within Channel n) is requesting interrupt service.				
			0 – Indicates that neither the Primary nor the Secondary DS3/E3 Fra Synchronizer block (within Channel n) is NOT requesting any inter service.				
			1 – Indicates, that, either, the Primary or the Secondary DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.				
6 - 2	Unused	R/O	et lo het				
1	DS3/E3 Frame	R/O	DS3/E3 Frame Generator Block Interrupt Status:				
	Generator Block Interrupt Status		This READ-ONLY bit-field indicates whether or not a "DS3/E3 Frame Generator", -related interrupt (within Channel n) is requesting interrupt service.				
		NO	0 - The DS3/E3 Frame Generator block (within Channel n) is NOT requesting any interrupt service.				
	~	0,0	1 – The DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.				
0	One Second	RUR	One Second Interrupt Status				
	Interrupt Status	ð	This RESET-upon-READ bit-field indicates whether or not a "One Second" Interrupt (from Channel n) has occurred since the last read of this register.				
			0 - The One Second Interrupt has NOT occurred since the last read of this register.				
			1 – The One Second Interrupt has occurred since the last read of this register.				

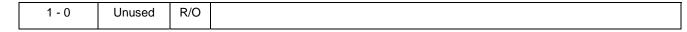


### Table 296: Test Register (Address Location= 0xN30C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxOHSrc	Unu	ised	RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	TxOHSrc	R/W	Transmit Overhead Bit Source:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to accept and insert overhead bits/bytes which are input via the "Transmit Payload Data Input Interface" block, as indicated below.
			0 – No overhbead bit insertion will occur. Overhead bits/bytes are internally generated by the DS3/E3 Frame Generator block.
			1 – Overhead bit insertion will occur. In this case, the Overhead bits/byte data is accepted from the Transmit Payload Data input Interface block.
			<b>Note:</b> This register bit applies to all framing formats that are supported by the Frame Generator block.
6 - 5	Unused	R/O	endi
4	RxPRBS	R/O	PRBS Lock Indicator:
	Lock		This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) has acquired "PRBS Lock" with the payload data of the incoming DS3 of E3 data stream, as described below.
			0 – Indicates that the PRBS Receiver does not have PRBS Lock with the incoming data stream.
			1 – Indicates that the PRBS Receiver does have PRBS Lock with the incoming data stream.
			Note: This bit-field is not valid if the PRBS Receiver is disabled, or if the Primary Frame Synchronizer block is bypassed.
3	RxPRBS	R/W	Receive PRBS Enable:
	Enable	6932	This READ/WRITE bit-field permits the user to either enable or disable the PRBS Receiver within the Primary Frame Synchronizer block. Once the user enables the PRBS Receiver, then it will proceed to attempt to acquire and maintain pattern (or PRBS Lock) within the payload bits, within the incoming DS3 or E3 data stream.
		2	0 – Disables the PRBS Receiver.
			1 – Enables the PRBS Receiver.
			<b>Note:</b> This bit-field is ignored if the Frame Synchronizer block is by-passed.
2	TxPRBS	R/W	Transmit PRBS Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the PRBS Generator within the DS3/E3 Frame Generator block. Once the user enables the PRBS Generator block, then it will proceed to insert a PRBS pattern into the payload bits, within the outbound DS3 or E3 data stream.
			0 – Disables the PRBS Generator.
			1 – Enables the PRBS Generator.
			<b>Note:</b> This bit-field is ignored if the Frame Generator block is by-passed.

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### 1.10.3 RECEIVE DS3 RELATED REGISTERS

# Table 297: RxDS3 Configuration and Status Register (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
DS3 AIS Defect Declared	DS3 LOS Defect Declared	DS3 Idle Condition Declared	OOF Defect Declared	Unused	Framing with Valid P- Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	1	0	0	1	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7	DS3 AIS	R/O	DS3 AIS Defect Declared Indicator Primary Frame Synchronizer Block:				
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition in its incoming path, as described below				
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the DS3 AIS Detect condition.				
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the DS3 AIS Defect condition.				
6	LOS Defect Declared	R/O	LOS Defect Condition Declared Indicator – Primary Frame Synchronizer Block:				
			This READ ONLY bit field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOS defect condition, in its incoming path, as described below.				
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOS defect condition in its incoming path.				
		Ċ	I – Indicates that the Primary Frame Synchronizer block is currently declaring the LOS defect condition in its incoming path.				
5						R/O	DS3 Idle Signal Pattern Detected – Primary Frame Synchronizer Block:
	Condition Declared	n she	This READ-ONLY bit-field indicates whether or not the Primary Frame synchronizer block is currently detecting the DS3 Idle pattern, in its incoming path.				
	1.8	at d	0 – Indicates that the Primary Frame Synchronizer block is NOT currently detecting the DS3 Idle Pattern, in its incoming path.				
		<i>®</i> .	1 – Indicates that the Primary Frame Synchronizer block is currently detecting the DS3 Idle Pattern in its incoming path.				
			<b>NOTE:</b> This bit-field is only valid of the DS3/E3 Framer block has been configured to operate in the DS3 Mode.				
4	OOF Defect Condition	R/O	OOF (Out of Frame) Defect Condition Declared Indicator – Primary Frame Synchronizer Block:				
	Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the OOF (Out of Frame) defect condition, as described below.				
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition.				
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition.				

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3	Unused	R/O	
2	Framing with	R/W	Framing with Valid P-Bit Select:
	Valid P Bits		This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Frame Acquisition/Maintenance criteria that the Primary Frame Synchronizer block will use to (1) acquire and declare Frame Synchronization, and (2) to declare the OOF defect condition.
			0 – Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking)
			In this mode, the Primary Frame Synchronizer block will declare the "In-frame" state, one it has successfully completed both the "F-Bit Search" and the "M-Bit Search" states.
			1 – Framing Acquisition/Maintenance with P-bit Checking
			In this mode, the Primary Frame Synchronizer block will (in addition to passing through the "F-Bit Search" and "M-Bit Search" states) also verify valid P-bits, prior to declaring the "In-Frame" state.
			<b>Note:</b> This bit-field is ignored if the DS3/E3 Framer block is configured to operate in the E3 Mode, or if the Primary Frame Synchronizer block is by-passed.
1	F-Sync Algo	R/W	F-Bit Search State Criteria Select:
			This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria.
			0 – Configures the Primary Frame Synchronizer block to declare the OOF defect condition anytime it determines that 6 out of the last 15 F-bits are erred.
			1 – Configures the Primary Frame Synchronizer block to declare the OOF is defect condition anytime it determines that 3 out of the last 15 F-bits are erred.
			<b>Note:</b> This bit-field is ignored if the DS3/E3 Framer block has been configured to operate in the E3 Mode, or if the Primary Frame Synchronizer block is by-passed.
0	M-Sync Algo	R/W	M-Bit Search State Criteria Select:
		2	This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria.
		oro	0 Configures the Primary Frame Synchronizer block to NOT declare the OOF defect condition, due to M-bit Errors.
	~*	623	1 Configures the Primary Frame Synchronizer block to declare the OOF defect condition anytime it determines that the M-bits within 3 out of 4 consecutive DS3 frames are in error.
		ัจ	<b>NOTE:</b> This bit-field is ignored if the DS3/E3 Framer block has been configured to operate in the E3 Mode.

### Table 298: RxDS3 Status Register (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		FERF/RDI Defect Declared	RxAIC	RxFEBE[2:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4	FERF/RDI Defect	R/O	FERF/RDI (Far-End Receive Failure/Remote Defect Indicator) Defect Declared Indicator:
	Declared		This READ-ONLY bit-field indicates whether or not the PrimaryFrame Synchronizer block is currently declaring the FERF/RDI defect condition as described below.
			0 – The Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition.
			1 – The Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition.
			<b>Note:</b> This bit-field is not valid if the Primary Frame Synchronizer block has been by-passed.
3	RxAIC	R/O	Receive Alc State:
			This READ-ONLY bit-field indicates the current state of the AIC bit-field within the incoming DS3 data-stream.
			0 – Indicates that the Frame Synchronizer block has received at least 2 consecutive M-frames that have the AIC bit-field set to "0".
		JUC	1 - Indicates that the Frame Synchronizer block has received at least 63 consecutive M-frames that have the AIC bit-field set to "1".
	C C	ro ne	<b>NOTE:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.
2 – 0	RxFEBE[2:0]	R/O	Receive FEBE (Far-End Block Error) Value:
	11.8		These READ-ONLY bit-fields reflect the FEBE value within the most recently received DS3 frame.
		S.	RxFEBE[2:0] = [1, 1, 1] indicates a normal condition. All other values for RxFEBE[2:0] indicates an erred condition at the remote terminal equipment.
			Note:
			1. This bit-field is not valid if the Primary Frame Synchronizer block has been by-passed.
			2. This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the DS3, C-bit Parity Framing format.

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# Table 299: RxDS3 Interrupt Enable Register (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of CP Bit Error Interrupt Enable	Change of LOS Defect Condition Interrupt Enable	Change of AIS Defect Condition Interrupt Enable	Change of Idle Condition Interrupt Enable	Change of FERF/RDI Defect Condition Interrupt Enable	Change of AIC State Interrupt Enable	Change of OOF Defect Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Detection of	R/W	Detection of CP-Bit Error Interrupt Enable:
	CP Bit Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of CP-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects CP bit errors. 0 – Disables the "Detection of CP Bit Error" Interrupt.
			1 – Enables the "Detection of CR-Bit Error" Interrupt.
			<b>Note:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
6	Change of	R/W	Change in LOS Defect Condition Interrupt Enable:
	LOS Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronized block will generate an interrupt in response to either of the following conditions.
		2	The instant that the Primary Frame Synchronizer block declares an LOS defect condition.
		or of	• The instant that the Primary Frame Synchronizer block clears the LOS defect condition.
	N	0.0	0 visables the "Change in LOS Defect Condition" Interrupt.
		10	- Enables the "Change in LOS Defect Condition" Interrupt.
		័ភ	<b>NOTE:</b> This configuration setting only applies to the Primary Frame Synchronizer block. This configuration setting does not apply to the Secondary Frame Synchronizer block.
5	Change of AIS	R/W	Change in AIS Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable	Condition Interrupt	This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS (Alarm Indication Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			• The instant that the Primary Frame Synchronizer block declares an AIS defect condition.
			• The instant that the Primary Frame Synchronizer block clears the AIS defect condition.
			0 – Disables the "Change in AIS Defect Condition" Interrupt.



			1 – Enables the "Change in AIS Defect Condition" Interrupt.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
4	Change of	R/W	Change in DS3 Idle Condition Interrupt Enable:
	DS3 Idle Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in DS3 Idle Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			• The instant that the Primary Frame Synchronizer block declares the DS3 Idle condition.
			• The instant that the Primary Frame Synchronizer block clears the DS3 Idle condition.
			0 – Disables the "Change in DS3 Idle Condition" Interrupt.
			1 – Enables the "Change in DS3 Idle Condition" Interrupt.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
3	Change of	R/W	Change in FERF/RDI Defect Condition Interrupt Enable:
	FERF/RDI Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF/RDI (Far-End Receive Failure/Remote Defect Indicator) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			• The instant that the Primary Frame Synchronizer block declares the FERF/RDI defect condition.
			<ul> <li>The instant that the Primary Frame Synchronizer block clears the FERF/RDI defect condition.</li> </ul>
			0 + Disables the "Change in FERF/RDI Defect Condition" Interrupt.
			P-Enables the "Change in FERF/RDI Defect Condition" Interrupt.
		duci	<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
2	Change of AIC	R/W	Change in AIC State Interrupt Enable:
	State Interrupt Enable	atord	This READ/WRITE bit-field permits the user to either enable or disable the Change in AIC State" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to it detecting a change in the AIC bit-field, within the incoming DS3 data stream.
			0 – Disables the "Change in AIC State" Interrupt.
			1 – Enables the "Change in AIC State" Interrupt.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
1	Change of	R/W	Change in OOF Defect Condition Interrupt Enable:
	OOF Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			• The instant that the Primary Frame Synchronizer block declares the OOF defect condition.

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			• The instant that the Primary Frame Synchronizer block clears the OOF defect condition.
			0 – Disables the "Change in OOF Defect Condition" Interrupt.
			1 – Enables the "Change in OOF Defect Condition" Interrupt.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
0	Detection of P- Bit Error Interrupt Enable	R/W	Detection of P-Bit Error Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Detection of P-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects P bit errors.
			0 – Disables the "Detection of P Bit Error" Interrupt.
			1 – Enables the "Detection of P-Bit Error" werrupt
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
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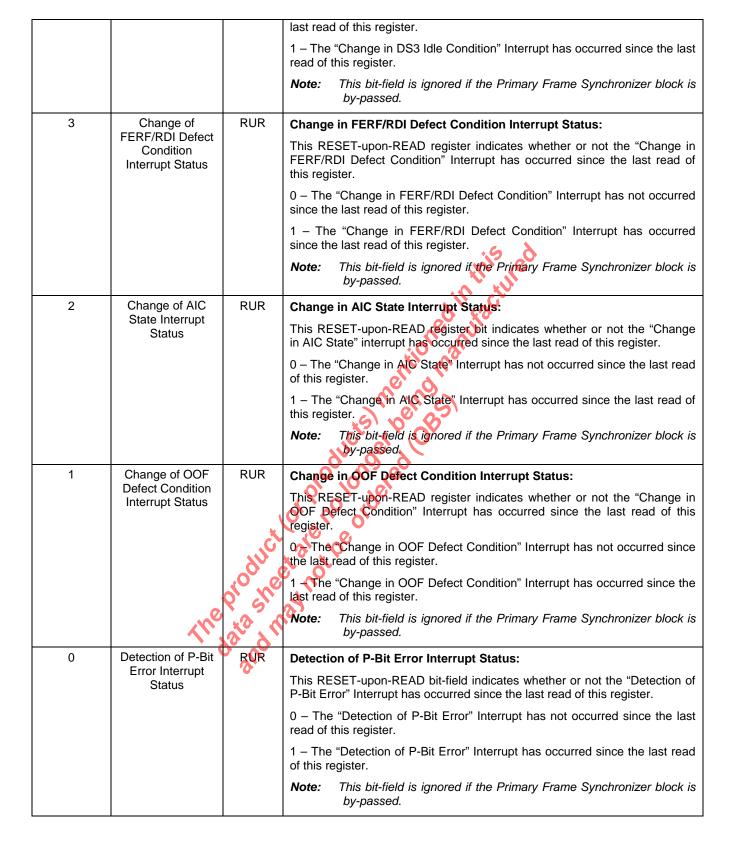


# Table 300: RxDS3 Interrupt Status Register (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of CP Bit Error Interrupt Status	Change of LOS Defect Condition Interrupt Status	Change of AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Change of FERF/RDI Condition Interrupt Status	Change of AIC State Interrupt Status	Change of OOF Defect Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of CP Bit Error Interrupt Status	RUR	<ul> <li>Detection of CP-Bit Error Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.</li> <li>0 - The "Detection of CP-Bit Error" Interrupt has not occurred since the last read of this register.</li> <li>1 - The "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.</li> <li>Note: This bit-field is only active if the DS3/E3 Framer block has been</li> </ul>
6	Change of LOS	RUR	configured to operae in the DS3, C-bit Parity Framing Format. This bit field is also ignored if the Primary Frame Synchronizer block is by passed.
6	Defect Condition Interrupt Status	RUR CHICE CON CHICE CON CHICE CON CHICE CON CON	<ul> <li>Change in LOS Defect Condition Interrupt Status:</li> <li>This RESET upon-READ register indicates whether or not the "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>O - The "Change in LOS Defect Condition" Interrupt has not occurred since the last read of this register.</li> <li>The "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>The "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>Note: This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.</li> </ul>
5	Change of AIS Defect Condition Interrupt Status	<b>R</b> ŮR	<ul> <li>Change in AIS Defect Condition Interrupt Status</li> <li>This RESET-upon-READ register indicates whether or not the "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>0 - The "Change in AIS Defect Condition" Interrupt has not occurred since the last read of this register.</li> <li>1 - The "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register.</li> <li>Note: This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.</li> </ul>
4	Change of DS3 Idle Condition Interrupt Status	RUR	<ul> <li>Change in DS3 Idle Condition Interrupt Status:</li> <li>This RESET-upon-READ register indicates whether or not the "Change in DS3 Idle Condition" interrupt has occurred since the last read of this register.</li> <li>0 – The "Change in DS3 Idle Condition" Interrupt has not occurred since the</li> </ul>

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# Table 301: RxDS3 Sync Detect Register (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	P-Bit Correct	F Algorithm	One and Only		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
2	P-Bit Correct	R/W	P-Bit Correct:
			This READ/WRITE bit-field permits the user to enable or disable the "P-Bit Correct" feature within the Primary Frame Synchronizer block. If the user enables this feature, then the Primary Frame Synchronizer block will automatically invert the state of any P-bits, whenever it detects "P-bit errors" within the incoming DS3 data stream.
			0 – Disables the "P-Bit Correct" feature.
			1 – Enables the "P-Bit Correct" feature
1	F Algorithm	R/W	F-Bit Search Algorithm Select:
			This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria that the Primary Frame Synchronizer block will use whenever it is operating in the "F-Bit Search" state, as depicted below.
			0 – Configures the Primary Frame Synchronizer block will move on to the "M-Bit Search" state, whenever it has properly located 10 consecutive F- bits within the incoming DS3 data-stream.
			1 + Primary Frame Synchronizer block will move on to the "M-Bit Search" state, when it has properly located 16 consecutive F-bits within the incoming DS3 data-stream.
			<b>NOTE:</b> This bit-field is only active if the user has configured the DS3/E3 Framer block to operate in the DS3 Mode.
0	One and Only	R/W	F-Bit Search/Mimic-Handling Algorithm Select:
	ner	Ata d ma	This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria that the Primary Frame Synchronizer block will use whenever it is operating in the "F-Bit Search" state.
	1.8	andn	0 – Configures the Primary Frame Synchronizer block to move on to the "M-Bit Search" state, when it has properly located 10 (or 16) consecutive F- bits (as configured in Bit 1 of this register).
			1 – Configures the Primary Frame Synchronizer block to move on to the "M-Bit Search" state, when (1) it has properly located 10 (or 16) consecutive F-bits; and (2) when it has located and identified only one viable "F-Bit Alignment" candidate.
			<b>Note:</b> If this bit is set to "1", then the Primary Frame Synchronizer block will NOT transition into the "M-Bit Search" state, as long as at least two viable candidate set of bits appear to function as the F-bits.

## 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



#### Table 302: RxDS3 FEAC Register (Address Location= 0xN316, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused		RxFEACCode[5:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	1	1	1	1	1	1	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	
6 - 1	RxFEAC_Code[5:0]	R/O	Receive FEAC Code Word:
			These READ-ONLY bit-fields contain the value of the most recently "validated" FEAC Code word. <b>NOTE:</b> These bit-fields are only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
0	Unused	R/O	2 5 5 B

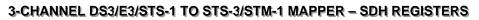
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# Table 303: RxDS3 FEAC Interrupt Enable/Status Register (Address Location= 0xN317, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" (the default value) for normal operation.
4	FEAC Valid	R/O	FEAC Message Validation Indicator:
			This READ-ONLY bit-field indicates that the FEAC Code (which resides within the "RxDS3 FEAC" Register) has been validated by the Receive FEAC Controller block. The Receive FEAC Controller block will validate a FEAC codeword if it has received this codeword in 8 out of the last 10 FEAC Messages. Polled systems can monitor this bit-field, when checking for a newly validated FEAC codeword.
			0 – FEAC Message is not (or no longer) validated.
			1 – FEAC Message has been validated.
			<b>NOTE:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
3	RxFEAC	R/W	FEAC Message Remove Interrupt Enable:
	Remove Interrupt Enable	du	This READ/WRITE bit-field permits the user to either enable or disable the "Receive FEAC Remove Interrupt". If the user enables this interrupt, then the Primary Framer Synchronizer block will generate an interrupt anytime the most recently validated FEAC Message has been removed. The Receive FEAC Controller sub-block will remove a validated FEAC codeword, if it has received a different codeword in 3 out of the last 10 FEAC Messages.
		5 5	0 – Receive FEAC Remove Interrupt is disabled.
		50	Receive FEAC Remove Interrupt is enabled.
		datind	<b>Note:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. Further, this bit-field is ignored if the Primary Frame Synchronizer block is by-passed.
2	RxFEAC	RUR	FEAC Message Remove Interrupt Status:
	Remove Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "FEAC Message Remove Interrupt" has occurred since the last read of this register.
			0 – FEAC Message Remove Interrupt has NOT occurred since the last read of this register.
			1 – FEAC Message Remove Interrupt has occurred since the last read of this register.
			NOTE: This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
1	RxFEAC	R/W	FEAC Message Validation Interrupt Enable:
	Valid Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the



	Interrupt Enable		FEAC Message Validation Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime a new FEAC Codeword has been validated by the Receive FEAC Controller sub-block.
			0 – FEAC Message Validation Interrupt is NOT enabled.
			1 – FEAC Message Validation Interrupt is enabled.
			<b>NOTE:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
0	RxFEAC	RUR	FEAC Message Validation Interrupt Status:
	Valid Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "FEAC Message Validation" Interrupt has occurred since the last read of this register.
			0 – FEAC Message Validation Interrupt has not occurred since the last read of this register.
			1 – FEAC Message Validation Interrupt has occurred since the last read of this register.
			<b>NOTE:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.

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# Table 304: RxDS3 LAPD Control Register (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any		Unu	used		Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLAPD Any	R/W	<ul> <li>Receive LAPD – Any kind:</li> <li>This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block) to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes.</li> <li>0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.</li> <li>Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values.</li> <li>Note:</li> <li>This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.</li> <li>The user can determine the size (or byte-count) of the most recently received</li> </ul>
6-3	Unused	RIO	LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384)
2	Receive LAPD Enable	R/W	Receive LAPD Controller sub-block Enable: This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller sub-block within the Primary Frame Synchronizer block. If the user enables the Receive LAPD Controller sub-block, then it will immediately begin extracting out and monitoring the data (being carried via the "DL" bits) within the incoming DS3 data stream.
			0 – Enables the Receive LAPD Controller sub-block.
			1 – Disables the Receive LAPD Controller sub-block.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
1	Receive LAPD	R/W	Receive LAPD Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller sub- block receives a new PMDL Message.
			0 – Disables the "Receive LAPD Message" Interrupt.
			1 – Enables the "Receive LAPD Message" Interrupt.



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			<b>Note:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.
0	Receive LAPD	RUR	Receive LAPD Message Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register.
			0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register.
			1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register.
			<b>Note:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.

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# Table 305: RxDS3 LAPD Status Register (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION					
7	Unused	R/O						
6	RxABORT	R/O	Receive A	BORT Sec	uence Indicator			
			<ul> <li>This READ-ONLY bit-field indicates that the Receive LAPD Controller sub-block has received an ABORT sequence (e.g., a string of seven consecutive "0s").</li> <li>0 – Indicates that the Receive LAPD Controller sub-block has NOT received an ABORT sequence.</li> <li>1 - Indicates that the Receive LAPD Controller sub-block has received an ABORT sequence.</li> <li>Note: Once the Receive LAPD Controller sub-block receives an ABORT sequence, it will set this bit-field "high", until it receives another LAPD Messages.</li> </ul>					
5 – 4	RxLAPDType[1:0]	R/O	Receive LAPD Message Type Indicator: These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.					
	61	a.	RxLAPD	Type[1:0]	Message Type			
	aro x	6 (	o	0	CL Path Identification			
		23	0	1	Idle Signal Identification			
	11, 21, 5		1	0	Test Signal Identification			
	31		1	1	ITU-T Path Identification			
3	RxCR Type	R/O		C/R Value:				
					field indicates the value of the C/R bit (within or of the most recently received LAPD Message.	ne		
					s only active if the DS3/E3 Framer block has bee in the DS3, C-bit Parity Framing format.	en		
2	RxFCS Error	R/O	Receive Frame Check Sequence (FCS) Error Indicator:					
			This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error.					
			0 – The m an FCS er		/ received LAPD Message frame does not conta	ain		
			1 – The m	nost recently	y received LAPD Message frame does contain a	an		

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			FCS error.
			<b>NOTE:</b> This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
1	End of Message	R/O	End of Message Indicator
			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message, as described below.
			0 – The Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message.
			1 – The Receive LAPD Controller sub-block has received a completed LAPD Message.
			<b>Note:</b> Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.
0	Flag Present	R/O	Receive Flag Sequence Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel), as described below.
			0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet.
			1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.
	theba	andma	1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.

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### Table 306: RxDS3 Pattern Register (Address Location= 0xN32F, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
DS3 AIS Unframed All Ones	DS3 AIS Non Stuck Stuff	Unused	Receive LOS Pattern		Receive DS3 lo	dle Pattern[3:0]	
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	DS3 AIS	R/W	DS3 AIS - Unframed All Ones – AIS Pattern
	Unframed All Ones		This READ/WRITE bit-field, (along with the "Non-Stuck-Stuff" bit) permits the user specify the "AIS Declaration" criteria for the Primary Frame Synchronizer block, as described below.
			0 – Configures the Primary Frame Synchronizer block to declare the AIS defect condition, when receiving a DS3 signal carrying a "framed 1010" pattern.
			1 – Configures the Primary Frame Synchronizer block to declare the AIS defect condition, when receiving either an unframed, All Ones pattern or a "framed 1010" pattern.
6	DS3 AIS	R/W	DS3 AIS - Non Stuck Stuff Option – AIS Pattern
	Non-Stuck Stuff		This READ/WRITE bit-field (along with the "Unframed All Ones – AIS Pattern bit-field) permits the user to define the "AIS Defect Declaration" criteria for the Primary Frame Synchronizer block, as described below.
			0 – Configures the Primary Frame Synchronizer block to require that all "C" bits are set to "0" before it will declare the AIS defect condition.
			1 - Configures the Primary Frame Synchronizer block to NOT require that all "C" bits are set to "0" before it will declare the AIS defect condition. In
		wit.	this mode, no attention will be paid to the state of the "C" bits within the incoming DS3 data-stream.
5	Unused	R/00	
4	Receive LOS	RAW	Receive LOS Pattern:
	Patterno	a n'	This READ/WRITE bit-field permits the user to define the "LOS Defect Declaration" criteria for the Primary Frame Synchronizer block, as described below.
	•	<b>2</b> ,	0 – Configures the Primary Frame Synchronizer block to declare the LOS defect condition if it receives a string of a specific length of consecutive zeros.
			1 – Configures the Primary Frame Synchronizer block to declare the LOS defect condition if it receives a string (of a specific length) of consecutive ones.
			<b>NOTE:</b> This bit-field is only enabled if the "Internal LOS Enable" feature has been enabled within the Primary Frame Synchronizer block.
3 – 0	Receive DS3	R/W	Receive DS3 Idle Pattern:
	Idle Pattern[3:0]		These READ/WRITE bit-fields permit the user to specify the pattern in which the Primary Frame Synchronizer will recognize as the "DS3 Idle Pattern".
			<b>Note:</b> The Bellcore GR-499-CORE specified value for the Idle Pattern is a framed repeating "1, 1, 0, 0…" pattern. Therefore, if the user wishes to configure the "Primary Frame Synchronizer" to declare

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



an "Idle Pattern" when it receives this pattern, then he/she writ the value [1100] into these bit-fields.
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#### 1.10.4 RECEIVE E3, ITU-T G.751 RELATED REGISTERS

# Table 307: RxE3 Configuration and Status Register # 1 - G.751 (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		RxFERF		Unused		RxBIP-4
			Algo				Enable
R/O	R/O	R/O	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

			.6 2
BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 5	Unused	R/O	in tetuli
4	RxFERF Algo	R/W	Receive FERF Algorithm Select:
			This READ/WRITE bit-field permits the user to select the "FERF Declaration" and "Clearance" criteria that will be used by the Primary Frame Synchronizer block.
			<ul> <li>0 – The Primary Frame Synchronizer block declares the FERF/RDI defect condition if the "A" bit-field (within the incoming E3 data-stream) is set to "1" for 3 consecutive frames. The Primary Frame Synchronizer block will clear the FERF/RDI defect condition if the "A" bit-field is set to "0" for 3 consecutive frames.</li> <li>1 – The Primary Frame Synchronizer block declares the FERF/RDI defect</li> </ul>
			condition if the "A" bit field (within the incoming E3 data-stream) is set to "1" for 5 consecutive frames. The Primary Frame Synchonizer block will clear the FERF/RDI defect condition if the "A" bit-field is set to "0" for 5 consecutive frames.
		and and	<b>NOTE:</b> This bit-field is only valid if the DS3/E3 Framer block has been configured to operate in the E3, ITU-T G.751 Framing format.
3 – 1	Unused	R/O	8
0	RxBIP4 Enable	RING	<ul> <li>Enable BIP-4 Verification:</li> <li>This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to compute and verify the BIP-4 value, within the incoming E3 data-stream.</li> <li>0 – BIP-4 Verification is NOT performed.</li> </ul>
			1 – BIP-4 Verification is performed.



# Table 308: RxE3 Configuration and Status Register # 2 - G.751 (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLOF Algo	LOF Defect Condition Declared	OOF Defect Condition Declared	LOS Defect Condition Declared	AIS Defect Condition Declared	Unused		FERF/RDI Defect Condition Declared
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	0	0	1

BIT NUMBER	NAME	Түре	DESCRIPTION		
7	RxLOF Algo	R/W	Receive LOF (Loss of Frame) Defect Declaration/Clearance Criteria Select:		
			This READ/WRITE bit-field permits the user to select the Loss of Frame (LOF) Declaration and Clearance Criteria that the Primary Frame Synchronizer block will use.		
			0 – The Primary Frame Synchronizer block will declare the LOF defect condition if the Primary Frame Synchronizer block resides within the OOF (Out-of-Frame) state for 24 E3 frame periods. The Primary Frame Synchronizer block will clear the LOF defect condition once it (the Primary Frame Synchronizer block) resides within the "In-Frame" state for 24 E3 frame period.		
			1 – The Primary Frame Synchronizer block will declare the LOF defect condition if the Primary Frame Synchronizer block resides within the OOF state for 8 E3 frame periods. The Primary Frame Synchronizer block will clear the LOF defect condition once it (the Primary Frame Synchronizer block) resides within the "In-Frame" state for 8 E3 frame periods.		
6	LOF Defect Condition Declared	ion	LOF (Loss of Frame) Defect Declared Indicator		
			This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOF defect condition, as described below.		
			0 Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOF defect condition within the incoming data stream.		
			1 - Indicates that the Primary Frame Synchronizer block is currently declaring the LOF defect condition within the incoming data stream.		
		· 8° 8	<b>Note:</b> This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.		
5	OOF Defect	t R/O	OOF (Out of Frame) Defect Condition Indicator		
	Condition Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the OOF defect condition, as depicted below.		
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition with the incoming data stream.		
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition with the incoming data stream.		
			<b>Note:</b> This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.		
4	LOS Defect	R/O	LOS (Loss of Signal) Defect Condition Indicator		
	Condition		This READ-ONLY bit-field indicates whether or not the Primary Frame		



	Declared		Synchronizer block is currently declaring the LOS defect condition, as described below.
			0 – Indicates that the Primary Frame Synchronizer/Channel is NOT currently declaring the LOS defect condition in the incoming data stream.
			1 – Indicates that the Primary Frame Synchronizer/Channel is currently declaring the LOS defect condition in the incoming data stream.
3	AIS Defect	R/O	AIS Defect Condition Indicator:
	Condition Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data-stream, as described below.
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the AIS defect condition with the incoming data stream.
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the AIS defect condition with the incoming data stream.
			<b>Note:</b> This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.
2 – 1	Unused	R/O	ACO JEO
0	FERF/RDI Defect Condition Declared	R/O	<ul> <li>FERF/RDI (Far-End-Receive Failure/Remote Defect Indicator) Defect Condition Indicator:</li> <li>This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition as described below.</li> <li>0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition.</li> <li>1 – Indicates that the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition.</li> <li>Note: This bit-field is ignored if the Primary Frame Synchronizer block is by-passed or if the user has configured the Primary Frame Synchronizer block is by-nchronizer block to compute and verify the BIP-4 within the incoming E3 data-stream.</li> </ul>
The data difference in the ser has configured the Primary Frame Synchronizer block to compute and verify the BIP-4 within the incoming E3 data-stream.			



# Table 309: RxE3 Interrupt Enable Register # 1 - G.751 (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	wis eo
4	COFA Interrupt Enable	R/W	<ul> <li>Change of Framing Alignment Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" Interrupt within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects a Change in Frame Alignment (e.g., the FAS bits have appeared to move to a different location in the E3 data stream).</li> <li>0 – Disables the "Change of Framing Alignment" Interrupt</li> <li>1 – Enables the "Change of Framing Alignment" Interrupt</li> </ul>
3	Change in OOF Defect Condition Interrupt Enable	R/W	<ul> <li>Change in OOF Defect Condition Interrupt Enable</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Defect Condition" Interrupt, within the Channel of the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions:</li> <li>The instant that the Primary Frame Synchronizer block declares the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the OOF defect condition.</li> <li>This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.</li> </ul>
2	Change in LOF Defect Condition Interrupt Enable	R/W	<ul> <li>Change in LOF Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOF (Loss of Frame) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.</li> <li>The instant that the Primary Frame Synchronizer block declares the LOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOF defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOF defect condition.</li> </ul>



			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
1	Change in LOS Defect Condition Interrupt Enable	R/W	<ul> <li>Change in LOS Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.</li> <li>The instant that the Primary Frame Synchronizer block declares an LOS defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOS defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the LOS defect condition.</li> <li>Disables the "Change in LOS Defect Condition" Interrupt.</li> <li>Enables the "Change in LOS Defect Condition" Interrupt.</li> </ul>
0	Change in AIS Defect Condition Interrupt Enable	R/W	<ul> <li>Change in AIS Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS (Alarm Indication Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.</li> <li>The instant that the Primary Frame Synchronizer block declares the AIS defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the AIS defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the AIS defect condition.</li> <li>The instant that the Primary Frame Synchronizer block clears the AIS defect condition.</li> <li>The "Change in AIS Defect Condition" Interrupt can be enabled or disabled, as described below.</li> <li>O – Disables the "Change in AIS Defect Condition" Interrupt.</li> <li>This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.</li> </ul>
	The	bata nd	Note: This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.



Table 310: RxE3 Interrupt Enable Register # 2 - G.751 (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-4 Error Interrupt Enable	Detection of FAS Bit Error Interrupt Enable	Reserved
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 4	Unused	R/O	Please set to "0" (the default value) for normal operation
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	Change in FERF/RDI Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF/RDI Defect Condition" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following events.
			<ul> <li>Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition.</li> <li>Whenever the Primary Frame Synchronizer block clears the FERF/RDI Defect condition</li> </ul>
			The user car enable or disable this particular interrupt as described below.
			0 – Disables the Change in FERF/RDI Defect Condition" Interrupt.
		م	1 – Enables the "Change in FERF/RDI Defect Condition" Interrupt. Note: This bit-field is ignored if the Primary Frame Synchronizer block is configured to verify BIP-4 values within each incoming E3 frame. Further, this bit-field is ignored anytime the Primary Frame Synchronizer block is by-passed.
2	Detection of BIP-4 Error Interrupt	R/W	Detection of BIP-4 Error Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the
	Enable	1,9st	"Detection of BIP-4 Error" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects a BIP-4 error, within the incoming E3 data stream.
		.0.	The user can enable or disable this interrupt as described below.
			0 – Disables the "Detection of BIP-4 Error" Interrupt.
			1 – Enables the "Detection of BIP-4 Error" Interrupt.
			<b>Note:</b> This bit-field is only active if the Receive E3 Framer block has been configured to compute and verify the BIP-4 values within each incoming E3 frame. This bit-field is ignored anytime the Primary Frame Synchronizer block is by-passed.
1	Detection of FAS Bit	R/W	Detection of FAS (Framing Alignment Signal) Bit Error Interrupt Enable:
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "FAS Bit Error" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects an FAS error within the incoming E3 data stream.



			0 – Disables the "Detection of FAS Bit Error" Interrupt.
			1 – Enables the "Detection of FAS Bit Error" Interrrupt.
			<i>Note:</i> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
0	Unused	R/O	Please set to "0" (the default value) for normal operation.

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# Table 311: RxE3 Interrupt Status Register # 1 - G.751 (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	*histor
4	COFA Interrupt	RUR	Change of Framing Alignment (COFA) Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of
	Status		Framing Alignment (COFA) interrupt has occurred since the last read of this register.
			0 – The "COFA" Interrupt has NOT occurred since the last read of this register.
			1 – The "COFA" Interrupt has occurred since the last read of this register.
3	Change in OOF Defect	RUR	Change of OOF (Out of Frame) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of OOF Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Primary Frame Synchronizer block declares the OOF Defect Condition
		proc	Whenever the Primary Frame Synchronizer block clears the OOF Defect
			Indicates that the "Change in OOF Defect Condition" Interrupt has NOT occurred since the last read of this register.
		(ne ato	1 Indicates that the "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register.
		~ *	<b>Note:</b> The user can obtain the current state of the OOF Defect condition within the DS3/E3 Framer block by reading out the state of Bit 5 (OOF Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).
2	Change in	RUR	Change of LOF (Loss of Frame) Defect Condition Interrupt Status:
	LOF Defect Condition Interrupt		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" Interrupt has occurred since the last read of this register.
	Status	-	If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			• Whenever the Primary Frame Synchronizer block declares the LOF Defect Condition.
			• Whenever the Primary Frame Synchronizer block clears the LOF Defect Condition.
			0 - Indicates that the "Change in LOF Defect Condition" Interrupt has NOT



			occurred since the last read of this register.
			1 – Indicates that the "Change in LOF Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can obtain the current state of the LOF defect condition within the DS3/E3 Framer block by reading out the state of Bit 6 (LOF Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).
1	Change in	RUR	Change of LOS (Loss of Signal) Defect Condition Interrupt Status:
	LOS Defect Condition Interrupt		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register.
	Status		If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Primary Frame Synchronizer block declares the LOS Defect Condition.
			<ul> <li>Whenever the Primary Frame Synchronizer block clears the LOS Condition.</li> </ul>
			0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register.
		1 – Indicates that the Change of LOS Defect Condition" Interrupt has occurred since the last read of this register.	
			<b>Note:</b> The user can obtain the current state of the LOS Defect Condition within the DS3/E3 Framer block by reading out the state of Bit 4 (LOS Defect Declared) within the "RxE3 Configuration and Status # $2 - 6.751$ " (Address Location= 0xN311).
0	Change in	RUR	Change of AIS Defect Condition Interrupt Status:
	AIS Defect Condition Interrupt		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Defect Condition" Interrupt has occurred since the last read of this register.
	Status		If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
		, jč	Whenever the Primary Frame Synchronizer block declares the AIS Defect Condition
		none	Whenever the Primary Frame Synchronizer block clears the AIS Defect Condition.
	-The	the stand	Indicates that the "Change of AIS Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AIS Defect Condition" Interrupt has occurred since the last read of this register.
			<b>Note:</b> The user can obtain the current state of the AIS defect condition within the DS3/E3 Framer block by reading out the state of Bit 3 (AIS Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).



Table 312: RxE3 Interrupt Status Register # 2 - G.751 (Address Location= 0xN315, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Change of FERF/RDI Defect Condition Interrupt Status	Detection of BIP-4 Error Interrupt Status	Detection of FAS Bit Error Interrupt Status	Reserved
R/O	R/O	R/O	R/O	RUR	RUR	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7 – 4	Unused	R/O	att ure
3	Change of FERF/RDI Defect Condition Interrupt Status	RUR	<ul> <li>Change of FERF/RDI Defect Condition Interrupt – Primary Frame Synchronizer block:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Change in FERF/RDI Condition" interrupt has occurred since the last read of this register.</li> <li>The Primary Frame Synchronizer block will generate this interrupt in response to either of the following events.</li> <li>Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition.</li> <li>Whenever the Primary Frame Synchronizer block clears the FERF/RDI Defect condition.</li> <li>O – Indicates that the "Change in FERF/RDI Defect Condition" interrupt has NOT occurred since the last read of this register.</li> </ul>
			1 – Indicates that the "Change in FERF/RDI Defect Condition" interrupt has occurred since the last read of this register.
2	Detection of BIP-4 Error Interrupt Status	RUR	Detection of BIP-4 Error Interrupt – Primary Frame Synchronizer block: This "RESET-upon-READ" bit-field indicates whether or not the "Detection of BIP-4 Error" interrupt has occurred since the last read of this register. The Primary Frame Synchronizer block will generate this interrupt anytime it detects BIP-4 errors within the incoming E3 data-stream.
		31	0 – Indicates that the "Detection of BIP-4 Error" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of BIP-4 Error" Interrupt has occurred since the last read of this register.
1	Detection of FAS Bit Error Interrupt Status	RUR	Detection of FAS Bit Error Interrupt – Primary Frame Synchronizer block: This "RESET-upon-READ" bit-field indicates whether or not the "Detection of FAS Bit Error" interrupt has occurred since the last read of this register.
			The Primary Frame Synchronizer block will generate this interrupt anytime it detects FAS bit errors within the incoming E3 data-stream.
			0 – Indicates that the "Detection of FAS Bit Error" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Detection of FAS Bit Error" Interrupt has occurred



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			since the last read of this register.
0	Unused	R/O	

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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 313: RxE3 LAPD Control Register – G.751 (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any	Message Check Disable	Unused			Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/W	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	RxLAPD Any	R/W	Receive LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes.
			0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			1 - Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
			The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message, by reading the contents of the "Receive LAPD Byte Count" Register (Address Location= 0xN384).
6	Message Check Disable	R/W	Message Check Disable: This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt.
		0	0 - Enables the new message comparison logic
	l i i i i i i i i i i i i i i i i i i i	10 70	1 Disables the new message comparison logic
5 – 3	Unused	R/O	0
2	Receive	R/W	Receive LAPD Controller Sub-Block Enable:
	LAPD Enable		This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller sub-block within the channel. If the user enables the Receive LAPD Controller sub-block, then it will immediately begin extracting out and monitoring the data (being carried via the "N" bits) within the incoming E3 data stream.
			0 – Enables the Receive LAPD Controller sub-block.
			1 – Disables the Receive LAPD Controller sub-block.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
1	Receive	R/W	Receive LAPD Message Interrupt Enable:
	LAPD Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the



	Enable		"Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller sub- block receives a new PMDL Message.
			0 – Disables the "Receive LAPD Message" Interrupt.
			1 – Enables the "Receive LAPD Message" Interrupt.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
0	Receive	RUR	Receive LAPD Message Interrupt Status:
	LAPD Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register.
			0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register.
			1 – "Receive LAPD Message" Interrupthas occurred since the last read of this register.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.
			C N

passed.

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



# Table 314: RxE3 LAPD Status Register – G.751 (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR	RxFCS	End of	Flag
				Туре	Error	Message	Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре			DESCRIPTION
7	Unused	R/O			
6	RxABORT	R/O	Receive A	BORT Seq	uence Indicator:
			Controller :	sub-block h	-field indicates whether or not the Receive LAPD has received an ABORT sequence (e.g., a string of s"), as described below.
			0 – Indica received a	tes that th n ABORT s	e Receive LAPD Controller sub-block has NOT
			1 – Indicat an ABORT		Receive LAPD Controller sub-block has received
			ŀ	ABORT se	eceive LAPD Controlller sub-block receives an quence, it will set this bit-field "high", until it other LAPD Messages.
5 – 4	RxLAPDType[1:0]	R/O	Receive	APD Mess	age Type Indicator:
		(	residing w between t	ithin the R	LY bits indicate the type of LAPD Message that is eceive LAPD Message buffer. The relationship of these two bit-fields and the corresponding ented below.
		- X	10 O		
		200	RxLAPD	Type[1:0]	Message Type
			<b>0</b>	0	CL Path Identification
	e V	5	0	1	Idle Signal Identification
	Thepr		1	0	Test Signal Identification
		2	1	1	ITU-T Path Identification
3	RxCR Type	R/O	Received	C/R Value:	
					field indicates the value of the C/R bit (within one of the most recently received LAPD Message.
2	RxFCS Error	R/O	Receive F	rame Chec	k Sequence (FCS) Error Indicator:
					-field indicates whether or not the most recently age frame contained an FCS error.
			0 – Indica does not co		e most recently received LAPD Message frame CS error.
			1 – Indica does conta		e most recently received LAPD Message frame error.
1	End of Message	R/O	End of Me	ssage Indi	cator

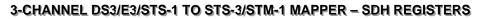


			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message, as described below.
			0 – Indicates that the Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message.
			1 – Indicates that the Receive LAPD Controller sub-block has received a completed LAPD Message.
			<b>Note:</b> Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.
0	Flag Present	R/O	Receive Flag Sequence Indicator:
			<ul> <li>This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel) as described below.</li> <li>0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet.</li> <li>1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.</li> </ul>

	.751 (Address Location= 0xN31A, where N ranges from 0x02
Table 315: RxE3 Service Bits Register – G.	.751 (Address Location= 0xN31A, where N ranges from 0x02
to 0x04)	*S 0 8

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0
		RxA	RxN				
R/O							
0	0	0		0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/0	
1	RxA	R CON	Received A Bit Value: This READ-ONLY bit-field reflects the value of the "A" bit, within the most recently received E3 frame. NOTE: This register bit pertains to the "A" bit that has been received by the Primary Frame Synchronizer block.
0	RxN	R/O	Received N Bit Value: This READ-ONLY bit-field reflects the value of the "N" bit, within the most recently received E3 frames. NOTE: This register bit pertains to the "N" bit that has been received by the Primary Frame Synchronizer block.





### 1.10.5 RECEIVE E3, ITU-T G.832 RELATED REGISTERS

# Table 316: RxE3 Configuration and Status Register # 1 - G.832 (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxPLDType[2:0]			RxFERF Algo.	RxTMark Algo	RxPLDTypeExp[2:0]		
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	1	0

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 5	RxPLDType[2:0]	R/O	Received PLD (Payload) Type[2:0
			These three READ-ONLY bit-fields reflect the value of the Payload Type bits, within the MA byte of the most recently received E3 frame.
4	RxFERF Algo	R/W	Receive FERF/RDI Defect Declaration/Clearance Algorithm:
			This READ/WRITE bit field permits the user to select a "FERF/RDI Defect Declaration and Clearance" Algorithm, as indicated below.
			0 – Configures the Primary Frame Synchronizer block to declare the FERF/RDI defect condition anytime that it receives the FERF/RDI indicator in 3 consecutive E3 frames. Additionally, this same setting will also configure the Primary Frame Synchronizer block to clear the FERF/RDI defect condition if it no longer receives the FERF/RDI indicator (within the E3 data-stream) for 3 consecutive E3 frames.
		مالات	1 – Configures the Primary Frame Synchronizer block to declare the FERF/RDI defect condition anytime it receives the FERF/RDI indicator (within the incoming E3 data-stream) in 5 consecutive E3 frames. Additionally, this same seting will also configure the Primary Frame Synchronizer block to clear the FERF/RDI defect condition anytime it ceases to receive the FERF/RDI indicator for 5 consecutive E3 frames.
3	RxTMark Algo	R/W	Receive Timing Marker Validation Algorithm:
		SU	This READ/WRITE bit-field permits the user to select the "Receive Timing Marker Validation" algorithm, as indicated below.
	11.8		0 – The Timing Marker will be validated if it is of the same state for three (3) consecutive E3 frames.
		<u> </u>	1 – The Timing Marker will be validated if it is of the same state for five (5) consecutive E3 frames.
2 - 0	RxPLDTypExp[2:0]	R/W	Receive PLD (Payload) Type – Expected:
			This READ/WRITE bit-field permits the user to specify the "expected value" for the Payload Type, within the MA bytes of each incoming E3 frame. If the Primary Frame Synchronizer block receives a Payload Type that differs then what has been written into these register bits, then it will generate the "Payload Type Mismatch" Interrupt.



# Table 317: RxE3 Configuration and Status Register # 2 - G.832 (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLOF Algo	LOF Defect Condition Declared - Primary Frame Synchronizer Block	OOF Defect Condition Declared – Primary Frame Synchronizer Block	LOS Defect Condition Declared – Primary Frame Synchronizer Block	AIS Defect Condition Declared – Primary Frame Synchronizer Block	RxPLD Unstab	RxTMark	FERF/RDI Defect Condition Declared – Primary Frame Synchronizer Block
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	1	1	1



BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	RxLOF Algo	R/W	Receive LOF (Loss of Frame) Defect Declaration Algorithm:
			This READ/WRITE bit-field permits the user to select a "Receive LOF Defect Declaration" Algorithm, as indicated below.
			0 – Configures the Primary Frame Synchronizer block to declare the LOF defect condition after it has resided within the "OOF" (Out of Frame) condition for 24 E3 frame periods.
			1 – Configures the Primary Frame Synchronizer block to declare the LOF defect condition after it has resided within the "OOF" condition for 8 E3 frame periods.
6	LOF Defect Condition	R/O	LOF (Loss of Frame) Defect Condition Indicator – Primary Frame Synchronizer Block:
	Declared	فر	This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOF defect condition, as indicated below
		produc	0 Ondicates that the Primary Frame Synchronizer block is NOT currently declaring the LOF defect condition.
	C		1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOF defect condition.
5	OOF Defect Condition	R/O	OOF (Out of Frame) Defect Condition Indicator – Primary Frame Synchronizer Block:
	Declared	31	This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer is currently declaring an Out of Frame (OOF) defect condition, as indicated below.
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition.
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition.
			<b>Note:</b> The Primary Frame Synchronizer block will declare the "OOF" defect condition anytime it detects FA1 or FA2 byte errors within four (4) consecutive "incoming" E3 frames.
4	LOS Detect Condition	R/O	LOS (Loss of Signal) Defect Condition Indicator – Primary Frame Synchronizer Block:
	Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOS (Loss of Signal) defect

			condition, as indicated below.
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOS defect condition.
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOS defect condition.
3	AIS Defect	R/O	AIS Defect Condition Indicator – Primary Frame Synchronizer Block:
	Condition Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data stream; as indicated below.
			0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the AIS defect condition within the incoming E3 data stream.
			1 – Indicates that the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data stream.
			<b>Note:</b> The Primary Frame Synchronizer block will declare an "AIS" condition if it detects 7 or less "0s" within two consecutive "incoming" E3 frames.
2		R/O	Receive Payload-Type Unstable Indicator:
	Unstab		This READ-ONLY bit-field indicates whether or not the Payload Type (within the MA bytes of each incoming E3 frame) has been consistent in the last 5 frames, as indicated below
			0 – The Payload Type value has been consistent for at least 5 consecutive E3 frames.
			1 – The Payload Type value has NOT been consistence for the last 5 E3 frames.
1	RxTMark	R/O	Received (Validated) Timing Marker:
			This READ-ONLY bit field indicates the value of the most recently validated "Timing Marker".
0	FERF/RDI Defect	R/O	FERF/RDI/(Far-End-Receive Failure) Defect Condition Indicator – Primary Frame Synchronizer block:
	Condition Declared		This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition, as indicated below.
			0ndicates that the Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition.
			P- Indicates that the Primary Frame Synchronizer block is currently declaring the FERF/RDI condition.





# Table 318: RxE3 Interrupt Enable Register # 1 - G.832 (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in SSM MSG Interrupt Enable	Change in SSM OOS Interrupt Enable	COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	this rec
6	Change in SSM MSG Interrupt Enable	R/W	<ul> <li>Change of Synchronization Status Message (SSM) Condition Interrupt Enable:</li> <li>This READ/WRITE bit field permits the user to either enable or disable the "Change in SSM Message" Interrupt, as indicated below.</li> <li>0 – Disables the "Change in SSM Message" Interrupt.</li> <li>1 – Enables the "Change of SSM Message" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a new (or different) SSM Message in the incoming E3 data-stream.</li> </ul>
5	Change in SSM OOS State Interrupt Enable	R/WO	<ul> <li>Change of SSM OOS (Out of Sequence) Condition Interrupt Enable</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change of SSM OOS Condition" Interrupt, as indicated below.</li> <li>0 – Disables the "Change of SSM OOS Condition" Interrupt.</li> <li>1 – Enables the "Change of SSM OOS Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions.</li> <li>Whenever the Primary Frame Synchronizer block declares the SSM OOS condition.</li> <li>When the Primary Frame Synchronizer block clears the SSM OOS condition.</li> </ul>
4	COFA Interrupt Enable	R/W	<ul> <li>Change of Framing Alignment Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" condition interrupt, as indicated below.</li> <li>0 – Disables the "Change of Framing Alignment" Interrupt.</li> <li>1 – Enables the "Change of Framing Alignment" Interrupt.</li> </ul>
3	Change in OOF Defect Condition Interrupt Enable	R/W	Change of OOF (Out of Frame) Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of OOF Defect Condition" Interrupt, as indicated below.



		0 – Disables the "Change of OOF Defect Condition" Interrupt.
		1 – Enables the "Change of OOF Defect Condition" Interrupt. In this configuration setting, the Primary Frame Synchronizer block will generate an interrupt under the following conditions.
		Whenever the Primary Frame Synchronizer block declares the OOF defect condition.
		• Whenever the Primary Frame Synchronizer block clears the OOF defect condition.
2	Change in LOF Defect R. Condition Interrupt Enable	V Change of LOF (Loss of Frame) Defect Condition Interrupt Enable:
		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" Interrupt, as indicated below.
		0 – Disables the "Change of LOF Defect Condition" Interrupt.
		1 – Enables the "Change of LOF Defect Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions.
		Whenever the Primary Frame Synchronizer block declares the LOF defect condition.
		Whenever the Primary Frame Synchronizer block clears the LOF defect condition.
1	Change in LOS Defect R. Condition Interrupt Enable	V Change of LOS (Loss of Signal) Defect Condition Interrupt Enable
		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOS Defect Condition" Interrupt, as indicated below.
		0 – Disables the "Change of LOS Defect Condition" Interrupt.
	Ct.	this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions.
		Whenever the Primary Frame Synchronizer block declares the LOS defect condition.
	Nº 3 A	Whenever the Primary Frame Synchronizer block clears the LOS defect condition.
0	Change of AIS Defect Condition Interrupt Enable	V Change of AIS (Alarm Indication Signal) Defect Condition Interrupt Enable:
	<b>*</b>	This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Defect Condition" Interrupt, as indicated below.
		0 – Disables the "Change of AIS Defect Condition" Interrupt.
		1 – Enables the "Change of AIS Defect Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions.
		Whenever the Primary Frame Synchronizer block declares the AIS defect condition.
		Whenever the Primary Frame Synchronizer block clears the AIS defect condition.



# Table 319: RxE3 Interrupt Enable Register # 2 - G.832 (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in Receive Trail- Trace Message Interrupt Enable	Reserved	Detection of FEBE Event Interrupt Enable	Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-8 Error Interrupt Enable	Detection of Framing Byte Error Interrupt Enable	RxPLD Mismatch Interrupt Enable
R/O	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

			is do
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	ATT OF
6	Change in Receive Trail-Trace Message Interrupt Enable	R/W	<ul> <li>Change in Receive Trail-Trace Message Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Change in Receive Trail-Trace Message" Interrupt, as indicated below.</li> <li>0 – Disables the "Change in Receive Trail-Trace Message" Interrupt.</li> <li>1 – Enables the "Change in Receive Trail-Trace Message" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a different Trail-Trace message, then what it had been receiving.</li> </ul>
5	Unused	R/W	or lo er
4	Detection of FEBE Event Interrupt Enable	RANGE	<ul> <li>Detection of FEBE Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Detection of FEBE" Interrupt, as indicated below.</li> <li>O – Disables the "Detection of FEBE" Interrupt.</li> <li>1 – Enables the "Detection of FEBE" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a FEBE (Far-End Block Error) indicator in the incoming E3 data-stream.</li> </ul>
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	<ul> <li>Change in FERF Defect Condition Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the Change in FERF/RDI Defect Condition Interrupt, as indicated below.</li> <li>0 – Disables the "Change in FERF/RDI Defect Condition" Interrupt.</li> <li>1 – Enables the "Change in FERF/RDI Defect Condition" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt, in response to either of the following conditions.</li> <li>Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition.</li> <li>Whenever the Primary Frame Synchronizer block clears the FERF/RDI defect condition.</li> </ul>
2	Detection of BIP-8 Error Interrupt Enable	R/W	Detection of BIP-8 Error Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of BIP-8 Error" Interrupt, as indicated below.

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			0 – Disables the "Detection of BIP-8 Error" Interrupt.
			1 – Enables the "Detection of BIP-8 Error" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a BIP-8 error in the incoming E3 data-stream.
1	Detection of Framing	R/W	Detection of Framing Byte Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Framing Byte Error" Interrupt, as indicated below.
			0 – Disables the "Detection of Framing Byte Error" Interrupt.
			1 – Enables the "Detection of Framing Byte Error" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a FA1 or FA2 byte error in the incoming E3 data stream.
0	RxPLD Mis Interrupt		Received Payload Type Mismatch Interrupt Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Payload Type Mismatch" interrupt, as indicated below.
			0 – Disables the "Received Payload Type Mismatch" Interrupt.
			1 – Enables the "Received Payload Type Mismatch" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a "Payload Type" value (within the MA byte) that differs from that written into the "RxPLDExp[2:0]" bit-fields.

innary Frame Sy anytime it receives a "Payloa differs from that written into the



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# Table 320: RxE3 Interrupt Status Register # 1 - G.832 (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in SSM MSG Interrupt Status	Change in SSM OOS Interrupt Status	COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Status	RUR	<ul> <li>Change in SSM (Synchronization Status Message) Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Change in SSM Message" Interrupt has occurred since the last read of this register.</li> <li>If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt, anytime it detects a change in the "SSMI3:0" value that it has received via the incoming E3 data-stream</li> <li>0 – Indicates that the "Change in SSM Message" Interrupt has NOT occurred since the last read of this register.</li> <li>1 – Indicates that the "Change in SSM Message" Interrupt has occurred since the last read of this register.</li> <li>Note: The user can obtain the newly received value for "SSM" by reading out the contents of Bits 3 through 1 (RxSSM[3:0]) within the "RxE3 SSM Register – G.832" (Address Location= 0xN32C).</li> </ul>
5	Change in SSM OOS State Interrupt Status	RUR	<ul> <li>Change in SSM OOS (Out of Sequence) State Interrupt Status:</li> <li>This RESET-upon-READ bit-field indicates whether or not the "Change in SSM OOS State" Interrupt has occurred since the last read of this register.</li> <li>If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in SSM OOS State" Interrupt will response to the following events.</li> <li>Whenever the Primary Frame Synchronizer block declares the SSM OOS Condition.</li> <li>Whenever the Primary Frame Synchronizer block clears the SSM OOS condition.</li> <li>O – Indicates that the "Change in SSM OOS Condition" Interrupt has NOT occurred since the last read of this register.</li> <li>1 – Indicates that the "Change in SSM OOS Condition" Interrupt has occurred since the last read of this register.</li> </ul>
4	COFA Interrupt Status	RUR	COFA Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "COFA" (Change of Framing Alignment) Interrupt has occurred



			since the last read of this register.
			If this interrupt is enabled, then the Primary Frame Synchronizer
			block will generate an interrupt anytime it detects a new "Framing Alignment" with the incoming E3 data-stream.
			0 – Indicates that the "COFA Interrupt" has not occurred since the last of this register.
			1 – Indicates that the "COFA Interrupt" has occurred since the last read of this register.
3	Change in OOF Defect Condition Interrupt Status	RUR	Change in OOF (Out of Frame) Defect Condition Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in OOF Defect Condition" Interrupt in response to the following events.
			• Whenever the Primary Frame Synchronizer block declares the "OOF Condition".
			• Whenever, the Primary Frame Synchronizer block clears the "OOF Condition".
			0 – Indicates that the "Change in OOF Defect Condition Interrupt has not occurred since the last of this register.
			1 - Indicates that the "Change in OOF Defect Condition Interrupt" has occurred since the last read of this register.
		orpro	Note: The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 5 (OOF Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
2	Change in LOF Defect Condition Interrupt Status	RUR	Change in LOF (Loss of Frame) Defect Condition Interrupt Status:
	produce	y not	This RESET-upon-READ bit-field indicates whether or not the "Change in LOF Defect Condition Interrupt has occurred since the last read of this register.
	the stand m	<b>,</b>	If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in LOF Defect Condition" Interrupt will occur in response to the following events.
	<u></u> ক		• Whenever the Primary Frame Synchronizer block declares the "LOF Defect Condition".
			• When the Primary Frame Synchronizer block clears the "LOF Defect Condition".
			0 – Indicates that the "Change in LOF Defect Condition Interrupt" has not occurred since the last of this register.
			1 – Indicates that the "Change in LOF Defect Condition Interrupt" has occurred since the last read of this register.
			<b>Note:</b> The user can determine the current state of the "LOF Condition" by reading out the contents of Bit 6 (LOF Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
1	Change in LOS Defect	RUR	Change in LOS (Loss of Signal) Defect Condition Interrupt
			-



	Condition Interrupt Status		Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in LOS Defect Condition" Interrupt will occur in response to the following events.
			• Whenever the Primary Frame Synchronizer block declares the "LOS Defect Condition".
			• When the Primary Frame Synchronizer block clears the "LOS Defect Condition".
			0 – Indicates that the "Change in LOS Defect Condition Interrupt" has not occurred since the last of this register.
			1 – Indicates that the "Change in LOS Defect Condition Interrupt" has occurred since the last read of this register.
			<b>Note:</b> The user can determine the current state of the "LOS Condition" by reading out the contents of Bit 4 (LOS Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
0	Change in AIS Defect	RUR	Change in AIS Defect Condition Interrupt Status:
	Condiiton Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register.
		.0011	If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in AIS Defect Condition" Interrupt will occur in response to the following events.
	the product or area		• Whenever the Primary Frame Synchronizer block declares the "AIS Condition".
	it at	y ve	<ul> <li>Whenever the Primary Frame Synchronizer block clears the "AIS Condition".</li> </ul>
	olleet	0	0 – Indicates that the "Change in AIS Defect Condition Interrupt" has not occurred since the last of this register.
	ne P'strat		1 – Indicates that the "Change in AIS Defect Condition Interrupt" has occurred since the last read of this register.
	The prosher in average and may not and may not a stand may not		<b>Note:</b> The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 3 (AIS Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).

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# Table 321: RxE3 Interrupt Status Register # 2 - G.832 (Address Location= 0xN315, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in Receive Trail-Trace Message Interrupt Status	Reserved	Detection of FEBE/REI Event Interrupt Status	Change in FERF/RDI Defect Condition Interrupt Status	Detection of BIP-8 Error Interrupt Status	Detection of Framing Byte Error Interrupt Status	RxPLD Mismatch Interrupt Status
R/O	RUR	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	the ure
6	Change in Receive	RUR	Change in Receive Trail-Trace Message Interrupt Status:
	Trail-Trace Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Receive Trail-Trace Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime it receives a Trail-Trace Message, that is different from that of the previously received message.
			0 – Indicates that the Change in Receive Trail-Trace Message" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in Receive Trail-Trace Message" Interrupt has occurred since the last read of this register.
		uct.	Note: The user can obtain the value of the most recently received Trail-Trace Message by reading out the contents of the "RxE3 Trail-Trace Message Byte-0" through "RxE3 Trail-Trace Message Byte-15" registers (Address Location= 0xN31C through 0xN32B).
5	Unused	R/O	
4	Detection of	RUR	Detection of FEBE/REI Event Interrupt Status:
	FEBE/REI Event Interrupt Status	atand m.	This RESET-upon-READ bit-field indicates whether or not the "Detection of FEBE/REI Event" Interrupt has occurred since the last read of this register.
		<b>%</b>	If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime is detects a FEBE/REI event in the incoming E3 data-stream.
			0 – Indicates that the "Detection of FEBE/REI Event" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of FEBE/REI Event" Interrupt has occurred since the last read of this register.
3	FERF/RDI Defect		Change in FERF/RDI (Far-End Receive Failure) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Primary Frame Synchronizer block



		will generate an interrupt in response to the following events.
		• Whenever the Primary Frame Synchronizer block declares the FERF/RDI defect condition.
		• Whenever the Primary Frame Synchronizer block clears the FERF/RDI condition.
		0 – Indicates that the "Change in FERF/RDI Defect Condition" Interrupt has NOT occurred since the last read of this register.
		1 – Indicates that the "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of the register.
		<b>Note:</b> The user can obtain the state of the FERF/RDI defect condition, by reading out the contents of Bit 0 (FERF/RDI Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
2	Detection of BIP-8 RUR	Detection of BIP-8 Error Interrupt Status:
	Error Interrupt Status	This RESET-upon-READ bit-field indicates whether or not the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register.
		If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime is detects a BIP-8 Error in the incoming E3 data-stream.
		0 – Indicates that the "Detection of BIP-8 Error" Interrupt has NOT occurred since the last read of this register.
		1 – Indicates that the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register.
1	Detection of RUR Framing Byte Error	Detection of Framing Byte Error Interrupt Status:
	Interrupt Status	This RESET-upon-READ bit-field indicates whether or not the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block
	NG.	will generate an interrupt anytime is detects an error in either the FA1 or FA2 byte, within the incoming E3 data-stream.
	orotheet	O – Indicates that the "Detection of Framing Byte Error" Interrupt has NOT occurred since the last read of this register.
	the ta ma	1 – Indicates that the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register.
0	Detection of RLD Type Mismatch Interrupt Status	<b>Detection of Payload Type Mismatch Interrupt Status:</b> This RESET-upon-READ bit-field indicates whether or not the "Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register.
		If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime it receives an E3 data-stream that contains a "RxPLDType[2:0]" that is different from the "RxPLDTypeExp[2:0]" value.
		0 – Indicates that the "Detection of Payload Type Mismatch" Interrupt has NOT occurred since the last read of this register.
		1 – Indicates that the "Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register.
		<b>Note:</b> The user can obtain the contents of the most recently received Payload Type by reading out the contents of Bits 7 through 5 (RxPLDType[2:0]) within the "RxE3 Configuration and Status



	Register # 1 – G.832" (Address Location= 0xN310).

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# Table 322: RxE3 LAPD Control Register – G.832 (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any	Message Check Disable	Unı	ised	Receive LAPD from NR Byte	Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/W	R/O	R/O	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	RxLAPD Any	R/W	Receive LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block) to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes.
			0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			1-Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values.
			Note: This bit-field is ignored if the Primary Frame Synchronizer block is by- passed
		,Č	The user can determine the size (or byte count) fo the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384).
6	Message	R/W	Message Check Disable:
	Check Disable	or she	This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt.
		3° 25	0 – Enables the new message comparison logic
			1 – Disables the new message comparison logic
6 – 4	Unused	R/O	
3	Receive	R/W	Receive LAPD Message from NR Byte Select:
	LAPD from NR Byte		This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block to extract out the PMDL data from the NR or GC byte, within the incoming E3 data stream.
			0 – Configures the Receive LAPD Controlller sub-block to extract PMDL information from the GC byte, within the incoming E3 data stream.
			1 – Configures the Receive LAPD Controller sub-block to extract PMDL information from the NR byte, within the incoming E3 data stream.
			<b>Note:</b> This bit-field is ignored if the Primary Frame Synchronizer block is by- passed.



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sub-block, then it will that is being carried figuration) within the
chronizer block is by-
nable or disable the his interrupt, then the Frame Synchronizer APD Controller sub-
ontroller sub-block is
t the "Receive LAPD register.
t has NOT occurred
t has occurred since
ontroller sub-block is
nab his in Fran API ontro

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# Table 323: RxE3 LAPD Status Register – G.832 (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPD ⁻	Туре[1:0]	RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре			DESCRIPTION		
7	Unused	R/O					
6	RxABORT	R/O	Receive A	BORT Sec	uence Indicator		
			received	LAPD/PMD	-field indicates whether or not the most rece DL Message was interrupted by an ABC ng of seven consecutive "1s") as described bel	ORT	
			0 – Indicates that the Receive LAPD Controller sub-block has NOT received an ABORT sequence within the most recently LAPD/PMDL Message.				
			1 - Indicates that the Receive LAPD Controller sub-block has received an ABORT sequence within the most recently received LAPD/PMDL Message.				
			C ²	ABORT se	eceive LAPD Controller sub-block receives quence, it will set this bit-field "high", un other LAPD Message.		
5 – 4	RxLAPDType[1:0]	R/O	Receive L	APD Mess	age Type Indicator[1:0]:		
	The produces	ct ar	These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.				
	NO.	е° (	RxLAPD	Type[1:0]	Message Type		
		AS!	0	0	CL Path Identification		
	11. 932. 9		0	1	Idle Signal Identification		
	311		1	0	Test Signal Identification		
			1	1	ITU-T Path Identification		
3	RxCR Type	R/O	Received	C/R Value:			
					field indicates the value of the C/R bit (within f the most recently received LAPD Message.	one	
2	RxFCS Error	R/O	Receive Frame Check Sequence (FCS) Error Indicator:				
			This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error as described below.				
				ates that th ontain an F	e most recently received LAPD Message fr	ame	
			1 – Indica	ates that th	e most recently received LAPD Message fr	ame	

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			does contain an FCS error.
1	End of Message	R/O	End of Message Indicator
			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message as described below.
			0 – Indicates that the Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message.
			1 – Indicates that the Receive LAPD Controller sub-block has received a completed LAPD Message.
			<b>Note:</b> Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.
0	Flag Present	R/O	Receive Flag Sequence Indicator
			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel).
			0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet.
			1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.

1 - Indicates that the Reference in receiving the Flag Sequence



# Table 324: RxE3 NR Byte Register – G.832 (Address Location= 0xN31A, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxNR_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxNR_Byte[7:0]	R/O	Receive NR Byte Value:
			These READ-ONLY bit-fields contain the value of the NR byte, within the most recently received E3 frame.
			the re-

# Table 325: RxE3 GC Byte Register – G.832 (Address Location 0xN31B, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Ви 3	Віт 2	Віт 1	Віт 0
			RxGC_E	Byte[7:0]			
R/O	R/O	R/O	R/O	Ø R/Q	R/O	R/O	R/O
0	0	0	0	0	0	0	0
			45	\$ \$			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxGC_Byte[7:0]	R/O	Receive GC Byte Value: These READ-ONLY bit-fields contain the value of the GC byte, within the most recently received E3 frame.

# Table 326: RxE3 Trail-Trace 0 Register G.832 (Address Location= 0xN31C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Bin 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	RxTTB_0[7:0]						
R/O	R/O	RO	R/O	R/O	R/O	R/O	R/O
0	0	00	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_0[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 0:
			These READ-ONLY bit-fields contain the contents of Byte 0 (e.g., the "Marker" Byte), within the most recently received Trail-Trace Buffer" Message.

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Table 327: RxE3 Trail-Trace-1 Register – G.832 (Address Location= 0xN31D, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	RxTTB_1[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_1[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 1:
			These READ-ONLY bit-fields contain the contents of Byte 1, within the most recently received Trail-Trace Buffer" Message.

# Table 328: RxE3 Trail-Trace-2 Register – G.832 (Address Location= 0xN31E, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			RxTTB	2[7:0]	<u>,</u> ,		
R/O	R/O	R/O	R/O	B/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0
	5 5 5						

BIT NUMBER	Nаме	Түре	
7 - 0	RxTTB_2[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 2: These READ-ONLY bit-fields contain the contents of Byte 2, within the most recently received Trail-Trace Buffer" Message.

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# Table 329: RxE3 Trail-Trace-3 Register - 6.832 (Address Location= 0xN31F, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Вл 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		N 20 1	RxTTB	3[7:0]			
R/O	R/O	RIŎ	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_3[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 3:
			These READ-ONLY bit-fields contain the contents of Byte 3, within the most recently received Trail-Trace Buffer" Message.



# Table 330: RxE3 Trail-Trace-4 Register – G.832 (Address Location= 0xN320, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxTTB_4[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_4[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 4:
			These READ-ONLY bit-fields contain the contents of Byte 4, within the most recently received Trail-Trace Buffer" Message.

# Table 331: RxE3 Trail-Trace-5 Register – G.832 (Address Location=0xN321, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	ВпЗ	Віт 2	Віт 1	Віт 0
			RxTTB	_5[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0 📢	0	0	0	0
			5	ve. 8			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_5[7:0]	R/O	Receive Trail Trace Buffer Message – Byte 5: These READ-ONLY bit-fields contain the contents of Byte 5, within the most recently received Trail-Trace Buffer" Message.

# Table 332: RxE3 Trail-Trace-6 Register – G.832 (Address Location= 0xN322, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	BIT 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_6[7:0]							
R/O	R/O	R/Q	R/O	R/O	R/O	R/O	R/O
0	0		0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_6[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 6:
			These READ-ONLY bit-fields contain the contents of Byte 6, within the most recently received Trail-Trace Buffer" Message.

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# Table 333: RxE3 Trail-Trace-7 Register – G.832 (Address Location= 0xN323, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_7[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_7[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 7:
			These READ-ONLY bit-fields contain the contents of Byte 7, within the most recently received Trail-Trace Buffer" Message.

# Table 334: RxE3 Trail-Trace-8 Register – G.832 (Address Location 0xN324, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	RxTTB_8[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		
	*5 0° 0°								

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 0	RxTTB_8[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 8: These READ-ONLY bit-fields contain the contents of Byte 8, within the most recently received Trail-Trace Buffer" Message.

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# Table 335: RxE3 Trail-Trace-9 Register – G.832 (Address Location= 0xN325, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Вл 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxTTB_9[7:0]							
R/O	R/O	RIÖ	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_9[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 9:
			These READ-ONLY bit-fields contain the contents of Byte 9, within the most recently received Trail-Trace Buffer" Message.



# Table 336: RxE3 Trail-Trace-10 Register – G.832 (Address Location= 0xN326, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_10[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_10[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 10:
			These READ-ONLY bit-fields contain the contents of Byte 10, within the most recently received Trail-Trace Buffer" Message.

# Table 337: RxE3 Trail-Trace-11 Register – G.832 (Address Location = 0xN327, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Вл 3	Віт 2	Віт 1	Віт 0	
RxTTB_11[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0 📢	0	0	0	0	
			5	ve. 8				

BIT NUMBER NAME TYPE	
7 - 0 RxTTB_11[7:0] R/O	Receive Trail-Trace Buffer Message – Byte 11: These READ-ONLY bit-fields contain the contents of Byte 11, within the most recently received Trail-Trace Buffer" Message.

# Table 338: RxE3 Trail-Trace-12 Register – G.832 (Address Location= 0xN328, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_12[7:0]							
R/O	R/O 🔨	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_12[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 12:
			These READ-ONLY bit-fields contain the contents of Byte 12, within the most recently received Trail-Trace Buffer" Message.

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Table 339: RxE3 Trail-Trace-13 Register – G.832 (Address Location= 0xN329, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	RxTTB_13[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_13[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 13:
			These READ-ONLY bit-fields contain the contents of Byte 13, within the most recently received Trail-Trace Buffer" Message.

# Table 340: RxE3 Trail-Trace-14 Register – G.832 (Address Location= 0xN32A, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 💉	Віт 2	Віт 1	Віт 0
			RxTTB_	_14[7:0]	<u>, , , , , , , , , , , , , , , , , , , </u>		
R/O	R/O	R/O	R/O	B/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0
	*5 0° 83						

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 0	RxTTB_14[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 14: These READ-ONLY bit-fields contain the contents of Byte 14, within the most recently received Trail-Trace Buffer" Message.

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# Table 341: RxE3 Trail-Trace-15 Register – G.832 (Address Location= 0xN32B, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Вл 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		N 20 1	RxTTB	_15[7:0]			
R/O	R/O	RIŎ	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	RxTTB_15[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 15:
			These READ-ONLY bit-fields contain the contents of Byte 15, within the most recently received Trail-Trace Buffer" Message.



# Table 342: RxE3 SSM Register – G.832 (Address Location= 0xN32C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxSSM Enable	MF[1:0]		Reserved	RxSSM[3:0]			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	RxSSM Enable	R/W	Receive SSM Enable:
			This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to operate in either the "Old ITU-T G.832 Framing" format or in the "New ITU-T G.832 Framing" format, as described below.
			0 – Configures the Primary Frame Synchronizer block to support the "Pre October 1998" version of the E3, ITU-T G.832 Framing format.
			1 – Configures the Primary Frame Synchronizer block to support the "October 1998" version of the E3, ITU-T G.832 framing format.
6 - 5	MF[1:0]	R/O	Multi-Frame Identification:
			These READ ONLY bit-fields reflect the current frame number, within the Received Multi-Frame.
			<b>Note:</b> These bit-fields are only active if the Primary Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".
4	Unused	R/O	9° ~~ 8°
3 - 0	RxSSM[3:0]	R/00	Receive Synchronization Status Message[3:0]:
	<b></b>	JC2 2	These READ-ONLY bit-fields reflect the content of the "SSM" bits, within the most recently received SSM Multiframe.
	eprof	sheet	<b>Write:</b> These bit-fields are only active if the Primary Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".
	TH Jato	iq u.	

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### 1.10.6 DS3/E3 FRAME GENERATOR BLOCK RELATED REGISTERS – DS3 APPLICATIONS

# Table 343: TxDS3 Configuration Register (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

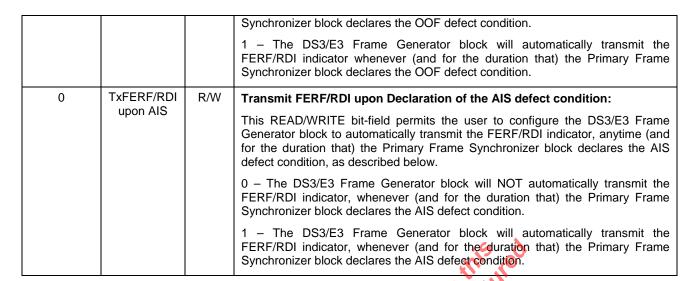
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Force TxFERF/ RDI	Tx X-Bits	Txldle	TxAIS	TxLOS	TxFERF/RDI upon LOS	TxFERF/RDI upon OOF	TxFERF/RDI upon AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	1		. <u></u>
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Force TxFERF/RDI	R/W	Force Transmit Yellow Alarm (FERF/RDI) indicator:
			This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit the FERF/RDI indicator to the remote terminal equipment by setting both of the X-bits (within each outbound DS3 frame) to "0".
			0 – Does not force the DS3/E3 Frame Generator block to transmit the FERF/RDI indicator. In this case, the DS3/E3 Frame Generator block will set the "X" bits (within each outbound DS3 frame) to the appropriate value, depending upon receive conditions (as detected by the Primary Frame Synchronizer block).
			1 – Forces the DS3/E3 Frame Generator block to transmit the FERF/RDI indicator. In this case, the DS3/E3 Frame Generator block will force the "X" bits (within each outbound DS3 frame) to "0". Thereby transmitting the FERF/RDI indicator to the remote terminal equipment.
			<b>NOTE:</b> For normal operation, (e.g., where the DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever the Primary Frame Synchronizer block declares either the LOS, AIS or LOF/OOF defect condition), the user MUST set this bit-field to "0"
6	Tx X-Bits	R/W	Force X bits to 1":
		~	This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to set the X-bits (within each outbound DS3 frame) to "1".
		ner	62- Configures the DS3/E3 Frame Generator block to automatically set the "X" bits to the appropriate value, depending upon the receive conditions (as detected by the corresponding Primary Frame Synchronizer block).
			Configures the DS3/E3 Frame Generator block to force all of the "X" bits (within the outbound DS3 data-stream) to "1". In this configuration setting, the DS3/E3 Frame Generator block will set all "X" bits to "1" independent of whether the corresponding Primary Frame Synchronizer block is currently declaring any defect conditions.
			<b>NOTE:</b> For normal operation (e.g., where the DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever the Primary Frame Synchronizer block declares the LOS, AIS or LOF/OOF defect condition) the user MUST set this bit-field to "0".
5	TxIdle	R/W	Transmit DS3 Idle Signal:
			This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the DS3 Idle signal pattern to the remote terminal equipment, as described below.
			0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment.



			1 – Configures the DS3 Frame Generator block transmits the DS3 Idle Pattern to
			the remote terminal equipment.
			<b>Note:</b> This bit-field is ignored if "TxAIS" or "TxLOS" bit-fields are set to "1".
			The exact pattern that the Frame Generator transmits (whenever this bit-field is set to "1") depends upon the contents within Bits 3 through 0 (Tx_Idle_Pattern[3:0]) within the "Transmit DS3 Pattern" Register (Address Location= 0xN34C).
4	TxAIS	R/W	Transmit AIS Pattern:
			This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the AIS indicator to the remote terminal equipment as described below.
			0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment.
			1 – Configures the DS3/E3 Frame Generator block to transmit the DS3 AIS indicator to the remote terminal equipment.
			<b>Note:</b> This bit-field is ignored if the "TXLOS" bit-field is set to "1".
			When this bit-field is set to "1" fewill transmit either a "Framed, repeating 1, 0, 1, 0," pattern, or an "Unframed, All Ones" pattern, depending upon the state of Bit 7 (TxAIS Unframed All Ones), within the "Transmit DS3 Pattern Register (Address Location= 0xN34C).
3	TxLOS	R/W	Transmit LOS Pattern:
			This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the LOS signal pattern to the remote terminal equipment as described below.
			0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment.
			1 – Configures the DS3/E3 Frame Generator block to transmit the LOS Pattern (e.g., All Zeros or an All Ones, depending upon user configuration).
			Note: This bit-field is ignored if "TxAIS" or "TxLOS" are set to "1".
		odu	When this bit-field is set to "1", it will transmit either an "All Zeros" pattern, or an "All Ones" pattern; depending upon the state of Bit 4 (TxLOS Pattern) within the "Transmit DS3 Pattern Register (Address Location=0xN34C).
2	TxFERF/RDI	R/W	Transmit FERF/RDI upon Declaration of the LOS defect condition:
	upon LOS	03t310	Generator block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the corresponding Primary Frame Synchronizer block declares the LOS defect condition.
			0 – The DS3/E3 Frame Generator block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame Synchronizer block declares the LOS defect condition.
			1 – The DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Primary Frame Synchronizer block declares LOS defect condition.
1	TxFERF/RDI	R/W	Transmit FERF/RDI upon Declaration of the OOF defect condition:
	upon OOF		This READ/WRITE bit-field permits the user to configure the DS3 Frame Generator block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the DS3/E3 Frame Synchronizer block declares the OOF defect condition, as described below.
			0 – The DS3/E3 Frame Generator block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame

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Table 344: TxDS3 FEAC Configuration and Status Register (Address Location= 0xN331, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
R/O	R/O	R/O	R/W	RUR	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" for normal operation.
4	TxFEAC Interrupt Enable	R/W	<ul> <li>Transmit FEAC Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Transmit FEAC" Interrupt. If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt, once the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message to the remote terminal equipment.</li> <li>0 – Disables the Transmit FEAC Interrupt.</li> <li>In this configuration setting, the DS3/E3 Frame Generator block will NOT generate an interrupt after the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message.</li> <li>1 – Enables the Transmit FEAC Interrupt</li> <li>In this configuration setting, the DS3/E3 Frame Generator block will generate an interrupt after the Transmit FEAC Message.</li> <li>1 – Enables the Transmit FEAC Interrupt</li> <li>In this configuration setting, the DS3/E3 Frame Generator block will generate an interrupt after the Transmit FEAC Message.</li> <li>1 – Enables the Transmit FEAC Interrupt</li> <li>In this configuration setting, the DS3/E3 Frame Generator block will generate an interrupt after the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message.</li> <li>NOTE: This bit field is only active if Bit 2 (TxFEAC Enable) within this register is</li> </ul>
3	TxFEAC Interrupt Status	RUR	<ul> <li>Transmit FEAC Interrupt Status:</li> <li>Tris RESET-upon-READ bit-field indicates whether or not the "Transmit FEAC Interrupt" has occurred since the last read of this register, as described below.</li> <li>Indicates that the Transmit FEAC Interrupt has NOT occurred since the last read of this register.</li> <li>I – Indicates that the Transmit FEAC Interrupt has occurred since the last read of this register.</li> <li>NOTE: This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".</li> </ul>
2	TxFEAC Enable	R/W	<ul> <li>Transmit FEAC Controller Sub-block Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the Transmit FEAC Controller sub-block, within the DS3/E3 Frame Generator block, as described below.</li> <li>0 – Disables the Transmit FEAC Controller sub-block.</li> <li>1 – Enables the Transmit FEAC Controller sub-block.</li> </ul>
1	TxFEAC Go	R/W	<b>Transmit FEAC Message Command:</b> A "0" to "1" transition, within this bit-field configures the Transmit FEAC Controller sub-block to begin its transmission of the FEAC Message (which consists of the FEAC code, as specified within the "TxDS3 FEAC" Register).



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			<b>Note:</b> The user is advised to perform a write operation that resets this bit-field back to "0", following execution of the command to transmit a FEAC Message.
0	TxFEAC	R/O	Transmit FEAC Controller BUSY Indicator:
	Busy	This READ-ONL	This READ-ONLY bit-field indicates whether or not the Transmit FEAC Controller sub-block is currently busy transmitting a FEAC Message to the remote terminal.
			0 – Transmit FEAC Controller sub-block is NOT busy.
			1 – Transmit FEAC Controller sub-block is currently transmitting the FEAC Message to the remote terminal.

### Table 345: TxDS3 FEAC Register (Address Location= 0xN332, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	BIT 1	Віт 0	
Unused			TxFEAC	Code[5:0]	1		Unused	
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/O	
0	1	1	1	1	10	0 1	0	
	on on on the							

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	
7	Unused	R/O	no no
6 - 1	TxFEACCode[5:0]	R/W	Transmit FEAC Code Word[5:0] These six (6) READ/WRITE bit-fields permit the user to specify the FEAC Code word that the Transmit FEAC Controller sub-block (within the DS3/E3 Frame Generator block) should transmit to the remote terminal equipment. Once the user enables the "Transmit FEAC Controller sub-block" and commands it to begin its transmission, the Transmit FEAC Controller sub- block will then (1) encapsulate this six-bit code word into a 16-bit structure, (2) proceed to transmit this 16-bit structure 10 times, repeatedly, and then halt. Note: These bit-fields are ignored if the user does not enable and use the Transmit FEAC Controller sub-block (within the DS3/E3 Frame Generator block).
0	Unused	R/O	
		2310	



Table 346: TxDS3 LAPD Configuration Register (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxLAPD Any		Unused		Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/W	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	TxLAPD Any	R/W	<ul> <li>Transmit LAPD – Any kind:</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block) to transmit any kind of LAPD Message (or HDLC Message) with a size of 82 byte or less. If the user implements this option, then the Transmit LAPD Controller sub-block will be capable of transmitting any kind of HDLC frame (with any value of header bytes). The only restriction is that the size of the HDLC frame must not exceed 82 bytes.</li> <li>0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the LAPD Transmitter will only transmit HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.</li> <li>1- Invokes this "Any Kind of HDLC Message" feature. In this case, the LAPD Transmitter will be able to transmit HDLC Messages that contain any header byte values.</li> <li>Note: If the user invokes the "Any Kind of HDLC Message" feature, then he she must indicate the size of the information payload (in terms of bytes) within the "Transmit LAPD Byte Count" Register (Address Location=0xN383).</li> </ul>
6 - 4	Unused	R/O	
3	Auto Retransmit	Prosto Prosto	<ul> <li>Auto-Retransmit of LAPD Message:</li> <li>This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message; the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals.</li> <li>0 – Disables the Auto-Retransmit Feature.</li> <li>In this case, the PMDL Message will only be transmitted once. Afterwards the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission.</li> <li>1 – Enables the Auto-Retransmit Feature.</li> <li>In this case, the Transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals.</li> </ul>

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2	Reserved	R/O	
1	TxLAPD	R/W	Transmit LAPD Message Length Select:
	Message Length		This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below.
			0 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes.
			1 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
			<b>NOTE:</b> This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.
0	Transmit	R/W	Transmit LAPD Controller sub-block Enable:
	LAPD Enable		This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller sub-block, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octer (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The Transmit LAPD Controller sub-block will continue to repeatedly transmit the Flag Sequence octet until the user commands the Transmit LAPD Controller sub-block to transmit a PMDL Message. 0 – Disables the Transmit LAPD Controller sub-block. 1 – Enables the Transmit LAPD Controller sub-block.

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## Table 347: TxDS3 LAPD Status/Interrupt Register (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		Initiate Transmission of LAPD/PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	*hister
3	Initiate Transmission of LAPD/ PMDL Message	R/W	<ul> <li>Transmit LAPD Message Command:</li> <li>A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller sub-block to begin the following activities:</li> <li>Reading out the contents of the Transmit LAPD Message Buffer.</li> <li>Zero-Stuffing of this data</li> <li>FCS Calculation and Insertion</li> <li>Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame.</li> <li>NOTE: This bit-field is only active if the Transmit LAPD Controller block has been enabled.</li> </ul>
2	Transmit LAPD Controller Busy	R/O Produ Data and	<ul> <li>Transmit LAPD Controller Busy Indicator:</li> <li>This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.</li> <li>- Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message.</li> <li>1 Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message.</li> <li>NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.</li> </ul>
1	Transmit LAPD Interrupt Enable	R/W	<ul> <li>Transmit LAPD Interrupt Enable:</li> <li>This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal.</li> <li>0 – Disables the Transmit LAPD Interrupt.</li> <li>1 – Enables the Transmit LAPD Interrupt.</li> </ul>
0	Transmit LAPD Interrupt Status	RUR	Transmit LAPD Interrupt Status:This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPDInterrupt" has occurred since the last read of this register as described below.0 – Indicates that the Transmit LAPD Interrupt has NOT occurred since the last

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

read of this register.	
1 – Indicates that the Transmit LAPD Interrupt has occurred since the last r of this register.	ead

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Table 348: TxDS3 M-Bit Mask Register (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxFEBEDat[2:0]			FEBE Register Enable	Tx P-Bit Error	TxM_Bit_Mask[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DECRIPTION
7 - 5	TxFEBEDat	R/W	Transmit FEBE Value:
	[2:0]		These READ/WRITE bit-fields, along with "FEBE Register Enable" permit the user to configure the DS3/E3 Frame Generator block to transmit "user-specified" FEBE values (to the remote terminal) based upon the contents of these bit-fields.
			If the user sets the "FEBE Register Enable" bit-field to "1", then the DS3/E3 Frame Generator block will write the contents of these bit-fields into the FEBE bits, within each outbound DS3 frame.
			If the user sets the "FEBE Register Enable" bit-field to "0" then these register bits will be ignored.
4	FEBE	R/W	Transmit FEBE (by Software) Enable:
	Register Enable		This READ/WRITE bit field permits the user to configure the DS3/E3 Frame Generator block to transmit "user-specifed" FEBE values (to the remote terminal) per register setting via the "TxFEBEDat[2:0]" bit-field. This option provides the user with software control over the "outbound" FEBE values, within the DS3 data stream.
		odu	0 – Configures the DS3/E3 Frame Generator block to set the FEBE bit-fields (within each outbound DS3 frame) to the appropriate values based upon receive conditions, as determined by the companion Primary Frame Synchronizer block.
			1 – Configures the DS3/E3 Frame Generator block to write the contents of the "TxFEBEDat[2:0]" bit-fields into the FEBE bits, within each "outbound" DS3 frame.
3	Tx P-Bit	R/W	Transmit P-Bit Error:
	Error	220	This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with erred P-bits, as indicated below.
		SU	0 – Configures the DS3/E3 Frame Generator block to generate and transmit DS3 frames, to the remote terminal equipment.
			1 – Configures the DS3/E3 Frame Generator block to generate and transmit DS3 frames, to the remote terminal equipment.
2 – 0	TxM_Bit_	R/W	Transmit M-Bit Error:
	Mask[2:0]		These READ/WRITE bit-fields permit the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with erred M-bits.
			These three (3) bit-fields correspond to the three M-bits, within each outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these bit-fields and the value of the three M-bits. The results of this calculation will be written back into the M-bit positions within each outbound DS3 frame.
			The user should set these bit-fields to "0, 0, 0" for normal (e.g., un-erred) operation.

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 349: TxDS3 F-Bit Mask # 1 Register (; Address Location= 0xN336, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		F, M, P Bit Pass Thru Enable	F_Bit Mask[27]/ UDL Bit # 9 (C73)	F_Bit Mask [26]/ UDL Bit # 8 (C72)	F_Bit Mask [25]/ UDL Bit # 7 (C71)	F_Bit Mask [24]/
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	is d
4	F, M, P Bit Pass Thru	R/W	F-Bit, M-Bit, P-Bit Pass-Thru Enable
	Enable		This READ/WRITE bit-field permits the user to configure Frame Generator block to allow any F, M and P bits (within the DS3 signal) that it accepts to pass through in an un-altered manner.
			This feature is useful whenever the XRT94L33 device is handling unframed data that is operating at the DS3-rate (44.736MHz).
			0 – Disables this feature
			1 – Enables this feature
3	F Bit Mask[27]/	R/W	Transmit F-Bit Error – Bit 28/UDL Bit # 9 (C73):
	UDL Bit # 9 (C73)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxQHSrc" = 0 - Transmit F-Bit Error – Bit 28:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
		produ	This particular F-bit corresponds with the 28 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 28 th F-bit. The results of this calculation will be written back into the 28 th F-bit position, within each outbound DS3 frame.
	~	× 20.	the user should set this bit-field to "0" for normal (e.g., un-erred) operation.
		80 2	If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 9 or C73 bit:
		<i>?</i> `	This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #9 (or C73)" bit-fields, within the outbound DS3 data-stream.
			0 – Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 9 or the C73 bit-field).
			1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask	R/W	Transmit F-Bit Error – Bit 27/UDL Bit # 8 (C72):
	[26]/ UDL Bit #8 (C72)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	( -		If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 27
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame



Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 27th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 27th F-bit. The results of this calculation will be written back into the 27th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 8 or C72 bit: This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #8 (or C72)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 8 or the C72 bit-field). 1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field. Transmit F-Bit Error – Bit 26/UDL Bit # 7 (C71): 1 F Bit Mask R/W [25]/ The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), UDL Bit #7 within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". (C71) If "TxOHSrc" = 0 Transmit F-Bit Error – Bit 26: This READ/WRITE bit field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 26th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 26th F-bit. The results of this calculation will be written back into the 26th F-bit position. within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. If TxOHSrc" = 1 – Insert Enable for UDL Bit # 7 or C71 bit: This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #7 (or C71)" bit-fields, within the outbound DS3 data-stream. 0 – Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 7 or the C71 bit-field). 1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field. F Bit Mask [24] 0 R/W Transmit F-Bit Error – Bit 25: This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 25th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 25th F-bit. The results of this calculation will be written back into the 25th F-bit position. within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. Note: This bit-field is ignored if Bit 7 (TxOHSrc), within the "Test Register (Address Location= 0xN30C) is set to the "1".

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 350: TxDS3 F-Bit Mask # 2 Register (Address Location= 0xN337, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [23]/	F_Bit Mask [22]/	F_Bit Mask [21]/	F_Bit Mask [20]	F_Bit Mask [19]/	F_Bit Mask [18]/	F_Bit Mask [17]/	F_Bit Mask [16]
UDL Bit	UDL Bit	UDL Bit		DL Bit	DL Bit	DL Bit	
# 6 (C63)	# 5 (C62)	# 4 (C61)		# 3 (C53)	# 2 (C52)	# 1 (C51)	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	F Bit Mask[23]/	R/W	Transmit F-Bit Error – Bit 24/UDL Bit #6(C63);
	UDL Bit # 6 (C63)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Indirect Address = 0xNE, 0x0C; Direct Address Address Location= 0xNFN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit FBit Error – Bit 24:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 24th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 24th F-bit. The results of this calculation will be written back into the 24th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" - Insert Enable for UDL Bit # 6 or C63 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 6 (or C63)" bit-fields, within the outbound DS3 data-stream.
		orodi	0 -Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g, the UDL Bit # 6 or the C63 bit-field).
	~	0,0	1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask	R/W	Transmit F-Bit Error – Bit 23/UDL Bit # 5 (C62):
	[22]/ UDL Bit # 5 (C62)	<u>o</u> .	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(002)		If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 23:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 23 rd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 23 rd F-bit. The results of this calculation will be written back into the 23rd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 5 or C62 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame



		-	
			Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 5 (or C62)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 5 or the C62 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask	R/W	Transmit F-Bit Error – Bit 22/UDL Bit # 4 (C61):
	[21]/ UDL Bit # 4 (C61)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 22:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 22 nd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this pit-field and value of the 22 nd F-bit. The results of this calculation will be written back into the 22 nd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 Insert Enable for UDL Bit # 4 or C61 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 4 (or C61)" bit-fields, within the outbound DS3 data-stream.
			<ul> <li>0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 4 or the C61 bit-field).</li> <li>Configures the DS3/E3 Frame Generator block to NOT externally accept</li> </ul>
			and insert data into this overhead bit-field.
4	F Bit Mask [20]	R/W	Transmit F-Bit Error – Bit 21:
		10 hee	This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
	The	atann	This particular F-bit corresponds with the 21 st F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 21 st F-bit. The results of this calculation will be written back into the 21 st F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask	R/W	Transmit F-Bit Error – Bit 20/DL Bit # 3 (C53):
	[19]/ DL Bit # 3 (C53)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 20:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the $20^{th}$ F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the $20^{th}$ F-bit. The results of this calculation will be written back into the $20^{th}$ F-bit position, within each outbound DS3 frame.

### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

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			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for DL Bit # 3 or C53 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 3 (or C53)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL # Bit 3 or the C53 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask	R/W	Transmit F-Bit Error – Bit 19/DL Bit # 2 (C52):
	[18]/ DL Bit # 2 (C52)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 19:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 19 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 19 th F-bit. The results of this calculation will be written back into the 19 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" ∈ 1 - Insert Enable for DL Bit # 2 or C52 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 2 (or C52)" bit-fields, within the outbound DS3 data-stream.
			0 Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL Bit # 2 or the C52 bit-field).
		NOO	1. Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask	R/W	Transmit F-Bit Error – Bit 18/DL Bit # 1 (C51):
	[17]/ DL Bit # 1 (C51)	O R/VV	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
		<b>N</b>	If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 18:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 18 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 18 th F-bit. The results of this calculation will be written back into the 18 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for DL Bit # 1 or C51 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 1 (or C51)" bit-fields, within the outbound DS3 data-stream.



			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL Bit # 1 or the C51 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [16]	R/W	Transmit F-Bit Error – Bit 17:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 17 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 17 th F-bit. The results of this calculation will be written back into the 17 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "Offor normal (e.g., un-erred) operation.

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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 351: TxDS3 F-Bit Mask # 3 Register (Address Location= 0xN338, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [15]/ FEBE Bit 3 (C43)	F_Bit Mask [14]/ FEBE Bit 2 (C42)	F_Bit Mask [13]/ FEBE Bit 1 (C41)	F_Bit Mask [12]	F_Bit Mask [11]/ CP Bit # 3 (C33)	F_Bit Mask [10]/ CP Bit # 2 (C32)	F_Bit Mask [9]/ CP Bit # 1 (C31)	F_Bit Mask [8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	F Bit Mask[15]/	R/W	Transmit F-Bit Error – Bit 16/FEBE Bit #3 (C43);
	FEBE Bit # 3 (C43)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location=0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 16:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 16 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 16 th F-bit. The results of this calculation will be written back into the 16 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 Insert Enable for FEBE Bit # 3 or C43 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEBE Bit # 3 (or C43)" bit-fields, within the outbound DS3 data-stream.
		, o ²	0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the FEBE Bit # 3 or the C43 bit-field).
		22	Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [14]/	R/W	Transmit F-Bit Error – Bit 15/FEBE Bit # 2 (C42):
	FEBE Bit # 2 (C42)	ଁ ଚ	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 15:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 15 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 15 th F-bit. The results of this calculation will be written back into the 15 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 2 or C42 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream"



			circuitry) and insert it into the "FEBE Bit # 2 (or C42)" bit-fields, within the
			outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the FEBE Bit # 2 or the C42 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask [13]/	R/W	Transmit F-Bit Error – Bit 14/FEBE Bit # 1 C41):
	FEBE Bit 1 (C41)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 14:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 14 th F-bit, within a given outbound DS3 frame. The DS3/E# Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 14 th F-bit. The results of this calculation will be written back into the 14 th F-bit position, within each outbound DS3 frame.
			The user should set this bit field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 1 or C41 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEBE Bit # 1 (or C41)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g, the FEBE Bit # 1 or the C41 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [12]	R/W	Trahsmit EBit Error – Bit 13:
	م. ا	odue	This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
	the p	a a d	This particular F-bit corresponds with the 13 th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 13 th F-bit. The results of this calculation will be written back into the 13 th F-bit position, within each outbound DS3 frame.
		<b>'</b> 0'	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask [11]/	R/W	Transmit F-Bit Error – Bit 12/CP Bit # 3 (C33):
	CP Bit # 3 (C33)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 12:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 12th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 12th F-bit. The results of this calculation will be written back into the 12th F-bit position, within each outbound DS3 frame.

			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.				
			If "TxOHSrc" = 1 - Insert Enable for CP Bit # 3 or C33 bit:				
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 3 (or C33)" bit-fields, within the outbound DS3 data-stream.				
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 3 or the C33 bit-field).				
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.				
2	F Bit Mask [10]/	R/W	Transmit F-Bit Error – Bit 11/CP Bit # 2 (C32):				
	CP Bit # 2 (C32)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".				
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 11:				
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.				
			This particular F-bit corresponds with the 11th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 11th F-bit. The results of this calculation will be written back into the 11th F-bit position, within each outbound DS3 frame.				
			The user should set this bill field to '0" for normal (e.g., un-erred) operation.				
			If "TxOHSrc" = 1 - Insert Enable for CP Bit # 2 or C32 bit:				
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 2 (or C32)" bit-fields, within the outbound DS3 data stream.				
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 2 or the C32 bit-field).				
		No	1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.				
1	F Bit Mask [9]/	R/W	Transmit F-Bit Error – Bit 10/CP Bit # 1 (C31):				
	CP Bit # 1 (C31)	93,0	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".				
		ି	If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 10:				
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.				
			This particular F-bit corresponds with the 10th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 10th F-bit. The results of this calculation will be written back into the 10th F-bit position, within each outbound DS3 frame.				
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.				
			If "TxOHSrc" = 1 - Insert Enable for CP Bit # 1 or C31 bit:				
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 1 (or C31)" bit-fields, within the outbound DS3 data-stream.				





			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 1 or the C31 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [8]	R/W	Transmit F-Bit Error – Bit 9:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 9th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 9th F-bit. The results of this calculation will be written back into the 9th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

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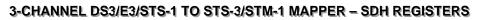
Table 352: TxDS3 F-Bit Mask # 4 Register (Address Location= 0xN339, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/ X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/ NA Bit (C12)	F_Bit Mask [1]/ AIC Bit (C11)	F_Bit Mask [0]/ X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION			
7	F Bit Mask[7]/	R/W	Transmit F-Bit Error – Bit 8/UDL Bit # 3 (C23):			
	UDL Bit # 3 (C23)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".			
			If "TxOHSrc" = 0 – Transmit F-Bit Error Bit 8:			
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.			
			This particular F-bit corresponds with the 8th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 8th F-bit. The results of this calculation will be written back into the 8th F-bit position, within each outbound DS3 frame.			
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation			
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 3 or C23 bit:			
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 3 (or C23)" bit-fields, within the outbound DS3 data-stream.			
		.0	O Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 3 or the C23 bit-field).			
		e?	1. Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.			
6	F Bit Mask [6]	R/W	Fransmit F-Bit Error – Bit 7/UDL Bit # 2 (C22):			
	UDL Bit # 2 (C22)	<u> </u>	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".			
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 7:			
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.			
			This particular F-bit corresponds with the 7th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 7th F-bit. The results of this calculation will be written back into the 7th F-bit position, within each outbound DS3 frame.			
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.			
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 2 or C22 bit:			
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from			



0       - Configures the DS3/E3 Frame Generator block to externally accelinsert data into this particular overhead bit-field (e.g., the UDL Bit # 2 or the bit-field).         1       - Configures the DS3/E3 Frame Generator block to NOT externally accelinsert data into this overhead bit-field.         5       F Bit Mask [5]/       R/W         UDL Bit # 1       (C21)         R/W       Transmit F-Bit Error – Bit 6/UDL Bit # 1 (C21):         The exact function of this register bit depends upon whether Bit 7 (TxG within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0"         If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 6:         This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to transmit DS3 frames with a single/particular erred F b         This particular F-bit corresponds with the 6th F-bit, within a given outbou frame. The DS3/E3 Frame Generator block will perform an XOR operative context of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit, within each ou DS3 frame.         The user should set this bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 or C21 bit:         This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.         0       - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g.,	he C22 ept and DHSrc),
5       F Bit Mask [5]/ UDL Bit # 1 (C21)       R/W       Transmit F-Bit Error – Bit 6/UDL Bit # 1 (C21): The exact function of this register bit depends upon whether Bit 7 (Tx0 within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0" If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 6: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to transmit DS3 frames with a single/particular erred F b This particular F-bit corresponds with the 6th F-bit, within a given outbou frame. The DS3/E3 Frame Generator block will perform an XOR operati the contents of this bit-field and value of the 6th F-bit, not not perform Calculation will be written back into the 6th F-bit position, within each ou DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.         0       - Configures the DS3/E3 Frame Generator block to externally accept insert data into the overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit)	DHSrc),
UDL Bit # 1 (C21)The exact function of this register bit depends upon whether Bit 7 (Tx0 within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0" If "Tx0HSrc" = 0 - Transmit F-Bit Error - Bit 6: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to transmit DS3 frames with a single/particular erred F b This particular F-bit corresponds with the 6th F-bit, within a given outbou frame. The DS3/E3 Frame Generator block will perform an XOR operati the contents of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit position, within each ou DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation If "Tx0HSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.0 - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit)	
(C21) (C21) The exact function of this register bit depends upon whether bit 7 (1xk within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0" If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 6: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to transmit DS3 frames with a single/particular erred F b This particular F-bit corresponds with the 6th F-bit, within a given outbout frame. The DS3/E3 Frame Generator block will perform an XOR operation the contents of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit position, within each our DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation of this READ/WRITE bit-field bermits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" candinasert it into the "UDL Bit # 1 or C21 bit. This READ/WRITE bit-field DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" candinasert and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" candinasert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit)	
<ul> <li>This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to transmit DS3 frames with a single/particular erred F b</li> <li>This particular F-bit corresponds with the 6th F-bit, within a given outbour frame. The DS3/E3 Frame Generator block will perform an XOR operation the contents of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit position, within each our DS3 frame.</li> <li>The user should set this bit-field to "0" for normal (e.g., un-erred) operation of the field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" or and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.</li> <li>0 - Configures the DS3/E3 Frame Generator block to externally accept in sert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit)</li> </ul>	_
Generator block to transmit DS3 frames with a single/particular erred F bThis particular F-bit corresponds with the 6th F-bit, within a given outbou frame. The DS3/E3 Frame Generator block will perform an XOR operati the contents of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit position, within each ou DS3 frame.The user should set this bit-field to "0" for normal (e.g., un-erred) operation If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit:This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.0 - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit	_
<ul> <li>frame. The DS3/E3 Frame Generator block will perform an XOR operation the contents of this bit-field and value of the 6th F-bit. The results calculation will be written back into the 6th F-bit position, within each our DS3 frame.</li> <li>The user should set this bit-field to "0" for normal (e.g., un-erred) operation if "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit:</li> <li>This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" cand insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream.</li> <li>0 - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit)</li> </ul>	
<ul> <li>If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit: This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outboundata-stream.</li> <li>0 - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit</li> </ul>	on with of this
This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" of and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbound data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit	n.
Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbour data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally acce insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit	
insert data into this overhead bit-field (e.g., the UDL Bit #1 or the C21 bit	ircuitry)
1- Configures the D\$3/E3 Frame Generator block to NOT externally acc	
insert data into this overhead bit-field.	ept and
4 F Bit Mask [4]/ R/W Transmit F-Bit Error – Bit 5/X Bit # 2:	
X Bit # 2 The exact function of this register bit depends upon whether Bit 7 (TxC within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0"	
Cif "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 5:	
This READ/WRITE bit-field permits the user to configure the DS3/E3	
This particular F-bit corresponds with the 5th F-bit, within a given outbou frame. The DS3/E3 Frame Generator block will perform an XOR operation the contents of this bit-field and value of the 5th F-bit. The results calculation will be written back into the 5th F-bit position, within each our DS3 frame.	on with of this
The user should set this bit-field to "0" for normal (e.g., un-erred) operation	n.
If "TxOHSrc" = 1 - Insert Enable for X Bit # 2:	
This READ/WRITE bit-field permits the user to configure the DS3/E3 Generator block to externally accept an overhead bit (from "up-stream" c and insert it into the "X-Bit # 2" bit-field, within the outbound DS3 data-str	
0 - Configures the DS3/E3 Frame Generator block to externally accertion insert data into this overhead bit-field (e.g., the X bit # 2).	ircuitry)
1- Configures the DS3/E3 Frame Generator block to NOT externally acc insert data into this overhead bit-field.	ircuitry) eam.
3 F Bit Mask [3]/ R/W Transmit F-Bit Error – Bit 4/FEAC Bit (C13):	ircuitry) eam. ept and





	FEAC Bit (C13)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 4:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 4th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 4th F-bit. The results of this calculation will be written back into the 4th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEAC or C13 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEAC (or C13)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g. the FEAC or the C13 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [2]/	R/W	Transmit F-Bit Error – Bit 3/NA Bit (C12):
	NA Bit (C12)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error – Bit 3:
			This READ/WRITE bit field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 3rd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 3rd F-bit. The results of this calculation will be written back into the 3 rd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
		0	If "TxOHSrc" = 1 - Insert Enable for NA or C12 bit:
	~	0 12	This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "NA (or C12)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the NA or the C12 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [1]/	R/W	Transmit F-Bit Error – Bit 2/AIC Bit (C11):
	AIC Bit (C11)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 2:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 2 nd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 2 nd F-bit. The results of this



			أمم
			calculation will be written back into the 2 nd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for AIC or C11 bit:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "AIC (or C11)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the AIC or the C11 bit-field).
			1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0 F	F Bit Mask [0]/	R/W	Transmit F-Bit Error – Bit 1/X Bit # 1:
	X Bit # 1		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 1:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit.
			This particular F-bit corresponds with the 1 st F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 1 st F-bit. The results of this calculation will be written back into the 1 st F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 15 Insert Enable for X Bit # 1:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "X-Bit # 1" bit-field, within the outbound DS3 data-stream.
		, c	O Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the X-bit # 1 bit-field).
			1-Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



## Table 353: Transmit DS3 Pattern Register (Address Location= 0xN34C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxAIS - Unframed All Ones	DS3 AIS Non-Stuck Stuff		TxLOS Pattern Select		Transmit_Idle	e_Pattern[3:0]	
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7	TxAIS - Unframed All	R/W	Transmit AIS – Unframed All Ones:
	Ones		This READ/WRITE bit-field permits the user to configure the "DS3/E3 Frame Generator" block to transmit either of the following patterns, anytime it is configured to transmit the AIS indicator.
			• A "Framed, repeating 1, 0, 7, 0 pattern (per Bellcore GR-499- CORE) or
			An "Unframed All Ones" pattern.
			0 – Configures both the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) to transmit the "Framed, Repeating 1, 0, 1, 0, pattern; whenever it is configured to transmit the AIS indicator.
			1- Configures both the DS3/E3 Frame Generator and the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) to transmit an "Untramed, All-Ones" pattern, whenever it is configured to transmit the AIS indicator.
		je	<b>NOTE:</b> This configuration setting applies to both the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub- block (within the Primary Frame Synchronizer block)
6	DS3 AIS Non-Stuck	R/W	DS3 AIS – Non-Stuck Stuff Option – AIS Pattern:
	Stuff The ata		This READ/WRITE bit-field (along with the "TxAIS – Unframed All Ones" bit-field) permits the user to define the type of AIS data-stream that both the DS3/E3 Frame Generator and the AIS/DS3 Idle Signal Pattern Generator sub-block (within the Primary Frame Synchronizer block) will transmit, as described below.
			0 – Configures the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block to force all of the "C" bits to "0", whenever it is configured to transmit a Framed AIS signal.
			1 – Configures the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block to NOT force all of the "C" bits to "0", when it is configured to transmit a Framed AIS signal. In this case, the "C" bits can be used to transport FEAC and PMDL Messages.
			<b>NOTE:</b> This bit-field is ignored if the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block has been configured to transmit an "Unframed – All Ones" type of AIS signal.
5	Unused	R/W	
4	TxLOS Pattern Select	R/W	Transmit LOS Pattern Select:
			This READ/WRITE bit-field permits the user to configure the "DS3/E3 Frame Generator" block to transmit either an "All Zeros" or an "All Ones" pattern, anytime it is configured to transmit the "LOS Pattern" to



			the remote terminal equipment, as described below.			
			0 – Configures the DS3/E3 Frame Generator to transmit an "All Zeros" pattern, whenever it is configured to transmit the LOS pattern.			
			1 – Configures the DS3/E3 Frame Generator to transmit an "All Ones" pattern, whenever it is configured to transmit the LOS pattern.			
3 - 0	Tx_Idle Pattern[3:0]	R/W	Transmit DS3 Idle Signal Pattern:			
			These READ/WRITE bit-fields permit the user to specify the type of framed, repetitive four-bit pattern that the DS3/E3 Frame Generator block should send, whenever it is transmitting the "DS3 Idle" pattern.			
			<b>Note:</b> Setting these bit-fields to "[1, 1, 0, 0] configures the DS3/E3 Frame Generator block to transmit the standard "Framed, repeating "1, 1, 0, 0," pattern (per Bellcore GR-499-CORE) requirements.			

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### 3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



### 1.10.7 TRANSMIT E3, ITU-T G.751 RELATED REGISTERS

## Table 354: TxE3 Configuration Register – G.751 (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxBIP-4 Enable	TxASrc	TxASrcSel[1:0]		Sel[1:0]	TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре								
7	TxBIP-4 Enable	R/W	Transmi	Transmit BIP-4 Enable:						
					bit-field permits the user to configure lock to do the following:	the DS3/E3				
			• To c	<ul> <li>To compute the BIP-4 value over a given outbound E3 frame.</li> </ul>						
			• To insert this BIP-4 value into the last nibble-field within the very next E3 frame.							
			0 – Does "outboun	0 – Does not configure this option. In this case, the last nibble (of each "outbound" E3 frame) will contain payload data.						
			1 – Configures the DS3/E3 Frame Generator block to compute and insert the BIP-4 value.							
6 - 5	TxASrcSel[1:0]	R/W	Transmi	t A Bit So	urce Select[1:0]:					
		č	These two READ/WRITE bit-fields permit the user to specify the source or type of data that is being carried via the "A" bits, within each "outbound" E3 data stream, as indicated below.							
		XVV	TxASrcSel[1:0] Resulting Source of A Bit							
	the	in she	ala	0	The "TxA" bit-field, within the "TxE3 Service Bit" register (Address Location= 0xN335).					
		9,9	0	1	Not Valid - Do not use.					
		31	1	0	The "A" bit is sourced via up-stream circuitry and inserted into the "outbound E3 data-stream.					
					This is discussed in greater detail in Section					
			1	1	The Companion Primary Frame Synchronizer block. In this case, the A bit will transmit the FEBE indicator to the remote terminal equipment. The A bit will be set to "1" when the companion Primary Frame Synchronizer block detects a BIP-4 error, and will be set to "0" when the Primary Frame Synchronizer block detects un-erred E3 frames.					



4 – 3	TxNSrcSel[1:0]	R/W	Transmit	N Bit So	urce Select[1:0]:	
			type of da	ata that is	VRITE bit-fields permit the user to specify the being carried via the "N" bits, within each indicated below.	
			TxNSrc	Sel[1:0]	Resulting Source of N Bit	
			0	0	The "TxN" bit-field, within the "TxE3 Service Bit" register (Address Location= 0xN335).	
			0	1	Not Valid – Do not use.	
			1	0	The Transmit LAPD Controller sub- block (within, the DS3/E3 Frame Generator block)	
					In this case, the N bit will function as the LARD/PMDL channel.	
			1	1	The "N" bit is accepted (via "up-stream" circuitry) and inserted into the outbound E3 data-stream.	
				ner	This is discussed in greater detail in Section	
2	TxAIS Enable	R/W	Transmit	AIS Indi	cator:	
			the DS3/I indicator t	E3 Frame o the rem	bit-field permits the user to (by software c Generator block to generate and trans note terminal equipment, as described below	mit the AIS v.
		101	and transi	mit the Al	igure the DS3/E3 Frame Generator block S indicator. In this case, the DS3/E3 Fram normal E3 traffic.	
	, co	UC 2	transmit tl	he AIS in bits (within	e DS3/E3 Frame Generator block to ge dicator. In this case, the DS3/E3 Frame G n the "outbound" E3 data stream) to an "U	enerator will
	ne l'a	shad			eld is ignored if the DS3/E3 Frame Generat figured to transmit the LOS pattern.	or block has
1	TxLOS Enable	R/W	Transmit	LOS (Pa	ttern) Enable:	
	~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~		the DS3/E	3 Frame	bit-field permits the user to (by software c Generator block to transmit the LOS (Los te terminal equipment, as described below.	ss of Signal)
			and trans	mit the LO	igure the DS3/E3 Frame Generator block DS pattern. In this case, the DS3/E3 Fram niting normal E3 traffic.	
			transmit t	he LOS force all	e DS3/E3 Frame Generator block to ge pattern. In this case, the DS3/E3 Frame bits (within the "outbound" E3 data stream	e Generator
0	TxFAS Source Sel	R/W	Transmit	FAS Sou	Irce Select:	
				ming Alig	bit-field permits the user to specify the sender of the se	
			0 – Config	gures the	DS3/E3 Frame Generator block to interna	Illy generate



and insert the FAS bits within the outbound E3 data-stream.
1 – Configures the DS3/E3 Frame Generator block to accept the FAS bits from "up-stream" circuitry (via the Transmit Payload Data Input Interface block) and to insert this data into the outbound E3 data-stream. This is discussed in greater detail in Section

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Table 355: TxE3 LAPD Configuration Register – G.751 (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	5 S
3	Auto Retransmit	R/W	Auto-Retransmit of LAPD Message This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block) to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message, the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 – Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmited until the user commands another transmission. 1 – Enables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit PMDL Message only once afterwards the Transmitsion. 1 – Enables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. <i>Note: This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.</i>
2	Reserved	R/O	
1	Transmit LAPD Message Length	A A A A A A A A A A A A A A A A A A A	 Transmit LAPD Message Length Select: This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 - Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 - Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
0	Transmit LAPD Enable	R/W	Transmit LAPD Controller sub-block Enable: This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller subblock, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The Transmit LAPD Controller sub-block will continue to do this until the user commands the Transmit LAPD Controller sub-block to transmit a PMDL Message.



0 – Disables the Transmit LAPD Controller sub-block.
1 – Enables the Transmit LAPD Controller sub-block.





Table 356: TxE3 LAPD Status/Interrupt Register – G.751 (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Initiate Transmission of LAPD/ PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	this reo
3	Initiate Transmission of LAPD/ PMDL Message	R/W	 Transmit LAPD Message Command: A "0" to "1" transition, within this pit-field commands the Transmit LAPD Controller sub-block to begin the following activities: Reading out the contents of the Transmit LAPD Message Buffer.
	moodgo		 Zero-Stuffing of this data FCS Calculation and Insertion
			 Fragmentation of this composite PMDL Message, and insertion into the "N" bit-fields, within each outbound E3 frame.
			NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
2	Transmit LAPD	R/O	Transmit LAPD Controller Busy Indicator:
	Controller Busy	, J	This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.
			O – Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message.
	the	20	16 Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message.
		d'a no	NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
1	Transmit	R/W	Transmit LAPD Interrupt Enable:
	LAPD Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal.
			0 – Disables Transmit LAPD Interrupt.
			1 – Enables Transmit LAPD Interrupt.
0	Transmit	RUR	Transmit LAPD Interrupt Status:
	LAPD Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register.
			0 - Transmit LAPD Interrupt has NOT occurred since the last read of this

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	register.
	1 – Transmit LAPD Interrupt has occurred since the last read of this register.

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Table 357: TxE3 Service Bits Register – G.751 (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		TxA	TxN				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	TxA	R/W	Transmit A Bit:
			This READ/WRITE bit-field permits the user to control the state of the "A" bit, within each "outbound" E3 frame, as indicated below.
			0 – Forces each A bit (within the "outbound" E3 frame) to "0".
			1 – Forces each A bit (within the "outbound" E3 frame) to "1".
			Note: This bit-field is only valid if the DS3/E3 Frame Generator block has been configured to use this bit-field as the source of the "A" bit (e.g., if "TxASrcSel[1:0] = "0, 0").
0	TxN	R/W	Transmit N Bit: This READ/WRITE bit-field permits the user to control the state of the "N" bit, within each "outbound" E3 frame as indicated below.
			0 – Forces each N bit (within the "outbound" E3 frame) to "0".
			1 – Forces each N bit (within the "outbound" E3 frame) to "1".
			Note: This bit field is only valid if the DS3/E3 Frame Generator block has been configured to use this bit-field as the source of the "N" bit (e.g., if "TNNSrSel[1:0] = "0, 0").

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Table 358: TxE3 FAS Error Mask Upper Register – G.751 (Address Location= 0xN348, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			TxFAS_Error_Mask_Upper[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 5	Unused	R/O	
4 – 0	TxFAS_Error_Mask_ Upper[4:0]	R/W	 TxFAS Error Mask Upper[4:0]: These READ/WRITE bit-fields permit the user to insert bit errors into the upper five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the upper 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. Note: For normal operation, the user should set this register to 0x00.

Table 359: TxE3 FAS Error Mask Lower Register G.751 (Address Location= 0xN349, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	BIT 4	BIT 3	Віт 2	Віт 1	Віт 0
	Unused		18.0	TxFAS_	_Error_Mask_Lo	wer[4:0]	
R/O	R/O	R/O	RW C	R/W	R/W	R/W	R/W
0	0	0	0,00	0	0	0	0

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BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4 - 0	TxFAS_Error Mask Lower[4:0]	R/W	 TxFAS Error Mask Lower[4:0]: These READ/WRITE bit-fields permit the user to insert bit errors into the lower five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the lower 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. Note: For normal operation, the user should set this register to 0x00.

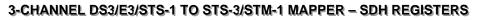


Table 360: TxE3 BIP-4 Mask Register – G.751 (Address Location= 0xN34A, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unu	ised		TxBIP-4_Mask[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 4	Unused	R/O	
3 - 0	TxBIP-4_Mask_[3:0]	R/W	TxBIP-4 Error Mask[3:0]:
			 These READ/WRITE bit fields permit the user to insert bit errors into the BIP-4 bits, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the BIP-4 bits, and this register. The results of this calculation will be inserted into the BIP-4 bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the BIP-4 will be in error. Note: For normal operation, the user should set this register to 0x00.

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1.10.8 TRANSMIT E3, ITU-T G.832 RELATED REGISTERS

Table 361: TxE3 Configuration Register – G.832 (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		TxDL in NR	Reserved	TxAIS Enable	TxLOS Enable	TxMA Rx
R/O	R/O	R/O	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	things
4	TxDL in NR	R/W	Transmit DL (Data Link Channel) in NR Byte:
			This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/F3 Frame Generator block) to use either the NR or the GC byte as the LAPD/PMDL channel, as described below.
			0 – Configures the Transmit LAPD Controller sub-block to transmit all "outbound" LAPD/PMDL Messages via the GC byte.
			1 – Configures the Transmit LAPD Controller sub-block to transmit all "outbound" LAPD/PMDL Messages via the NR byte.
3	Unused	R/O	inc et (O
2	TxAIS Enable	R/W	Transmit AIS Indicator
			This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to generate and transmit the AIS indicator to the remote terminal equipment as described below.
		\$	Does not configure the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit normal E3 traffic.
		eero	Configures the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator will force all bits (within the "outbound" E3 data stream) to an "Unframed, All Ones" pattern.
		931	Note: This bit-field is ignored if the DS3/E3 Frame Generator block has been configured to transmit the LOS pattern.
1	TxLOS Enable	R/W	Transmit LOS (Pattern) Enable:
			This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment.
			0 – Does not configure the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will transmit normal E3 traffic.
			1 – Configures the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will force all bits (within the "outbound" E3 data stream) to an "All Zeros" pattern.
0	TxMA Primary	R/W	Transmit MA Byte from Primary Frame Synchronizer Block Select:
	Frame Synchronizer Block		This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to use either the Primary Frame Synchronizer block or the "Tx MA Pute" Register as the source of the EEEE/PDI and EEEE/PEI bit fields



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MA Byte" Register as the source of the FERF/RDI and FEBE/REI bit-fields (within the MA byte-field of the "outbound" E3 data stream); as indicated below.
0 – Configures the DS3/E3 Frame Generator block to read in the contents of the "Tx MA Byte" register (Address Location= 0xN336), and write this value into the "MA" byte-field within each "outbound" E3 frame.
Note: This option permits the user to send the FERF/RDI and FEBE/REI indicators, under software control.
1 – Configures the DS3/E3 Frame Generator block to set the FERF/RDI and FEBE/REI bit-fields to values, based upon conditions detected by the companion Priimary Frame Synchronizer block.

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Table 362: TxE3 LAPD Configuration Register – G.832 (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable		
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	 Auto-Retransmit of LAPD Message: This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message; the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 – Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will only transmit the PMDL Message once. Afterwards the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via either the NR of GC byte, within each output E3 frame. The Transmit LAPD Controller sub-block will not transmit any more PMDL Messages until the user commands another transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. Note. This bit-field is ignored if the Transmit LAPD Controller sub-block is
2	Reserved	R/O	disabled.
1	Transmit LAPP Message Length	RAN	 Transmit LAPD Message Length Select: This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 - Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 - Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes. NOTE: This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.
0	Transmit LAPD Enable	R/W	Transmit LAPD Controller Sub-Block Enable: This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller sub-block, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via either the "NR" or "GC" bytes, within the outbound E3 data stream. The Transmit LAPD Controller sub-block will continue to do this until the user commands the



	Fransmit LAPD Controller sub-block to transmit a PMDL Message.
0) – Disables the Transmit LAPD Controller sub-block.
1	 Enables the Transmit LAPD Controller sub-block.

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Table 363: TxE3 LAPD Status/Interrupt Register – G.832 (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	is co
3	Initiate Transmission of LAPD/ PMDL Message	R/W	 Transmit LAPD Message Command: A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller sub-block to begin the following activities: Reading out the contents of the Transmit LAPD Message Buffer. Zero-Stuffing of this data FCS Calculation and Insertion Fragmentation of this composite PMDL Message, and insertion into either the "NR" or "GC" byte-fields, within each outbound E3 frame. NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
2	Transmit LAPD Controller Busy	R/O	 Transmit LAPD Controller Busy Indicator: This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 - Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message. 1 - Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message. NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
1	Transmit LAPD Interrupt Enable	R/W	 Transmit LAPD Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 – Disables Transmit LAPD Interrupt. 1 – Enables Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	Transmit LAPD Interrupt Status:This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPDInterrupt" has occurred since the last read of this register, as described below.0 – Indicates that the Transmit LAPD Interrupt has NOT occurred since the last



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	read of this register.
	1 – Indicates that the Transmit LAPD Interrupt has occurred since the last read of this register.

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Table 364: TxE3 GC Byte Register – G.832 (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TxGC_E	Byte[7:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxGC_Byte[7:0]	R/W	Transmit GC Byte:
			This READ/WRITE bit-field permits the user to specify the contents of the GC byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the GC byte-field, within each outbound E3 frame. Note: This register is ignored if the GC byte is configured to be the "LAPD/PMDL" channel.
Tabla 265.		ogiotor	G 832 (Address Location - 02N336, where N ranges from 0x02 to

Table 365: TxE3 MA Byte Register – G.832 (Address Location=0xN336, where N ranges from 0x02 to 0x04)

	-					
Віт 7	Віт 6	Віт 5	Віт 4 Віт 3	Віт 2	Віт 1	Віт 0
			TxMA Byte[7:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0		0	0	0
			or lot at			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
ВІТ NUMBER 7 – 0	NAME TxMA_Byte[7:0]	Type R/W Produce data	DESCRIPTION Transmit MA Byte: This READWRITE bit-field permits the user to specify the contents of the MA byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the MA byte-field, within each outbound E3 frame. Note: This register is ignored if the "Transmit MA Byte – from Primary Frame Synchronizer block" option is selected (e.g., by setting "TxMA Primary Frame Synchronizer block = 1").
			This feature permits the user to transmit the FERF/RDI and FEBE/REI indicators upon software command.



Table 366: TxE3 NR Byte Register – G.832 (Address Location= 0xN337, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxNR_Byte[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxNR_Byte[7:0]	R/W	Transmit NR Byte:
			This READ/WRITE bit-field permits the user to specify the contents of the NR byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the NR byte-field, within each outbound E3 frame. Note: This register is ignored if the NR byte is configured to be the "LAPD/PMDL" channel.
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Table 367: TxE3 Trail-Trace - 0 Register – G.832 (Address Location= 0xN338, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TxTTB	Byte_0			
R/W	R/W	R/W	R/W	OR/W	R/W	R/W	R/W
1	0	0	0		0	0	0
			11 10				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_0[7:0]	R/W	 Transmit Trail-Trace Message - Byte 0: These READ/WRITE bits permit the user to specify the contents of Byte 0, within the "outbound" Trail-Trace Message, which is to be transmitted via the outbound E3 data stream. By default, the MSB (Most Significant Bit) of this register bit will be set to identify this particular byte, as being the first byte of the "Trail-Trace Buffer" Message.
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Table 368: TxE3 Trail-Trace-1 Register – G.832 (Address Location = 0xN339, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_1						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7 – 0	TxTTB_Byte_1[7:0]	R/W	Transmit Trail-Trace Message - Byte 1:
			These READ/WRITE bits permit the user to specify the contents of the second byte (Byte 1) within the "Trail-Trace Message" that is be be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
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Table 369: TxE3 Trail-Trace-2 Register – G.832 (Address Location= 0xN33A, where N ranges from 0x02 to 0x04) o A

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0	
	TxTTB_Byte_2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	00	0	0	0	
	NO LONGIEU							

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_2[7:0]	R/W	Transmit Trail-Trace Message - Byte 2:
	ام	× *	These READ/WRITE bits permit the user to specify the contents of the third byte (Byte 2) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream.
	thep	S 2	NOTE: In order to permit the proper reception of this particular Trail- Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to "0".
	. 9.	ano	



Table 370: TxE3 Trail-Trace-3 Register – G.832 (Address Location= 0xN33B, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_3						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_3[7:0]	R/W	Transmit Trail-Trace Message - Byte 3:
			These READ/WRITE bits permit the user to specify the contents of the fourth byte (Byte 3) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to "0".
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Table 371: TxE3 Trail-Trace-4 Register – G.832 (Address Location= 0xN33C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3	Віт 2	Віт 1	Віт 0	
TxTTB_Byte_4							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	0000	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_4[7:0]	R/W	Transmit Trail-Trace Message - Byte 4:
	odi		These READ/WRITE bits permit the user to specify the contents of the tight byte (Byte 4) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream.
	the ato	may	NOTE: In order to permit the proper reception of this particular Trail- Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
	or all		

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Table 372: TxE3 TTB-5 Register – G.832 (Address Location= 0xN33D, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TxTTB_	_Byte_5			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_5[7:0]	R/W	Transmit Trail-Trace Message - Byte 5:
			These READ/WRITE bits permit the user to specify the contents of the sixth byte (Byte 5) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to '0".
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Table 373: TxE3 Trail-Trace-6 Register – G.832 (Address Location= 0xN33E, where N ranges from 0x02 to 0x04)

							Віт 0
			TxTTB	Byte_6	,		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	00	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре		~	DESCRIPTION
7 – 0	TxTTB_Byte_6[7:0]	R/W	Trans	smit T	rail-Trace Message - Byte 6:
		oduce	sever	nth by	AD/WRITE bits permit the user to specify the contents of the /te (Byte 6) within the "Trail-Trace Message" that is to be d vai the outbound E3 data stream.
	the	3 11	Trace	e Mes	order to permit the proper reception of this particular Trail- ssage, it is imperative that the user set the MSB (Most bit) within this register to "0".
	0	and			



Table 374: TxE3 Trail-Trace-7 Register – G.832 (Address Location= 0xN33F, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_7						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_7[7:0]	R/W	Transmit Trail-Trace Message - Byte 7:
			These READ/WRITE bits permit the user to specify the contents of the eighth byte (Byte 7) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

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Table 375: TxE3 Trail-Trace- 8 Register - G.832 (Address Location = 0xN340, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_8						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_8[7:0]	R/W	Transmit Trail-Trace Message - Byte 8:
			These READ/WRITE bits permit the user to specify the contents of the ninth byte (Byte 8) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
			oneanth

Table 376: TxE3 Trail-Trace-9 Register – G.832 (Address Location = 0xN341, where N ranges from 0x02 to 0x04) 0 3

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
			TxTTB	Byte_9				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0		0	0	0	
	or lottere							

BIT NUMBER	Nаме	
7 – 0	TxTTB_Byte_9[7:0]	R/W Transmit Trail-Trace Message - Byte 9:
		These READ/WRITE bits permit the user to specify the contents of the tenth byte (Byte 9) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream.
	thep	NOTE: In order to permit the proper reception of this particular Trace Trail Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
	0	and



Table 377: TxE3 Trail-Trace-10 Register – G.832 (Address Location= 0xN342, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TxTTB_	Byte_10			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_10[7:0]	R/W	Transmit Trail-Trace Message - Byte 10:
			These READ/WRITE bits permit the user to specify the contents of the eleventh byte (Byte 10) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

ever to permit the ace Message, it is imperat Significant bit) within this registe

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Table 378: TxE3 Trail-Trace-11 Register – G.832 (Address Location= 0xN343, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxTTB_Byte_11								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_11[7:0]	R/W	Transmit Trail-Trace Message - Byte 11:
			These READ/WRITE bits permit the user to specify the contents of the twelfth byte within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
			one null

Table 379: TxE3 Trail-Trace-12 Register – G.832 (Address Location= 0xN344, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxTTB_Byte_12								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	00	0	0	0		
	or lot ere								

BIT NUMBER	Nаме	
7 – 0	TxTTB_Byte_12[7:0]	R/W Transmit Trail-Trace Message - Byte 12:
	a C	These READ/WRITE bits permit the user to specify the contents of the 13 th byte (Byte 12) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream.
	thep	NOTE: In order to permit the proper reception of this particular Trail- Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
	0	and



Table 380: TxE3 TTB-13 Register – G.832 (Address Location= 0xN345, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxTTB_Byte_13								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_13[7:0]	R/W	Transmit Trail-Trace Message - Byte 13:
			These READ/WRITE bits permit the user to specify the contents of the 14 th byte (Byte 13) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

ered to permit the ace Message, it is impera Significant bit) within this registres.

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Table 381: TxE3 Trail-Trace-14 Register – G.832 (Address Location= 0xN346, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxTTB_Byte_14								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION
7 – 0	TxTTB_Byte_14[7:0]	R/W	Transmit Trail-Trace Message - Byte 14:
			These READ/WRITE bits permit the user to specify the contents of the 15 th byte (Byte 14) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. NOTE: In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to 0".
			oneonut

Table 382: TxE3 Trail-Trace-15 Register – G.832 (Address Location= 0xN347, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxTTB_Byte_15								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0		0	0	0		
	or lot ere								

BIT NUMBER	Nаме	
7 – 0	TxTTB_Byte_15[7:0]	R/W Transmit Trail-Trace Message - Byte 15:
	a C	These READ/WRITE bits permit the user to specify the contents of the 16 th (and last) byte within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream.
	the at	NOTE: In order to permit the proper reception of this particular Trail- Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".
	0	and



Table 383: TxE3 FA1 Error Mask Register – G.832 (Address Location= 0xN348, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	TxFA1_Mask_Byte[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	TxFA1_Mask_Byte[7:0]	R/W	TxFA1 Error Mask Byte[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the FA1 bytes, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the FA1 byte, and this register. The results of this calculation will be inserted into the FA1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA1 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

Table 384: TxE3 FA2 Error Mask Register – G 832 (Address Location= 0xN349, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0		
TxFA2_Mask_Byte[7:0]									
R/W	R/W	R/W	R/W O	R/W	R/W	R/W	R/W		
0	0	0	0 0	0	0	0	0		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxFA2_Mask Byte[7:0]	R/W	TxFA2 Error Mask Byte[7:0]:
	The star ma		These READ/WRITE bit-fields permit the user to insert bit errors into the FA2 bytes, within the outbound E3 data stream.
	orant		The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the FA2 byte, and this register. The results of this calculation will be inserted into the FA2 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA2 byte will be in error.
			<i>Note:</i> For normal operation, the user should set this register to 0x00.

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Table 385: TxE3 BIP-8 Error Mask Register – G.832 (Address Location= 0xN34A, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	TxBIP-8_Mask_Byte[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	TxBIP-8_Mask_Byte[7:0]	R/W	TxBIP-8 (B1) Error Mask[7:0]:
			 These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

Note: For normal opera to 0x00.



Table 386: TxE3 SSM Register – G.832 (Address Location= 0xN34B, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
TxSSM Enable	Unused			TxSSM[3:0]				
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	TxSSM Enable	R/W	Transmit SSM Enable:
			This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to operate in either the "Old ITU-T G.832 Framing" format or in the "New TU-T G.832 Framing" format, as described below.
			0 – Configures the DS3/E3 Frame Generator block to support the "Pre October 1998" version of the E3, ITU-T G.832 framing format.
			1 – Configures the DS3/E3 Frame Generator block to support the "October 1998" version of the E3, ITU-T G.832 framing format.
6 - 4	Unused	R/O	nthe mo
3 - 0	TxSSM[3:0]	R/W	Transmit Synchronization Status Message[3:0]:
			These READ/WRITE bit-fields permit the user to specify the contents of the "outbound" Synchronization Status Message (SSM) that is to be transported vai the "outbound" E3 data-stream. The Transmit SSM Controller sub-block (within the DS3/E3 Frame Generator block) will then proceed to transport this SSM via the outbound E3 data-stream. Note: These bit-fields are only active if the DS3/E3 Frame Generator block is active, and if Bit 7 (TxSSM Enable) of this register is set to "1".

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1.10.9 AIS/PDI-P ALARM ENABLE REGISTER

Table 387: Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block (Address Location= 0xN34D, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit PDI- P (Down- stream) upon LOS	Transmit AIS (Down- stream) upon LOS	Transmit PDI- P (Down- stream) upon LOF	Transmit AIS (Down- stream) upon LOF	Transmit PDI- P (Down- stream) upon AIS	Transmit AIS (Down- stream) upon AIS
R/O	D R/O R/W		R/W	R/W	R/W	R/W	R/W
0	0 0 0		0	0	0	0	

			.6 8
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 6	Unused	R/O	in the second
5	Transmit PDI-P (Down-stream)	R/W	Transmit the PDI-P indicator (Down-stream) upon declaration of the DS3/E3 LOS defect condition:
	upon LOS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOS defect is declared within the DS3/E3 Ingress Path.
			More specifically, if this configuration is implemented then the following events will occur
	the	oduct	
		%	the C2 byte (within each "down-stream" VC-3) to the "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOS feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon LOS feature.
			NOTE: The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.



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4	Transmit AIS (Down-stream)	R/W	Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOS defect condition:
	upon LOS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOS defect is declared.
			If the Primary Frame Synchronizer block declares the LOS detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle Signal Pattern Generator will transmit the AIS indicator (in the down- stream path) for the duration that the Primary Frame Synchronizer block declares the LOS defect condition.
			Once the Primary Frame Synchronizer block clears the LOS defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path)
			0 – Disables the "Transmit AIS (Down-stream) upon LOS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
3	Transmit PDI-P (Down-stream)	R/W	Transmit PDI-P indicator (Down-stream) upon declaration of the DS3/E3 LOF defect condition:
	upon LOF	or of the state	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Primary Frame Synchronizer block is operating in the "DS3/E3 ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in the Frame Generator/Frame Synchronizer Configuration # 0xE6), and if it were to declare the LOF/OOF defect condition (within the Ingress Path), then the corresponding Transmit TUG-3/AU-3 Mapper VC- 3 POH Processor block will automatically transmit the PDI-P indicator (via its STM-0 signal, within the outbound composite STM-1 signal), by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will continue to transmit the PDI-P indicator for the duration that the Primary Frame Synchronizer block declares the LOF defect condition.
			Once the Primary Frame Synchronizer block clears the LOF defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the "0x04".
			0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon LOF feature.
			NOTES:
			i. The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
			ii. For DS3 Applications, this Automatic Transmission of PDI-P will occur whenever the Primary Frame Synchronizer block declares the OOF defect condition.

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2	Transmit AIS (Down-stream)	R/W	Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOF defect condition:
	upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOF defect is declared.
			If the Primary Frame Synchronizer block declares the LOF detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle Signal Pattern Generator will transmit the AIS indicator (in the down- stream path) for the duration that the Primary Frame Synchronizer block declares the DS3/E3 LOF defect condition.
			Once the Primary Frame Synchronizer block clears the LOF/OOF defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path).
			0 – Disables the "Transmit AIS (Down-stream) upon LOF feature.
			1 – Enables the "Transmit AS (Down-stream) upon LOF feature.
1	Transmit PDI-P	R/W	Transmit PDI-P (Down stream) upon AIS:
	(Down-stream) upon AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3/E3 Ingress Path.
0	Transmit AIS	oduct and m and m	 More specifically, if this configuration is implemented then the following events will occur. If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xE6), and if it were to declare the AIS defect condition (within the Ingress Path), then the corresponding Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically transmit the PDI-P indicator, by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will continue to transmit the PDI-P indicator for the duration that the Primary Frame Synchronizer block declares the AIS defect condition. Once the Primary Frame Synchronizer block clears the AIS defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon AIS feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature. NOTE: The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
0	Transmit AIS (Down-stream) upon AIS	R/W	Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the AIS defect condition: This READ/WRITE bit-field permits the user to configure the DS3/E3
			Framer block to do all of the following, if the AIS defect is declared. If the Primary Frame Synchronizer block declares the AIS detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle



Signal Pattern Generator will transmit the AIS Indicator (in the down- stream path) for the duration that the Primary Frame Synchronizer block declares the DS3/E3 AIS defect condition.
Once the Primary Frame Synchronizer block clears the AIS defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path).
0 – Disables the "Transmit AIS (Down-stream) upon AIS feature.
1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.





Table 388: Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F2, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit PDI-P (Down- stream) upon LOS	I-P (Down- eam) upon stream) upon		Transmit AIS (Down- stream) upon LOF	Transmit PDI-P (Down- stream) upon AIS	Transmit AIS (Down- stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 6	Unused	R/O	will reo
5	Transmit PDI- P (Down- stream) upon LOS	R/W	 Transmit PDI-Pindicator (Down-stream) upon declaration of the DS3/E3 LOS defect condition: This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronzer block) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOS defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the LOS defect condition (within the Ingress Path), then the corresponding Transmit TUG-3/AU-3 Otapper VC-3 POH Processor block will automatically transmit the PDI-P indicator (via its STM-0 signal, within the outbound composite STM- Gignal) by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically transmit the PDI-P indicator for the duration that the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmistion of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". Once the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the value "0xAU". Once the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the va
4	Transmit AIS (Down-stream) upon LOS	R/W	 Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOS defect condition: This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOS defect is declared. If the Secondary Frame Synchronizer block declares the LOS defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down-stream path) for the duration that the Secondary Frame Synchronizer block declares the LOS defect condition. Once the Secondary Frame Synchronizer block clears the LOS defect condition,



1	Transmit PDI- P (Down- stream) upon	R/W	Transmit PDI-P Indicator (Down-stream) upon declaration of the DS3/E3 AIS defect condition:
	T 10001	D/M	1 – Enables the "Transmit AIS (Down-stream) upon LOF feature.
			0 – Disables the "Transmit AIS (Down-stream) upon LOF feature.
			transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path).
			Once the Secondary Frame Synchronizer block clears the LOF defect condition, then the DS3/E3 Frame Generator block will automatically terminate its
	0	and	If the Secondary Frame Synchronizer block declares the LOF defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down-stream path) for the duration that the Secondary Frame Synchronizer block declares the LOF defect condition.
	upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOF defect is declared.
2	Transmit AIS (Down-stream)	R/W	Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOF defect condition:
			NOTE: The user should only invoke this feature if the Secondary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
			Cenables this "Transmit PDI-P (Down-stream) upon LOF feature.
			Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate us transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the value "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature.
			Frame Synchronizer block declares the LOF defect condition. Once the Secondary Frame Synchronizer block clears the LOF defect, then the
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the LOF defect condition (within the Ingress Path), then the corresponding Transmit TUG-3/AU-3 Mapper VO-3 POH Processor block will automatically transmit the PDI-P indicator (via its STM-0 signal, within the outbound composite STM-1 signal) by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will continue to transmit the PDI-P indicator for the duration that the Secondary
			More specifically, if this configuration is implemented then the following events will occur.
	stream) upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronizer block) and the corresponding Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3 Ingress Path.
3	Transmit PDI- P (Down-	R/W	Transmit PDI-P Indicator (Down-stream) upon declaration of the DS3/E3 LOF defect condition:
			1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
			0 – Disables the "Transmit AIS (Down-stream) upon LOS feature.
			then the DS3/E3 Frame Generator block will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path).

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



	AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronizer block) and the corresponding Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3 Ingress Path.
			More specifically, if this configuration is implemented then the following events will occur.
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the AIS defect condition (within the Ingress Path), then the corresponding Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically transmit the PDI-P indicator (via its STM-0 signal, within the outbound composite STM-1 signal) by setting the C2 byte (within each "down-stream" VC-3) to the value "0xFC". The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will continue to transmit the PDI-P indicator for the duration that the Secondary Frame Synchronizer block declares the AIS defect condition.
			Once the Secondary Frame Synchronizer block clears the AIS defect, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" VC-3) to the value "0x04".
			0 – Disables this "Transmit PDCP (Down-stream) upon AIS feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature.
			NOTE: The user should only invoke this feature if the Secondary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
0	Transmit AIS (Down-stream)	R/W	Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the AIS defect condition:
	upon AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the AIS defect is declared.
		.0	If the Secondary Frame Synchronizer block declares the AIS defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down stream path) for the duration that the Secondary Frame Synchronizer block declares the AIS defect condition.
	×	6 32 0 22	Once the Secondary Frame Synchronizer block clears the AIS defect condition, then the DS3/E3 Frame Generator block will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path).
		2	0 – Disables the "Transmit AIS (Down-stream) upon AIS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.



1.10.10 PERFORMANCE MONITOR REGISTERS

Table 389: PMON Excessive Zero Count Registers – MSB (Address Location= 0xN34E, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	PMON_EXZ_Count_Upper_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	Performance Monitor – Excessive Zero Event Count – Upper Byte:
	product	i de le d	These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – LSB" combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. NOTE: This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.
	The product of pre-10 The data duration of the of t	io-	



Table 390: PMON Excessive Zero Count Registers – LSB (Address Location= 0xN34F, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
PMON_EXZ_Count_Lower_Byte[7:0]									
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	Performance Monitor – Excessive Zero Event Count – Lower Byte: These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – MSB" combine to reflect the cumulative number of instances that a string of three or more consecutive
		uctsh	 zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. NOTE: This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.
	The product or product are not the data drives and may not the data drives are the dat	londer porder	and hag EX2 events.



Table 391: PMON Line Code Violation Count Registers – MSB (Address Location= 0xN350, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	PMON_LCV_Count_Upper_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7 – 0	PMON LCV Count Upper Byte[7:0]	RUR	Performance Monitor- Line Code Violation Count Register – Upper Byte:				
			These RESET-upon-READ bits along with that within the "PMON Line Code Violation Count LSB" combine to reflect the cumulative number of Line Code Violations that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. NOTE: This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag LCV events.				
	*S belles						

Table 392: PMON Line Code Violation Count Registers LSB (Address Location= 0xN351, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	PMON_LCV_Count_Lower_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	N N	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	PMON LCV Count Lower Byte[7:0]	RUR	Performance Monitor- Line Code Violation Count Register – Lower Byte:
	diand		These RESET-upon-READ bits along with that within the "PMON Line Code Violation Count – MSB" combine to reflect the cumulative number of Line Code Violations that have been detected by the Primary Frame Synchronizer block, since the last read of this register.
			This register contains the Least Significant byte of this 16-bit expression.
			NOTE: This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 393: PMON Framing Bit/Byte Error Count Register – MSB (Address Location= 0xN352, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	PMON_Framing_Bit/Byte_Error_Count_Upper_Byte[7:0]									
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Upper Byte[7:0]	RUR	 Performance Monitor – Framing Bit/Byte Error Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – LSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: For DS3 applications, this register will increment for each F or M bit error detected. For E3, ITU-T G.751 applications, this register will increment for each FAS error detected. For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected. These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

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Table 394: PMON Framing Bit/Byte Error Count Register – LSB (Address Location= 0xN353, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	PMON_Framing_Bit/Byte_Error_Count_Lower_Byte[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Lower Byte[7:0]	RUR	 Performance Monitor – Framing Bit/Byte Error Count – Lower Byte: These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – MSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. Note: For DS3 applications, this register will increment for each F or M bit error detected. For E3, ITU-T G.751 applications, this register will increment for each FAS error detected. For E3, ITU-T G 832 applications, this register will increment for each FA1 or FA2 byte error detected. These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 395: PMON Parity/P-Bit Error Count Register – MSB (Address Location= 0xN354, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	PMON_Parity_Error_Count_Upper_Byte[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION				
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Upper Byte[7:0]	RUR	 Performance Monitor – P Bit/Parity Bit Error Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON P- Bit/Parity Bit Error Count Register – LSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP- 4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed. 				
	All Mo						

Table 396: PMON Parity/P-Bit Error Count Register – LSB (Address Location= 0xN355, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4 🥇	Віт 3	Віт 2	Віт 1	Віт 0				
		PMON	_Parity_Error_Co	unt_Lower_B	yte[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	8	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Lower Byte[7:0]	DRUR C	 Performance Monitor – P Bit/Parity Bit Error Count – Lower Evte: These RESET-upon-READ bits, along with that within the "PMON P-Bit/Parity Bit Error Count Register – MSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.



Table 397: PMON FEBE Event Count Register – MSB (Address Location= 0xN356, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	PMON_FEBE_Event_Count_Upper_Byte[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION				
7 - 0	PMON_FEBE Event_Count_Upper Byte[7:0]	RUR	 Performance Monitor – FEBE Event Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – LSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed. 				
	ntie mo						

Table 398: PMON FEBE Event Count Register – LSB Address Location= 0xN357, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Вп 3	Віт 2	Віт 1	Віт 0
		PMON_	_FEBE_Event	Count_Lower_E	Byte[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0 0 0	0	0	0	0
		10	the oto				

BIT NUMBER	N аме	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Lower Byte[7:0]	BUR	 Performance Monitor – FEBE Event Count – Lower Byte: These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – MSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 399: PMON CP-Bit Error Count Register – MSB (Address Location= 0xN358, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	PMON_CP-Bit_Error_Count_Upper_Byte[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Upper Byte[7:0]	RUR	Performance Monitor – CP Bit Error Count – Upper Byte:
			These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – LSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by- passed, or if the DS3/E3 Framer block has not been configured to operate in the DS3 C- Bit Parity Framing format.

Table 400: PMON CP-Bit Error Count Register – LSB (Address Location= 0xN359, where N ranges from 0x02 to 0x04)

0							
Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_CP-Bit_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	PMON_CP-Bit Error Count Lower Byter 0	RUR	Performance Monitor – CP Bit Error Count – Lower Byte:
	<u>91</u> ,		These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – MSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been by- passed, or if the DS3/E3 Framer block has not been configured to operate in the DS3 C- Bit Parity Framing Format.



Table 401: PRBS Error Count Register – MSB (Address Location= 0xN368, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	PRBS_Error_Count_Upper_Byte[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	PRBS Error_Count_Upper Byte[7:0]	RUR	PRBS Error Count – Upper Byte:
		e e e e e e e e e e e e e e e e e e e	These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – LSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by- passed, and if the PRBS Receiver has not been enabled.
		SI'	einsi

Table 402: PRBS Error Count Register – LSB (Address Location= 0xN369, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
NUC A A P							

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	PRBS Error_Count_Lower Byte[7:0]	RUR	PRBS Error Count – Lower Byte:
	The ato dri		These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – MSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed, and if the PRBS Receiver has not been enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 403: PMON Holding Register (Address Location= 0xN3, 0x6C; Address Location= 0xN36C, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	PMON_Hold_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	PMON Holding Value	R/O	PMONHoldingValue:These READ-ONLY bit-fields were specifically allocated to support READ operations to the PMON (Performance Monitor) Registers, within the DS3/E3 Framer blocks.Since the PMON Register (within the DS3/E3 Framer block) are 16- bit registers. Therefore, given that the bi-directional data bus of the XRT94L33 is only 8-bits wide, it will require two read operations in order to read out the entire 16 bit content of these registers.The other thing to note is that the PMON Registers (within the DS3/E3 Framer blocks) are RESET-upon-READ type registers. As consequence, the entire 16-bit contents of a given PMON Register will be cleared to "0x0000" immediately after the user has executed the first (of two) read operations to this register. In order to avoid losing the contents of the other byte, the contents of the "un-read" byte is automatically loaded into this register.Hence, once the user reads a register, from a given PMON Register, he/she is suppose to obtain the contents of the other byte, by reading the contents of this register.

Hence once he/she is sup the contents o



Table 404: One Second Error Status Register (Address Location= 0xN36D, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	ised			Errored Second	Severe Errored Second
R/O	R/O						
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Errored Second	R/O	Errored Second Indicator:
			This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one second accumulation period as a "Errored Second".
			The DS3/E3 Framer block will declare an "errored second" if the Primary Frame Synchronizer block detects any of the following events.
			For DS3 Applications
			P-Bit Errors
			CP Bit Errors
			Framing Bit (F or M bit) Errors
			For E3 Applications
			BIR-4/BIP-8/Errors
			FAS or Framing Byte (FA1, FA2) Errors
		, c	02 Indicates that the DS3/E3 Framer block has NOT declared the last one- second accumulation period as being an errored second.
			10 Indicates that the DS3/E3 Framer block has declared the last one- second accumulation period as being an errored second.
	, ot		Note: This bit-field is only active if the Primary Frame Synchronizer block is enabled.
0	Severely Errored	R/O	Severely Errored Second Indicator:
	Second	0 111	This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one second accumulation period as being a "Severely Errored Second".
	'ð		The DS3/E3 Framer block will declare a given second as being a "severely errored" second if it determines that the BER (Bit Error Rate) during this "one-second accumulation" period is greater than 10 ⁻³ errors/second.
			0 – Indicates that the DS3/E3 Framer block has not declared the last one- second accumulation period as being a "severely-errored" second.
			1 – Indicates that the DS3/E3 Framer block has declared the last one- second accumulation period as being a "severely-errored" second.
			Note: This bit-field is only active if the Primary Frame Synchronizer block is enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 405: One Second – LCV Count Accumulator Register – MSB (Address Location= 0xN36E, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 3 Віт 2		Віт 0
		One_S	econd_LCV_Co	ount_Accum_M	SB[7:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

7 - 0 One_Second_LCV_Count Accum_LSB[7:0] R/O One Second LCV Count Accumulator Register – MSB: These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – MSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. Note: This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Path.	BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
	7 - 0		R/O	 These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – MSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. Note: This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in

Table 406: One Second – LCV Count Accumulator Register – LSB (Address Location= 0xN36F, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	ОВіт 3	Віт 2	Віт 1	Віт 0	
		One_S	Second_LCV_C	ount_Accum_L	SB[7:0]			
R/O	R/O	R/O	R/O V	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER		Түре	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	RO	One Second LCV Count Accumulator Register – LSB: These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – LSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. Note: This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Path



Table 407: One Second – Parity Error Accumulator Register – MSB (Address Location= 0xN370, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		One_S	econd_Parity_E	rror_Accum_M	SB[7:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_MSB[7:0]	R/O	 One Second Parity Error Accumulator Register – MSB: These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – LSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. Note: For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period. For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period. For E3, ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.

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Table 408: One Second – Parity Error Accumulator Register – LSB (Address Location= 0xN371, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Or	ne_Second_P	arity_Error_Ac	cum_LSB[7:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_LSB[7:0]	R/O	 One Second Parity Error Accumulator Register – LSB: These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – MSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression Note: For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period. For E3, ITU-T G-751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period. For E3, ITU-T G-832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.

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Table 409: One Second – CP Bit Error Accumulator Register – MSB (Address Location= 0xN372, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		One_Se	econd_CP_Bit_I	Error_Accum_N	ISB[7:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
	Second_CP Bit Error Accum_MSB[7:0]	R/O	One Second CP Bit Error Accumulator Register – MSB: These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – LSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. Note: This register is inactive if the Primary Frame Synchronizer block is "by-passed" or if the DS3/E3 Framer block has not been configured to operate in the DS3, C-Bit Parity framing format.

Table 410: One Second – CP Bit Error Accumulator Register – LSB (Address Location= 0xN373, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	BIT4	BIT 3	Віт 2	Віт 1	Віт 0	
		_	econd_CP_Bit_E					
R/O	R/O	R/O	RO N	 R/O	R/O	R/O	R/O	
0	0	0 0	00	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Fror Accum_LSB[7:0]	R/O	 One Second CP Bit Error Accumulator Register – LSB: These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – MSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. Note: This register is inactive if the Primary Frame Synchronizer block is "by-passed" or if the DS3/E3 Framer block has not been configured to operate in the DS3, C-Bit Parity framing format.

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1.10.11 GENERAL PURPOSE I/O PIN CONTROL REGISTERS

Table 411: Line Interface Drive Register (Address Location= 0xN380, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Internal Remote Loop-back	Transmit Frame Pulse Disable			Unu	ised		
R/W	R/W	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	0	0

			is d
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Internal Remote Loop-	R/W	Internal Remote Loop-back Mode:
	back		This READ/WRITE bit field permits the user to configure the DS3/E3 Framer block to operate in the "Remote Loop-back" Mode.
			If the user enables this feature, then the Receive Input of the Primary Frame Synchronizer block will automatically be routed to the Transmit Output of the Frame Generator block.
			0 – Disables the Remote Loop-back Mode.
			1 – Enables the Remote Loop-back Mode.
			Note: This feature is only available if both the DS3/E3 Frame Generator and the Primary Frame Synchronizer blocks are enabled.
6	Transmit Frame Pulse Disable	RAW	
			Note: This bit-field is ignored if the Channel is configured to exchange data (with the off-chip DS3/E3/STS-1 LIU IC) via the Dual-Rail Manner.
5 - 0	Unused	R/O	



,							
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Framer Bypass	HDLC On	CRC32	Unused	HDLC LoopBack		Unused	
R/W	R/W	R/W	R/O	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Table 412: Payload HDLC Control Register (Address Location= 0xN382, where N ranges from 0x02 to 0x04)

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Framer Bypass	R/W	Framer Bypass: This READ/WRITE bit-field permits the user to bypass DS3/E3 framer. 0 – DS3/E3 framer is not bypassed. 1 – DS3/E3 framer is bypassed.
6	HDLC On	R/W	HDLC on: This READ/WRITE bit-field permits the user to either disable or enable the Payload HDLC processor. When payload HDLC processor is enabled, the payload portion of the DS3 data stream will come from this HDLC formatter which provides an external byte-wide data (TxHDLCData from pin STS1TxA_D) and a byte clock (TxHDLCClk, from pin StuffCntl) 0 – Payload HDLC processor is disabled 1 – Payload HDLC processor is enabled
5	CRC32	R/W	CRC32: This READ/WRITE bit field permits the user to select the length of FCS to be 16-bit or 32-bit. If 16-bit FCS is selected, the FCS is calculated with polynomial: $x^{16} + x^{12} + x^5 + 1$, If 32-bit FCS is selected, it is then calculated with polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ 0 - CRC16 is used 1 - CRC32 is used
4	Unused	R/0	S. A.
3	HDLC LoopBack	R/W	HDLC Loopback: This READ/WRITE bit-field permits the user to either enable or disable the HDLC loopback. 0 – TxHDLC loopback is disabled. 1 – TxHDLC loopback is enabled. Transmit HDLC processor will loopback to the receive side.
2-0	Unused	R/O	

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1.10.12 LAPD CONTROLLER BYTE COUNT REGISTERS

Table 413: TxLAPD Byte Count Register (Address Location= 0xN383, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxLAPD_MESSAGE_SIZE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	TxLAPD_MESSAGE_SIZE[7:0]	R/W	Transmit LAPD Message Size: These READ/WRITE bit-fields permit the user to specify the size of the information payload (in terms of bytes) within the very next outbound LAPD/PMDL Message, whenever Bit 7 (TxLAPD Any) within the "Transmit Tx LAPD Configuration" Register has been set to "1".
			All Mar

Table 414: RxLAPD Byte Count Register (Address Location 0xN384, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Вгт 3	Вит 2	Віт 1	Віт 0
RxLAPD_MESSAGE_SIZE[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0 👌	00	0	0	0
	lot to do						

BIT NUMBER		DESCRIPTION
7 – 0	RxLAPD_MESSAGE_SIZE[7:0]	Receive LAPD Message Size:
	the ta may	These READ-ONLY bit-fields indicate the size of the most recently received LAPD/PMDL Message, whenever Bit 7 (RxLAPD Any) within the "Rx LAPD Control" Register; has been set to "1".
	1 do no	The contents of these register bits, reflects the Received LAPD Message size, in terms of bytes.



 Table 415: Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer (Address Location= 0xN3F0, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Primary Frame - Clock Output Invert	Primary Frame – Transmit AIS Enable	Secondary Frame – Single-Rail Input	Primary Frame - Dual- Rail Output	Primary Frame – Idle Pattern Insert
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	Unused	R/O	will reo
4	Primary Frame –	R/W	Primary Frame Synchronizer Clock Output Invert:
	Clock Output Invert		The exact function of this bit field depends upon whether the Primary Frame Synchronizer Block has been configured to operate in Ingress or Egress Direction, as described below.
			If the Primary Frame Synchronizer Block has been configured to operate in the Egress Direction
			This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to update the "TxDS3POS_n/TxDS3NEG_n" output pins upon either the rising or falling edge of "TxDS3LineClk_n.
			0 – "TxDS3POS_n/TxDS3NEG_n is updated upon the rising edge of "TxDS3LineClk_n" The user should insure that the LIU IC will sample the "TxDS3POS_n/TxDS3NEG_n" input pins upon the falling edge of "TxDS3LincClk_n"
			1 – "TxDS3POS_n/TxDS3NEG_n" is updated upon the falling edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the "TxDS3POS_n/TxDS3NEG_n" input pins upon the rising edge of "TxDS3LineClk_n".
	a lor		If the Primary Frame Synchronizer Block has been configured to operate in the Ingress Direction:
	The prof	id ma	This READ/WRITE bit-field permis the user to configure the Primary Frame Synchronizer block to update the "Ingress Direction" DS3/E3 data-stream (which is being routed to the DS3/E3 Mapper block) upon either the rising or falling edge of the Recovered Line (Ingress Direction) DS3/E3 Clock signal (from the LIU IC).
			0 – "Ingress Direction DS3/E3 Data" is updated upon the rising edge of the "Recovered" Clock Signal.
			1 – "Ingress Direction DS3/E3 Data" is updated upon the falling edge of the "Recovered" Clock Signal.
			NOTE: If the Primary Frame Synchronizer block is configured to operate in the Ingress Direction, then we recommend that the user set this register bit to "1". This setting will insure that the DS3/E3 Mapper block will be able to sample the Ingress Direction DS3/E3 data-stream with proper set-up and hold times.
3	Primary Frame –	R/W	Primary Frame Synchronizer Block – Transmit AIS Enable:
	Transmit AIS Enable		This READ/WRITE bit-field permits the user to configure the AIS/DS3 Idle Pattern Generator, within the Primary Frame Synchronizer block to transmit the DS3/E3 AIS indicator to the remote terminal equipment (per Software

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			Command).
			If the user commands the "AIS/DS3 Idle Signal Pattern Generator", to generate and transmit the DS3/E3 AIS pattern, then the data, that is output via the Primary Frame Synchronizer block, will be overwritten with this DS3/E3 AIS Pattern.
			0 –Disables the "AIS/DS3 Idle Signal Pattern Generator" within the Primary Frame Synchronizer block. In this setting, normal traffic will pass through the Primary Frame Synchronizer block
			1 – Configures the "AIS/DS3 Idle Signal Pattern Generator" (within the Primary Frame Synchronizer block) to generate and transmit the DS3/E3 AIS indicator.
2	Secondary Frame – Single-Rail Input	R/W	Secondary Frame Synchronizer Block –Single-Rail/Dual Rail Input Select:
			This READ/WRITE bit-field permits the user to configure the Secondary Frame Synchronizer block to accept data via either the "Single-Rail" or "Dual-Rail" manner.
			0 – Configures the Secondary Frame Synchronizer block to accept data via the "Dual-Rail" Mode.
			1 – Configures the Secondary Frame Synchronizer block to accept data via the "Single-Rail" Mode.
			Note: This register bit is only valid if the Secondary Frame Synchronizer block has been configured to operate in the "Ingress" Direction.
1	Primary Frame –	R/W	Primary Frame Synchronizer - Dual-Rail Output:
	Dual-Rail Output		This READ/WRITE bit-field permits the user configure the Primary Frame Synchronizer block to output data (to the LIU IC) in either the Single-Rail or Dual-Rail Mannet.
			0 – Configures the Primary Frame Synchronizer block to output data (to the LIU IO) in a Single-Rail Manner.
			Configures the Primary Frame Synchronizer block to output data (to the
		du	Note: This register bit is only valid if the Primary Frame Synchronizer block has been configured to operate in the "Egress" Direction.
0	Primary Frame –	R/O	Primary Frame Synchronizer Block – DS3 Idle Pattern Insert:
	Idle Pattern Insert	atano	This READ/WRITE bit-field permits the user to configure the AIS/DS3 Idle Signal Pattern Generator, within the Primary Frame Synchronizer block to transmit the DS3 Idle signal to the remote terminal equipment (per Software Command).
			If the user commands the "AIS/DS3 Idle Signal Pattern Generator" to generate and transmit the DS3 Idle Signal pattern, then the data, that is output via the Primary Frame Synchronizer block, will be overwritten with the DS3 Idle Signal Pattern.
			0 –Disables the "AIS/DS3 Idle Signal Pattern Generator" within the Primary Frame Synchronizer block. In this setting, normal traffic will pass through the Primary Frame Synchronizer block
			1 – Configures the "AIS/DS3 Idle Signal Pattern Generator" (within the Primary Frame Synchronizer block) to generate and transmit the DS3 Idle Signal.



Table 416: Receive DS3/E3 Status Register – Secondary Frame Synchronizer (Address Location= 0xN3F1, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Secondary Frame Synchronizer - DS3/E3 AIS Defect Declared	Secondary Frame Synchronizer – DS3/E3 LOS Defect Declared	Secondary Frame Synchronizer – DS3 Idle Pattern Detected	Secondary Frame Synchronizer – LOF/OOF Defect Declared	Unused			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	1	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Secondary Frame Synchronizer – DS3/E3 AIS Defect Declared	R/O	 DS3/E3 AIS Defect Declared – Secondary Frame Synchronizer Block: This READ-ONY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the AIS defect condition in its incoming path, as described below. 0 – Indicates that the Secondary Frame Synchronizer block is NOT declaring the DS3/E3 AIS defect condition. 1 – Indicates that the Secondary Frame Synchronizer block is currently declaring the AIS defect condition.
6	Secondary Frame Synchronizer – LOS Defect Declared	R/O	 DS3/E3 LOS Defect Declared – Secondary Frame Synchronizer Block: This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the LOS defect condition as described below. Indicates that the Secondary Frame Synchronizer block is NOT declaring the LOS defect condition in its incoming path. I – Indicates that the Secondary Frame Synchronizer block is currently declaring the LOS defect is incoming path.
5	Secondary Frame Synchronizer – DS3 Idle Pattern Detected	Rock	 DS3 Idle Signal Pattern Detected – Secondary Frame Synchronizer Block: This READ-ONY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern, within its incoming Receive Path. 0 – Indicates that the Secondary Frame Synchronizer block is NOT detecting the DS3 Idle Pattern, in its incoming path. 1 – Indicates that the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern in its incoming path. Note: This bit-field is only valid if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.
4	Secondary Frame Synchronizer – OOF Defect Declared	R/O	 OOF/LOF Defect Declared – Secondary Frame Synchronizer Block: This READ-ONLY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the OOF/LOF defect condition, as described below. 0 – Indicates that the Secondary Frame Synchronizer block is NOT declaring the OOF/LOF defect condition. 1 – Indicates that the Secondary Frame Synchronizer block is currently declaring the OOF/LOF defect condition.

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3 – 0	Unused	R/O		
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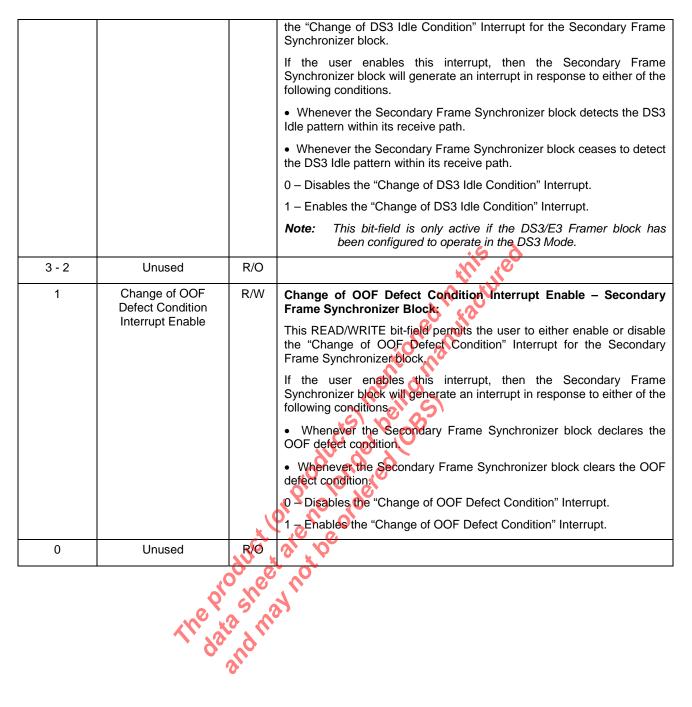


Table 417: Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F8, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change of LOS Defect Condition Interrupt Enable	Change of AIS Defect Condition Interrupt Enable	Change of DS3 Idle Condition Interrupt Enable	Unused		Change of OOF Defect Condition Interrupt Enable	Unused
R/O	R/W	R/W	R/W	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	ΤΥΡΕ	DESCRIPTION
7	Unused	R/O	*his rec
6	Change of LOS Defect Condition Interrupt Enable	R/W	 Change of LOS Defect Condition Interrupt Enable – Secondary Frame Synchronizer Block: This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOS (Loss of Signal) Defect Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. Whenever the Secondary Frame Synchronizer block declares the LOS defect condition. Whenever the Secondary Frame Synchronizer block clears the LOS defect condition. Disables the "Change of LOS Defect Condition" Interrupt. I = Enables the "Change of LOS Defect Condition" Interrupt. NOTE: This configuration setting only applies to the Secondary Frame Synchronizer block. This configuration setting does not apply to the Primary Frame Synchronizer block.
5	Change of AIS Defect Condition Interrupt Enable	R/W	 Change of AIS Defect Condition Interrupt Enable – Secondary Frame Synchronizer Block: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Defect Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. Whenever the Secondary Frame Synchronizer block declares the AIS defect condition. Whenever the Secondary Frame Synchronizer block clears the AIS defect condition. D – Disables the "Change of AIS Defect Condition" Interrupt. 1 – Enables the "Change of AIS Defect Condition" Interrupt.
4	Change in DS3 Idle Condition Interrupt Enable	R/W	Change of DS3 Idle Condition Interrupt Enable – Secondary Frame Synchronizer Block: This READ/WRITE bit-field permits the user to either enable or disable

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Table 418: Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F9, where N ranges from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change of LOS Defect Condition Interrupt Status	Change of AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Unused		Change of OOF Defect Condition Interrupt Status	Unused
R/O	RUR	RUR	RUR	R/O	R/O	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	this too
6	Change of LOS Defect Condition Interrupt Status	RUR	Change of LOS Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:
			This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			0 – Indicates that the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
		.o	Indicates that the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
	Change of AIS Defect	aren	Note: The user can determine the current state of "LOS Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 6 (Secondary Frame Synchronizer – LOS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
5	Change of AIS Defect Condition Interrupt Status	RUR	Change of AIS Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:
	The atom m		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			0 – Indicates that the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			Note: The user can determine the current state of "AIS Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 7 (Secondary Frame Synchronizer – AIS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).

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4	Change of DS3 Idle Condition Interrupt Status	RUR	Change of DS3 Idle Condition Interrupt Status – Secondary Frame Synchronizer Block:
			This RESET-upon-READ bit-field indicates whether or not the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			0 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			Note: The user can determine the current "DS3 Idle" state (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 5 (Secondary Frame Synchronizer – DS3 Idle Pattern Detected) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
3 - 2	Unused	R/O	ne ulio
1	Change of OOF Defect Condition Interrupt Status	RUR	Change of OOF Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:
			This RESET upon READ bit-field indicates whether or not the "Change of OOF Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			0 - Indicates that the "Change of OOF Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
		lor	1 Indicates that the "Change of OOF Defect Condition" Interrupt per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
	Unused Unused	eet n	Note: The user can determine the current state of "OOF Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 4 (Secondary Frame Synchronizer – OOF Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
0	Unused	R/O	

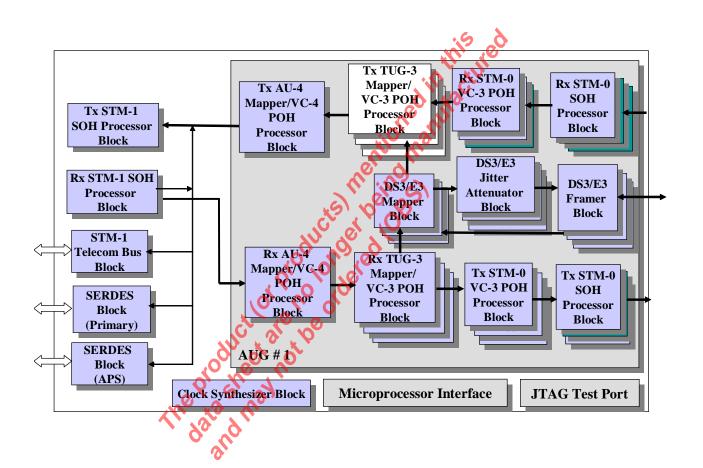


1.11 TRANSMIT TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK

The register map for the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block "highlighted" is presented below in Figure 8.

Figure 8: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block "High-lighted".



1.11.1 TRANSMIT TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK REGISTER

Table 419: Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block Register - Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0xN800 – 0xN981	Reserved	0x00
0xN982	Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN8992	Reserved	0x00
0xN993	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0×N996	Transmit TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Control Register	0x00
0×N997	Transmit TUG-3/AU-3 Mapper VC-3 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit TUG-3/AU-3 Mapper VC 3 Path Transmit C2 Byte Value Register	0x00
0xN99C - 0xN99E	Reserved	0x00
0xN99F	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit G1 Byte Value Register	0x00
0xN9A0 - 0xN9A2	Reserved	0x00
0xN9A3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit TOG-3/AU-3 Mapper VC-3 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 - 0xN9B2	Reserved	0x00
0xN9B3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control Register – Byte 0	0x00





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Address Location	REGISTER NAME	DEFAULT VALUES
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit J1 Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 - 0xN9C2	Reserved	0x00
0xN9C3	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 - 0xN9C5	Reserved	0x00
0xN9C6	Transmit TUG-3/AU-3 Mapper VC-3 Path - Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit TUG-3/AU-3 Mapper VC-3 Path - Fransmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit TUG-3/AU-3 Mapper VC-3 Path – RDI-P Control Register – Byte	0x40
0xN9CA	Transmit TUG-3/AU-3 Mapper VC-3 Path- RDI-P Control Register – Byte	0xC0
0xN9CB	Transmit TUG-3/AU-3 Mapper VC-3 Path – RDI-P Control Register – Byte	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 – 0xN9FF	Reserved	0x00

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



1.11.2 TRANSMIT TUG-3/AU-3 MAPPER VC-3 POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 420: Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 1 (Address Location= 0xN982, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 4	Unused	R/O	this ed
3	Z5 Byte Insertion Type	R/W	 Z5 Byte Insertion Type: This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to use either the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z5 Byte Value" Register or the TPOH input on as the source for the Z5 byte, in the outbound VC-3 data-stream, as described below. 0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 PAH – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound VC-3. 1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z5 byte position within each outbound VC-3. NOTE: The Address Location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor Block – Transmit Z5 Byte Value Register is 0xN9B3.
2	Z4 Byte Insertion Type	R/W	 24 Byte Insertion Type: This READ/WRITE bit-field permits the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use either the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z4 Byte Value" Register or the TPOH input pin as the source for the Z4 byte, in the outbound VC-3 data-stream, as described below. 0 - Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z4 byte position within each outbound VC-3. NOTE: The address location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block – Transmit Z4 Byte Value Register is 0xN9AF.
1	Z3 Byte Insertion Type	R/W	Z3 Byte Insertion Type: This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to use either the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z3 Byte Value" Register or the TPOH input pin as the source for the Z3 byte, in the outbound VC-3 data-stream, as described below.
			0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path –



			Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound VC-3.		
			1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z3 byte position within each outbound VC-3.		
			NOTE: The Address Location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block – Transmit Z3 Byte Value Register is 0xN9AB.		
0	0 H4 Byte Insertion R/W		H4 Byte Insertion Type:		
	Туре	This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to use either the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit H4 Byte Value" Register or the TPOH input pin as the source for the H4 byte, in the outbound VC-3 data-stream, as described below.			
		 0 - Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound VC-3. 1 - Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound VC-3. 			
		NOTE: The Address Location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processro block – Transmit H4 Byte Value Register is 0xN9A7.			

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Table 421: Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0 (Address Location= 0xN983, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F2 Byte Insertion Type		REI Insertion [1:0]		nsertion 9[1:0]	C2 Byte Insertion Type	C2 Byte Auto Insert Mode Enable	Force Transmission of AU-AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION		
7	F2 Byte Insertion	R/W	F2 Byte Insertion Type:		
	Туре		This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to use either the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit F2 Byte Value" Register or the TPOH input pin as the source for the F2 byte, in the outbound VC-3 data-stream, as described below.		
			0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to insert the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit F2 Byte Value" Register into the F2 Byte position within each outbound VC-3.		
			1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound VC-3.		
			NOTE: The Address Location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block – Transmit F2 Byte Value Register is 0xN9A3.		
6 - 5	HP-REI/LP-REI	R/W	HP-REI/LP-RELInsertion Type[1:0]:		
	Insertion Type[1:0]	negrod	he sta	Type[1:0] These two READ TUG-3/AU 3 Mar following sources	These two READ/WRITE bit-fields permit the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use one of the three following sources for the HP-REI/LP-REI bit-fields (e.g., bits 1 through 4, within the G1 byte of the outbound VC-3).
	The			• From the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (e g., the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will set the HP-REI/LP-REI bit-fields to the appropriate value, based upon the number B3 byte errors that the corresponding Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block detects and flags, within its incoming VC-3 data-stream).	
		- S	• From the "Transmit G1 Byte Value" Register. In this case, the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block – Transmit G1 Byte Value" Register into the HP-REI/LP-REI bit-fields within each outbound VC-3.		
			• From the "TPOH" input pin. In this case, the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the HP-REI/LP-REI bit-fields within each outbound VC-3.		
			00/11 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the corresponding Receive TUG- 3/AU-3 Mapper VC-3 POH Processor block detects and flags within the incoming STM-0 data-stream.		
			01 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based		



			upon the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH
			Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor
			block to accept externally supplied data (via the TPOH input port) and to insert this data into the HP-REI/LP-REI bit-positions within each outbound VC-3.
			NOTE: The Address location of the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block – Transmit G1 Byte Value Register is 0xN99F.
4 - 3	RDI-P Insertion	R/W	RDI-P Insertion Type[1:0]:
	Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte of the outbound VC-3).
			• From the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (e.g., when it detects various defect conditions within its incoming SPE data).
			 From the "Transmit G1 Byte Value" Register (Address Location= 0xN99F).
			From the "TPOH" input pn.
			00/11 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) to the appropriate value coincident to whenever the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares any defect conditions" within the incoming STM-0 data-stream.
			01 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit G1 Byte Value" register.
			10 - Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use the TPOH input pin as the source of Bits 5 through 7 (in the G1 byte of the outbound SPE).
2	C2 Byte Insertion	R/W	C2 Insertion Type:
	Туре	ducte	This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to use either the "Transmit TUG- 3/AU-3 Mapper VC-3 Path – Transmit C2 Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound VC-3 data-stream.
	Theat	0 <u>7</u> 7	Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit C2 Value" Register (Address Location= 0xN99B).
		2	1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to use the "TPOH" input as the source for the C2 byte, in the outbound VC-3.
1	Auto-Insert	R/W	Auto-Insert PDI-P Indicator Enable:
	PDI-P Indicator Enable		This READ/WRITE bit-field permit the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the PDI- P (Path - Payload Defect Indicator) whenever the DS3/E3 Framer block declares an LOS, OOF or AIS condition.
			If this feature is enabled, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will automatically set the C2 byte (within the outbound SPE) to 0xFC (to indicate a PDI-P condition) whenever the DS3/E3 Framer block declares the LOS, OOF or AIS condition.
			0 – Disables the "Auto-Insert PDI-P" feature.
			1 – Enables the "Auto-Insert PDI-P" feature.
			NOTE: This bit-field is only value if the DS3/E3 Framer block (within the



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

			corresponding Channel) has been enabled.
0	Transmit AU-AIS	R/W	Transmit AU-AIS Enable:
	Enable	Enable	This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to (via software control) transmit an AU-AIS indicator to the remote PTE.
		If this feature is enabled, then the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will unconditionally set the H1, H2, H3 and all the SPE bytes to an "All Ones" pattern, prior to routing this data to the Transmit STM-1 SOH Processor block.	
		0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT transmit the AU-AIS indicator to the remote PTE.	
		1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to transmit the AU-AIS indicator to the remote PTE.	
			NOTE: For normal operation, the user should set this bit-field to "0".

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Table 422: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmitter J1 Byte Value Register (Address Location= 0xN993, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	Transmit J1 Byte Value[7:0]	R/W	Transmit J1 Byte Value:These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound VC-3.If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location,

Adapter VC-3 Path - TUS Control Register" register (Add



Table 423: Transmit TUG-3/AU-3 Mapper VC-3 Path - B3 Byte Control Register (Address Location = 0xN996, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unused							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 1	Unused	R/O	
0	0 B3 Pass Thru Mode	R/W	B3 Pass-Thru Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to do either of the following.
			o. To operate in the "Normal" Mode.
			p. To operate in the "B3 Pass Thru" Mode.
			If in Normal Mode
			If the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor has been configured to operate in the "Normal" Mode, then it will compute and insert a new B3 byte into each outbound VC-3.
			If in the B3 Pass-Thru Mode
			If the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block has been configured to operate in the "B3 Pass-Thru" Mode, then it will NOT modify the B3 byte values within the VC-3s that it receives from its corresponding Receive STM-0 POH Processor Block.
			0 - Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to operate in the "Normal" Mode.
		, jct	1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to operate in the "B3 Pass-Thru" Mode.
		100 ne	Note: This bit-field is NOT active if the corresponding channel has been configured to operate in the DS3/E3 Mode.
	The	atad	123



Table 424: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmitter B3 Byte Error Mask Register (Address Location= 0xN997, where N ranges in value from 0x02 to 0x04)

١	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit B3 Byte Error Mask[7:0]	R/W	Decent now Transmit B3 Byte Error Mask[7:0]: This READ/WRITE bit-field permits the user to insert errors into the B3 byte, within each "outbound" VC-3, prior to transmission to the Transmit STM-1 SOH Processor block. The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte position within each "outbound" VC-3. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. Note: For normal operation, the user should set this register to 0x00.
	l		

Table 425: Transmit TUG-3/AU-3 Mapper VC-3 Path Transmit C2 Byte Value Register (Address Location= 0xN99B, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
			Transmit_C2_B	yte_Value[7:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	<u> </u>	0	0	0	0	

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 - 0	Transmit C2 Byte Value[7:0]	R/M A	 Transmit C2 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the Value of the C2 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Byte Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" register (Address Location= 0xN983).

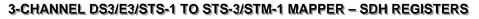




Table 426: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit G1 Byte Value Register (Address Location= 0xN99F, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit G1	R/W	Transmit G1 Byte Value:
	Byte Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the contents of the RDI-P and HP-REI/LP-REI bit-fields, within each G1 byte in the "outbound" VC-3. If the users sets "HP-REI/LP-REI_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the HP-REI/LP-REI and the RDI-P bit-fields (within each G1 byte of the "outbound" VC-3) will be dictated by the contents of this register Note: The "HP-REI/LP REI_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bit-fields are located in the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" Register (Address Location= 0xN983)

Table 427: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit F2 Byte Value Register (Address Location= 0xN9A3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4 🎸	Вп 3	Віт 2	Віт 1	Віт 0	
			Transmit	_F2_Byte_Va	lue[7:0]		I	
R/W	R/W	R/W	R/W	RW	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	
	AN A A							

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 - 0	Transmit F2 Byte Value[7:0]	RW	 Transmit F2 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" register (Address Location= 0xN983).



Table 428: Transmit TUG-3/AU-3 Mapper VC-3 Path - Transmit H4 Byte Value Register (Address Location= 0xN9A7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	R/W	 Transmit H4 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 1" register (Address Location= 0xN9A7). NOTE: This bit-field is configured if the XRT94L33 device has been configured to operate in "STM-0 POH Pass-Thru" Mode.
			ts per by

Table 429: Transmit TUG-3/AU-3 Mapper VC-3 Path OTransmit Z3 Byte Value Register (Address Location= 0xN9AB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
			Transmit_Z3_E	3yte_Value[7:0]				
R/W	R/W	R/W	R/WO	R/W	R/W	R/W	R/W	
0	0	00		0	0	0	0	
	all at at							

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Z3 Byte Value[7:0]		Transmit Z3 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).

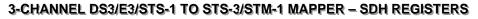




Table 430: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z4 Byte Value Register (Address Location= 0xN9AF, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit Z4 Byte Value[7:0]	R/W	Transmit Z4 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).

Table 431: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Z5 Byte Value Register (Address Location= 0xN9B3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	0 0 0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	
7 - 0	Transmit Z5 Byte Value[7:0]	RAV PIS	 Transmit Z5 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound VC-3. If the user configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" VC-3. This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).



Table 432: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control Register (Address Location= 0xN9B7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	Pointer Force:
			This READ/WRITE bit-field permits the user to load the values contained within the "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H1 Pointer" and "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3) into the H1 and H2 bytes (within the outbound STM-0 data stream).
			Note: The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition.
			0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to transmit STM-0/STM-1 data with normal and correct H1 and H2 bytes.
		(1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STM-0/STM-1 data-stream) with the values in the "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H1 and H2 Pointer" registers.
4	Check Stuff	R/W	Check Stuff Monitoring:
	thepr	asheet	This BEAD/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods.
	, 9.0	20	0 – Disables this feature.
	•	9.	In this mode, the Transmit TUG-3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods.
			1 – Enables this feature.
			In this mode, the Transmit TUG-3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.
3	Insert Negative	R/W	Insert Negative Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to insert a negative-stuff into the outbound STM-0/STM-1 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote

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			terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STM-0/STM-1 data stream).
			• The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on.
			Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2	Insert Positive	R/W	Insert Positive Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to insert a positive-stuff into the outbound STM-0/STM-1 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STM-0/STM-1 data stream, immediately after the H3 byte position within the outbound STM-0/STM-1 data stream).
			• The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on.
			Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
1	Insert	R/W	Insert Continuous NDF Events:
	Continuous NDF Events	Pro S	This READ/WRITE bit-field permits the user configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STM-0/STM-1 data stream.
		93 no	Note: As the Transmit TUG-3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks insert the NDF event into the STM-0/STM-1 data stream, it will proceed to load in the contents of the "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H1 Pointer" and "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STM-0/STM-1 data stream).
			0 – Configures the "Transmit SONET SOH and Transmit STM-1 POH Processor" blocks to not continuously insert NDF events into the "outbound" STM-0/STM-1 data stream.
			1- Configures the "Transmit SONET SOH and Transmit STM-1 POH Processor" blocks to continuously insert NDF events into the "outbound" STM-0/STM-1 data stream.
0	Insert Single	R/W	Insert Single NDF Event:
	NDF Event		This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH and Transmit STM-1 SOH Processor blocks to



insert a New Data Flag (NDF) pointer adjustment into the outbound STM- 0/STM-1 data stream.
Writing a "0" to "1" transition into this bit-field causes the following to happen.
• The "N" bits, within the H1 byte will set to the value "1001"
• The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit TUG-3/AU-3 Mapper VC-3 POH – Arbitrary H1 Pointer" and "Transmit TUG-3/AU-3 Mapper VC-3 POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3).
• Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on.
Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".

, a "1", , this bit-field , et this bit-field ,

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Table 433: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Trace Message Control Register (Address Location= 0xN9BB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			Transmit Path Trace Message_Length[1:0]		Transmit Path Tarce Message Source[1:0]		
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION	
7 – 4	Unused	R/O			
3 - 2	Transmit Path Trace R/W Transmit Path Trace Message Length[1:0]: Message_Length [1:0] These READ/WRITE bit-fields permit the user to specify the len Path Trace Message, that the Transmit TUG-3/AU-3 Mapper V Processor block will repeatedly transmit to the remote PT relationship between the content of these bit-fields and the correct Path Trace Message Length is presented below.				
			Transmit Path Trace Message Length	Resulting Path Trace Message Length (in terms of bytes)	
			00	1 Byte	
			01	16 Bytes	
			10/21	64 Bytes	
	Trace Message Source[1:0]		"outbound" Path T channer within the c Transmit Path Trace Message	E bit-fields permit the user to specify the so race Message that will be transported via outbound VC-3 data-stream as depicted below Resulting Source of the Path Trace Mess Fixed Value: The Transmit TUG-3/AU-3 Mapper VC-3	the J1 byte w. sage
		93.49		Processor block will automatically set th byte, within each outbound VC-3 to the "0x00"	ie J1
			01	The Transmit Path Trace Message Buffer The Transmit TUG-3/AU-3 Mapper VC-3 Processor block will read out the contents of the Transmit Path Trace Message Buffer, will transmit this message to the remote PTE The Transmit TUG-3/AU-3 Mapper VC-3 Processor block – Transmit Path Trace Mess Buffer Memory is located at Address Loca 0xND00 through 0xND3F (where N range value from 0x02 to 0x04)	POH within , and E. POH ssage ations
			10	From the "Transmit J1 Byte Value[Register:	7:0]"



	In this setting, the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will read out the contents of the Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit J1 Byte Value Register, and will insert this value into the J1 byte-position within each outbound VC-3.
11	From the "TxPOH" Input pin:
	In this configuration setting, the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block will externally accept the contents of the "Path Trace Message" via the "TxPOH Input Port" and it will transport this message (via the J1 Byte-Channel) to the remote PTE.

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Table 434: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H1 Byte Pointer Register (Address Location= 0xN9BF, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	NDF Bits			SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 4	NDF Bits	R/W	NDF (New Data Flag) Bits:
			These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control" Register (Address Location= 0xN9B7).
3 - 2	SS Bits	R/W	SS Bits
			These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control" Register (Address Location= 0xN9B7). Note: For SONETApplications, the "SS" bits have no functional value, within the H1 byte.
1 - 0	H1 Pointer	R/W	H1 Pointer Value[1:0]:
	Value[1:0]		These two READ/WRITE bit-fields, along with the constants of the "Transmit TOG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H2 Byte Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the Pointer Word.
		Ċ	These two READ/WRITE bit-fields permits the user to define the value of the two most significant bits within the Pointer word.
		rodue	Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control" Register (Address Location= 0xN9B7), the values of these two bits will be toaded into the two most significant bits within the Pointer Word.
	100	and	



Table 435: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H2 Byte Pointer Register (Address Location= 0xN9C3, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
H2 Pointer Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	H2 Pointer Value[7:0]	R/W	H2 Pointer Value[1:0]:
			These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Arbitrary H1 Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the 10-bit Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Path Control" Register (Address Location= 0xN9B7), the values of these eight bits will be loaded into the H2 byte, within the outbound STM-0/STM-1 data stream.

Table 436: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Current Pointer Byte Register – Byte 1 (Address Location= 0xN9C6, where N ranges in value from 0x02 to 0x04)

Ø

Віт 7	Віт 6	Віт 5	BIT 4	Віт З	Віт 2	Віт 1	Віт 0			
	Unused Q X X X Tx_Pointer_High[1:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0		0	0	1	0			

BIT NUMBER		DESCRIPTION
7 – 2	Unused R/Q	
1 - 0	Tx_Pointer_High[1:0]	Transmit Pointer Word – High[1:0]: These two READ-ONLY bits, along with the contents of the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Current Pointer Byte Register – Byte 0" (Address Location= 0xN9C7) reflect the current value of the pointer (or offset of the VC-3 within the outbound STM-0 frame).
		These two bits contain the two most significant bits within the "10-bit pointer" word.

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Table 437: Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0xN9C7, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Tx_Pointer_Low[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	1	0	1	0		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	Tx_Pointer_Low[7:0]	R/O	Transmit Pointer Word – Low[7:0]:
			These two READ-ONLY bits, along with the contents of the "Transmit TUG-3/AU-3 Mapper VC-3 Path – Transmit Current Pointer Byte Register – Byte 1" (Address Location= 0xN9C6) reflect the current value of the pointer (or offset of the VC3 within the outbound STM-0 frame). These two bits contain the eight least significant bits within the "10-bit pointer" word.

enter word.



Table 438: Transmit TUG-3/AU-3 Mapper VC-3 Path – RDI-P Control Register – Byte 2 (Address Location= 0xN9C9, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Ur	nused		PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 5	Unused	R/O	
3 - 1	PLM-P RDI-P Code[2:0]	R/W	 PLM-P (Path – Payload Mismatch) Defect – RDI-P Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the each "outbound" VC-3), whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects and declares the PLM-P defect condition. Note: In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon PLM-P) within this register to "1".
0	Transmit RDI-P upon PLM-P	R/W	 Transmit the RDI-P Indicator upon declaration of the PLM-P defect condition: This READWRITE bit-field permits the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition. 0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition. 0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition. 1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition. NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition. NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit the RDI-P indicator (in response to the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the PLM-P defect condition.



Table 439: Transmit TUG-3/AU-3 Mapper VC-3 Path – RDI-P Control Register – Byte 1 (Address Location= 0xN9CA, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P RDI-P Code[2:0]		Transmit RDI-P upon TIM-P	UNEQ-P RDI-P Code[2:0]			Transmit RDI-P upon UNEQ-P	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	TIM-P RDI-P	R/W	TIM-P (Path – Trace Identification Mismatch) Defect – RDI-P Code:
	Code[2:0]		 These three READ/WRITE bit-fields permit the user to specify the value that the Transmit TUG-3/AU-3 Mapper VC 3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" VC-3), whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects and declares the TIM-P defect condition. Note: In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon TIM-P) within this register to "1".
4	Transmit RDI-P upon TIM-P	R/W	Transmit the RDI-P indicator upon declaration of the TIM-P defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI- P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition 0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processro block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH
		X	Processor block declares the TIM-P defect condition.
	we	PIO	1 Contigures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the TIM-P defect condition.
		931	NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit the RDI-P indicator (in response to the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declaring the TIM-P defect condition) by setting the RDI-P bit-fields (within each outbound VC-3) to the contents within the "TIM-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	UNEQ-P RDI-P	R/W	UNEQ-P (Path – Unequipped) Defect – RDI-P Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" VC-3), whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects and declares the UNEQ-P defect condition.
			Note: In order to enable this feature, the user must set Bit 0 (Transmit RDI- P upon UNEQ-P) within this register to "1".
0	Transmit RDI-P upon UNEQ-P	R/W	Transmit the RDI-P Indicator upon declaration of the UNEQ-P defect condition:



This READ/WRITE bit-field permits the user to configure the Transmit TUG- 3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI- P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.
0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.
1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the UNEQ-P defect condition.
NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit the RDI-P indicator (in response to the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declaring the UNEQ-P defect condition) by setting the RDI-P bit-fields (within each outbound VC-3) to the contents within the "UNEQ-P RDI-P Code[2:0]" bit-fields within this register.

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Table 440: Transmit TUG-3/AU-3 Mapper VC-3 Path – RDI-P Control Register – Byte 0 (Address Location= 0xN9CB, where N ranges in value from 0x02 to 0x04)

Віт 7	Віт 6	Віт 5	BIT 4 BIT 3 BIT 2 BIT 1		Віт 0		
AU-LOP/TU-LOP RDI-P Code[2:0]			Transmit RDI-P upon AU- LOP/TU-LOP	AU-AIS/TU-AIS RDI-P Code[2:0]			Transmit RDI-P upon AU-AIS/ TU-AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	AU-LOP/TU-LOP RDI-P Code[2:0]	R/W	 AU-LOP/TU-LOP (Path – Loss of Pointer) Defect – RDI-P Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" VC-3), whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects and declares the AU-LOP/TU-LOP defect condition. Note: In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon AU-LOP/TU-LOP) within this register to "1"
4	Transmit RDI-P upon AU-LOP/TU-LOP	R/W	 Transmit the RDI-P Indicator upon declaration of the AU-LOP/TU-LOP defect condition: This READ/WRITE bit-field permits the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition. O – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition. 1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-LOP/TU-LOP defect condition. NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit the RDI-P indicator (in response to the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declaring the AU-LOP/TU-LOP defect condition) by setting the RDI-P bit-fields (within each outbound VC-3) to the contents within the "AU-LOP/TU-LOP RDI-P Code[2:0]" bit-fields within this register.
3 - 1	AU-AIS RDI-P Code[2:0]	R/W	AU-AIS (Path – AIS) Defect – RDI-P Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" VC-3), whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block detects and declares the AU-AIS defect condition. Note: In order to enable this feature, the user must set Bit 0



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			(Transmit RDI-P upon AU-AIS) within this register to "1".
0	Transmit RDI-P upon AU-AIS	R/W	Transmit the RDI-P Indicator upon declaration of the AU-AIS defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-AIS defect condition.
			 0 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to NOT automatically transmit the RDI-P Indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU- AIS defect condition. 1 – Configures the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declares the AU-
			AIS defect condition. NOTE: The Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will transmit the RDI-P indicator (in response to the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block declaring the AU- AIS defect condition) by setting the RDI-P bit-field (within each outbound VC-3) to the contents within the "AU-AIS RDI-P Code[2:0]" bit-fields within this register.

AIS defect cont outbound VC 3) t bit-fields within th

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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 441: Transmit TUG-3/AU-3 Mapper VC-3 Path – Serial Port Control Register (Address Location= 0xN9CF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused			TxP	OH Clock Speed	[4:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxPOH_CLOCK_S	R/W	TxPOHClk Output Clock Signal Speed:
	PEED[7:0]		These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHCIk output clock signal.
			The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below.
			FREQ = 19.44 /[2 * (TxPOH_CLOCK_SPEED + 1)
			Note: For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz

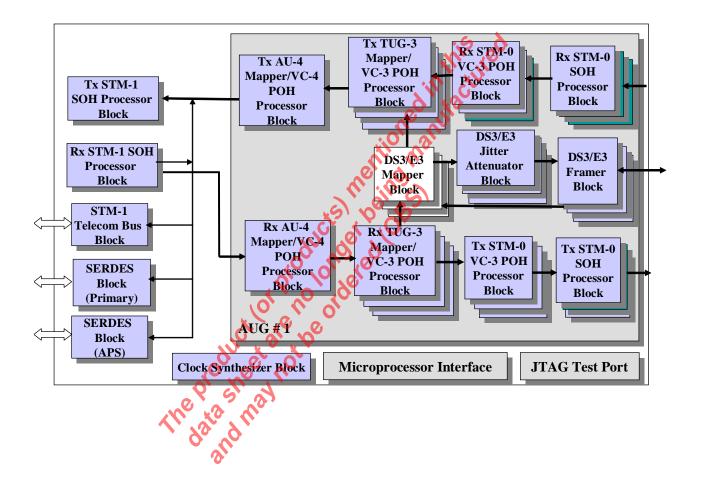


1.12 DS3/E3 MAPPER BLOCK CONTROL BLOCK

The register map for the DS3/E3 Mapper Block is presented in the Table below. Additionally, a detailed description of each of the "DS3/E3 Mapper" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "DS3/E3 Mapper" Block "highlighted" is presented below in Figure 9

Figure 9: Illustration of the Functional Block Diagram of the XRT94L33, with the DS3/E3 Mapper Block "High-lighted".





1.12.1 DS3/E3 MAPPER BLOCK CONTROL REGISTERS

Table 442: DS3/E3 Mapper Block – Register Address Map

Address Location	REGISTER NAME	DEFAULT VALUE
0xNA00 – 0xNB00	Unused	0x00
0xNB01	Mapper Control Register – Byte 2	0x00
0xNB02	Mapper Control Register – Byte 1	0x03
0xNB03	Mapper Control Register – Byte 0	0x80
0xNB04, 0xNB05	Unused	0x00
0xNB06	Receive Mapper Status Register – Byte 1	0x03
0xNB07	Receive Mapper Status Register – Byte 0	0x00
0xNB08 – 0xNB0A	Unused	0x00
0xNB0B	Receive Mapper Interrupt Status Register – Byte	0x00
0xNB0C – 0xNB0E	Unused	0x00
0xNB0F	Receive Mapper Interrupt Enable Register Byte 0	0x00
0xNB10 – 0xNB12	Unused	0x00
0xNB13	T3/E3 Routing Register	0x00
0xNB14 – 0xNB16	Reserved	0x00
0xNB17	Jitter Attenuator – Clock Source Routing Register	0x00
0xNB18 – 0xNBFF	Reserved	0x00

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1.12.2 DS3/E3 MAPPER BLOCK CONTROL REGISTER DESCRIPTION

Table 443: Mapper Control Register – Byte 2 (Address Location= 0xNB01, where N ranges from 0x02
to 0x04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STM-0 POH Pass Thru	STM-0 Remote Loop-back	STM-0 Local Loop- back	STM-0 SOH Insert	Loop-Timing	STM-1 POH Pass Thru	Receive (Ingress) STM-0 Enable	Transmit (Egress) STM-0 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	STM-0 POH	R/W	STM-0 POH (Path Overhead) Pass-Thru:
	Pass Thru		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 circuitry (within this particular channel) to operate in the "STM-0 POH Pass-Thru" Mode. If the user configures the Channel to operate in the "STM-0 POH Pass-Thru" Mode, then the Transmit (or Egress Direction) STM-0 circuitry will use the "upstream" Receive TUG-3/AU-3 Mapper VC-3 POH Processor block as the source for the POH bytes within each outbound VC-3. In the "STM-0 POH Pass Thru" Mode, the Transmit STM-0 POH Processor block will be disabled and will NOT assume the responsibility for computing and inserting the POH byte values into the "POH byte-positions" within the "Transmit (or Egress Direction) VC-3s. The POH bytes (within these VC-3s) will pass from the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block to the Transmit STM-0 SOH Processor block without modification.
	The prot	ret	0 - Configures the Transmit STM-0 circuitry to NOT operate in the "STM-0 POH Pass-Thru" Mode. 1 – Configures the Transmit STM-0 circuitry to operate in the "STM-0 POH Pass-Thru" Mode.
	the to		NOTES:
	, 9 <u>,0</u> ,2	0	1. The "STM-0 POH Pass-Thru" Mode will be disabled, if the channel is configured to operate in the Loop-Timing Mode.
			2. The "STM-0 POH Pass-Thru" Mode is very useful for those applications in which the XRT94L33 device is handling STM-0 data-stream that is transporting VT-Mapped T1/E1 data-streams (in which it is imperative that the user retain the value of the H4 byte).
			3. This register bit is only active if a given channel (on the "Slow-Speed" Side of the XRT94L33 device) has been configured to operate in the STM-0 Mode. This register bit is NOT active if a given channel has been configured to operate in the DS3/E3 Mode.
6	STM-0 Remote	R/W	STM-0 Remote Loop-back Operation:
	Loop-back		This READ/WRITE bit-field permits the user to configure the Channel to operate in the Remote Loop-back Mode.
			0 – No Loop-back Mode



			A Deveta Leave head Made
			1 – Remote Loop-back Mode
			In this case, the Receive (Ingress) STM-0 signal will be looped back out into the Transmit (Egress) STM-0 signal path.
5	STM-0 Local	R/W	STM-0 Local Loop-back Operation:
	Loop-back		This READ/WRITE bit-field permits the user to configure the Channel to operate in the Local Loop-back Mode.
			0 – No Loop-back Mode.
			1 – Local Loop-back Mode
			In this case, the Transmit (Egress) STM-0 signal will be looped back into the Receive (Ingress) STM-0 signal path.
4	STM-0 SOH	R/W	STM-0 SOH (Section Overhead) Insert:
	Insert		This READ/WRITE bit-field permits the user to configure each Transmit STM-0 SOH Processor block to accept its SOH data from the "TxPOH" input pins.
			 Input pins. 0 – Disables this feature. 1 – Enables this feature.
			1 – Enables this feature.
			Note: The user must also configure the Transmit Section of a given Channel to operate in the STM-0 Mode, by setting Bit 0 (Transmit Egress STM 0 Enable) to "1".
3	Loop-Timing	R/W	Loop-Timing Mode:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 circuitry (e.g., the Transmit STM-0 POH and SOH Processor blocks) to operate in the Loop-Timing Mode. If the user opts to configure the Transmit STM-0 circuitry (within this particular channel) to operate in the loop-timing mode, then the Transmit STM-0 circuitry will use the recovered clock signal (within the corresponding Receive STM-0 SOH and POH Processor blocks) as its timing reference.
		<i>colut</i>	If the user opts to NOT configure the Transmit STM-0 circuitry into the "loop timing? mode, then the Transmit STM-0 circuitry will use a 51.84MHz clock signal (that is ultimately derived from the 155.52MHz or 19.44MHz clock signal, that is being applied to the Receive STM-1 PECL Interface or Receive STM-1 Telecom Bus Interface block) as its timing source
	e	5	0 Configures the Transmit STM-0 SOH and POH Processor blocks to operate in the "Local-Timing" Mode.
	×1.8	and	1 – Configures the Transmit STM-0 SOH and POH Processor blocks to operate in the Loop-Timing Mode
2	STM-1 POH	R/W	STM-1 POH (Path Overhead) Pass-Thru:
	Pass-Thru		This READ/WRITE bit-field permits the user to configure the Transmit STM-1 circuitry (within this particular channel) to operate in the "STM-1 POH Pass-Thru" Mode. If the user configures the Channel to operate in the "STM-1 POH Pass-Thru" Mode, then the Transmit STM-1 circuitry will use the (upstream) Receive STM-0 POH Processor block as the source for the POH bytes within each outbound VC-3. In the "STM-1 POH Pass Thru" Mode, the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block will be disabled and will NOT assume the responsibility for computing and iinserting the POH byte values into the "POH byte-positions" within these "Transmit STM-1 SOH Processor-block desitined" VC-3s. The POH bytes (within these VC-3s) will pass from the Receive STM-0 POH Processor block to the Transmit STM-1 SOH Processor block without modification.
			If the user does NOT configure the Transmit STM-1 circuitry to operate in the "STM-1 POH Pass-Thru" Mode, then the POH bytes (within these VC-



			3s) will undergo "modification" as they pass from the Receive STM-0 POH Processor block to the Transmit STM-1 SOH Processor block (via the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block).
			0 – Configures the Transmit STM-1 circuitry to NOT operate in the "STM-1 POH Pass-Thru" Mode.
			1 – Configures the Transmit STM-1 circuitry to operate in the "STM-1 POH Pass-Thru" Mode.
			NOTES:
			 The "STM-1 POH Pass-Thru" Mode is very useful for those applications in which the XRT94L33 device is handling STM-0 data-stream that is transporting VT-Mapped T1/E1 data-streams (in which it is imperative that the user retain the value of the H4 byte).
			 This register bit is only active if a given channel (on the "Slow- Speed" side of the XRT94L33 device) has been configured to operate in the STM-0 Mode. This register bit is NOT active if a given channel has been configured to operate in the DS3/E3 Mode.
1	Receive	R/W	Receive (Ingress) STM-0 Enable:
	(Ingress) STM-0 Enable		This READ/WRITE bit field permits the user to configure the Ingress path (of the channel) to operate in either the STM-0 Mode, or in the DS3/E3 Mode.
			0 – Ingress Direction of Channel will operate in the DS3/E3 Mode.
			1 – Ingress Direction of Channel will operate in the STM-0 Mode.
0	Transmit (Egress) STM-0 Enable	R/W	Transmit (Egress) STM-0 Enable: This READ/WRITE bit-field permits the user to configure the Egress path (of the channe) to operate in either the STM-0 Mode, or in the DS3/E3 Mode 0 – Egress Direction of Channel will operate in the DS3/E3 Mode – Egress Direction of Channel will operate in the STM-0 Mode.
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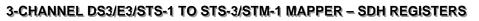




Table 444: Mapper Control Register – Byte 1 (Address Location= 0xNB02)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				STM-0 CLK_IN Invert (Ingress Direction)	STM-0 CLK_OUT Invert (Egress Direction)	DEFAULT R	DEFAULT O
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	STM-0 CLK_IN Invert (Ingress Direction)	R/W	STM-0 CLK_IN Invert (Ingress Direction): This READ/WRITE bit-field permits the user to configure the DS3/E3 Mapper Block (of Channel n), within the XRT94L33; to sample and latch the "RxDS3POS_n" input pins (pin B14. C21. AG15) upon either the rising or falling edge of "RxDS3LineClk_n" (pin D14, A24, AF14). 0 – "RxDS3POS_n" is sampled upon the falling edge of the "RxDS3LineClk_n". 1 – "RxDS3POS_n" is sampled upon the rising edge of the "RxDS3LineClk_n".
2	STM-0 CLK_OUT Invert (Egress Direction)	R/W	 STM-0 CLK_OUT Invert (Egress Direction): This READ/WRITE bit-field permits the user to configure the DS3/E3 Mapper block (of Channel n), within the XRT94L33, to update the "TxDS3POS_n" output pins (pin B18, G24, AG9) upon either the rising or falling edge of the "TxDS3LineClk_n" (pin C17, E25, AF10) 0 - "TxDS3POS_n" is updated upon the rising edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the output data upon the falling edge of the "TxDS3LineClk_n" 1 - "TxDS3POS_n" is updated upon the falling edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the output data upon the rising edge of "TxDS3LineClk_n". Note: This bit-field is only active if the DS3/E3 Mapper block has been configured to operate in the Egress Path.
1	Default R	RIV	 Default R Value: When a DS3 signal is mapped into a VC-3 there are numerous bits that are also stuffed into the STM-0 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STM-0 SPE or an SDH VC-3. One such bit is referred to as an "R" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment. This READ/WRITE bit-field permits the user to set the value for the "R" bits in the outbound STM-0 SPE or SDH VC-3. Note: The XRT94L33 includes a corresponding "READ-ONLY" register bit, in which one can obtain the value for the "R" bits in the incoming STM-0 SPE or SDH VC-3. This register bit is located in Bit 1 (Received R) within the "Receive Mapper Status Register - Byte 1(Address Location= 0xNB06).
0	Default O	R/W	Default O Value:



When a DS3 signal is mapped into a STM-0 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that are also stuffed into the STM-0 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STM-0 SPE or an SDH VC-3.
One such bit, is referred to as an "O" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.
This READ/WRITE bit-field permits the user to set the value for the "O" bits in the outbound STM-0 SPE or SDH VC-3.
Note: The XRT94L33 includes a corresponding "READ-ONLY" register bit, in which one can obtain the value for the "O" bits in the incoming STM-0 SPE or SDH VC-3. This register bit is located in Bit 0 (Received O) within the "Receive Mapper Status Register – Byte 1 (Address Location= 0xNB06).

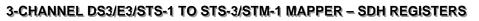




Table 445: Mapper Control Register – Byte 0 (Address Location= 0xNB03)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
JA RESET*		Սու	ised		Level 2 Monitor	Unused	Jitter Attenuator Enable
R/W	R/O	R/O	R/O	R/O	R/W	R/O	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	JA_RESET*	R/W	JA FIFO RESET:
			A "1" to "0" transition, within this bit-field commands the FIFO_READ and FIFO_WRITE pointers (within the Jitter Attenuator FIFO) to be reset to their default positions.
			Note: After the user has commanded the RESET to the Jitter Attenuator circuit, the user must set this bit-field back to "1" in order to permit proper operation.
6 - 3	Unused	R/O	tionant
2	Level 2	R/W	Level 2 Monitor Enable:
	Monitor	à	 This READ/WRITE bit field permits the user to enable the "Level 2" feature, within the DS3/E3 Mapper Block. If the user enables this feature, then the Channel will perform "Performance Monitoring" of the DS3 data, being carried by the Receive (or Ingress) STM-0 signal. The location of this monitoring will be between the Receive STM-0 SOH Processor block and the Receive STM-0 POH Processor block. This STM-0 signal will still proceed onto the "Receive STM-0 POH Processor" block, intact. 0 – Disables the Level 2 Monitor Feature. 1 – Enables the Level 2 Monitor Feature. Note: This feature is only useful if the Ingress STM-0 signal is carrying a DS3 signal. This feature would not be of any use if the STM-0 signal were carrying VT-mapped DS1 or E1 signals, for instance.
1	Unused	R/O	
0	Jitter	R/W	Jitter Attenuator Enable:
	Attenuator Enable	90.00	These two READ/WRITE bit-fields permits the user to either enable or disable the Jitter Attenuator circuit within the Mapper Block, as indicated below.
			0 – Disables the Jitter Attenuator circuit.
			1 – Enables the Jitter Attenuator circuit.



Table 446: Receive Mapper Status Register – Byte 1 (Address Location= 0xNB06)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Received_R	Received_O				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Received	R/W	Incoming "R" Value:
	R		When a DS3 signal is de-mapped from an STM-0 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STM-0 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STM-0 SPE or an SDH VC-3.
			One such bit is referred to as an "R" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.
			This READ-ONLY bit-field contains the value of the "R" bits within the most recently received STM-0 SPE of SDH VC-3.
			Note: The XRT94L33 includes a corresponding "READ/WRITE" register bit, in which one can set the value for the "R" bits, in the "outbound" STM-0 SPE or SDH VC-3. This register bit is located in Bit 1 (Default R) within the "Mapper Control Register – Byte 1" (Address Location= 0xNB02)
0	Received O	R/W	Incoming "O" Value:
			When a DS3 signal is de-mapped from an STM-0 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STM-0 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STM-0 SPE or an SDH VC-3.
		odu	One such bit is referred to as an "O" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment.
		8°, 5	This READ-ONLY bit-field contains the value of the "O" bits within the most recently received STM-0 SPE or SDH VC-3.
		931.0	Note: The XRT94L33 includes a corresponding "READ/WRITE" register bit, in which one can set the value for the "R" bits, in the "outbound" STM-0 SPE or SDH VC-3. This register bit is located in Bit 1 (Default R) within the "Mapper Control Register – Byte 1" (Address Location= 0xNB02)

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Table 447: Receive Mapper Status Register – Byte 0 (Address Location= 0xNB07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Receive STM-0 Overrun Condition	Receive STM-0 Underrun Condition	Transmit STM-0 Overrun Condition	Transmit STM-0 Underrun Condition	Receive DS3/E3 Overrun Condition	Receive DS3/E3 Underrun Condition	Transmit DS3/E3 Overrun Condition	Transmit DS3/E3 Underrun Condition
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Receive	R/O	Receive STM-0 Overrun Indicator:
	STM-0 Overrun Indicator		This READ-ONLY bit-field indicates whether opport the Channel is declaring a "Receive STM-0 Overrun" Condition.
			A "Receive STM-0 Overrun" condition will only occur if data is arriving into the Receive STM-0 POH Processor blocks at a much faster rate, than that being removed, by the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block.
			 0 – Indicates that the Channel is NOT declaring the "Receive STM-0 Overrun" condition. 1 – Indicates that the Channel is currently declaring the "Receive STM-0
			Overrun" condition.
			1. There will invariably be a timing mismatch between the clock signal driving the Receive STM-0 POH Processor block (e.g., the Recovered clock signal from the LIU IC) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.
			2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
6	Receive	R/O	Receive STM-0 Underrun Indicator:
	STM-0 Underrun Indicator	- Pro	This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive STM-0 Underrun" Condition.
		19313	A Receive STM-0 Underrun" condition will only occur if data is arriving into the Receive STM-0 POH Processor blocks at a much slower rate, than that being removed, by the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block.
		6	0 – Indicates that the Channel is NOT declaring the "Receive STM-0 Underrun" condition.
			1 – Indicates that the Channel is currently declaring the "Receive STM-0 Underrun" condition.
			Note:
			1. There will invariably be a timing mismatch between the clock signal driving the Receive STM-0 POH Processor block (e.g., the Recovered clock signal from the LIU IC) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.
			2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.



5	Transmit	R/O	Transmit STM-0 Overrun Indicator:
	STM-0 Overrun Indicator		This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit STM-0 Overrun" Condition.
	indicator		A "Transmit STM-0 Overrun" condition will only occur if data is arriving into the Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks at a much faster rate, than that being removed, by the Transmit STM-0 POH Processor block.
			0 – Indicates that the Channel is NOT declaring the "Transmit STM-0 Overrun" condition.
			1 – Indicates that the Channel is currently declaring the "Transmit STM-0 Overrun" condition.
			Note:
			1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the Transmit STM-0 POH Processor block and the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STM-1 Clock signal).
			However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode.
			2. Minor timing differences are easily handled by pointer adjustments.
			3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
4	Transmit	R/O	Transmit STM-0 Underrun Indicator:
	STM-0 Underrun Indicator		This READ ONLX bit-field indicates whether or not the Channel is declaring a "Transmit STM-0 Underrun" Condition. A "Transmit STM-0 Underrun" condition will only occur if data is arriving into the Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks at a much slower rate, than that being removed, by the Transmit STM-0 POH Processor block.
		ð	- Indicates that the Channel is NOT declaring the "Transmit STM-0 Underrun" condition
		du	- Indicates that the Channel is currently declaring the "Transmit STM-0 Underrun" condition.
		l' l'	Note:
	the	ato de	A normal system of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the Transmit STM-0 POH Processor block and the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STM-1 Clock signal).
			However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode.
			2. Minor timing differences are easily handled by pointer adjustments.
			3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
3	Receive	R/O	Receive DS3/E3 Overrun Indicator:
	DS3/E3 Overrun Indicator		This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive DS3/E3 Overrun" Condition.
			A "Receive DS3/E3 Overrun" condition will only occur if data is arriving into the DS3/E3 Framer block (in the Ingress Direction) at a much faster rate, than that being removed, by the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor



			block.
			0 – Indicates that the Channel is NOT declaring the "Receive DS3/E3 Overrun" condition.
			1 – Indicates that the Channel is currently declaring the "Receive DS3/E3 Overrun" condition.
			Note:
			1. There will invariably be a timing mismatch between the clock signal driving the Ingress Direction of the DS3/E3 Framer block (e.g., the Recovered clock signal from the LIU IC) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.
			2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
2	Receive	R/O	Receive DS3/E3 Underrun Indicator: 💦 🦿
	DS3/E3 Underrun Indicator		This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive DS3/E3 Underrun" Condition.
			A "Receive DS3/E3 Underrun" condition will only occur if data is arriving into the DS3/E3 Framer block (in the Ingress Direction) at a much slower rate, than that being removed, by the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block.
			0 – Indicates that the Channel is NOT declaring the "Receive DS3/E3 Underrun" condition.
			1 – Indicates that the Channel is currently declaring the "Receive DS3/E3 Underrun" condition.
			Note:
			1. There will invariably be a timing mismatch between the clock signal driving the Ingress Direction of the DS3/E3 Framer block (e.g., the Recovered clock signal from the LIU IC) and the Transmit TUG-3/AU-3 Mapper VC-3 POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.
		oroč	2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
1	Transmit	R/O	Transmit DS3/E3 Overrun Indicator:
	DS3/E3 Overrun Indicator	gar	This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit DS3/E3 Overrun" Condition.
		.0	A "Transmit DS3/E3 Overrun" condition will only occur if data is arriving into the Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks at a much faster rate, than that being removed, by the DS3/E3 Framer block.
			0 – Indicates that the Channel is NOT declaring the "Transmit DS3/E3 Overrun" condition.
			1 – Indicates that the Channel is currently declaring the "Transmit DS3/E3 Overrun" condition.
			Note:
			1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the DS3/E3 Framer block (in the Egress Direction) and the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STM-1 Clock signal).
			However, timing differences can exist if the Channel is configured to operate in



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			the Loop-Timing Mode.
			2. Minor timing differences are easily handled by pointer adjustments.
			3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.
0	Transmit	R/O	Transmit DS3/E3 Underrun Indicator:
	DS3/E3 Underrun Indicator		This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit DS3/E3 Underrun" Condition.
			A "Transmit DS3/E3 Underrun" condition will only occur if data is arriving into the Receive TUG-3/AU-3 Mapper VC-3 POH Processor blocks at a much slower rate, than that being removed, by the DS3/E3 Framer block.
			0 – Indicates that the Channel is NOT declaring the "Transmit DS3/E3 Underrun" condition.
			1 – Indicates that the Channel is currently declaring the "Transmit DS3/E3 Underrun" condition.
			Note:
			1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the DS3/E3 Framer block (in the Egress Direction) and the Receive TUG-3/AU-3 Mapper VC-3 POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STM-1 Clock signal).
			However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode
			2. Minor timing differences are easily handled by pointer adjustments.
			3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.

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Table 448: Receive Mapper Interrupt Status Register – Byte 0 (Address Location= 0xNB0B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Rx STM-0 Overrun Interrupt Status	Rx STM-0 Underrun Interrupt Status	Tx STM-0 Overrun Interrupt Status	Tx STM-0 Underrun Interrupt Status	Rx Overrun Interrupt Status	Rx Underrun Interrupt Status	Tx Overrun Interrupt Status	Tx Underrun Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Receive STM-0	RUR	Receive STM-0 Overrun Interrupt Status:
	Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive STM-0 Overrun" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive STM-0 Overrun" condition.
			0 – Indicates that the Receive STM-0 Overrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Receive STM-0 Overrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Receive STM-0 Overrun" condition can be obtained by reading the state of Bit 7 (Receive STM-0 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
6	Receive STM-0	RUR	Receive STM-0 Underrun Interrupt Status:
	Underrun Interrupt Status	بلغ	This RESET-upon-READ bit-field indicates whether or not the "Receive STM-0 Underrun" interrupt has occurred since the last read of this register.
		du	If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive STM-0 Underrun" condition.
	Q	odue	0 - Indicates that the "Receive STM-0 Underrun" interrupt has NOT occurred since the last read of this register.
	140.93		1 – Indicates that the "Receive STM-0 Underrun" interrupt has occurred since the last read of this register.
	•	ali	Note: The current status of the "Receive STM-0 Underrun" condition can be obtained by reading the state of Bit 6 (Receive STM-0 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
5	Transmit STM-0	RUR	Transmit STM-0 Overrun Interrupt Status:
	Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit STM-0 Overrun" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Transmit STM-0 Overrun" condition.
			0 – Indicates that the "Transmit STM-0 Overrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Transmit STM-0 Overrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Transmit STM-0 Overrun" condition



			can be obtained by reading the state of Bit 5 (Transmit STM-0 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
4	Transmit STM-0	RUR	Transmit STM-0 Underrun Interrupt Status:
	Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit STM-0 Underrun" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Transmit STM-0 Underrun" condition.
			0 – Indicates that the "Transmit STM-0 Underrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Transmit STM-0 Underrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Transmit STM-0 Overrun" condition can be obtained by reading the state of Bit 4 (Transmit STM-0 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
3	Receive DS3/E3	RUR	Receive DS3/E3 Overrun Interrupt Status:
	Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive DS3/E3 Overrup" intertupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive DS3/E3 Overrun" condition.
			0 – Indicates that the "Receive DS3/E3 Overrun" interrupt has NOT occurred since the last read of this register.
			15 Indicates that the "Receive DS3/E3 Overrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Receive DS3/E3 Overrun" condition can be obtained by reading the state of Bit 3 (Receive DS3/E3 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
2	Receive DS3/E3	RUR	Receive DS3/E3 Underrun Interrupt Status:
	Underrun Interrupt Status	nat	This RESET-upon-READ bit-field indicates whether or not the "Receive DS3/E3 Underrun" interrupt has occurred since the last read of this register.
	1. 93. 1		If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive DS3/E3 Underrun" condition.
			0 – Indicates that the "Receive DS3/E3 Underrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Receive DS3/E3 Underrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Receive DS3/E3 Underrun" condition can be obtained by reading the state of Bit 2 (Receive DS3/E3 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
1	Transmit DS3/E3	RUR	Transmit DS3/E3 Overrun Interrupt Status:
	Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit DS3/E3 Overrun" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt

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			anytime it declares a "Transmit DS3/E3 Overrun" condition.
			0 – Indicates that the "Transmit DS3/E3 Overrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Transmit DS3/E3 Overrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Transmit DS3/E3 Overrun" condition can be obtained by reading the state of Bit 1 (Transmit DS3/E3 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
0	Transmit DS3/E3	RUR	Transmit DS3/E3 Underrun Interrupt Status:
	Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit DS3/E3 Underrun" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Transmit DS3/E3 Underrun" condition.
			0 – Indicates that the "Transmit DS3/E3 Underrun" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Transmit DS3/E3 Underrun" interrupt has occurred since the last read of this register.
			Note: The current status of the "Transmit DS3/E3 Overrun" condition can be obtained by reading the state of Bit 0 (Transmit DS3/E3 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).

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Table 449: Receive Mapper Interrupt Enable Register – Byte 0 (Address Location= 0xNB0F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Receive STM-0 Overrun Interrupt Enable	Receive STM-0 Underrun Interrupt Enable	Transmit STM-0 Overrun Interrupt Enable	Transmit STM-0 Underrun Interrupt Enable	Receive Overrun Interrupt Enable	Receive Underrun Interrupt Enable	Transmit Overrun Interrupt Enable	Transmit Underrun Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Receive STM-0	R/W	Receive STM-0 Overrun Interrupt Enable:
	Overrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive STM-0 Overrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive STM-0 Overrun" condition is declared.
			0 – Disables this interrupt.
			1 – Enables this interrupt.
6	Receive STM-0	R/W	Receive STM-0 Underrun Interrupt Enable:
	Underrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive STM-0 Underrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive STM-0 Underrun" condition is declared.
		0	0 Disables this interrupt.
		10	9 – Enables this interrupt.
5	Transmit STM-0	R/W	Transmit STM-0 Overrun Interrupt Enable:
	Transmit STM-0 Overrun Interrupt Enable Transmit STM-0	et jo	This READ/WRITE bit-field permits the user to either enable or disable the "Transmit STM-0 Overrun" interrupt.
	presh	2	If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit STM-0 Overrun" condition is declared.
	AN XON		0 – Disables this interrupt.
	, 90° UO		1 – Enables this interrupt.
4	Transmit STM-0	R/W	Transmit STM-0 Underrun Interrupt Enable:
	Underrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit STM-0 Underrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit STM-0 Underrun" condition is declared.
			0 – Disables this interrupt.
			1 – Enables this interrupt.
3	Receive DS3/E3	R/W	Receive DS3/E3 Overrun Interrupt Enable:
	Overrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive DS3/E3 Overrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive DS3/E3 Overrun" condition is declared.

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			0 Disables this interrupt
			0 – Disables this interrupt.
			1 – Enables this interrupt.
2	Receive DS3/E3	R/W	Receive DS3/E3 Underrun Interrupt Enable:
	Underrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive DS3/E3 Underrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive DS3/E3 Underrun" condition is declared.
			0 – Disables this interrupt.
			1 – Enables this interrupt.
1	Transmit DS3/E3	R/W	Transmit DS3/E3 Overrun Interrupt Enable:
	Overrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit DS3/E3 Overrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit DS3/E3 Overrun" condition is declared.
			0 – Disables this interrup
			1 – Enables this interrupt.
0	Transmit DS3/E3	R/W	Transmit DS3/E3 Underrun Interrupt Enable:
	Underrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit DS3/E3 Underrun" interrupt.
			If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit DS3/E3 Underrun" condition is declared.
			0 – Disables this interrupt.
			1. Enables this interrupt.

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0

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Віт 7 Віт 6 Віт 5 Віт 4 Віт 3 Віт 2 Віт 1 Віт 0 TxSRC[1:0] TxDES[1:0] RxSRC[1:0] RxDES[1:0] R/W R/W R/W R/W R/W R/W R/W R/W

Table 450: Mapper Control Register – T3/E3 Routing Register Byte (Address Location= 0xNB13)

0

Table 146: Mapper Control Register – Jitter Attenuator Clock Source Control/Routing" F	Register
(Address Location= 0xNB17, where N ranges in value from 0x02 to 0x04)	-

0

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	ised			JA Sou	rce[1:0]
R/O	R/O	R/O	R/O	R/O	R /0	R/W	R/W
0	0	0	0	0	1 0 C	0	0

BIT NUMBER	NAME	ΤΥΡΕ	.0	DESCRIPTION
7 - 2	Unused	R/O	ion	all
1 - 0	JA Source[1:0]	R/W	Jitter Attenuator Co	onfiguration/Orientation:
			Attenuator to operation	bit-field permits the user to configure the Jitter to in either in the Ingress Direction, the Egress assed altogether, as depicted below.
			JA Source[1:0]	Resuting Jitter Attenuator Configuration
			C C C C C C C C C C C C C C C C C C C	By-Passed
		<u> </u>	01	Jitter Attenuator is in Egress Direction
		lo.e	10	Jitter Attenuator is in Ingress Direction
	, u ^c	. 0	11	Do NOT use
	The program	nay no	NOTE: For most ap two bits to the value	plications, we recommend that the user set these of "[0, 1]".

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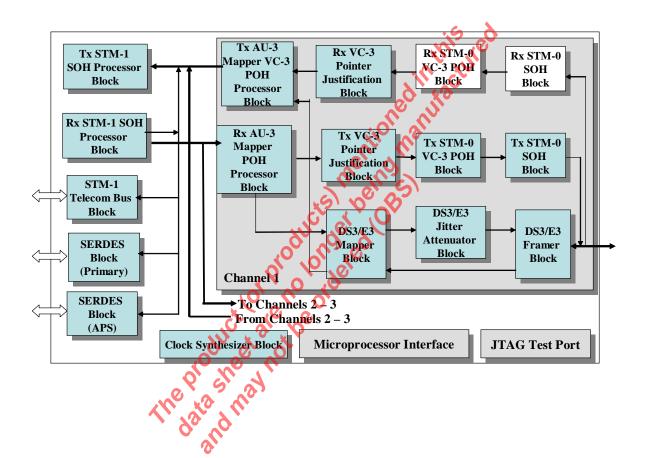


1.13 RECEIVE STM-0 SOH AND POH PROCESSOR BLOCK

The register map for the Receive STM-0 SOH and POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STM-0 SOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STM-0 SOH and POH Processor Blocks "highlighted" is presented below in Figure 10

Figure 10: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive STM-0 SOH and POH Processor Blocks "High-lighted".





1.13.1 RECEIVE STM-0 SOH AND POH PROCESSOR BLOCK REGISTER

Table 451: Receive STM-0 SOH and POH Processor Block Control Register Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0xN000 – 0xN102	Reserved	0x00
0xN103	Receive STM-0 Section Control Register – Byte 0	0x00
0xN104 – 0xN105	Reserved	0x00
0xN106	Receive STM-0 Section Status Register – Byte 1	0x00
0xN107	Receive STM-0 Section Status Register – Byte 0	0x02
0xN108	Reserved	0x00
0xN109	Receive STM-0 Section Interrupt Status Register - Byte 2	0x00
0xN10A	Receive STM-0 Section Interrupt Status Register - Byte 1	0x00
0xN10B	Receive STM-0 Section Interrupt Status Register Byte 0	0x00
0xN10C	Reserved	0x00
0xN10D	Receive STM-0 Section Interrupt Enable Register – Byte 2	0x00
0xN10E	Receive STM-0 Section Interrupt Enable Register – Byte 1	0x00
0xN10F	Receive STM-0 Section Interrupt Enable Register – Byte 0	0x00
0xN110	Receive STM-0 Section B1 Byte Error Count – Byte 3	0x00
0xN111	Receive STM-0 Section B Byte Error Count – Byte 2	0x00
0xN112	Receive STM-0 Section B1 Byte Error Count – Byte 1	0x00
0xN113	Receive STM-0 Section B1 Byte Error Count – Byte 0	0x00
0xN114	Receive STM-0 Section B2 Byte Error Count – Byte 3	0x00
0xN115	Receive STM-0 Section B2 Byte Error Count – Byte 2	0x00
0xN116	Receive STM-0 Section B2 Byte Error Count – Byte 1	0x00
0xN117	Receive STM-0 Section B2 Byte Error Count – Byte 0	0x00
0xN118	Receive STM-0 Section MS-REI Error Count – Byte 3	0x00
0xN119	Receive STM-0 Section MS-REI Error Count – Byte 2	0x00
0xN11A	Receive STM-0 Section MS-REI Error Count – Byte 1	0x00
0xN11B	Receive STM-0 Section MS-REI Error Count – Byte 0	0x00
0xN11C	Reserved	0x00
0xN11D – 0xN11E	Reserved	0x00
0xN11F	Receive STM-0 Section – Received K1 Byte Value Register	0x00
0xN120 – 0xN122	Reserved	0x00



Address Location	REGISTER NAME	DEFAULT VALUES
0xN123	Receive STM-0 Section – Received K2 Byte Value Register	0x00
0xN124 – 0xN126	Reserved	0x00
0xN127	Receive STM-0 Section – Received S1 Byte Value Register	0x00
0xN128 – 0xN12D	Reserved	0x00
0xN12E	Receive STM-0 Section – LOS Threshold Value – MSB	0xFF
0xN12F	Receive STM-0 Section – LOS Threshold Value – LSB	0xFF
0xN130	Reserved	0x00
0xN131	Receive STM-0 Section – Receive SF Set Monitor Interval – Byte 2	0x00
0xN132	Receive STM-0 Section – Receive SF Set Monitor Interval Byte 1	0x00
0xN133	Receive STM-0 Section – Receive SF Set Monitor Interval – Byte 0	0x00
0xN134, 0xN135	Reserved	0x00
0xN136	Receive STM-0 Section – Receive SF Set Threshold Byte 1	0x00
0xN137	Receive STM-0 Section – Receive SF Set Threshold – Byte 0	0x00
0xN138 – 0xN139	Reserved	0x00
0xN13A	Receive STM-0 Section – Receive SF Clear Threshold – Byte 1	0x00
0xN13B	Receive STM-0 Section – Receive SF Clear Threshold – Byte 0	0x00
0xN13C	Reserved	0x00
0xN13D	Receive STM-0 Section Receive SD Set Monitor Interval – Byte 2	0x00
0xN13E	Receive STM-0 Section - Receive SD Set Monitor Interval - Byte 1	0x00
0xN13F	Receive STM-0 Section - Receive SD Set Monitor Interval - Byte 0	0x00
0xN140 - 0xN141	Reserved of the the	0x00
0xN142	Receive STM-0 Section - Receive SD Set Threshold - Byte 1	0x00
0xN143	Receive STM-0 Section – Receive SD Set Threshold – Byte 0	0x00
0xN144, 0xN145	Reserved	0x00
0x46 0xN146	Receive STM-0 Section – Receive SD Clear Threshold – Byte 1	0x00
0xN147	Receive STM-0 Section – Receive SD Clear Threshold – Byte 0	0x00
0xN14B – 0xN14A	Reserved	0x00
0xN14B	Receive STM-0 Section – Force SEF Condition	0x00
0xN14C - 0xN14E	Reserved	0x00
0xN14F	Receive STM-0 Section – Receive J0 Byte Trace Buffer Control Register	0x00
0xN150 – 0xN151	Reserved	



Address Location	REGISTER NAME	DEFAULT VALUES
0xN152	Receive STM-0 Section – Receive SD Burst Error Count Tolerance – Byte 1	0x00
0xN153	Receive STM-0 Section – Receive SD Burst Error Count Tolerance – Byte 0	0x00
0xN154, 0xN155	Reserved	0x00
0xN156	Receive STM-0 Section – Receive SF Burst Error Count Tolerance – Byte 1	0x00
0xN157	Receive STM-0 Section – Receive SF Burst Error Count Tolerance – Byte 0	0x00
0xN158	Reserved	0x00
0xN159	Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 2	0x00
0xN15A	Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 1	0x00
0xN15B	Receive STM-0 Section – Receive SD Clear Monitor Interval Byte 0	0x00
0xN15C	Reserved	0x00
0xN15D	Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 2	0x00
0xN15E	Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 1	0x00
0xN15F	Receive STM-0 Section – Receive SFClearMonitor Interval – Byte 0	0x00
0xN160 - 0xN162	Reserved	0x00
0xN163	Receive STM-0 Section – Auto AIS Control Register	0x00
0xN164 – 0xN16A	Reserved	0x00
0x6B 0xN16B	Receive STM-0 Section - Auto AIS (in Downstream STM-0s) Control Register	0x00
0x6C – 0x82 0xN16C – 0xN182	Reserved	0x00
0xN183	Receive STM-0 Path - Control Register - Byte 2	0x00
0xN184 - 0xN185	Reserved	0x00
0xN186	Receive STM-0 Path – Control Register – Byte 1	
0xN187	Receive STM-0 Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive STM-0 Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive STM-0 Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive STM-0 Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive STM-0 Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive STM-0 Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive STM-0 Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00



Address Location	REGISTER NAME	DEFAULT VALUES
0xN193	Receive STM-0 Path – SONET Receive HP-RDI Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive STM-0 Path – Received Path Label Value (C2 Byte) Register	0x00
0xN197	Receive STM-0 Path – Expected Path Label Value (C2 Byte) Register	0x00
0xN198	Receive STM-0 Path – B3 Error Count Register – Byte 3	0x00
0xN199	Receive STM-0 Path – B3 Error Count Register – Byte 2	0x00
0xN19A	Receive STM-0 Path – B3 Error Count Register – Byte 1	0x00
0xN19B	Receive STM-0 Path – B3 Error Count Register – Byte 0	0x00
0xN19C	Receive STM-0 Path – HP-REI Error Count Register – Byte 3	0x00
0xN19D	Receive STM-0 Path – HP-REI Error Count Register – Byte 2	0x00
0xN19E	Receive STM-0 Path – HP-REI Error Count Register – Byte 1	0x00
0xN19F	Receive STM-0 Path – HP-REI Error Count Register Byte 0	0x00
0xN1A0 – 0xN1A5	Reserved	0x00
0xN1A6	Receive STM-0 Path – Pointer Value Register - Byte	0x00
0xN1A7	Receive STM-0 Path – Pointer Value Register Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive STM-0 Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved 0 10 10	0x00
0xN1BF	Receive STM-0 Path - Setial Port Control Register	0x00
0xN1C0 - 0xN1C2	Reserved	0x00
0xN1C3	Receive STM-0 Path - SONET Receive Auto Alarm Register - Byte 0	0x00
0xN1C4 - 0xN1D2	Reserved	
0xN1D3	Receive STM-0 Path – Receive J1 Byte Capture Register	0x00
0xN1C4 - 0xN1C6	Reserved	0x00
0xN1D7	Receive STM-0 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive STM-0 Path – Receive C2 Byte Capture Register	0x00
0xN1DC -0xN1DE	Reserved	0x00
0xN1DF	Receive STM-0 Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00
0xN1E3	Receive STM-0 Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00



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Address Location	REGISTER NAME	DEFAULT VALUES
0xN1E7	Receive STM-0 Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive STM-0 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive STM-0 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 - 0xN1F2	Reserved	0x00
0xN1F3	Receive STM-0 Path – Receive Z5 Byte Capture Register	0x00
0xN1F6 – 0xN1FF	Reserved	0x00



1.13.2 RECEIVE STM-0 SOH AND POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 452: Receive STM-0 Section Control Register – Byte 0 (Address Location = 0xN103, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble Disable	Unused	MS-REI Error Type	B2 Error Type	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7	Unused	R/O	ALL IN
6	SF Defect	R/W	Signal Failure (SF) Defect Condition Detect Enable:
	Condition Detect Enable		This READ/WRITE bit-field permits the user to enable or disable SF Defect Detection and Declaration by the Receive STM-0 SOH Processor block.
			0 – Configures the Receive STM-0 SOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified SF defect declaration and clearance" criteria
			1 – Configures the Receive STM-0 SOH Processor block to declare and clear the SF defect condition per the "user-specified SF defect declaration and clearance" criteria.
5	SD Defect	R/W	Signal Degrade (SD) Defect Condition Detect Enable:
	Condition Detect Enable		This READ/WRITE bit-field permits the user to enable or disable SD Detection and Declaration by the Receive STM-0 SOH Processor block.
		prod	0 - Configures the Receive STM-0 SOH Processor block to NOT declare nor clear the SD defect condition per the "user-specified SD defect declaration and clearance" criteria.
			1 Configures the Receive STM-0 SOH Processor block to declare and clear the SD defect condition per the "user-specified SD defect declaration and clearance" criteria.
4	Descramble	R/W	De-Scramble Disable:
	Disable 🔨	, 93° U	This READ/WRITE bit-field permits the user to either enable or disable de- scrambling by the Receive STM-0 SOH Processor block, associated with channel N.
			0 – De-Scrambling is enabled.
			1 – De-Scrambling is disabled.
3	Unused	R/O	
2			MS-REI Error Type:
Error Type			This READ/WRITE bit-field permits the user to specify how the Receive STM-0 SOH Processor block will count (or tally) MS-REI events, for Performance Monitoring purposes. The user can configure the Receive STM-0 SOH Processor block to increment MS-REI events on either a "per- bit" or "per-frame" basis. If the user configures the Receive STM-0 SOH Processor block to increment MS-REI events on a "per-bit" basis, then it will increment the "Receive STM-0 Section MS-REI Error Count" register by the value of the lower nibble within the M0/M1 byte of the incoming STM-0 data-



			stream.
			If the user configures the Receive STM-0 SOH Processor block to increment MS-REI events on a "per-frame" basis, then it will increment the "Receive STM-0 Section MS-REI Error Count" register each time it receives an STM-0 frame, in which the lower nibble of the M0/M1 byte is set to a "non-zero" value.
			0 – Configures the Receive STM-0 SOH Processor block to count or tally MS-REI events on a per-bit basis.
			1 – Configures the Receive STM-0 SOH Processor block to count or tally MS-REI events on a per-frame basis.
1	B2 Error	R/W	B2 Error Type:
	Туре		This READ/WRITE bit-field permits the user to specify how the "Receive STM-0 SOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 SOH Processor block to increment B2 byte errors on either a "per-bit" or a "per-frame" basis. If the user configures the Receive STM-0 SOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the "Receive Section B2 Byte Error Count" register by the number of bits (within the B2 byte value) that is in error.
			If the user configures the Receive STM-0 SOH Processor block to increment B2 byte errors on a "per-frame" basis, then it will increment the "Receive Section B2 Byte Error Count" register each time it receives an STM-0 frame that contains an erred B2 byte.
			0 – Configures the Receive STM-0 SOH Processor block to count B2 byte errors on a "per-bit" basis
			1 – Configures the Receive STM-0 SOH Processor block to count B2 byte errors on a "per-frame" basis.
0	B1 Error Type	R/W	B1 Error Type: This READ/WBITE bit-field permits the user to specify how the Receive STM-0 SOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 SOH Processor block to increment B1 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive STM-0 SOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Receive Section B1 Byte Error Count" register by the number of bits (within the B1 byte value) that is in error.
	The a	ata di	If the user configures the Receive STM-0 SOH Processor block to increment B1 byte errors on a "per-frame" basis, then it will increment the "Receive Section B1 Byte Error Count" Register each time it receives an STM-0 frame that contains an erred B1 byte.
			0 – Configures the Receive STM-0 SOH Processor block to count B1 byte errors on a "per-bit" basis.
			1 – Configures the Receive STM-0 SOH Processor block to count B1 byte errors on a "per-frame" basis.

Table 453: Receive STM-0 Section Status Register – Byte 1 (Address Location= 0xN106, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6 Віт 5 Віт 4 Віт 3				Віт 2	Віт 1	Віт 0
		Unused	MS-TIM Defect Declared	Section Trace Message (J0) Unstable Defect Declared	MS-AIS Defect Declared		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 3	Unused	R/O	this rec
2	MS-TIM Defect Declared	R/O	 MS-TIM Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the MS-TIM defect condition. The Receive STM-0 SOH Processor block will declare the MS-TIM defect condition, whenever it accepts a Section Trace Message (via the J0 byte, within the incoming STM-0 data-stream) that differs from the "Expected Section Trace Message" 0 – Indicates that the Receive STM-0 SOH Processor block is NOT currently declaring the MS-TIM Defect Condition is NOT currently being declared. 1 – Indicates that the Receive STM-0 SOH Processor block is currently declaring the MS-TIM Defect Condition is currently being declared.
1	Section Trace Message Unstable Defect Declared	R/O	 Section Trace Message Unstable Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STM-0 SOH Processor block will declare the Section Trace Message Unstable' counter reaches the value 8. The "Section Trace Message Unstable" counter reaches the value 8. The "Section Trace Message Unstable" counter will be incremented for each time that it receives a Section Trace message that differs from the "Expected Section Trace Message". The "Section Trace Message Unstable" counter is cleared to "0" whenever the Receive STM-1 SOH Processor block has received a given Section Trace Message 3 (or 5) consecutive times. Note: Receiving a given Section Trace Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 – Section Trace Message Unstable defect condition is NOT currently being declared. 1 – Section Trace Message Unstable defect condition is currently being declared.
0	MS-AIS Defect Detected	R/O	 MS-AIS Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the MS-AIS (Line AIS) defect condition. The Receive STM-0 SOH Processor block will declare the MS-AIS defect condition within the incoming STM-0 data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STM-0 frames. 0 – Indicates that the MS-AIS defect condition is NOT currently being declared.



	1 – Indicates that the MS-AIS defect condition is currently being declared.

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Table 454: Receive STM-0 Section Status Register – Byte 0 (Address Location = 0xN107, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
MS-RDI Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Detected	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	MS-RDI Defect Declared	R/O	 MS-RDI Defect Declared Indicator: This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is detecting the MS-RDI Line-Remote Defect Indicator) defect condition, within the incoming STM-0 signal. The Receive STM-0 SOH Processor block will declare the MS-RDI defect condition whenever bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive incoming STM-0 frames. 0 – Indicates that the MS-RDI defect condition is NOT currently being declared. 1 – Indicates that the MS-RDI defect condition is currently being declared.
6	S1 Byte Unstable Defect Declared	R/O	 S1 Byte Unstable Defect Declared: This READ-ONLY bit field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Receive STM-0 SOB Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Receive STM-0 SOH Processor block receives an STM-0 frame that contains an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STM-0 frames. Nore: Receiving a given S1 byte, in 8 consecutive STM-0 frames also sets this bit-field to "0". 0 - Indicates that the S1 Byte Unstable Defect Condition is NOT currently being declared. 1 - Indicates that the S1 Byte Unstable Defect Condition is currently being declared.
5	K1, K2 Byte Unstable Defect Declared	R/O	 K1, K2 Byte Unstable Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Receive STM-0 SOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever the Receive STM-0 SOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive incoming STM-0 frames. The "K1, K2 Byte Unstable" defect condition is cleared whenever the Receive STM-0 SOH Processor block has received a given set of K1, K2 byte values within three consecutive incoming STM-0 frames. 0 – Indicates that the K1, K2 Byte Unstable Defect Condition is NOT currently being declared. 1 – Indicates that the K1, K2 Byte Unstable Defect Condition is currently being declared.



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4	SF Defect Declared	R/O	SF (Signal Failure) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the SF defect condition. The Receive STM-0 SOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user- selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold.
			0 – Indicates that the SF Defect condition is NOT currently being declared.
			This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold.
			1 – Indicates that the SF Defect condition is currently being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Defect Declaration" threshold.
3	SD Defect	R/O	SD (Signal Degrade) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the SD defect condition. The Receive STM-0 SOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a user- selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold. 0 – Indicates that the SD Defect condition is NOT currently being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given
			interval of time) does not exceed the "SD Declaration" threshold.
			1 – Indicates that the SD Defect condition is currently being declared.
			This bit is set to 1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Defect Declared:
	Defect Declared	roduce souther	This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the LOF defect condition. The Receive STM-0 SOH Processor block will declare the LOF defect condition if it has been declaring the SEF condition for 24 consecutive STM-0 frame periods. Once the LOF defect is declared, then the Receive STM-0 SOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STM-0 frame periods).
	A. 8		declaring the LOF defect condition. 1 – Indicates that the Receive STM-0 SOH Processor block is currently
		Q.	declaring the LOF defect condition.
1	SEF	R/O	SEF (Severely Errored Frame) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOH Processor block is currently declaring the SEF defect condition. The Receive STM-0 SOH Processor block will declare the SEF defect condition if it detects Framing Alignment byte errors in four consecutive STM-0 frames. Once the Receive SOH Processor block declares the SEF defect condition, the Receive STM-0 SOH Processor block will then clear the SEF defect condition if it detects two consecutive STM-0 frames with un-erred framing alignment bytes. If the Receive SOH Processor block declares the SEF defect condition for 24 consecutive STM-0 frame periods, then it will declare the LOF defect condition.
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			 Indicates that the Receive STM-0 SOH Processor block is currently declaring the SEF defect condition.
0	LOS	R/O	LOS (Loss of Signal) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 SOF Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Receive STM-0 SOH Processor block will declare the LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STM-0 data stream.
			Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STM-0 Section – LOS Threshold Value" Register (Address Location= 0xN12E and 0xN12F, where N ranges in value from 0x05 to 0x07).
			0 – Indicates that the Receive STM-0 SOH Processor block is NOT currently declaring the LOS defect condition.
			1 – Indicates that the Receive STM-0 SOH Processor block is currentl declaring the LOS defect condition.
			1 - Indicates that the Receive STM-0 SOH Processor block is current declaring the LOS defect condition.



Table 455: Receive STM-0 Section Interrupt Status Register – Byte 2 (Address Location= 0xN109, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	6 BIT 5 BIT 4 BIT 3 BIT 2		Віт 1	Віт 0		
		Change of MS- AIS Defect Condition Interrupt Status	Change of MS- RDI Defect Condition Interrupt Status				
R/O	R/O R/O R/O R/O R/O R/O					RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of MS- AIS Defect	RUR	Change of MS-AIS (Line AIS) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of MS-AIS Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			Whenever the Receive STM-0 SOH Processor block declares the MS- AIS defect condition.
			Whenever the Receive STM-0 SOH Processor block clears the MS-AIS defect condition
			0 – Indicates that the "Change of MS-AIS Defect Condition" interrupt has not occurred since the last read of this register.
			1 Indicates that the "Change of MS-AIS Defect Condition" interrupt has occurred since the last read of this register.
		duct of	Note: The user can obtain the current state of the MS-AIS defect condition by reading the contents of Bit 0 (MS-AIS Defect Declared) within the "Receive STM-0 Section Status Register – Byte 1" (Address Location= 0xN106, where N ranges in value from 0x05 to 0x07).
0	Change of MS-RDI Defect	RUR	Change of MS-RDI (Line - Remote Defect Indicator) Defect Condition Interrupt Status:
	Condition Interrupt Status	andme	This RESET-upon-READ bit-field indicates whether or not the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following occurrences.
			• Whenever the Receive STM-0 SOH Processor block declares the MS-RDI defect condition.
			• Whenever the Receive STM-0 SOH Processor block clears the MS-RDI defect condition.
			0 – Indicates that the "Change of MS-RDI Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of MS-RDI Defect Condition" interrupt has occurred since the last read of this register.
			Note: The user can obtain the current state of the MS-RDI defect condition by reading out the state of Bit 7 (MS-RDI Defect Declared) within the "Receive STM-0 Section Status Register – Byte 0" (Address Location= 0xN107, where N ranges in value from 0x05 to 0x07).

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Table 456: Receive STM-0 Section Interrupt Status Register – Byte 1 (Address Location= 0xN10A, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status	Change in Section Trace Message Unstable Defect Condition Interrupt Status	New Section Trace Message Interrupt Status	Change in MS-TIM Defect Declared Interrupt Status	Unused	Change in K1, K2 Byte Unstable Defect Condtion Interrupt Status	NEW K1K2 Byte Value Interrupt Status		
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR		
0	0	0	0	0	0.6	0	0		
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		_	
BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	Description New S1 Byte Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate the "New S1 Byte Value" Interrupt, anytime it has "accepted" a new S1 byte, from the incoming STM-0 data-stream 0 - Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. 1 - Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register.
6	Change in S1 Byte Unstable Defect Condition Interrupt Status	BUR O	 Change in S1 Byte Unstable Defect Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events. Whenever the Receive STM-0 SOH Processor block declares the "S1 Byte Unstable" defect condition. Whenever the Receive STM-0 SOH Processor block clears the "S1 Byte Unstable" defect condition. Whenever the Receive STM-0 SOH Processor block clears the "S1 Byte Unstable" defect condition. I – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. I – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has not occurred since the last read of this register. Note: The user can obtain the current "S1 Byte Unstable Defect" condition by reading the contents of Bit 6 (S1 Byte Unstable Defect Declared) within the "Receive STM-0 Section Status Register – Byte 0" (Address



			Location= 0xN107, where N ranges in value from 0x05 to 0x07).
5	Change in Section Trace Message Unstable Defect	RUR	Change in Section Trace Message Unstable Defect condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Message Unstable" defect condition interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-0 SOH Processor block declares the "Section Trace Message Unstable defect" condition.
			• Whenever the Receive STM-0 SOH Processor block clear the "Section Trace Message Unstable defect" condition.
			0 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has not occurred since the last read of this register.
			1 – Indicates that the Change in Section Trace Message Unstable defect condition interrupt has occurred since the last read of this register.
4	New Section Trace	RUR	New Section Trace Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New Section Trace Message" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt anytime it has accepted a new "Section Trace" Message within the incoming STM-0 data- stream. Indicates that the "New Section Trace Message Interrupt" has not occurred since the last read of this register.
		01 10	19 Indicates that the "New Section Trace Message Interrupt" has occurred since the last read of this register.
	roduct	of produces of the second seco	Note: The user can read out the contents of the "Receive Section Trace Message Buffer", which is located at Address Locations 0xN300 through 0xN33F (where N ranges in value from 0x05 to 0x07).
3	Change in MS-TIM	RUR	Change in MS-TIM Defect Condition" Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in MS-TIM Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-0 SOH Processor block declares the MS-TIM defect condition
			• Whenever the Receive STM-0 SOH Processor block clears the MS-TIM defect condition.
			0 – Indicates that the "Change in MS-TIM Defect Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in MS-TIM Defect Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of the MS-TIM defect condition by reading the state of Bit 2 (MS-TIM Defect Declared) within the "Receive STM-0 Section

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			Status Register – Byte 1 (Address Location = 0xN106).	
2	Unused	R/O		
1	Change in K1, K2 Byte Unstable Defect	RUR	Change in K1, K2 Byte Unstable Defect Condition Interrupt Status:	
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.	
			• Whenever the Receive STM-0 SOH Processor block declares the "K1, K2 Byte Unstable Defect" condition.	
			• Whenever the Receive STM-0 SOH Processor block clears the "K1, K2 Byte Unstable Defect" condition.	
			0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register.	
			1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register.	
			Note: The user can determine whether the "K1, K2 Byte Unstable Defect Condition" is currently being declared or cleared by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Receive STM-0 Section Status Register – Byte 0" (Address Location= 0xN107).	
0	New K1, K2 Byte Value	RUR	New K1, K2 Byte Value Interrupt Status:	
	Interrupt Status	t lor pr	e product or product o	This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt whenever its has "accepted" a new set of K1, K2 byte values from the incoming STM-0 data-stream.
	الم		0 – Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.	
	Pres	n°31	1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.	
	The star		Note: The user can obtain the contents of the new K1 byte by reading out the contents of the "Receive STM-0 Section K1 Byte Value" Register (Address Location= 0xN11F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STM-0 Section K2 Byte Value" Register (Address Location= 0xN123).	

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Table 457: Receive STM-0 Section Interrupt Status Register – Byte 0 (Address Location= 0xN10B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Defect Condition Interrupt Status	Change of SD Defect Condition Interrupt Status	Detection of MS-REI Event Error Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Change of SF	RUR	Change of Signal Failure (SF) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
			Whenever the Receive STM SOH Processor block declares the SF Defect Condition.
			Whenever the Receive STM-0 SOH Processor block clears the SF Defect Condition.
			0 - Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register.
		ٹی	Note: The user can determine whether or not the SF defect condition is currently being declared by reading out the state of Bit 4(SF Defect Declared) within the "Receive STM-0 Section Status Register – Byte O(Address Location= 0xN107).
6	Change of SD	RUR	Change of Signal Degrade (SD) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status	o he	This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
	. 80	3110	• Whenver the Receive STM-0 SOH Processor block declares the SD Defect Condition.
			• Whenever the Receive STM-0 SOH Processor block clears the SD Defect Condition.
			0 – Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine whether or not the SD Defect condition is currently being declareds by reading out the state of Bit 3 (SD Defect Declared) within the "Receive STM-0 Section Status Register – Byte 0 (Address Location= 0xN107).
5	Detection of MS- REI Event	RUR	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of

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			MS-REI Event" Interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt anytime it detects an MS-REI event within the incoming STM-0 data-stream.
			0 - Indicates that the "Detection of MS-REI Event" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of MS-REI Event" Interrupt has occurred since the last read of this register.
4	Detection of B2 Byte Error	RUR	Detection of B2 Byte Error Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STM-0 data-stream.
			0 – Indicates that the "Detection of B2 Byte Error Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.
3	Detection of B1	RUR	Detection of B1 Byte Error Interrupt Status:
	Byte Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt anytime it detects a B1 byte error within the incoming STM-0 data-stream.
			0 - Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register
2	Change of LOF Defect Condition	RUR	Change of Loss of Frame (LOF) Defect Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
		, O	• Whenever the Receive STM-0 SOH Processor block declares the LOF Defect condition.
		2	Whenever the Receive STM-0 SOH Processor block clears the LOF Defect condition.
		9als	OC Indicates that the "Change of LOF Defect Condition" interrupt has NOT Occurred since the last read of this register.
		ð	1 – Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-0 SOH Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STM-0 Section Status Register – Byte 0 (Address Location= 0xN107).
1	Change of SEF	RUR	Change of SEF Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-0 SOH Processor block declares the SEF defect condition.



			• Whenever the Receive STM-0 SOH Processor block clears the SEF defect condition.
			0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-0 SOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STM-0 Section Status Register – Byte 0 (Address Location= 0xN107).
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Defect Condition Interrupt Status:
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Receive STM-0 SOH Processor block will generate this interrupt in response to either of the following events.
			• Whenever the Receive STM-0 SOH Processor block declares the LOS defect condition.
			Whenever the Receive STM-0 SOH Processor block clears the LOS defect condition.
			0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-0 SOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STM-0 Section Status Register – Byte 0 (Address Location= 0xN107).

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Table 458: Receive STM-0 Section Interrupt Enable Register – Byte 2 (Address Location= 0xN10D, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	BIT 4 BIT 3 BIT 2		Віт 1	Віт 0	
		Change of MS- AIS Defect Condition Interrupt Enable	Change of MS- RDI Defect Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of MS- AIS Defect Condition Interrupt Enable	R/W	 Change of MS-AIS (Line AIS) Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of MS-AIS Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. When the Receive STM-0 SOH Processor block declares the "MS-AIS" defect condition. When the Receive STM-0 SOH Processor block clears the "MS-AIS" defect condition. O – Disables the "Change of MS-AIS Defect Condition" Interrupt. 1 – Enables the "Change of MS-AIS Defect Condition" Interrupt.
0	Change of MS- RDI Defect Condition Interrupt Enable	R/W	 Change of MS-RDI (Line Remote Defect Indicator) Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the Change of MS-RDI Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. When the Receive STM-0 SOH Processor block declares the "MS-RDI" defect condition. When the Receive STM-0 SOH Processor block clears the "MS-RDI" defect condition. O – Disables the "Change of MS-RDI Defect Condition" Interrupt. 1 – Enables the "Change of MS-RDI Defect Condition" Interrupt.



Table 459: Receive STM-0 Section Interrupt Enable Register – Byte 1 (Address Location= 0xN10E, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	New Section Trace Message Interrupt Enable	Change in MS-TIM Defect Condition Interrupt Enable	Unused	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	New K1K2 Byte Value Interrupt Enable		
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W		
0	0	0	0	0		0	0		
	things								

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	 New S1 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STM-0 SOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STM-0 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1 Byte Unstable Defect Condition Interrupt Enable	R/W	 Change in S1 Byte Unstable Defect Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Receive STM-0 SOH Processor block will generate an interrupt in response to either of the following conditions. When the Receive STM-0 SOH Processor block declares the "S1 Byte Unstable" defect condition. When the Receive STM-0 SOH Processor block clears the "S1 Byte Unstable" defect condition. O – Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	R/W	 Change in Section Trace Message Unstable defect condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Message Unstable Defect Condition" Interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate an interrupt in response to either of the following conditions. Whenever the Receive STM-0 SOH Processor block declares the "Section Trace Message Unstable" defect condition. Whenever the Receive STM-0 SOH Processor block clears the "Section Trace Message Unstable" defect condition. O – Disable the "Change of Section Trace Message Unstable defect condition" Interrupt.

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			1 – Enables the "Change of Section Trace Message Unstable defect condition" Interrupt.
4	New Section Trace	R/W	New Section Trace Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New Section Trace Message" interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message within the incoming STM-0 data-stream. The Receive STM-0 SOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times.
			0 – Disables the "New Section Trace Message" Interrupt.
			1 – Enables the "New Section Trace Message" Interrupt.
3	Change in MS-TIM	R/W	Change in "MS-TIM Defect Condition" interrupt enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in MS-TIM defect condition" interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate an interrupt in response to either of the following events.
			 a. Whenever the Receive STM-0 SOH Processor block declares the "MS-TIM Defect" condition.
			 Whenever the Receive STM-0 SOH Processor block clears the "MS-TiM detect" condition.
			Note: The user can determine the current state of the MS-TIM defect condition by reading the state of Bit 2 (MS-TIM Defect Condition Declared) within the "Receive STM-0 Section Status Register – Byte 1 (Address Location= 0xN106).
2	Unused	R/O	ot no d
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	R/W	Change of K1, K2 Byte Unstable Defect Condition - Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate an Interrupt in response to either of the following events.
		100 re	Whenever the Receive STM-0 SOH Processor block declares the "K1, K2 Byte Unstable defect" condition.
	the	20	 b. Whenever the Receive STM-0 SOH Processor block clears the "K1, K2 Byte Unstable defect" condition.
	8	and	0 – Disables the "Change of K1, K2 Byte Unstable Defect Condition" Interrupt.
			1 – Enables the "Change of K1, K2 Byte Unstable Defect Condition" Interrupt.
0	New K1K2 Byte	R/W	New K1, K2 Byte Value Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STM-0 SOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STM-0 frames.
			0 – Disables the "New K1, K2 Byte Value" Interrupt.
			1 – Enables the "New K1, K2 Byte Value" Interrupt.



Table 460: Receive STM-0Section Interrupt Status Register – Byte 0 (Address Location= 0xN10F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of MS-REI Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Change of SF	R/W	Change of Signal Failure (SF) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events.
			• Whenever the Receive STM-0 SOH Processor block declares the SF defect condition.
			Whenever the Receive STM-0 SOH Processor block clears the SF defect condition.
			0 – Disables the "Change of SF Defect Condition Interrupt".
			1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD	R/W	Change of Signal Degrade (SD) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable	e de la construcción de la const	This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events.
	The ba	ducet	• Whenever the Receive STM-0 SOH Processor blolck declares the SD defect condition.
	epi	Shoo	• Whenever the Receive STM-0 SOH Processor block clears the SD defect condition.
		6 <u>6</u>	0 – Disables the "Change of SD Defect Condition Interrupt".
	. 90	no	1 – Enables the "Change of SD Defect Condition Interrupt".
5	REI Event	R/W	Detection of MS-REI (Line – Remote Error Indicator) Event Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of MS-REI Event" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STM-0 SOH Processor block detects an MS-REI condition within the incoming STM-0 data-stream.
			0 – Disables the "Detection of MS-REI Event" Interrupt.
			1 – Enables the "Detection of MS-REI Event" Interrupt.
4	Detection of B2	R/W	Detection of B2 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STM-0

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			SOH Processor block detects a B2 byte error within the incoming STM-0 data-stream.
			0 – Disables the "Detection of B2 Byte Error Interrupt".
			1 – Enables the "Detection of B2 Byte Error Interrupt".
3	Detection of B1	R/W	Detection of B1 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STM-0 SOH Processor block detects a B1 byte error within the incoming STM-0 data-stream.
			0 – Disables the "Detection of B1 Byte Error Interrupt".
			1 – Enables the "Detection of B1 Byte Error Interrupt".
2	Change of LOF	R/W	Change of Loss of Frame (LOF) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			• When the Receive STM-0 SOH Processor block declares the "LOF" defect condition.
			• When the Receive STM-0 SOH Processor block clears the "LOF" defect condition.
			0 – Disables the "Change of LOF Defect Condition Interrupt.
			1 – Enables the "Change of LOF Defect Condition" Interrupt.
1	Change of SEF	R/W	Change of SEF Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Defect Condition" Interrupt. If the user enables this interrupt then the XRT94L33 will generate an interrupt in response to either of the following conditions.
		dut	• When the Receive STM-0 SOH Processor block declares the "SEF" defect condition.
		pro sr	When the Receive STM-0 SOH Processor block clears the "SEF" defect condition.
			O Disables the " Change of SEF Defect Condition Interrupt".
		8°.0	1 – Enables the "Change of SEF Defect Condition Interrupt".
0	Change of LOS	R/W	Change of Loss of Signal (LOS) Defect Condition Interrupt Enable:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			• When the Receive STM-0 SOH Processor block declares the "LOF" defect condition.
			• When the Receive STM-0 SOH Processor block clears the "LOF" defect condition.
			0 – Disables the "Change of LOF Defect Condition Interrupt.
			1 – Enables the "Change of LOF Defect Condition" Interrupt.



Table 461: Receive STM-0 Section – B1 Byte Error Count Register – Byte 3 (Address Location= 0xN110, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	B1_Byte_Error_Count[31:24]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_Count[31:24]	RUR	B1 Byte Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STM-0 Section – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor Block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error
			2. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.
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Table 462: Receive STM-0 Section – B1 Byte Error Count Register – Byte 2 (Address Location= 0xN111, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B1_Byte_Error_Count[23:16]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_Count[23:16]	RUR	B1 Byte Error Count (Bits 23 through 16):
			This RESET-upon-READ register, along with "Receive STM-0 Section – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.
	The ata the	or pro-	



Table 463: Receive STM-0 Section – B1 Byte Error Count Register – Byte 1 (Address Location= 0xN112, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B1_Byte_Error_Count[15:8]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_Count[15:8]	RUR	B1 Byte Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive STM-0 Section – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error
			2. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.
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Table 464: Receive STM-0 Section – B1 Byte Error Count Register – Byte 0 (Address Location= 0xN113, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	B1_Byte_Error_Count[7:0]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B1_Byte_Error_Count[7:0]	RUR	B1 Byte Error Count – LSB:
			This RESET-upon-READ register, along with "Receive STM-0 Section – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B1 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor Block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.
	The produce	eet no	this 32 bit counter each time that it receives an STM-0 frame that contains an erred B1 byte.



Table 465: Receive STM-0 Section – B2 Byte Error Count Register – Byte 3 (Address Location= 0xN114, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B2_Byte_Error_Count[31:24]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_Count[31:24]	RUR	B2 Byte Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STM-0 Section – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.
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Table 466: Receive STM-0 Section – B2 Byte Error Count Register – Byte 2 (Address Location= 0xN115, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B2_Byte_Error_Count[23:16]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_Count[23:16]	RUR	B2 Byte Error Count (Bits 23 through 16):
			This RESET-upon-READ register, along with "Receive Section – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.
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Table 467: Receive STM-0 Section – B2 Byte Error Count Register – Byte 1 (Address Location= 0xN116, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
B2_Byte_Error_Count[15:8]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_Count[15:8]	RUR	B2 Byte Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Section – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-0 SOH Processror block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.
	The product C	areno	



Table 468: Receive STM-0 Section – B2 Byte Error Count Register – Byte 0 (Address Location= 0xN117, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	B2_Byte_Error_Count[7:0]										
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B2_Byte_Error_Count[7:0]	RUR	B2 Byte Error Count – LSB:
			This RESET-upon-READ register, along with "Receive Section – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a B2 byte error.
			Note:
			1. If the Receive STM-0 SOH Processor block is confiuged to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STM-0 frame) that are in error.
			2. If the Receive STM-0 SOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains an erred B2 byte.
	the produces	neet at	this 32 bit counter each time that it receives an STM-0 trame that contains an erred B2 byte.



Table 469: Receive STM-0 Section – MS-REI Event Count Register – Byte 3 (Address Location = 0xN118, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
MS-REI_Event_Count[31:24]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	MS-REI Event	RUR	MS-REI Event Count – MSB:
	Count[31:24]		This RESET-upon-READ register, along with "Receive STM-0 Section – MS-REI Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a Line - Remote Error Indicator event within the incoming STM-0 data-stream.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count MS-RELevents on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the MS-REI field of the M0 byte within each incoming STM-0 frame.
			2. If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a "non-zero" MS-REI value.
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	The product the sheet	y no	



Table 470: Receive STM-0 Section – MS-REI Event Count Register – Byte 2 (Address Location= 0xN119, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
MS-REI_Event_Count[23:16]										
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	MS-REI Event Count[23:16]	RUR	MS-REI Event Count (Bits 23 through 16):
			 This RESET-upon-READ register, along with "Receive STM-0 Section – MS-REI Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processon block detects a Line – Remote Error Indicator event within the incoming STM-0 data-stream. <i>Note:</i> If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the MS-REI field of the M0 byte within each incoming STM-0 frame. If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the MS-REI field of the M0 byte within each incoming STM-0 frame.



Table 471: Receive STM-0 Section – MS-REI Event Count Register – Byte 1 (Address Location= 0xN11A, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	MS-REI_Event_Count[15:8]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	MS-REI Event	RUR	MS-REI Event Count – (Bits 15 through 8)
	Count[15:8]		This RESET-upon-READ register, along with "Receive STM-0 Section – MS-REI Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM- 0 SOH Processor block detects a Line –Remote Error Indicator event within the incoming STM-0 data-stream.
			Note:
			1. If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the MS-REI field of the M0 byte within each incoming STM-0 frame.
			2. If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 frame that contains a "non-zero" MS-REI value.
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Table 472: Receive STM-0 Section – MS-REI Event Count Register – Byte 0 (Address Location= 0xN11B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
MS-REI_Event_Count[7:0]										
RUR	RUR	RUR	RUR RUR		RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	MS-REI Event Count[7:0]	RUR	MS-REI Event Count – LSB:
			This RESET-upon-READ register, along with "Receive STM-0 Section – MS-REI Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-0 SOH Processor block detects a Line – Remote Error Indicator event within the incoming STM-0 data stream. Note: 1. If the Receive STM-0 SOH Processor block is configured to count MS-REI events on a "per-bit" basis, then it will increment this 32 bit counter by the hibble-value within the MS-REI field of the M0 byte. 2. If the Receive STM-0 SOH Processor block is configured to count
			MS-REI events on a "per-frame" basis, then it will increment this 32
	the production of the producti	neet ar	bit counter each time that it receives an STM-0 trame that contains a "non-zero" MS-REL value.



Table 473: Receive STM-0 Section - Received K1 Byte Value Register (Address Location= 0xN11F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	Filtered_K1_Byte_Value[7:0]										
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O				
0	0	0	0	0	0	0	0				

BIT NUMBER	NAME	Түре	DESCRIPTION					
7 – 0	Filtered_K1_Byte_Value[7:0]	R/O	Filtered/Accepted K1 Byte Value:					
			These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value that the Receive STM-0 SOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STM-0 frames. This register should be polled by Software in order to determine various APS codes.					
	tionality							

Table 474: Receive STM-0Section - Received K2 Byte Value Register (Address Location= 0xN123, where N ranges in value from 0x05 to 0x07) and in the

Віт 7	Віт 6	Віт 5	BIT 4 BIT 3	Віт 2	Віт 1	Віт 0			
Filtered_K2_Byte_Value[7:0]									
R/O	R/O	R/O	R/0 R/0	R/O	R/O	R/O			
0	0	0	0 0 0	0	0	0			
			8.0.00						

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7-0	Filtered_K2_Byte_Value[7:0]	10.0	Filtered/Accepted K2 Byte Value: These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 Byte value that the Receive STM-0 SOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STM-0 frames. This register should be polled by Software in order to determine various APS codes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 475: Receive STM-0 Section – Received S1 Byte Value Register (Address Location= 0xN127, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Filtered_S1_Byte_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Filtered_S1_Byte_Value[7:0]	R/O	Filtered/Accepted S1 Byte Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Receive STM-0 SOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STM-0 frames.

Table 476: Receive STM-0 Section – LOS Threshold Value - MSB (Address Location= 0xN12E, where N ranges in value from 0x05 to 0x07)

	1		1		<u> </u>		
Віт 7	Віт 6	Віт 5	Віт 4	Вгт 3	Віт 2	Віт 1	Віт 0
			LOS_THRES	GHOLD[15:8]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1 🎽		1	1	1
			AUL	de' de			

BIT NUMBER	ΝΑΜΕ	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
	roduct	are p	Dese READ/WRITE bits, along the contents of the "Receive STM-0 Section – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that th Receive STM-0 SOH Processor block must detect before can declare the LOS defect condition.
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Table 477: Receive STM-0 Section – LOS Threshold Value - LSB (Address Location= 0xN12F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	LOS_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
			These READ/WRITE bits, along the contents of the "Receive STM-0Section – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STM-0 SOH Processor block must detect before it can declare the LOS defect condition.



Table 478: Receive STM-0 Section – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0xN131, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[23:1	R/W	SF_SET_MONITOR_INTERVAL – MSB:
	6]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.
		ducts	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user- specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Receive STM-0 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-0 Section SF SET Threshold" register, then the Receive STM-0 SOH Processor block will declare the SF defect condition. NOTES:
	The product or pro-	pe ord	 The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect" Declaration Monitoring Period", in terms of ms.
	the ta may ne		 This particular register byte contains the "MSB" (most significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring Period".
	, <u>9</u> , 9, 10		



Table 479: Receive STM-0 Section – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0xN132, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SF_SET_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
SF_SET_MONITOR_WINDOW[15:8]	R/W	SF_SET_MONITOR_INTERVAL (Bits 15 through 8):
		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.
		When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-
	She	specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period" the Receive STM-0 SOH Processor block accumulate more B2 byte errors than that specified within the "Receive STM-0 Section SF SET Threshold"
, sé		register, then the Receive STM-0 SOH Processor block will declare the SF defect condition.
or produce	noter	NOTE: The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.

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Table 480: Receive STM-0 Section – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0xN133, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0	R/W	SF_SET_MONITOR_INTERVAL – LSB:
	J		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration.
			When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Receive
		NOOUCT	STM-0 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-0 Section SF SET Threshold" register, then the Receive STM-0 SOH Processor block will declare the SF defect condition.
	inct of	no	 The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.
	The product of the area	o	 This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".
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Table 481: Receive STM-0 Section – Receive SF SET Threshold – Byte 1 (Address Location= 0xN136, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	SF_SET_THRESHOLD – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-0 SOH Processor block to declare the SF (Signal Failure) Defect condition.
		و	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STM-0 Section SF SET Threshold – Byte 0" register, then the Receive STM-0 SOH Processor block will declare the SF defect condition.
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Table 482: Receive STM-0 Section – Receive SF SET Threshold – Byte 0 (Address Location= 0xN137, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:0]	R/W	SF_SET_THRESHOLD – LSB:
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STM-0 SOH Processor block to declare the SF (Signal Failure) Defect condition. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STM-0 SOH Processor block STM-0 SOH Processor block is checking the programmed into this and the SF defect condition.

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Table 483: Receive STM-0 Section – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0xN13A, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION				
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD – MSB:				
	[15:8]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STM-0 SOH Processor block to clear the SF (Signal Failure) defect condition.				
			When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-0 Section SF CLEAR Threshold – Byte 0" register, then the Receive STM-0 SOH Processor block clear the SF defect condition.				

Table 484: Receive STM-0 Section – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0xN13B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1			1	1	1	1	

		•	
BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD – LSB:
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STM-0 SOH Processor block to clear the SF (Signal Failure) defect condition.
			When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-0 Section SF CLEAR Threshold – Byte 1" register, then the Receive STM-0 SOH Processor block will clear the SF defect condition.

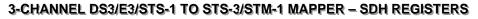




Table 485: Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0xN13D, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_SET_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SD_SET_MONITOR_INTERVAL – MSB:
	[23:16]	arod	These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration monitoring period". If, during this "SD Defect Declaration Monitoring period", the Receive STM-0 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-0 SOH Processor block will declare the SD defect condition. NOTES:
	o and		



Table 486: Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0xN13E, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SD_SET_MONITOR_INTERVAL – Bits 15 through 8:
	[15:8]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration.
		oduct	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Receive STM-0 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-0 Section SD SET Threshold" register, then the Receive STM-0 SOH Processor block will declare the SD defect condition. NOTE: The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.
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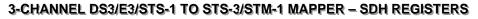




Table 487: Receive STM-0 Section – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0xN13F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SD_SET_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SD_SET_MONITOR_INTERVAL – LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period", the Receive STM-0 SOH Processor block accumulates more B2 byte errors than that specified within the "Receive STM-0 SOH Processor block will declare the SD defect on SD SET Threshold" register, then the Receive STM-0 SOH Processor block will declare the SD defect condition.
	the and the		



Table 488: Receive STM-0 Section – Receive SD SET Threshold – Byte 1 (Address Location= 0xN142, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	SD_SET_THRESHOLD – MSB:
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STM-0 SON Processor block to declare the SD (Signal Degrade) defect condition.
			When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STM-0 Section SD SET Threshold – Byte 0" register, then the Receive STM-0 SOH Processor block will declare the SD defect condition.
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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 489: Receive STM-0 Section – Receive SD SET Threshold – Byte 0 (Address Location= 0xN143, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	SD_SET_THRESHOLD[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
1	1	1	1	1	1	1	1				

BIT NUMBER	NAME	Түре	DESCRIPTION						
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD – LSB:						
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STM-0 SOH Processor block to declare an SD (Signal Degrade) defect condition. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STM-0 SOH Processor block sTM-0 SOH Processor block will declare the SD defect condition.						

 Table 490: Receive STM-0 Section – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN146, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0			
SD_CLEAR_THRESHOLD[15:8]										
R/W	R/W	R/W	R/W O	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD [15:8]	R/W	 SD_CLEAR_THRESHOLD – MSB: These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-0 SOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulate B2 byte errors is less than that programmed into this and the "Receive STM-0 Section SD CLEAR Threshold – Byte 0" register, then the Receive STM-0 SOH Processor block will clear the SD defect condition.



Table 491: Receive STM-0 Section – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN147, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	SD_CLEAR_THRESHOLD[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
1	1	1	1	1	1	1	1				

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD – LSB:
		et.	These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STM-0 SOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STM-0 Section SD CLEAR Threshold – Byte 1" register, then the Receive STM-0 SOH Processor block will clear the SD defect condition.

Table 492: Receive STM-0 Section – Force SEF Defect Condition Register (Address Location= 0xN14B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5 Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	Unused									
R/O	R/O	R/O R/O	R/O	R/O	R/O	R/W				
0	0		0	0	0	0				
	at stat									

BIT NUMBER	NAME VO	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	SEF Defect Condition Force:
			This READ/WRITE bit-field permits the user to force the Receive STM-0 SOH Processor block (within the corresponding Channel) to declare the SEF defect condition. The Receive STM-0 SOH Processor block will then attempt to reacquire framing.
			Writing a "1" into this bit-field configures the Receive STM-0 SOH Processor block to declare the SEF defect. The Receive STM-0 SOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STM-0 frames with the correct A1 and A2 bytes).



Table 493: Receive STM-0 Section – Receive Section Trace Message Buffer Control Register (Address Location= 0xN14F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

			.5 8
BIT NUMBER	ΝΑΜΕ	Түре	
7 – 5	Unused	R/O	
4	Receive Section Trace Message Buffer Read Select	R/W	 Receive Section Trace Message Buffer Read Selection: This READ/WRITE bit-field permits a user to specify which of the following Receive Section Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Section Trace Message Buffer. a. The "Actual" Receive Section Trace Message Buffer. The "Actual" Receive Section Trace Message Buffer contains the contents of the most receively received (and accepted) Section Trace Message via the incoming STM-0 data-stream. b. The "Expected" Receive Section Trace Message Buffer. The "Expected" Receive Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer contains the contents of the Section Trace Message Buffer address to receive. The contents of this particular buffer is usually specified by the user. C Executing a READ to the Receive Section Trace Message Buffer address space, will return contents within the "Actual" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer Section
	Ň	93.21	Note: In the case of the Receive STM-1 SOH Processor block, the "Receive Section Trace Message Buffer" is located at Address Location 0xN300 through 0xN33F (where N ranges in value from 0x05 through 0x07).
3	Receive Section Trace Message Accept Threshold	R/W	 Receive Section Trace Message Accept Threshold: This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STM-0 SOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given "Section Trace Message" has been accepted then it can be read out of the "Actual Receive Section Trace Message" Buffer. 0 - Configures the Receive STM-0 SOH Processor block to accept the incoming Section Trace Message after it has received it the third time in succession. 1 - Configures the Receive STM-0 SOH Processor block to accept the incoming Section Trace Message after it has received in the fifth time in succession.



2	Section Trace	R/W	Section Trace Message Alignment Type:					
	Message Alignment Type		This READ/WRITE bit-field permits a user to specify how the Receive STM SOH Processor block will locate the boundary of the incoming Section Tra Message within the incoming STM-0 data-stream, as indicated below.					
			0 – Configures the Receive STM-0 SOH Processor block to expect th Section Trace Message boundary to be denoted by a "Line Feed" character.					
			1 – Configures the Receive STM-0 SOH Processor block to expect the Section Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the very first byte (within the incomine Section Trace Message). In this case, all of the remaining bytes (within the incoming Section Trace Message) will each have a "0" within their MSBs.					
1 - 0	Receive Section	R/W	Receive Section Trace Message Length[1:0]:					
	Trace Message Length[1:0]		These READ/WRITE bit-fields permit the user to specify the length of th Section Trace Message that the Receive STM-0 SOH Processor block w accept and load into the "Actual" Receive Section Trace Message Buffer. Th relationship between the content of these bit-fields and the correspondin Receive Section Trace Message Length is presented below.					
			Receive Resulting Receive Section Trace					
			Section Trace Message Length[1:0]					
			00 01 00 1 Byte					
			010 16 Bytes					
			64 Bytes					

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Table 494: Receive STM-0 Section – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0xN152, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SD_BURST_TOLERANCE[15:8]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE	R/W	SD_BURST_TOLERANCE – MSB:
	[15:8]		These READ/WRITE bits, along with the contents of the "Receive STM-0 Section – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.
			Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-0 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-0 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
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Table 495: Receive STM-0 Section – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0xN153, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE[7:0]	R/W	SD_BURST_TOLERANCE – LSB:
			These READ/WRITE bits, along with the contents of the "Receive STM-0 Section – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.
		duce	Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-0 SOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STM-0 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS

Table 496: Receive STM-0 Section – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0xN156, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	SF_BURST_TOLERANCE – MSB:
		di	These READ/WRITE bits, along with the contents of the "Receive STM-0 Section – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-0 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM-0 SOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.
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Table 497: Receive STM-0 Section – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0xN157, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	SF_BURST_TOLERANCE – LSB:
		Auct	These READ/WRITE bits, along with the contents of the "Receive STM-0 Section – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STM-0 SOH Processor block can accumulate during a single Sub-Interval period (e.g., an STM-0 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STM-0 SOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STM-0 SOH Processor block to detect B2 bit errors in multiple "Sub- Interval" periods before it will declare the SF defect condition.
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Table 498: Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0xN159, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_CLEAR_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW	R/W	SD_CLEAR_MONITOR_INTERVAL – MSB:
	[23:16]	oduct	These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance" Monitoring period, the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Section SD Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SD defect condition. NOTES:
	A LOY	1000	1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.
	The product of the start	othe	 This particular register byte contains the "MSB" (Most significant byte) value of the three registers that specifiy the "SD Defect Clearance Monitoring" period.
	The atand man		



Table 499: Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 1 (Address Location=

0xN15A, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
	8	cts of	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine it it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period", the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Section SD Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SD defect condition.
	lor pro	order	NOTES: The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.
	The product are not product and may not produce and produc	0	<u> </u>



Table 500: Receive STM-0 Section – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0xN15B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance.
		odu	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring period, the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Soction SD Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SD defect condition. NOTES:
	t lor		The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.
	The product or and the start of	othe	 This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.
	The atand mo		·



Table 501: Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0xN15D, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL – MSB:
	[23:16]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section - SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance.
		ucts	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Section SF Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SF defect condition. NOTES:
	lot prov	long	 The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.
	roduct are not	Ø	 This particular register byte contains the "MSB" (Most significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.
	The data and may not		·



Table 502: Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0xN15E, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

7-0 SF_0	CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL – Bits 15 through
	[15:8]		 8: These READ/WRITE bits, along the contents of the "Receive STM-0 Section - SF Clear Monitor Interval - Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Section SF Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SF defect condition. NOTES: The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.



Table 503: Receive STM-0 Section – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0xN15F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SF_CLEAR_MONITOR_WINDOW[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL – LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STM-0 Section – SF Clear Monitor Interval – Byte 2 and Byte 1 registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance.
		ucts	When the Receive STM-0 SOH Processor block is checking the incoming STM-0 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance Monitoring" period, the Receive STM-0 SOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STM-0 Section SF Clear Threshold" register, then the Receive STM-0 SOH Processor block will clear the SF defect condition. NOTES:
	lot proc	londe	 The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.
	roduct are not	Ø	 This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.
	The product or prot		<u>.</u>

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Table 504: Receive STM-0 Section – Auto AIS Control Register (Address Location= 0xN163, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit AIS-P (Down- stream) upon Section Trace Message Unstable	Transmit AIS-P (Down- stream) Upon Section Trace Message Mismatch	Transmit AIS-P (Down- stream) upon SF	Transmit AIS-P (Down- stream) upon SD	Unused	Transmit AIS-P (Down- stream) upon LOF	Transmit AIS-P (Down- stream) upon LOS	Transmit AIS-P (Down- stream) Enable		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0.6	0	0		
	thire								

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Transmit AIS-P (Down- stream) upon Section	R/W	Transmit Path AIS upon Declaration of the Section Trace Message Unstable Detect Condition:
	Trace Message Unstable		This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor block), anytime it declares the Section Trace Message Unstable defect condition within the "incoming" STM-0 data-stream.
			0 – Does not configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition.
		101 of	1 Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition.
	neprof	heet	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
6	Transmit AIS-R (Down- stream) Upon Section	R/W	Transmit Path AIS (AIS-P) upon Declaration of the Section Trace Message Mismatch Defect Condition:
	Trace Message 🔗 Mismatch		This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Mismatch defect condition within the "incoming" STM-0 data stream.
			0 – Does not configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it declares the "Section Trace Mismatch" defect condition.
			1 – Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Mismatch" defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1"



			to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Down- stream) upon SF	R/W	Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the SF defect condition.
			0 – Does not configure the Receive STM-0 SOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect.
			1 – Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the SF defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Down- stream) upon SD	R/W	Transmit Path AlS upon declaration of the Signal Degrade (SD) defect:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor block) anytime (and for the duration that) it declares the SD defect condition.
		orpr	0 Does not configure the Receive STM-0 SOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
	e product	et no	10- Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the SD defect condition.
	The ata dr	137	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Unused	R/O	
2	Transmit AIS-P (Down- stream) upon LOF	R/W	Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the LOF defect condition.
			0 – Does not configure the Receive STM-0 SOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			1 – Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the LOF defect



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			condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P (Down- stream) upon LOS	R/W	Transmit Path AIS upon declaration of the Loss of Signal (LOS) defect:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STM-0 POH Processor block), anytime (and for the duration that) it declares the LOS defect condition.
			0 – Does not configure the Receive STM-0 SOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect condition
			1 – Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the LOS defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	AUTO AIS	R/W	Automatic Transmission of AIS-P Enable:
			This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STM-0 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF or LOS defect conditions. It also permits the user to configure the Receive STM-0 SOH Processor block to automatically transmit a Path AIS (AIS-P)
	, ob	reet	Indicator via the "downstream" traffic (e.g., towards the Receive STM- OPOH Processor block) anytime it declares the MS-AIS defect condition within the "incoming" STM-0 datastream.
	Thelata	dmay	0 – Configures the Receive STM-0 SOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the MS-AIS defect condition or any of the "above-mentioned" defect conditions.
	o		1 – Configures the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the MS-AIS defect or any of the "above-mentioned" defect conditions.
			Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STM-0 SOH Processor block to automatically transmit the AIS-P indicator upon declaration of a given alarm/defect condition.



Table 505: Receive STM-0 Section – Auto AIS (in Downstream STM-0s) Control Register (Address Location= 0xN16B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
Unu	Unused		Transmit AIS- P (via Downstream STM-0s) upon LOF	Transmit AIS- P (via Downstream STM-0s) upon SD	Transmit AIS- P (via Downstream STM-0s) upon SF	Unused	Transmit AIS-P (via Downstream STM-0s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 6	Unused	R/O	this rec
5	Transmit AIS-P (via Downstream STM-0s) upon LOS	R/W	Transmit AIS-P (via Downstream STM-0s) upon declaration of the LOS (Loss of Signal) defect condition:
			 This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the LOS defect condition. 0 - Dees not configure the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 SOH Processor block declares to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 SOH Processor block declares the LOS defect condition.
	du	et at	1 – Configures the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the downstream" STM-0 signals (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the LOS defect condition.
	The produces	may	1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream – Upon LOS), within the Receive STM-0 Section – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor block to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STM-0 SOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR- 253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
			In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STM-0 SOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STM-0s Enable) within this register, in order enable this feature.
4	Transmit AIS-P (via Downstream STM-0s) upon LOF	R/W	Transmit AIS-P (via Downstream STM-0s) upon declaration of the LOF (Loss of Frame) defect condition:

	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the LOF defect condition.
	0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals (within the outbound STM-1 signal), anytime the Receive STM-0 SOH Processor block declares the LOF defect condition.
	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the LOF defect condition.
	Note:
	1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Receive STM-0 Section – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STM-0 SOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.
	In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STM-1 SOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
	02. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STM-0s Enable) within this register, in order enable this feature.
3 Transmit AIS-P (via Downstream STM-0s)	Transmit AIS-P (via Downstream STM-0s) upon declaration of the SD (Signal Degrade) defect condition:
upon SD PI	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signals (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the SD defect condition.
	0 – Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signals (within the outbound STM-1 signal), anytime the Receive STM-0 SOH Processor block declares the SD defect condition.
	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the SD defect condition.
	Note:
	1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the



0	Transmit AIS-P (via Downstream STM-0s)	R/W	Automatic Transmission of AIS-P (via the downstream STM-0s) Enable:
1	Unused	R/O	
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STM-0s Enable) within this register, in order enable this feature.
			In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STM-0 SOH Processor block has declared the SF defect), before the corresponding Transmit SONET POH Processor blocks will begin the process of transmitting the AIS-P indicator.
	The proof	eet n	In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STM-0 Section – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STM-0 SOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect.
		or ar	 Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 SOH Processor block declares the SF defect condition.
			0 – Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 SOH Processor block declares the SF defect condition
			This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that)) the Receive STM-0 SOH Processor block declares the SF defect condition.
2	Transmit AIS-P (via Downstream STM-0s) upon SF	R/W	Transmit AIS-P (via Downstream STM-0s) upon declaration of the Signal Failure (SF) defect condition:
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STM-0s Enable) within this register, in order enable this feature.
			In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STM-0 SOH Processor block has declared the SD defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			Receive STM-0 Section – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STM-0 SOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.

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Enable	Enable:
	This READ/WRITE bit-field serves two purposes.
	It permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STM-0 signal (within the outbound STM-1 signal), upon declaration of either the SF, SD, LOS or LOF defect conditions via the Receive STM-0 SOH Processor block.
	It also permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STM-0 signal (within the outbound STM-1 signal), upon declaration of the MS-AIS defect condition, via the Receive STM-0 SOH Processor block.
	0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever the Receive STM-0 SOH Processor block declares either the LOS, LOF, SD, SF or MS-AIS defect conditions.
	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever (and for the duration that) the Receive STM-0 SOH Processor block declares either the LOS, LOF, SD, SF or MS-AIS defect conditions.

either the LOS, LOF, SD, SF or either the LOS, LOF, SD, SF or international the Receive either the LOS, LOF, SD, SF or international the receive either the receive e



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Table 506: Receive STM-0 Path – Control Register – Byte 2 (Address Location= 0xN183, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		Check	HP-RDI	HP-REI	B3 Error Type
					Туре	Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select:
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.
			0 – Disables this SONET standard implementation. In this mode, all pointer- adjustment operations that are detected will be accepted.
			1 – Enables this "SONET standard" implementation. In this mode, all pointer- adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation will be ignored.
2	HP-RDI Type	R/W	Path - Remote Defect Indicator Type Select:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to support either the "Single-Bit" or the "Enhanced" HP- RDI form of signaling, as described below.
		ٹ	0 – Configures the Receive STM-0 POH Processor block to support Single-Bit HP-RDI. In this mode, the Receive STM-0 POH Processor block will only monitor Bit 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the HP-RDI defect condition.
	Q	odule	 Configures the Receive STM-0 POH Processor block to support Enhanced HP-RDI (EHP-RDI). In this mode, the Receive STM-0 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the HP-RDI defect condition.
1	HP-RELETTOR	R/W	HP-REI Error Type:
	Type 🎸	ano	This READ/WRITE bit-field permits the user to specify how the Receive STM- 0 POH Processor block will count (or tally) HP-REI events, for Performance Monitoring purposes. The user can configure the Receive STM-0 POH Processor block to increment HP-REI events on either a "per-bit" or "per- frame" basis. If the user configures the Receive STM-0 POH Processor block to increment HP-REI events on a "per-bit" basis, then it will increment the "Receive STM-0 Path HP-REI Error Count" register by the value of the lower nibble within the G1 byte of the incoming STM-0 data-stream.
			If the user configures the Receive STM-0 POH Processor block to increment HP-REI events on a "per-frame" basis, then it will increment the "Receive STM-0 Path HP-REI Error Count" register each time it receives an STM-0 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value.
			0 – Configures the Receive STM-0 POH Processor block to count or tally HP-REI events on a per-bit basis.
			1 – Configures the Receive STM-0 POH Processor block to count or tally HP-

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			REI events on a "per-frame" basis.
0	B3 Error Type	R/W	B3 Error Type:
			This READ/WRITE bit-field permits the user to specify how the Receive STM- 0 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive STM-0 POH Processor block to increment B3 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive STM-0 POH Processor block to increment B3 byte errors on a "per-bit" basis, then it will increment the "Receive STM-0 Path B3 Byte Error Count" register by the number of bits (within the B3 byte value of the incoming STM-0 data-stream) that is in error.
			If the user configures the Receive STM-0 POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive STM- 0 Path - B3 Byte Error Count" register each time it receives an STM-0 SPE that contains an erred B3 byte.
			0 – Configures the Receive STM-0 POH Processor block to count B3 byte errors on a "per-bit" basis
			1 – Configures the Receive STM-0 POH Processor block to count B3 byte errors on a "per-frame" basis.

... PC ... es the Receive STM-0 PO. ... on a "per-frame" basis.



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Table 507: Receive STM-0 Path – Control Register – Byte 1 (Address Location= 0xN186, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused				Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 1	Unused	R/O	the res
0	Path Trace Message Unstable Defect Declared	R/O	 Path Trace Message Unstable Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive STM-0 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The "Path Trace Message Unstable" counter will be incremented for each time that it receives a Path Trace Unstable" counter will be incremented for each time that it receives a Path Trace Unstable" counter is cleared to "0" whenever the Receive STM-0 POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times. Note: Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 – Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the Path Trace Message Unstable defect condition. 1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the Path Trace Message Unstable defect condition.

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Table 508: Receive STM-0 Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	HP-UNEQ Defect Declared	PLM-P Defect Declared	HP-RDI Defect Declared	HP-RDI Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TIM-P	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition.
			The Receive STM-0 POH Processor block will declare the "TIM-P" defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STM-0 data stream) matches the expected 1, 16 or 64-byte message.
			The Receive STM-0 POH Processor block will clear the "TIM-P" defect condition, when 80% of the received 1, 16 or 64-byte string (received via the J1 byte) matches the expected 1, 16 or 64-byte message.
			0 – Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the TIM-P defect condition.
			1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Defect Declared:
	Unstable Defect Declared		This READ ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the "Path Signal Label Byte" Unstable detect condition.
		the p	The Receive STM-0 POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the "C2 Byte Unstable" counter reaches the value "5". The "C2 Byte Unstable" counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Byte Unstable" counter is cleared to "0" whenever the Receive STM-0 POH Processor block has received 3 (or 5) consecutive SPEs that each contains the same C2 byte value.
			Note: Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".
			0 – Indicates that the Receive STM-0 POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition.
			1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	HP-UNEQ	R/O	Path – Unequipped (HP-UNEQ) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the HP-UNEQ defect condition.
			The Receive STM-0 POH Processor block will declare the HP-UNEQ defect condition anytime that it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to the value "0x00" (which indicates that the SPE is



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			"Unequipped").
			The Receive STM-0 POH Processor block will clear the HP-UNEQ defect condition, if it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to a value other than 0x00.
			0 – Indicates that the Receive STM-0 POH Processor block is currently NOT declaring the HP-UNEQ defect condition.
			1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the HP-UNEQ defect condition.
			Note: The Receive STM-0 POH Processor block will not declare the HP-UNEQ defect condition if it configured to expect to receive STM-0 frames with C2 bytes being set to "0x00" (e.g., if the "Receive STM-0 Path – Expected Path Label Value" Register is set to "0x00").
4	4 PLM-P		Path Payload Mismatch (PLM-P) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the PLM-P defect condition.
			The Receive STM-0 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STM-0 frames, in which the C2 byte was set to a value other than that which it is expecting to receive.
			Whenever the Receive STM 0 POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers.
			• The "Receive STM-0 Path Received Path Label Value" Register (Address Location= 0xN196)
			• The "Receive STM-0 Path Expected Path Label Value" Register (Address Location= 0xN197).
			The "Receive STM-0 Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STM-0 POH Processor blocks expects to receive.
			The "Reserve STM 0 Dath - Descived Dath Label Value" Desister contains the

The "Receive STM-0 Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive STM-0 POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive STM-0 frames).

.0	The Receive STM-0 POH Processor block will declare the PLM-P defect condition
	the contents of these two register do not match. The Receive STM-0 POH
X 9	Processor block will clear the PLM-P defect condition if whenever the contents of
2	these two registers do match.
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Xo.	0 – Indicates	that the	Receive	STM-0	POH	Processor	block is	currently	NOT
ଁ _କ ୍	 0 – Indicates declaring the F 	^v LM-P def	ect cond	ition.					

1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the PLM-P defect condition.

Note: The Receive STM-0 POH Processor block will clear the PLM-P defect, upon declaring the HP-UNEQ defect condition.

Ĩ	3	HP-RDI	R/O	Path Remote Defect Indicator (HP-RDI) Defect Declared:
		Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the HP-RDI defect condition.
				If the Receive STM-0 POH Processor block is configured to support the "Single-bit HP-RDI" function, then it will declare the HP-RDI defect condition if Bit 5 (within the G1 byte of the incoming STM-0 frame) is set to "1" for "HP-RDI_THRD" number of incoming consecutive STM-0 SPEs.
		If the Receive STM-0 POH Processor block is configured to support the Enhanced HP-RDI" (EHP-RDI) function, then it will declare the HP-RDI defect condition if		

1

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9 Bits 5, 6 and 7 (within the C1 byte of the incoming STM-0 frame) sets 10.1, 1, 0, 11, 0, 10, 11, 0, 10 (Th-RDI. THRD' number of consecutive STM-0 trames. 0 Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the HP-RDI defect condition. 1 Indicates that the Receive STM-0 POH Processor block is currently declaring the HP-RDI defect condition. Note: The user can specify the value for "HP-RD_THRD" by writing the receive STM-0 POH Processor block is currently declaring the HP-RDI defect condition. 2 HP-RDI RNO Unstable Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the HP-RDI musble' defect condition. The Receive STM-0 POH Processor block is currently declaring the HP-RDI unstable' defect condition whenever the HP-RDI Unstable' conflict whenever the HP-RDI Unstable' conflict is cleared to 0" whenever the same HP-RDO value's received the HP-RDI Unstable' conflict whenever the HP-RDI Unstable' conflict is cleared to 0" Whenever the HP-RDI Unstable' conflict. Note: Receiving a given HP-RDI value's in a HP-RDI value that differs from that of the previous STM-0 POH Processor block is currently declaring the "HP-RDI Unstable' defect condition. 1 LOP-P Note: Receiving a given HP-RDI value's in a HP-RDI value that differs from that of the previous STM-0 FOH Processor block is currently declaring the "HP-RDI Unstable' defect condition. 1 Indicates that the Receive STM-0 POH P				
1 LOP-P Declaring the HP-RD1 defect condition. 1 Indicates that the Receive STM-0 POH Processor block is currently declaring the HP-RD1 defect condition. Note: The user can specify the value for "HP-RD1 THRD" by within the "Receive STM-0 Path – SONET Receive HP-RD1 Register (Address Location- 0x/193). 2 HP-RD1 BrO (Part – Receive STM-0 Path – SONET Receive HP-RD1 Register (Address Location- 0x/193). 2 HP-RD1 Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the "HP-RD1 Unstable" defect condition. The Receive STM-0 POH Processor block will defect condition whenever the "HP-RD1 Unstable" defect condition whenever the "HP-RD1 Unstable" counter to instable to "o" whenever the same HP-RD1 value is received in "HP-RD1. THRD" consecutive STM-0 TeMP. ThRD1 value is that differe the "WHP-RD1 Unstable" counter is defect to "o" whenever the same HP-RD1 value, in "HP-RD1. THRD" consecutive STM-0 TeMP. ThRD1 value is received in "HP-RD1. THRD" consecutive STM-0 TeMP. ThRD1. THRD2 value is received in "HP-RD1. THRD" consecutive STM-0 TeMP. PR0. THRD2 value, in "HP-RD1. THRD2 value is received in "HP-RD1. THRD2 value is received in "HP-RD1. THRD" to ustable defect condition. 1 LOP-P Note: Receive STM-0 POH Processor block is currently declaring the "HP-RD1. THRD2 within the represense block will declare the LOP-P defect condition. 1 LOP-P Delect Declared Note: The user can specify the value for "HP-RD1. THRD2 within the represense block will declare the LOP-P defect c				
1 LOP-P R/O HP-RDI defect condition. 2 HP-RDI Unstable Defect Declared R/O HP-RDI (Path - Remote Defect Indicator) Unstable Defect Declared: 1 Unstable Defect Declared R/O HP-RDI (Path - Remote Defect Indicates whether or not the Receive STM-O POH Processor block is currently declaring the 'HP-RDI Unstable' defect condition. The Receive STM-O POH Processor block will declare the 'HP-RDI Unstable' defect condition whenever the 'HP-RDI Unstable' defect condition. The Receive STM-O POH Processor block will declare the 'HP-RDI Unstable' defect condition whenever the 'HP-RDI Unstable' counter is neares the value 'HP- RDI 'HRD'. The 'HP-RDI Unstable' counter is neares the value 'HP-RDI THRD' consecutive STM-O Transe. Note: Receive STM-O POH Processor block is currently declaring the 'HP-RDI Unstable' counter is neares the value for 'HP-RDI.THRD' consecutive STM-O transe also clears the bid-Reld to 'O'. 0 Indicates that the Receive STM-O POH Processor block is currently declaring the 'HP-RDI Unstable' defect condition. Note: The user can specify the value for 'HP-RDI.THRD' by writing the appropriate data wind Bits's a through O (HP-RDI THRD) writin the reproductive STM-O POH Processor block will certerely by within the specific data wind Bits's a through O (HP-RDI THRD) writing the specific data wind Bits's a through O (HP-RDI THRD') writing the reproductive SOME' Transe. Turker, the Receive STM-O POH Processor block will declare the LOP-P defect condition. 1 LOP-P Defect Declared The Receive STM-O POH Processor block will declare th				
0 Als-P 0 Als-P 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P Defect Declared R/O 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P 1 LOP-P 0 Als.P Defect Declared R/O 1 LOP-P 2 R/O 3 R/O 4 Receive STM-O POH Processor block receives an HP-RDI ustable' defect condition. The Receive STM-O POH Processor block receives an HP-RDI_THRD' consecutive STM-O Trames also clears this blacked to 'O'. 1 LOP-W 2 0 - Indicates that the Receive STM-O POH Processor block is currently declaring the "HP-RDI Unstable' defect condition. 1 LOP-P Defect Defect Declared R/O Loss of Pointer indicator (LOP-P) Defect Declared: This READ-ONLY bit-field indicates whether or				
Unstable Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the "HP-RDI Unstable" defect condition. The Receive STM-0 POH Processor block will deare the "HP-RDI Unstable" defect condition whenever the "HP-RDI Unstable" counter is neremented for each time that the Receive STM-0 POH Processor block receives an HP-RDI value that differs from that of the previous STM-0 frames. Note: Receive STM-0 POH Processor block receives an HP-RDI value that differs from that of the previous STM-0 frames. Note: Receive STM-0 POH Processor block is not currently declaring the "HP-RDI Unstable" counter is necervity STM-0 frames also clears file bit-field to "0". 0 Indicates that the Receive STM-0 POH Processor block is currently declaring the "HP-RDI Unstable" defect condition. 1 LOP-P Defect Declared R/O 1 LOSS of Pointer Indicator (LOP-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 LOP-P Defect Declared R/O Loss of Pointer Indicator (LOP-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block will declare the LOP-P defect condition, it is cancel detect a valid pointer (H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF elemts. 0 AIS-P Defect Declared R/O <td< td=""><td></td><td></td><td></td><td>appropriate data into Bits 3 through 0 (HP-RDI THRD) within the "Receive STM-0 Path – SONET Receive HP-RDI Register (Address</td></td<>				appropriate data into Bits 3 through 0 (HP-RDI THRD) within the "Receive STM-0 Path – SONET Receive HP-RDI Register (Address
Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the "HP-RDI Unstable" defect condition. The Receive STM-0 POH Processor block will declare the "HP-RDI Unstable" defect condition whenever the "HP-RDI Unstable" counter is noremented for each time that the Receive STM-0 POH Processor block will declare the "HP-RDI Unstable" consecutive STM-0 POH Processor block will declare the that differs from that of the previous STM-0 frame. The HP-RDI Unstable" counter is cleared to "0" whenever the same HP-RDI value in "HP-RDI_THRD" consecutive STM-0 <i>Trames also clears this bit-field</i> to "0". 0 - Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the "HP-RDI Unstable" defect condition. 1 LOP-P Defect Declared R/O 1 LOP-P Defect Declared R/O 0 AIS-P Defect Declared R/O 0 Loss of Pointer Indicator (LOP-P) Defect Declared: This READ-ONLP bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 LOP-P Defect The Receive STM-0 POH Processor block will declare the LOP-P defect condition. 1 LOP-P Defect R/O Loss of Pointer Indicator (LOP-P) Defect Declared: This READ-ONLP bit-field indicates whether or not the Receive STM-0 POH Processor block will declare the LOP-P defect condition. 1 LOP-P defect condition. The Receive STM-0 POH Processor block will declare the LOP-P	2		R/O	HP-RDI (Path – Remote Defect Indicator) Unstable Defect Declared:
1 LOP-P Defect Declared R/O Loss of Pointer Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the "HP-RDI Unstable defect condition. 1 I.OP-P Defect Declared R/O Loss of Pointer Indicator (LOP-P) Defect Declared: The Receive STM-0 POH Processor block is currently declaring the approvinate data (into Bits 3 through 0 (HP-RDI THRD) within the "Receive STM-0 Path – SONET Receive HP-RDI Register (Address Location= 0x/0193). 1 LOP-P Defect Declared R/O Loss of Pointer Indicator (LOP-P) Defect Declared: This READ ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 LOP-P Defect Declared R/O Loss of POH Processor block will declare the LOP-P defect condition, it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STM-0 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 AIS-P Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition. 0 AIS-P Defect Declared Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Pro		Defect		Processor block is currently declaring the "HP-RDI Unstable" defect condition. The Receive STM-0 POH Processor block will declare the "HP-RDI Unstable" defect condition whenever the "HP-RDI Unstable Counter" reaches the value "HP- RDI THRD". The "HP-RDI Unstable" counter is incremented for each time that the Receive STM-0 POH Processor block receives an HP-RDI value that differs from that of the previous STM-0 frame. The "HP-RDI Unstable" counter is cleared to "0" whenever the same HP-RDI value is received in "HP-RDI_THRD"
0 AIS-P Defect R/O AIS-P Defect condition. 0 AIS-P Defect R/O R/O 0 AIS-P Defect R/O R/O 0 AIS-P Defect R/O R/O 1 LOP-P Defect R/O R/O 1 LOP-P Defect R/O Loss of Pointer Indicator (LOP-P) Defect Declared: This READ ONLY bit-field indicates whether or not the Receive STM-0 POH Processor black is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 LOP-P Defect R/O Loss of Pointer Indicator (LOP-P) Defect Declared: This READ ONLY bit-field indicates whether or not the Receive STM-0 POH Processor black is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 LOP-P Defect The Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. 1 Indicates that the Receive STM-0 POH Processor block will chear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 AIS-P Defect Declared P ant AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block				
0 AIS-P Defect Declared R/O R/O Loss of Pointer Indicator (LOP-P) Defect Declared: The Receive STM-0 POH Processor block will declare the LOP-P defect condition, it is cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within the SOH) Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 0 AIS-P Defect Declared R/O R/O 0 AIS-P Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block will declare the LOP-P defect condition, it is cannot detect a valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 AIS-P Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition. The Receive STM-0				
0 Als-P Defect Declared R/O R Case of Pointer Indicator (LOP-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 0 Als-P Defect Declared R/O R R/O R R/O Pointer Indicator (LOP-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. 1 The Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. 1 The Receive STM-0 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 AlS-P Defect Declared R/O Path AlS (AlS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AlS-P defect condition. The Receive STM-0 POH Processor block will declare the AlS-P defect condition. The Receive STM-0 POH Processor block will declare the AlS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.				
0 AIS-P Defect Declared R/O R/O AIS-P Defect Declared R/O R/O AIS-P Defect Declared R/O Path AIS (AIS-P) Defect Declared: Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. The Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STM-0 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 – Indicates that the Receive STM-0 POH Processor block is NOT declaring the LOP-P defect condition. 1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition. 0 AIS-P Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.				appropriate data into Bits 3 through 0 (HP-RDI THRD) within the "Receive STM-0 Path – SONET Receive HP-RDI Register (Address
Declared Ins. READ-ONLY bit-field indicates whether or not the Receive S1M-0 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. The Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STM-0 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames. 0 AIS-P Defect Declared R/O 0 AIS-P Defect Declared R/O 0 AIS-P Defect Declared R/O 0 AIS-P Defect Declared R/O 0 AIS-P Defect Declared R/O 0 AIS-P Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.	1	LOP-P	R/O	Loss of Pointer Indicator (LOP-P) Defect Declared:
0 AIS-P Defect Declared R/O R/O R/O Path AIS (AIS-P) Defect Declared: Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block will declare the LOP-P defect condition.				Processor block is currently declaring the LOP-P (Loss of Pointer) defect
whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH) and normal NDF value for three consecutive incoming STM-0 frames.0 - Indicates that the Receive STM-0 POH Processor block is NOT declaring the LOP-P defect condition.1 - Indicates that the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition.0AIS-P Defect DeclaredR/OR/OPath AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.			the P	if it cannot detect a valid pointer (H1 and H2 bytes, within the SOH) within 8 to 10 consecutive SONET frames. Further, the Receive STM-0 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF
0 AIS-P R/O Path AIS (AIS-P) Defect Declared: 0 AIS-P Defect Defect Declared 0 AIS-P R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.				whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the SOH)
0 AIS-P Defect Defect Declared R/O Path AIS (AIS-P) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.				-
Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.				
Declared This READ-ONLY bit-field indicates whether or not the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STM-0 frames.	0		R/O	Path AIS (AIS-P) Defect Declared:
The H1, H2 and H3 bytes are set to an "All Ones" pattern.				Processor block is currently declaring the AIS-P defect condition. The Receive STM-0 POH Processor block will declare the AIS-P defect condition if it detects all
				• The H1, H2 and H3 bytes are set to an "All Ones" pattern.



The entire SPE is set to an "All Ones" pattern.
The Receive STM-0 POH Processor block will clear the AIS-P defect condition when it detects a valid STM-0 pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive STM-0 frames.
0 – Indicates that the Receive STM-0 POH Processor block is NOT currently declaring the AIS-P defect condition.
1 – Indicates that the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition.
Note: The Receive STM-0 POH Processor block will NOT declare the LOP-P defect condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.





Table 509: Receive STM-0 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0
			~		nis	ed	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	6 1 4 2 C
4	Detection of AIS Pointer	RUR	Detection of AIS Pointer Interrupt Status:
	Interrupt Status		This RESET upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STM-0 data stream.
		A	Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the SOH) are each set to an "All Ones" pattern.
		01	0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register.
	AUC [®]	30	16 Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change	RUR	Detection of Pointer Change Interrupt Status:
	Detection of Pointer Change Interrupt Status	124	This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the SOH bytes).
			0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	Unused	R/O	
1	Change in TIM-P Defect Condition Interrupt Status	RUR	Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.
			This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of



			the following events.
			• Whenever the Receive STM-0 POH Processor block declares the TIM-P defect condition.
			• Whenever the Receive STM-0 POH Processor block clears the TIM-P defect condition.
			0 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.
0	Change in Path Trace Message Unstable Defect	RUR	Change in "Path Trace Identification Message Unstable Defect Condition" Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt in response to either of the following events.
			Whenever the Receive STM-0 POH Processor block declare the "Path Trace Message Unstable" Defect Condition.
			 Whenever the Receive STM-0 POH Processor block clears the "Path Trace Message Unstable" defect condition.
			0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
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3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - SDH REGISTERS



Table 510: Receive STM-0 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Status	Detection of HP-REI Event Interrupt Status	Change in HP-UNEQ Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in HP-RDI Unstable Defect Condition Interrupt Status	New HP-RDI Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

			<u> </u>
BIT NUMBER	ΝΑΜΕ	Түре	
7	New Path Trace	RUR	New Path Trace Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted (or validated) a new Path Trace Message.
			0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of HP-	RUR	Detection of HP-REI Event Interrupt Status:
	REI Event Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of HP-REI Event" Interrupt has occurred since the last read of this register.
		orodu	If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an HP-REI event within the incoming STM-0 data-stream.
			02- Indicates that the "Detection of HP-REI Event" Interrupt has NOT occurred since the last read of this register.
	The	10	1.9 Indicates that the "Detection of HP-REI Event" Interrupt has occurred since the last read of this register.
5	Change in HP- UNEQ Defect	RUR	Change in HP-UNEQ (Path – Unequipped) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in HP-UNEQ Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			• When the Receive STM-0 POH Processor block declares the HP-UNEQ Defect Condition.
			• When the Receive STM-0 POH Processor block clears the HP-UNEQ Defect Condition.
			0 – Indicates that the "Change in HP-UNEQ Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in HP-UNEQ Defect Condition" Interrupt has



			occurred since the last read of this register.
			_
			Note: The user can determine if the Receive STM-0 POH Processor block is currently declaring the HP-UNEQ defect condition by reading out the state of Bit 5 (HP-UNEQ Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
4	Change in PLM-P Defect	RUR	Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STM-0 POH Processor block declares the "PLM-P" Defect Condition.
			• When the Receive STM-0 POH Processor block clears the "PLM-P" Defect Condition.
			0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon-BEAD bit field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
		J.	1 - Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2	RUR	Change in C2 Byte Unstable Defect Condition Interrupt Status:
	Byte Unstable Defect Condition Interrupt Status	shee	This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.
	Theat		If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			• When the Receive STM-0 POH Processor block declares the "C2 Byte Unstable" defect condition.
			• When the Receive STM-0 POH Processor block clears the "C2 Byte Unstable" defect condition.
			0 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine whether or not the Receive STM-0 POH Processor block is currently declaring the "C2 Byte Unstable Defect Condition" by reading out the state of Bit 6 (C2 Byte Unstable Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
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1	Change in HP-	RUR	Change in HP-RDI Unstable Defect Condition Interrupt Status:
	RDI Unstable Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in HP-RDI Unstable Defect Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			• When the Receive STM-0 POH Processor block declares an "HP-RDI Unstable" defect condition.
			• When the Receive STM-0 POH Processor block clears the "HP-RDI Unstable" defect condition.
			0 – Indicates that the "Change in HP-RDI Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in HP-RDI Unstable Defect Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of "HP-RDI Unstable Defect condition" by reading out the state of Bit 2 (HP-RDI Unstable Defect Condition) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187)
0	New HP-RDI Value Interrupt Status	RUR	New HP-RDI Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New HP-RDI Value" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it receives and "validates" a new HP-RDI value. 0 – Indicates that the "New HP-RDI Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New HP-RDI Value" Interrupt has occurred since the last read of this register.
		odu	Note: The user can obtain the "New HP-RDI Value" by reading out the contents of the "HP-RDI ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STM-0 Path – SONET Receive HP-RDI Register" (Address Location= 0xN193).
	the	e si	Contents of the "HP-RDI ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STM-0 Path – SONET Receive HP-RDI Register" (Address Location= 0xN193).



Table 511: Receive STM-0 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B, where N ranges in value 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Status	RUR	 Detection of B3 Byte Error Interrupt Status: This RESET-upon-READ bitfield indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STM-0 data stream. 0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt. 1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of New Pointer Interrupt Status	RUR	 Detection of New Pointer Interrupt Status: This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STM-0 frame. Note: Pointer Adjustments with NDF will not generate this interrupt. 0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of Unknown Pointer Interrupt Status	RUR	 Detection of Unknown Pointer Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories. An Increment Pointer An ODF Pointer An AIS (e.g., All Ones) Pointer New Pointer

			0 Indicates that the "Detection of Linkneys Deinter" interrupt has NOT
			0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer	RUR	Detection of Pointer Decrement Interrupt Status:
	Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer	RUR	Detection of Pointer Increment Interrupt Status:
	Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF	RUR	Detection of NDF Pointer Interrupt Status:
	Pointer Interrupt Status	duct	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
	Q	she	0 – Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
	110 33		1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P Defect Condition	RUR	Change of LOP-P Defect Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive STM-0 POH Processor block declares the LOP-P defect condition.
			• Whenever the Receive "STM-0 POH Processor" block clears the LOP-P defect condition.
			0 – Indicates that the "Change in LOP-P Defect Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in LOP-P Defect Condition" interrupt has



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			occurred since the last read of this register.	
			Note: The user can determine if the Receive STM-0 POH Processor block is currently declaring the LOP-P defect condition by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" Register (Address Location=0xN187).	
0	Change of AIS-P	RUR	Change of AIS-P Defect Condition Interrupt Status:	
	Defect Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register.	
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.	
			• Whenever the Receive STM-0 POH Processor block declares the AIS-P defect condition.	
			• Whenever the Receive STM-0 POH Processor block clears the AIS-P defect condition.	
			0 – Indicates that the Change of AIS-P Defect Condition" Interrupt has NOT occurred since the last read of this register.	
			1 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register.	
			Note: The user can determine if the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).	
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reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0 Register (Address Location= 0xN187).				



Table 512: Receive STM-0 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location = 0xN18D, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0
					is	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7-5	Unused	R/O	A TR act
4	Detection of AIS Pointer	R/W	Detection of AIS Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE Dit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt.
			If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STM-0 data stream.
			Note: An "AIS Pointer" is defined as a condition in which both the H and H2 bytes (within the SOH) are each set to an "All Ones" Pattern.
			O - Disables the "Detection of AIS Pointer" Interrupt.
			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:
	Change Interrupt Enable	sheet a	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.
	The data		If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.
			0 – Disables the "Detection of Pointer Change" Interrupt.
			1 - Enables the "Detection of Pointer Change" Interrupt.
2	Unused	R/O	
1	Change in TIM-P Defect Condition Interrupt	R/W	Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive STM-0 POH Processor block declares the TIM-P defect condition.
			• Whenever the Receive STM-0 POH Processor block clears the TIM-P defect condition.



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			0 – Disables the "Change in TIM-P Defect Condition" Interrupt.
			1 – Enables the "Change in TIM-P Defect Condition" Interrupt.
0	Change in Path Trace Message Unstable	R/W	Change in Path Trace Message" Unstable Defect Condition" Interrupt Status:
	Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in Path Trace Message Unstable Defect Condition" Interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			• Whenever the Receive STM-0 POH Processor block declares the "Path Trace Message Unstable Defect" Condition.
			• Whenever the Receive STM-0 POH Processor block clears the "Path Trace Message Unstable Defect" Condition.
			0 – Disables the "Change in Rath Trace Message Unstable Defect Condition" interrupt.
			1 – Enables the "Change in Path Trace Message Unstable Defect Condition" interrupt

1 - Enables the "Change Condition" interrupt.



Table 513: Receive STM-0 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New Path Trace Message Interrupt Enable	Detection of HP-REI Event Interrupt Enable	Change in HP-UNEQ Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in HP-RDI Unstable Defect Condition Interrupt Enable	New HP-RDI Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	[<u>s</u>
BIT NUMBER	Nаме	ΤΥΡΕ	DESCRIPTION
7	New Path Trace	R/W	New Path Trace Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message.
			0 – Disables the "New Path Trace Message" Interrupt.
			1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of HP-REI	R/W	Detection of HP-RELEvent Interrupt Enable:
	Event Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of HP-REI Event" Interrupt.
		*	If this interrupt is enabled, then he Receive STM-0 POH Processor block will generate an interrupt anytime it detects an HP-REI event within the coming STM-0 data-stream.
		C.	Disables the "Detection of HP-REI Event" Interrupt.
		,0°,¢	1 - Enables the "Detection of HP-REI Event" Interrupt.
5	Change in HP-UNEQ Defect Condition	R/W	Change in HP-UNEQ (Path – Unequipped) Defect Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in HP-UNEQ Defect Condition" interrupt.
	•	31.	If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive STM-0 POH Processor block declares the HP-UNEQ Defect Condition.
			• Whenever the Receive STM-0 POH Processor block clears the HP-UNEQ Defect Condition.
			0 – Disables the "Change in HP-UNEQ Defect Condition" Interrupt.
			1 – Enables the "Change in HP-UNEQ Defect Condition" Interrupt.
4	Change in PLM-P Defect Condition	R/W	Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt.



			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive STM-0 POH Processor block declares the "PLM-P" defect Condition.
			• Whenever the Receive STM-0 POH Processor block clears the "PLM-P" defect Condition.
			0 – Disables the "Change in PLM-P Defect Condition" Interrupt.
			1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte	R/W	New C2 Byte Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Beceive STM-0 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New 22 Byte" Interrupt.
			Note: The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STM-0 Path – Received Path Label Value" Register (Address Location= 0xN196).
2	Change in C2 Byte Unstable Defect	R/W	Change in C2 Byte Instable Defect Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Condition" Interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
		101	When the Receive STM-0 POH Processor block declares the "C2 Byte Unstable defect" condition.
			• When the Receive STM-0 POH Processor block clears the "C2 Byte Unstable defect" condition.
	Jode Land	ee' n	Disables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
	neras	max	1 – Enables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
1	Change in HP-RDI Unstable Defect	R/W	Change in HP-RDI Unstable Defect Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in HP-RDI Unstable Defect Condition" interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following conditions.
			• Whenever the Receive STM-0 POH Processor block declares the "HP-RDI Unstable defect" condition.
			• Whenever the Receive STM-0 POH Processor block clears the "HP-RDI Unstable defect" condition.
			0 – Disables the "Change in HP-RDI Unstable Defect Condition" Interrupt.
			1 – Enables the "Change in HP-RDI Unstable Defect Condition" Interrupt.



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0	New HP-RDI Value Interrupt Enable	R/W	New HP-RDI Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New HP-RDI Value" interrupt.
			If this interrupt is enabled, then the Receive STM-0 POH Processor block will generate this interrupt anytime it receives and "validates" a new HP-RDI value.
			0 – Disables the "New HP-RDI Value" Interrupt.
			1 – Enable the "New HP-RDI Value" Interrupt.

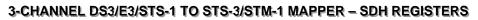
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Table 514: Receive STM-0 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Defect Condition Interrupt Enable	Change of AIS-P Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7	Detection of	R/W	Detection of B3 Byte Error Interrupt Enable
	B3 Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STM-0 data-stream.
			0 – Disables the "Detection of B3 Byte Error" interrupt.
			1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of	R/W	Detection of New Pointer Interrupt Enable:
	New Pointer Interrupt Enable		This READ/WRITE bitfield permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive STM 0 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STM-0 frame.
			Note: Pointer Adjustments with NDF will not generate this interrupt.
			0 – Disables the "Detection of New Pointer" Interrupt.
			1 – Enables the "Detection of New Pointer" Interrupt.
5	Detection of	R/W	Detection of Unknown Pointer Interrupt Enable:
	Unknown Pointer Interrupt Enable	Pro ata	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories.
		5	An Increment Pointer.
			A Decrement Pointer
			An NDF Pointer
			AIS Pointer
			New Pointer.
			0 – Disables the "Detection of Unknown Pointer" Interrupt.
			1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of	R/W	Detection of Pointer Decrement Interrupt Enable:
	Pointer Decrement Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STM-0 SOH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event.



			0 – Disables the "Detection of Pointer Decrement" Interrupt.
			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of	R/W	Detection of Pointer Increment Interrupt Enable:
	Pointer Increment Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Disables the "Detection of Pointer Increment" Interrupt.
			1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer	R/W	Detection of NDF Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
			0 – Disables the "Detection of NDF Pointer" interrupt.
			1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of	R/W	Change of LOP-P Defect Condition Interrupt Enable:
	LOP-P Defect Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Defect Condition interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			 Whenever the Receive STM-0 POH Processor block declares the LOP-P defect condition condition.
			 Whenever the Receive STM-0 POH Processor block clears the LOP-P defect condition 0 – Disable the "Change of LOP-P Defect Condition" Interrupt.
			1 – Enables the "Change of LOP-P Defect Condition" Interrupt.
		Q	Note: The user can determine if the Receive STM-0 POH Processor block is ourrently declaring the LOP-P defect condition by reading out the contents of Bit 1 (LOP-P Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).
0	Change of	R/W	Change of AIS-P Defect Condition Interrupt Enable:
	AIS-P Defect Condition Interrupt Enable	, 9 ₅	This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-P (Path AIS)" Defect Condition interrupt. If the user enables this interrupt, then the Receive STM-0 POH Processor block will generate an interrupt in response to either of the following events.
			Whenever the Receive STM-0 POH Processor block declares the AIS-P Defect condition.
			Whenever the Receive STM-0 POH Processor block clears the AIS-P Defect condition.
			0 – Disables the "Change of AIS-P Defect Condition" Interrupt.
			1 – Enables the "Change of AIS-P Defect Condition" Interrupt.
			Note: The user can determine if the Receive STM-0 POH Processor block is currently declaring the AIS-P defect condition by reading out the contents of Bit 0 (AIS-P Defect Declared) within the "Receive STM-0 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).



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Table 515: Receive STM-0 Path – SONET Receive HP-RDI Register (Address Location= 0xN193, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused	Unused HP-RDI_ACCEPT[2:0]			HP-RDI THRESHOLD[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Unused	R/O	
6 - 4	HP-RDI_ACCEPT[2:0]	R/O	 Accepted HP-RDI Value: These READ-ONLY bit-fields contain the value of the most recently "accepted" HP-RDI (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive STM-0 POH Processor block. Note: A given HP RDI value will be "accepted" by the Receive STM-0 POH Processor block, if this HP-RDI value has been consistently received in "HP-RDI THRESHOLD[3:0]" number of STM-0 frames.
3 - 0	HP-RDI THRESHOLD[3:0]	R/W	HP-RDI Threshold[3:0]: These READ/WRITE bit-fields permit the user to defined the "HP- RDI Acceptance Threshold" for the Receive STM-0 POH Processor Block. The "HP-RDI Acceptance Threshold" is the number of consecutive STM-0 frames, in which the Receive STM-0 POH Processor block must receive a given HP-RDI value, before it "accepts" or "validates" it The most recently "accepted" HP-RDI value is written into the "HP- RDI ACCEPT[2:0]" bit-fields, within this register.

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Table 516: Receive STM-0 Path – Received Path Label Value (Address Location= 0xN196, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Received_C2_Byte_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
1	1	1	1	1	1	1	1		

BIT NUMBER	Nаме	Түре	DESCRIPTION					
7 – 0	Received C2 Byte Value[7:0]	R/O	Received "Filtered" C2 Byte Value:					
			These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STM-0 POH Processor block. The Receive STM-0 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in tive (5) consecutive STM-0 frames. Note: The Receive STM-0 POH Processor block uses this register, along the "Receive STM-0 Path – Expected Path Label Value" Register (Address Location = 0xN197), when declaring or clearing the HP-UNEQ and PLM-P defect conditions.					
	s beiles							

Table 517: Receive STM-0 Path – Expected Path Laber Value (Address Location= 0xN197, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0		
Expected_C2_Byte_Value[7:0]									
R/W	R/W	R/W 📢	R/W	R/W	R/W	R/W	R/W		
1									

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value:
	The atand m		These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STM-0 POH Processor block should expect when declaring or clearing the HP-UNEQ and PLM-P defect conditions.
			If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STM-0 Path – Received Path Label Value" register) matches the contents in these register, then the Receive STM-0 POH will not declare any defect conditions.
			Note: The Receive STM-0 POH Processor block uses this register, along with the "Receive STM-0 Path – Receive Path Label Value" Register (Address Location = 0xN196), when declaring or clearing the HP-UNEQ and PLM-P defect conditions.

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Table 518: Receive STM-0 Path -B3 Byte Error Count Register -Byte 3 (Address Location= 0xN198, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B3_Byte_Error_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	B3_Byte_Error_Count[31:24]	RUR	B3 Byte Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STM-0 Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.
			2. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.
	the biasher	or pro-	be not end



Table 519: Receive STM-0 Path -B3 Byte Error Count Register -Byte 2 (Address Location= 0xN199, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
B3_Byte_Error_Count[23:16]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B3_Byte_Error_Count[23:16]	RUR	B3 Byte Error Count (Bits 23 through 16):
			 This RESET-upon-READ register, along with "Receive STM-0 Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error. <i>Note:</i> If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.
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Table 520: Receive STM-0 Path - B3 Byte Error Count Register - Byte 1 (Address Location= 0xN19A, wher N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
B3_Byte_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B3_Byte_Error_Count[15:8]	RUR	B3 Byte Error Count – (Bits 15 through 8):
			This RESET-upon-READ register, along with "Receive STM-0 Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.
			2. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte.
	The product	eet nor of the set of	this 32-bit counter each time that it receives an STM-0 SPE that contains an erred 83 byte.



Table 521: Receive STM-0 Path -B3 Byte Error Count Register -Byte 0 (Address Location= 0xN19B, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
B3_Byte_Error_Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	B3_Byte_Error_Count[7:0]	RUR	B3 Byte Error Count - LSB:
			This RESET-upon-READ register, along with "Receive STM-0 Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a B3 byte error.
			Note:
			1. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STM-0 SPE) that are in error.
			2. If the Receive STM-0 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains an erred B3 byte
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Table 522: Receive STM-0 Path – HP-REI Event Count Register – Byte 3 (Address Location= 0xN19C, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI Event_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	HP-REI Event	RUR	HP-REI Event Count – MSB:
	Count[31:24]		This RESET-upon-READ register, along with "Receive STM-0 Path – HP-REI Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path - Remote Error Indicator event within the incoming STM-0 SPE data-stream.
			Note:
			1. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the hibble-value within the HP-REI field of the incoming G1 byte within each incoming STM-0 SPE.
			2. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-0 SPE that contains a "non-zero" HP-REI value.
	rotur	eet n	this 32-bit counter each time that it receives an STM-0 SPE that contains a 'non-zero" HP-REI value.
	the para si	may	



Table 523: Receive STM-0 Path – HP-REI Event Count Register – Byte 2 (Address Location= 0xN19D, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI_Event_Count[23:16]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	HP-REI Event_Count[23:16]	RUR	HP-REI Event Count (Bits 23 through 16):
			 This RESET-upon-READ, register, along with "Receive STM-0 Path – HP-REI Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path – Remote Error Indicator event within the incoming STM-0 SPE data-stream. <i>Note:</i> If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the HP-REI field of the incoming G1 byte within each incoming STM-0 frame. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the HP-REI field of the incoming G1 byte within each incoming STM-0 frame. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-0 SPE that contains a "non-zero" HP-REI value.

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Table 524: Receive STM-0 Path – HP-REI Event Count Register – Byte 1 (Address Location= 0xN19E, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HP-REI_Event_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	HP-REI Event_Count[15:8]	RUR	HP-REI Event Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive STM-0 Path – HP-REI Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path –Remote Error Indicator event within the incoming STM-0 SPE data-stream.
			Note:
			1. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-bit" basis, then it will increment this 32-bit counter by the hibble-value within the HP-REI field of the incoming G1 byte within each incoming STM-0 SPE.
			2. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STM-0 SPE that contains a non-zero HP-REI value.
	The produce	eet nor	this 32-bit counter each time that it receives an STM-0 SPE that contains a non-zero HP-REI value.

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Table 525: Receive STM-0 Path – HP-REI Event Count Register – Byte 0 (Address Location= 0xN19F, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	HP-REI_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
Віт Number 7 - 0	NAME HP- REI_Event_Count[7:0]	Type RUR	 HP-REI Event Count – LSB: This RESET-upon-READ register, along with "Receive STM-0 Path – HP-REI Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STM-0 POH Processor block detects a Path – Remote Error Indicator event within the incoming STM-0 SPE data-stream. Note: 1. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-bit" basis, then it will increment this 32 bit
			 counter by the nibble-value within the HP-REI field of the incoming G1 byte. 2. If the Receive STM-0 POH Processor block is configured to count HP-REI events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STM-0 SPE that contains a "non-zero" HP-REI value.

2. If the HP-REI & counter ex zero" HP-H

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Table 526: Receive STM-0 Path – Receive Path Trace Message Buffer Control Register (Address Location= 0xN1A3, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	Message T Ready Me Buffe		Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Type	Receive Path Message Len	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION	
7 – 6	Unused	R/O	is eo	
5	New Message Ready	R/O	New Message Ready: This READ/WRITE bit-field indicates whether or not the Receive STM-0 POH Processor block has (1) accepted a new Receive Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register.	
			 0 – Indicates that the Receive STM-0 POH Processor block has (1) NOT accepted a new Path Trace Message, nor (2) has the Receive STM-0 POH Processor block loaded any new message into the Receive Path Trace Message buffer, since the last read of this register. 1 – Indicates that the Receive STM-0 POH Processor block has (1) accepted a new Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last 	
4	Possive Path Trace	P/W	read of this register.	
4	Receive Path Trace Message Buffer Read Select	R/W	G a	Receive Path Trace Message Buffer Read Selection: This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Path Trace Message Buffer.
	Select	dmax	a. The "Actual" Receive Path Trace Message Buffer. The "Actual" Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STM-0 data-stream.	
	·0·		b. The "Expected" Receive Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user "expects" to receive. The contents of this particular buffer are usually specified by the user.	
			0 – Executing a READ to the Receive Path Trace Message Buffer, will return contents within the "Actual" Receive Path Trace Message buffer.	
			1 – Executing a READ to the Receive Path Trace Message Buffer will return contents within the "Expected Receive Path Trace Message Buffer".	
			Note: In the case of the Receive STM-0 POH Processor block, the "Receive Path Trace Message Buffer" is located at Address Location 0xN500 through 0xN53F.	



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3	Path Trace Message	R/W	Path Trace Messag	ge Accept Threshold:
	Accept Threshold		consecutive times must receive a give	bit-field permits a user to select the number that the Receive STM-0 POH Processor bloc ven Receive Path Trace Message, before it ed into the "Actual" Receive Path Trace Messag below.
				Receive STM-0 POH Processor block to acce Trace Message after it has received it the thin
				Receive SONET POH Processor block to acce Trace Message after it has received in the fif
2	Path Trace Message	R/O	Path Trace Messag	ge Alignment Type:
	Alignment Type		STM-0 POH Proces	bit-field permits a user to specify how the Receives ssor block will locate the boundary of the incomir ge (within the incoming STM-0 data-stream), a
				Receive STM-0 POH Processor block to expe ssage boundary to be denoted by a "Line Fee
			the Path Trace Mes a "1" in the MSB (m incoming Path Tra	Receive STM-0 POH Processor block to expense sage boundary to be denoted by the presence tost significant bit) of the very first byte (within the Message). In this case, all of the remaining poming Path Trace Message) will each have a "for
1 – 0	Receive Path Trace	R/W	Receive Path Trac	e Message Length[1:0]:
	Message Length[1:0]	0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0	These READ/WRIT the Receive Path Processor block wi Trace Message Bu these bit-fields and Length is presented	E bit-fields permit the user to specify the length Trace Message that the Receive STM-0 PO II accept and load into the "Actual" Receive Par uffer. The relationship between the content the corresponding Receive Path Trace Message I below.
	The proshe	131	Receive Path Trace Message Length[1:0]	Resulting Path Trace Message Length (in terms of bytes)
	9.0 40		00	1 Byte
	<u>र</u>		01	16 Bytes
			10/11	64 Bytes
L	l			

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Table 527: Receive STM-0 Path – Pointer Value – Byte 1 (Address Location= 0xN1A6, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						ointer Value [9:8]
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[7:0]	R/O	Current Pointer Value - MSB: These READ-ONLY bit-fields, along with that from the "Receive STM-0 Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive STM-0 POH Processor" block is using to locate the SPE within the incoming STM-0 data stream. Note: These register bits comprise the Upper Byte value of the Pointer Value.

Table 528: Receive STM-0 Path – Pointer Value – Byte 0 (Address Location= 0xN1A7, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3	Віт 2	Віт 1	Віт 0		
			Current_Pointer_Value_LSB[7]	:0]				
R/O	R/O	R/O	R/0 R/0	R/O	R/O	R/O		
0	0	0	0 0 0	0	0	0		

BIT NUMBER		DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0] R/O	Current Pointer Value – LSB: These READ-ONLY bit-fields, along with that from the "Receive STM-0 Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STM-0 POH Processor" block is using to locate the SPE within the incoming STM-0 data stream.
	'0	<i>Note:</i> These register bits comprise the Lower Byte value of the Pointer Value.



Table 529: Receive STM-0 Path – AUTO AIS Control Register (Address Location= 0xN1BB, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (Down- stream) Upon C2 Byte Unstable	Transmit AIS-P (Down- stream) Upon HP- UNEQ	Transmit AIS-P (Down- stream) Upon PLM- P	Transmit AIS-P (Down- stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down- stream) upon TIM-P	Transmit AIS-P (Down- stream) upon LOP-P	Transmit AIS-P (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	<u>I </u>	I	····
BIT NUMBER	Nаме	Түре	DESCRIPTION
7	Unused	R/O	in cth
6	Transmit AIS-P (Downstream) upon C2 Byte Unstable	R/W	 Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the Unstable C2 Byte Detect Condition: This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the Unstable C2 Byte Defect condition within the "incoming" STM-0 data-stream. 0 – Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor
	Transmit AIS-P (Downstream) upon HP-		 Block whenever it declares the "Unstable C2 Byte" defect condition. Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Unstable C2 Byte" defect condition. Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Downstream) upon HP- UNEQ	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the HP-UNEQ (Path – Unequipped) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the HP-UNEQ defect condition.
			0 – Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the HP-UNEQ defect condition.
			1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the HP-UNEQ



			defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Downstream) upon PLM-P	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the PLM-P (Path – Payload Label Mismatch) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the PLM-P defect condition.
			0 – Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the PLM-P defect condition.
			1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the PLM-P defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Transmit AIS-P (Downstream) upon Path Trace Message	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon declaration of the Path Trace Message Unstable Defect Condition:
	Unstable	uct of	This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STM-0 data-stream.
	the pro	d may	0 – Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Path Trace Message Unstable" defect condition.
	ୖୖୖ		1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Path Trace Message Unstable" defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	Transmit Path AIS (Downstream towards the corresponding Transmit SONET POH Processor block) upon declaration of the TIM-P (Path Trace Message Indentification Mismatch) defect condition:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit a Path AIS



			(AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the TIM-P defect condition
			within the incoming STM-0 data-stream.
			0 – Does not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards the corresponding Transmit SONET POH Processor block) whenever it declares the TIM-P defect condition.
			1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the TIM-P defect condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P (Downstream) upon LOP-P	R/W	Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Detection of Loss of Pointer (LOP-P) Defect Condition:
			This READ/WRITE bit-field permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STM-0 data-stream.
		are	0 Cover not configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the LOP-P defect condition.
	eproduct	ore	1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the LOP-P defect condition.
	the tail	lay no	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	Transmit AIS-P (Downstream) Enable	R/W	Automatic Transmission of AIS-P Enable:
			This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STM-0 POH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), upon declaration of either an HP- UNEQ, PLM-P, LOP-P or LOS defect condition.
			It also permits the user to configure the Receive STM-0 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks) anytime it declares the AIS-P defect condition within the "incoming " STM-0 data-stream.
			0 – Configures the Receive STM-0 POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares any of the "above-mentioned" defect



conditions.
1 – Configures the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares any of the "above-mentioned" defect condition.
Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STM-0 POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.

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Table 530: Receive STM-0 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (via Downstream STM-0s) upon LOP-P	Transmit AIS-P (via Downstream STM-0s) upon PLM-P	Unused	Transmit AIS-P (via Downstream STM-0s) upon HP- UNEQ	Transmit AIS-P (via Downstream STM-0s) upon TIM-P	Transmit AIS-P (via Downstream STM-0s) upon AIS-P	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	
7	Unused	R/W	th ure
6	Transmit AIS-P (via Downstream STM-0s) upon LOP-P	R/O	 Transmit AIS-P (via Downstream STM-0s) upon declaration of the LOP-P defect condition: This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the LOP-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the LOP-P defect condition.
5	Transmit AIS-P (via Downstream STM-0s) upon PLM-P	RAN	 Transmit AIS-P (via Downstream STM-0s) upon declaration of the PLM-P defect condition: This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, anytime (and for the duration that) the Receive STM-0 POH Processor block declares the PLM-P defect condition. 0 - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the PLM-P defect condition. 1 - Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the PLM-P defect condition.
4	Unused	R/O	
3	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STM-0s) upon declaration of the



	Downstream STM-0s)		HP-UNEQ defect condition:
	upon HP-UNEQ		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal, (within the outbound STM-1 signal) anytime (and for the duration that) the Receive STM-0 POH Processor block declares the HP-UNEQ defect condition.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the HP- UNEQ defect condition.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the HP-UNEQ defect condition.
2	Transmit AIS-P (via Downstream STM-0s)	R/W	Transmit AIS-P (via Downstream STM-0s) upon declaration of the TIM-P defect condition:
	upon TIM-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the TIM-P defect condition.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the TIM-P defect condition.
	8	Jut 2	- Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the TIM-P defect condition.
1	Transmit AIS-P (via O Downstream STM-0s)	RXX	Transmit AIS-P (via Downstream STM-0s) upon declaration of the AIS-P defect condition:
	upon AIS-P	dno	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the AIS-P defect condition.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal (within the outbound STM-1 signal), anytime the Receive STM-0 POH Processor block declares the AIS-P defect condition.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STM-0 signal A(within the outbound STM-1 signal), anytime (and for the duration that) the Receive STM-0 POH Processor block declares the AIS-P defect condition.
0	Unused	R/O	



Table 531: Receive STM-0 Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
J1_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION			
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	J1 Byte Captured Value[7:0]			
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new J1 byte value.			

Table 532: Receive STM-0 Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0		
	B3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/Q	R/0	R/O	R/O	R/O		
0	0	0		0	0	0	0		
	100 19 e0								

BIT NUMBER	NAME	Type	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	B3 Byte Captured Value[7:0]
	Auct art		These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STM-0 frame.
	e prosheet n		This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new B3 byte value.
	11, 93, 10 h.		

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Table 533: Receive STM-0 Path – Receive C2 Byte Capture Register (Address Location= 0xN1DB, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
C2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	C2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STM-0 frame.
			This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new C2 byte value.

Table 534: Receive STM-0 Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF, where N ranges in value from 0x05 to 0x07)

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Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0		
G1_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	RO	R/O	R/O	R/O		
0	0	0	0 🗸	0,0	0	0	0		
	8° 8°								

BIT NUMBER	NAME	Т	PF	0	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R	•	Th wit Th fra	Byte Captured Value[7:0] ese READ-ONLY bit-fields contain the value of the G1 byte, nin the most recently received STM-0 frame. s particular value is stored in this register for one STM-0 me period. During the next STM-0 frame period, this value be overridden with a new G1 byte value.
	The stad ma	9			

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Table 535: Receive STM-0 Path – Receive F2 Byte Capture Register (Address Location=0xN1E3, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	F2_Byte_Captured_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	F2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new F2 byte value.

Table 536: Receive STM-0 Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/0	R/O	R/O	R/O
0	0	0		0	0	0	0

BIT NUMBER		Түре	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	H4 Byte Captured Value[7:0]
	uct are	pe	These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STM-0 frame.
	prosheetin	5	This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new H4 byte value.
	The atan me		

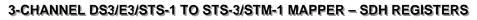




Table 537: Receive STM-0 Path - Receive Z3 Byte Capture Register (Address Location= 0xN1EB, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Z3_Byte_Captured_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Z3 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new Z3 byte value.

ed Table 538: Receive STM-0 Path - Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF, where N ranges in value from 0x05 to 0x07) 6 2

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Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0	
Z4(K3)_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O 🏓	R/0	R/O	R/O	R/O	
0	0	0	0	0 0	0	0	0	

BIT NUMBER	NAME	Түре	X [©]	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[71]	R/O C DC	These (K3) b This p frame	3) Byte Captured Value[7:0] e READ-ONLY bit-fields contain the value of the Z4 byte, within the most recently received STM-0 frame. particular value is stored in this register for one STM-0 period. During the next STM-0 frame period, this will be overridden with a new Z4 (K3) byte value.
	The at and me			



Table 539: Receive STM-0 Path – Receive Z5 Byte Capture Register (Address Location= 0xN1F3, where N ranges in value from 0x05 to 0x07)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Z5_Byte_Captured_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STM-0 frame. This particular value is stored in this register for one STM-0 frame period. During the next STM-0 frame period, this value will be overridden with a new Z5 byte value.

ins particular value is frame period. During the will be overridden with a

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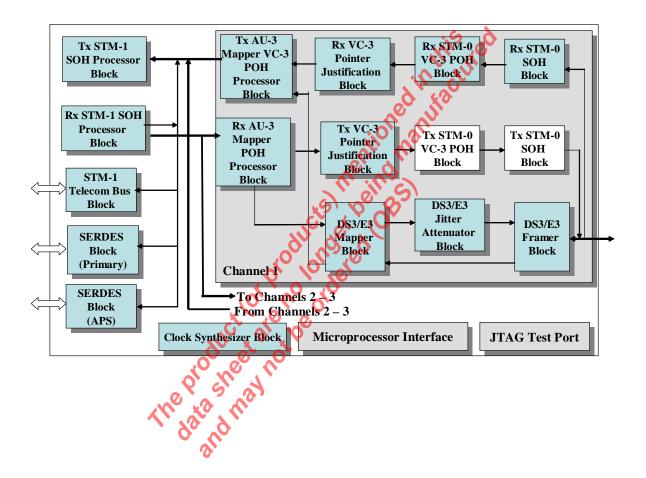


1.14 TRANSMIT STM-0 SOH AND POH PROCESSOR BLOCK

The register map for the Transmit STM-0 SOH and POH Processor Blocks are presented in the Table below. Additionally, a detailed description of each of the "Transmit STM-0 SOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STM-1 SOH Processor Block "highlighted" is presented below in **Figure 4**

Figure 11: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit STM-0 SOH and POH Processor Blocks "High-lighted".





TRANSMIT STM-0 SOH AND POH PROCESSOR BLOCK REGISTER

Table 540: Transmit STM-0 SOH and POH Processor Block Registers – Address Map

Address Location	REGISTER NAME	DEFAULT VALUES
0xN800 – 0xN901	Reserved	0x00
0xN902	Transmit STM-0 Section – SONET Transmit Control Register – Byte 1	0x00
0xN903	Transmit STM-0 Section – SONET Transmit Control Register – Byte 0	0x00
0xN904 – 0xN915	Reserved	0x00
0xN916	Reserved	0x00
0xN917	Transmit STM-0 Section – Transmit A1 Byte Error Mask – Low Register – Byte 0	0x00
0xN918 – 0xN91E	Reserved	0x00
0xN91F	Transmit STM-0 Section – Transmit A2 Byte Erro Mask – Low Register – Byte 0	0x00
0xN920 – 0xN921	Reserved	0x00
0xN923	Transmit STM-0 Section – B1 Byte Error Mask Register	0x00
0xN924 – 0xN926	Reserved	0x00
0xN927	Transmit STM-0 Section – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0xN928 – 0xN92A	Reserved	0x00
0xN92B	Transmit STM-0 Section Transmit B2 Byte - Bit Error Mask Register – Byte 0	0x00
0xN92C – 0xN92D	Reserved 6	0x00
0xN92E	Transmit STM-0 Section – K1K2 Byte (APS) Value Register – Byte 1	0x00
0xN92F	Transmit STM-0 Section - K1K2 Byte (APS) Value Register – Byte 0	0x00
0xN930 – 0xN931	Reserved	0x00
0xN933	Transmit STM-0 Section – MS-RDI Control Register	0x00
0xN934 – 0xN936	Reserved	0x00
0xN937	Transmit STM-0 Section – M1 Byte Value Register	0x00
0xN938 – 0xN93A	Reserved	0x00
0xN93B	Transmit STM-0 Section – S1 Byte Value Register	0x00
0xN93C – 0xN93E	Reserved	0x00
0xN93F	Transmit STM-0 Section – F1 Byte Value Register	0x00
0xN940 - 0xN942	Reserved	0x00
0xN943	Transmit STM-0 Section – E1 Byte Value Register	0x00
0xN944	Transmit STM-0 Section – E2 Byte Control Register	0x00
0xN945	Reserved	0x00

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Address Location	REGISTER NAME	DEFAULT VALUES
0xN946	Transmit STM-0 Section – E2 Byte Pointer Register	0x00
0xN947	Transmit STM-0 Section – E2 Byte Value Register	0x00
0xN948 - 0xN94A	Reserved	0x00
0xN94B	Transmit STM-0 Section – Transmit J0 Byte Value Register	0x00
0xN94C - 0xN94E	Reserved	0x00
0xN94F	Transmit STM-0 Section – Transmit J0 Byte Control Register	0x00
0xN950 – 0xN952	Reserved	0x00
0xN953	Transmit STM-0 Section – Serial Port Control Register	0x00
0xN954 –0xN9FF	Reserved	0x00
0xN900 – 0xN981	Reserved	0x00
0xN982	Transmit STM-0 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit STM-0 Path – SONET Control Register + Byte 0	0x00
0xN984 - 0xN992	Reserved	0x00
0xN993	Transmit STM-0 Path – Transmit J1 Byte Value Register	0x00
0xN994 - 0xN996	Reserved	0x00
0xN997	Transmit STM-0 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit STM-0 Path – Transmit C2 Byte Value Register	0x00
0xN99C - 0xN99E	Reserved	0x00
0xN99F	Transmit STM-0 Path - Transmit G1 Byte Value Register	0x00
0xN9A0 - 0xN9A2	Reserved	0x00
0xN9A3	Transmit STM-0 Path Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit STM-0 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit STM-0 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit STM-0 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 - 0xN9B2	Reserved	0x00
0xN9B3	Transmit STM-0 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 - 0xN9B6	Reserved	0x00
0xN9B7	Transmit STM-0 Path – Transmit Path Control Register – Byte 0	0x00



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Address Location	REGISTER NAME	DEFAULT VALUES
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit STM-0 Path – Transmit J1 Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit STM-0 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 - 0xN9C2	Reserved	0x00
0xN9C3	Transmit STM-0 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit STM-0 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit STM-0 Path – Transmit Pointer Byte Register Byte	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit STM-0 Path – HP-RDI Control Register – Byte 2	0x40
0xN9CA	Transmit STM-0 Path – HP-RDI Control Register – Byte 1	0xC0
0xN9CB	Transmit STM-0 Path – HP-RDI Control Register – Byte 0	0xA0
0xN9CC - 0xN9CE	Reserved	0x00
0xN9CF	Transmit STM-0 Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 – 0xN9FF	Reserved	0x00

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1.14.1 TRANSMIT STM-0 SOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 541: Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902, where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	STS-N Overhead Insert	E2 Byte Insert Method	E1 Byte Insert Method	F1 Byte Insert Method	S1 Byte Insert Method	K1K2 Byte Insert Method	M1 Byte Insert Method[1]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	Unused	R/O	this too
6	STS-N Overhead Insert	R/W	 STS-N Overhead Insert: This READ/WRITE bit-field permits the user to configure the TxSOH input port to insert the SOH for all lower-tributary STM-0s within the outbound STM-1 signal. 0 – Disables this feature. In this mode, the TxSOH input port will only accept the SOH for the first STM-0 within the outbound STM-1 signal. 1 – Enables this feature.
5	E2 Byte Insert Method	R/W	 E2 Byte Insert Method: This READ/WRITE bit-lield permits the user to configure the Transmit STM-0 SOH Processor block to use either the contents within the "Transmit STM-0 Section – E2 Byte Value" Register or the TxSOH input port as the source for the E2 byte, within the outbound STM-1 data-stream, as described below. O – Configures the Transmit STM-0 SOH Processor block to accept externally supplied data (via the "TxSOH serial input port) and to insert this data into the E2 byte position within each outbound STM-1 frame. I – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 SOH Processor block to insert the data into the E2 byte position within each outbound STM-1 frame. I – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 Section – E2 Byte Value" register (Address Location = 0xN947) into the E2 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the E2 byte within the "Transmit Output" STM-1 data-stream.
4	E1 Byte Insert Method	€ ₩	 E1 Byte Insert Method: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to use either the contents within the "Transmit STM-0 Section – E1 Byte Value" Register or the TxSOH Input port as the source for the E1 byte, within the outbound STM-1 data-stream, as described below. 0 – Configures the Transmit STM-0 SOH Processor block to accept externally supplied data (via the "TxSOH serial input port) and to insert this data into the E1 byte position within each outbound STM-1 frame. 1 – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 Section – E1 Byte Value" register (Address Location = 0xN943) into the E1 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the E1 byte within the "Transmit Output" STM-1 data-stream.



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3	F1 Byte Insert	R/W	F1 Byte Insert Method:
	Method		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to use either the contents within the "Transmit STM-0 Section – F1 Byte Value" Register or the TxSOH Input port as the source for the F1 byte, within the outbound STM-1 data-stream, as described below.
			0 – Configures the Transmit STM-0 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the F1 Byte position within each outbound STM-1 frame.
			1 – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 Section – F1 Byte Value" register (Address Location = 0xN93F) into the F1 byte-position, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the F1 byte within the "Transmit Output" STM-1 data-stream.
2	S1 Byte Insert	R/W	S1 Byte Insert Method:
	Method		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to use either the contents within the "Transmit STM-0 Section – S1 Byte Value" Register or the TxSOH Input port as the source for the E1 byte, within the outbound STM-1 data-stream, as described below.
			0 – Configures the Transmit STM-0 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the S1 Byte position within each outbound STM-1 frame.
			1 – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 Section – S1 Byte Value" register (Address Location = 0xN93B). This configuration selection permits the user to have software control over the value of the S1 byte within the "Transmit Output" STM-1 data-stream.
1	K1K2 Byte Insert Method	R/W	K1K2 Byte Insert Method: This READ/WRITE bit-field permits the user to configure the Transmit STMO SOH Processor block to use either the contents within the "Transmit STM-0 Section – K1 Byte Value" and "Transmit STM-0 Section K2 Byte Value" registers or the "TxSOH Input port as the source for the K1 and K2 bytes, within the outbound STM-1 data-stream, as described below.
	Theata	amas	0 – Configures the Transmit STM-0 SOH Processor block to accept externally supplied data (via the "TxSOH" serial input port) and to insert this data into the K1 and K2 Byte positions within each outbound STM-1 frame.
			1 – Configures the Transmit STM-0 SOH Processor block to insert the contents within the "Transmit STM-0 Section – K1 Byte Value" Register (Address Location = $0xN92E$) and the "Transmit STM-0 Section – K2 Byte Value" register (Address Location = $0xN92F$) into the K1 and K2 byte-positions, within each outbound STM-1 frame. This configuration selection permits the user to have software control over the value of the K1 and K2 bytes within the "Transmit Output" STM-1 data-stream.
0	M1 Byte Insert	R/W	M1 Byte Insert Method – Bit 1:
	Method[1]		This READ/WRITE bit-field, along with the "M1 Insert Method[0]" bit-field (located in the "Transmit STM-0 Section – SONET Control Register – Byte 0") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STM-1 data stream.
			The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STM-1 frame) is presented

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	below.		
	M1 Byte Metho		Source of M1 Byte
	0	0	Functions as the MS-REI indicator (based upon the number of B2 byte errors that have been detected by the Receive STM-1 SOH Processor block)
	0	1	The M1 byte value is obtained from the contents of the "Transmit STM-0 Section – M1 Byte Value" register (Address Location = 0xN937).
			NOTE: This configuration selection permits the user to exercise software control over the contents within the M1 byte, of each outbound STM-1 frame.
	1	0	The M1 byte value is obtained from the "TxSOH" Serial Input Port.
	1	1	Functions as the MS-REI bit-field (based upon the number of B2 byte errors that have been detected by the Receive STM-1 SOH Processor block).

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Table 542: Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
M1 Byte Insert Method[0]	Unused	Force Transmission of MS-RDI	Force Transmission of MS-AIS	Force Tranmission of LOS Patttern	Scrambler Enable	B2 Byte Error Insert	A1A2 Byte Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	M1 Byte Insert Method[0]	R/W	M1 Byte Insert Method – Bit 0: This READ/WRITE bit-field, along with the "M1 Insert Method[1]" bit-field (located in the "Transmit STM-0 Section – SONET Control Register – Byte 1") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STM-1 data stream. The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STM-1 frame) is presented below. M1 Insert Method[1:0] 0 Functions as the MS-REI indicator (based
6	Unused	R/O	have been detected by the Receive STM- 1 SOH Processor block.
5	Force Transmission of MS-RDI	R/W	Force Transmission of MS-RDI (Line - Remote Defect Indicator): This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-0 SOH Processor block to generate and transmit the MS-RDI indicator to the remote terminal equipment as described below.
			0 – Does not configure the Transmit STM-0 SOH Processor block to generate and transmit the MS-RDI indicator. In this setting, the Transmit STM-0 SOH Processor block will only generate and transmit the MS-RDI indicator whenever the Receive STM-1 SOH Processor

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			block is declaring a defect condition.
			1 – Configures the Transmit STM-0 SOH Processor block to generate and transmit the MS-RDI indicator to the remote terminal equipment. In this case, the STM-1 Transmitter will force bits 6, 7 and 8 (of the K2 byte) to the value "1, 1, 0".
			Note: This bit-field is ignored if the Transmit STM-0 SOH Processor block is transmitting the Line AIS (MS-AIS) indicator or the LOS pattern.
4	Force Transmission	R/W	Force Transmission of MS-AIS (Line AIS) Indicator:
	of MS-AIS		This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-0 SOH Processor block to generate and transmit the MS-AIS indicator to the remote terminal equipment, as described below.
			0 – Does not configure the Transmit STM-0 SOH Processor block to generate and transmit the MS-AIS indicator. In this case, the Transmit STM-0 SOH Processor block will continue to transmit normal traffic to the remote terminal equipment.
			1 – Configures the Transmit STM-0 SOH Processor block to generate and transmit the MS-AIS indicator to the remote terminal equipment. In this case, the Transmit STM-0 SOH Processor block will force all bits (within the "outbound" STM-0 frame) with the exception of the Section Overhead Bytes to an "All Ones" pattern.
			Note: This bicfield is ignored if the Transmit STM-0 SOH Processor block is transmitting the LOS pattern.
3	Force Transmission	R/W	Force Transmission of LOS Pattern:
	of LOS Pattern		This READ/WRITE bit-field permits the user to (by software control) force the Transmit STM-0 SOH Processor block to transmit the LOS (Loss of Signal) battern to the remote terminal equipment, as described below.
		AUC'L	0 – Does not configure the Transmit STM-0 SOH Processor block to generate and transmit the LOS pattern. In this case, the Transmit STM-0 SOH Processor block will continue to transmit "normal" traffic to the remote terminal equipment.
	the pro	she	1. Configures the Transmit STM-0 SOH Processor block to transmit the LOS pattern to the remote terminal equipment. In this case, the Transmit STM-0 SOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern.
2	Scrambler Enable	R/W	Scrambler Enable:
	¢		This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STM-0 SOH Processor block circuitry
			0 – Disables the Scrambler.
			1 – Enables the Scrambler.
1	B2 Byte Error Insert	R/W	Transmit B2 Byte Error Insert Enable:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STM-0 Section – Transmit B2 Byte Error Mask Registers" as described below.
			0 – Configures the Transmit STM-0 SOH Processor block to NOT insert errors into the B2 bytes, within the outbound STM-1 signal.
			1 - Configures the Transmit STM-0 SOH Processor block to insert



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			errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers").
0	0 A1A2 Byte Error R/W		Transmit A1A2 Byte Error Insert Enable:
	Insert		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STM-0 Section – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers.
			0 – Configures the Transmit STM-0 SOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STM-1 data-stream.
		1 – Configures the Transmit STM-0 SOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit A1 Byte Error Mask" and "Transmit A2 Byte Error Mask" Registers.	

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Table 543: Transmit STM-0 Section – Transmit A1 Byte Error Mask – Low Register – Byte 0 (Address Location= 0xN917; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	A1 Byte Error in STM-0 # 2	A1 Byte Error in STM-0 # 1	A1 Byte Error in STM-0 # 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-3	Unused	R/O	
2	A1 Byte Error in	R/W	A1 Byte Error in STM-0 # 2, within outbound STM-1 signal:
	STM-0 # 2		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A1 byte, within STM-0 # 2 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-0 SOH Processor block to NOT transmit an erred A1 byte within STM-0 Channel 2.
			1 – Configures the Transmit STM-0 SOH Processor block to transmit an erred A1 byte within STM-0 Channel 2. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred.
			Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".
1	A1 Byte Error in STM-0 # 1	R/W	A1 Byte Error in STM-0 # 1, within outbound STM-1 signal: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A1 byte, within STM- 0 # 1 within the outbound STM-1 signal, as described below.
		, ct	Configures the Transmit STM-0 SOH Processor block to NOT gransmit an erred A1 byte, within STM-0 Channel 1.
	e produce		1 Configures the Transmit STM-0 SOH Processor block to transmit an erred A1 byte, within STM-0 Channel 1. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred.
	A1 83	and th	Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".
0	A1 Byte Error in	R/W	A1 Byte Error in STM-0 # 0, within outbound STM-1 signal:
	STM-0 # 0		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A1 byte, within STM-0 # 0 within the outbound STM-1 signal, as described below.
			0 – Configures the Transmit STM-0 SOH Processor block to NOT transmit an erred A1 byte, within STM-0 Channel 0.
			1 – Configures the Transmit STM-0 SOH Processor block to transmit an erred A1 byte, within STM-0 Channel 0. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence, all 8-bits within this particular A1 byte will be erred.
			Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".



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Table 544: Transmit STM-0 Section – Transmit A2 Byte Error Mask – Low Register – Byte 0 (Address Location= 0xN91F; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	A2 Byte Error in STM-0 # 2	A2 Byte Error in STM-0 # 1	A2 Byte Error in STM-0 # 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION		
7-3	Unused	R/O	.5 8		
2	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 2, within outbound STM-1 signal:		
	STM-0 # 2		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 # 2 within the outbound STM-1 signal, as described below.		
			0 – Configures the Transmit STM-0 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 2.		
			1 – Configures the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 Channel 2. In this configuration setting, the state of bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred.		
			Note: This bit field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".		
1	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 1, within outbound STM-1 signal:		
	STM-0 # 1	STM-0 # 1	STM-0 # 1		This READWRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 # 1 within the outbound STM-1 signal, as described below.
		60,	0 Configures the Transmit STM-0 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 1.		
	The	P'a	1 – Configures the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 Channel 1. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred.		
		2	Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".		
0	A2 Byte Error in	R/W	A2 Byte Error in STM-0 # 0, within the outbound STM-1 signal:		
	STM-0 # 0		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 # 0 within the outbound STM-1 signal, as described below.		
			0 – Configures the Transmit STM-0 SOH Processor block to NOT transmit an erred A2 byte, within STM-0 Channel 0.		
			1 – Configures the Transmit STM-0 SOH Processor block to transmit an erred A2 byte, within STM-0 Channel 0. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence, all 8-bits within this particular A2 byte will be erred.		
			Note: This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the		



"Transmit STM-0 Section – SONET Transmit Control Register Byte 0 (Address Location= 0xN903) to "1".
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Table 545: Transmit STM-0 Section – B1 Byte Error Mask Register (Address Location= 0xN923; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	B1_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	B1_Byte_Error_Mask [7:0]	R/W	B1 Byte Error Mask[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound STM-1 data stream. The Transmit STM-0 SOH Processor block will perform an XOR operation with the contents of the B1 byte (within each outbound STM-1 frame), and the contents within this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" STM-1 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. Note: For normal operation, the user should set this register to 0x00.



Table 546: Transmit STM-0 Section – Transmit B2 Byte Error Mask Register – Byte 0 (Address Location= 0xN927; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused							B2 Byte Error in STM-0 Channel 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7-1	Unused	R/O	nis eo
0	B2 Byte Error in	R/W	B2 Byte Error in STM-0 Channel #0:
	STM-0 Channel # 0		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to transmit an erred B2 byte, within STM-0 Channel 0.
			If the user enables this feature, then the Transmit STM-0 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within STM-0 Channel 0) and the contents of the "Transmit STM-0 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0xN92B). The results of this calculation will be written back into the "B2 byte" position, within STM-0 Channel 0, prior to transmission to the remote terminal.
			0 Configures the Transmit STM-0 SOH Processor block to NOT insert errors into the B2 byte, within STM-0 Channel 0.
			1 – Configures the Transmit STM-0 SOH Processor block to insert errors into this particular B2 byte, within STM-0 Channel 0.
	5	uct a	Note: This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".
	The data	id may	

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Table 547: Transmit STM-0 Section – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0xN92B; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_B2_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

Bit Number	ΝΑΜΕ	Түре	DESCRIPTION				
7 – 0	Transmit_B2_Error_Mask[7:0]	R/W	Transmit B2 Error Mask Byte:				
			These READ/WRITE bit-fields permit the user to specify exact which bits, within the "selected" B2 byte (within the outbound STM-1 signal) will be erred				
			If the user configures the Transmit STM-0 SOH Processor block to transmit one or more erred B2 bytes, then the Transmit STM-0 SOH Processor block will perform an XOR operation of the contents of the B2 byte (within the "selected" STM-0 Channel) and the contents of this register. The results of this calculation will be written back into the "B2 byte" position within the "selected" STM-0 Channel, (within the outbound STM-1 signal) prior to transmission to the remote terminal.				
			The user can select which STM-0 channels (within the outbound STM-1 signal) will contain the "erred" B2 byte, by writing the appropriate data into the "Transmit STM-0 Section – Transmit B2 Byte Error Mask Register – Bytes 1 and 0 (Address Location= 0xN927).				
		orpri	Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".				



Table 548: Transmit STM-0 Section – K1K2 (APS) Value Register – Byte 1 (Address Location= 0xN92E; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit_K2_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit_K2_Byte_Value[7:0]	R/W	Transmit K2 Byte Value:
			If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K2 byte, within the "outbound" STM-1 signal. If Bit 1 (K1K2 Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "K2" byte-field, within each outbound STM-1 frame. Note: These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".

Table 549: Transmit STM-0 Section – K1K2 (APS) Value Register – Byte 0 (Address Location= 0xN92F; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmi_K1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0 0	0	0	0	0		

Bit Number	NAME OF FYPE	DESCRIPTION
7 – 0	Transmit_K1_Byte_Value[7:0] R/W	Transmit K1 Byte Value:
	Th data d n	If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K1 byte, within the "outbound" STM-1 signal.
		If Bit 1 (K1K2 Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "K1" byte-field, within each outbound STM-1 frame.
		Note: These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".

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Table 550: Transmit STM-0 Section – MS-RDI Control Register (Address Location= 0xN933; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		External	Transmit	Transmit	Transmit
				MS-RDI Enable	MS-RDI upon MS-AIS	MS-RDI upon LOF	MS-RDI upon LOS
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3	External MS-RDI Enable	R/W	External MS-RDI Insertion Enable:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor to accept data via the "TxSOH" input pin, when transmitting the MS-RDI indicator to the remote terminal equipment
			0 – Configures the Transmit STM-0 SOH Processor block to internally generate the MS-RDI indicator based upon defect conditions that are being declared by the Receive STM-1 SOH Processor block.
			1 – Configure the Transmit STM-0 SOH Processor block accept external data via the "TxSOH" input port and to load this value into Bits 6, 7 and 8 (within the K2 byte) within each outbound STM-1 data-stream.
2	Transmit MS-RDI upon MS- AIS	R/W	Transmit, Line Remote Defect Indicator (MS-RDI) upon Declaration of the MS-AIS defect condition:
	The product	et o	This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor is declaring the Line AIS (MS-AIS) defect condition as described below.
	The ata h	124	0 – Configures the Transmit STM-0 SOH Processor block to NOT automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block is declares the MS-AIS defect condition.
	o she		1 – Configures the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the MS-AIS defect condition.
1	Transmit MS-RDI upon LOF	R/W	Transmit Line Remote Defect Indicator (MS-RDI) upon Declaration of the LOF defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor block is declaring the LOF defect condition as described below.
			0 – Configures the Transmit STM-0 SOH Processor to NOT automatically transmit the MS-RDI indicator, whenever the Receive STM-1 SOH Processor block declares the LOF defect condition.



			1 – Configures the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the LOF defect condition.
0	Transmit MS-RDI upon LOS	R/W	Transmit Line Remote Defect Indicator (MS-RDI) upon Declaration of the LOS defect condition:
			This READ/WRITE bit-field permits the user to configure the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator to the remote LTE anytime (and for the duration) that the Receive STM-1 SOH Processor block declares the LOS defect condition.
			0 – Configures the Transmit STM-0 SOH Processor block to NOT automatically transmit the MS-RDI indicator, whenever the Receive STM-1 SOH Processor block declares the LOS defect condition.
			1 – Configures the Transmit STM-0 SOH Processor block to automatically transmit the MS-RDI indicator, whenever (and for the duration that) the Receive STM-1 SOH Processor block declares the LOS defect condition.

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Table 551: Transmit STM-0 Section – M1 Byte Value Register (Address Location= 0xN937; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit_M1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION						
7 – 0	Transmit_M1_Byte_Value [7:0]	R/W	Transmit M1 Byte Value: If the appropriate "M1 Byte Insert Method" is selected, then						
			these READ/WRITE bit-fields will permit the user to specify the contents of the M1 byte, within the "outbound" STM-1 signal.						
			If Bit 0 (M1 Byte Insert Method – Bit 1) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) and Bit 7 (M1 Byte Insert Method – Bit 0) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 0 (Address Location = 0xN903) is set to "[0, 1]", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "M1" byte-field, within each outbound STM-1 frame. Note: These register bits are ignored if the M1 Byte Insert Method[1:0] bits are set to any value other than "[0,]"						
	all								

Table 552: Transmit STM-0 Section – S1 Byte Value Register (Address Location= 0xN93B; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Bit 4	BIT 3	Віт 2	Віт 1	Віт 0		
C Transmit_S1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0 🜔	00	0	0	0	0		
	P Sh A								

BIT NUMBER	NAME	ΤΥΡΕ	DESCRIPTION						
7 – 0	Transmit_S1_Byte_Value[7:0]	R/W	 Transmit S1 Byte Value: If the appropriate "S1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the S1 byte, within the "outbound" STM-1 signal. If Bit 2 (S1 Byte Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "S1" byte-field, within each outbound STM-1 frame. Note: These register bits are ignored if Bit 2 (S1 Byte Insert Method) is set to "0". 						



Table 553: Transmit STM-0 Section – F1 Byte Value Register (Address Location= 0xN93F; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit_F1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 0	Transmit_F1_Byte_Value[7:0]	R/W	Transmit F1 Byte Value:
			If the appropriate "F1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the F1 byte, within the "outbound" STM-1 signal. If Bit 3 (F1 Byte Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "F1" byte-field, within each outbound STM-1 frame.
			Note: These register bits are ignored if Bit 3 (F1 Byte Insert Method) is set to "0".

Table 554: Transmit STM-0 Section – E1 Byte Value Register (Address Location= 0xN943; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0			
Transmit_E1_Byte_Value[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	00	0	0	0	0			

		~	
BIT NUMBER	NAME	Туре	DESCRIPTION
7 – 0	Transmit_E1_Byte_Value[7:0]	R/W	Transmit E1 Byte Value:
	The ata drive		If the appropriate "E1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E1 byte, within the "outbound" STM-1 signal.
	N		If Bit 4 (E1 Byte Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "E1" byte-field, within each outbound STM-1 frame.
			Note: These register bits are ignored if Bit 4 (E1 Byte Insert Method) is set to "0".

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Table 555: Transmit STM-0 Section – E2 Byte Control Register (Address Location= 0xN944; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Enable All STM-0s				Unused			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Enable All STM-	R/W	Enable All STM-0s:
	Os		This READ/WRITE bit-field permits the user to implement either of the following configurations options for software control of the E2 byte value, within the outbound STM-1 signal.
			0 – Configures the Transmit STM-0 SOH Processor block to read out the contents of the "Transmit STM-0 Section – E2 Byte Value" register and load that value into the E2 byte (within STM-0 # 1) within the outbound STM-1 signal.
			1 – Configures the Transmit STM-0 SOH Processor block to read out the contents of the 3 "shadow" registers, and to load these values into the E2 byte positions, within each corresponding STM-0 signal; within the outbound STM-1 signal.
			Note: This register bit is ignored if Bit 5 (E2 Byte Insert Method) within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 1" (Address Location= 0xN902) is set to "0".
6 - 0	Unused	R/O	ATO LONGICE

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Table 556: Transmit STM-0 Section – E2 Pointer Register (Address Location= 0xN946; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		E2_Poir	nter[1:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	E2_Pointer[1:0]	R/W	 E2 Pointer[3:0]: These READ/WRITE bit-fields permit the user to uniquely identify one of the 3 STM-0 E2 byte "shadow" registers, when performing read or write operations to these registers. If the user has set Bit 7 (Enable All STM-0s), within this register to "1", then the contents of these four register bits, act as a pointer to a given "shadow" register. Once the user specifies this pointer value; then he/she completes the read or write operation (to or from the "shadow" register) by performing a read or write to the "Transmit STM-0 Section – E2 Byte Value" register (Address Location= 0xN947). Valid "shadow" pointer values range from "0x00" to "0x02" (where the pointer value of "0x00" corresponds to the E2 "shadow" register, corresponding to STM-0 # 1; and so on). Note: This register bit is ignored if Bit 7 (Enable All STM-0s) is set to "1"; or if Bit 5 (E2 Byte Insert Method) within the "Transmit STM-0 Section – SONET Transmit Control Register – Byte 1" (Address Location= 0xN902) is set to "0".

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Table 557: Transmit STM-0 Section – E2 Byte Value Register (Address Location=0xN947; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
Transmit_E2_Byte_Value[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Transmit_E2_Byte_Value[7:0]	R/W	Transmit E2 Byte Value:
			The exact function of these register bits depends upon whether Bit 7 (Enable All STM-0s) within the "Transmit STM-0 Section – E2 Byte Control" Register (Address Location= 0xN944) has been set to "0" or "1"; as described below.
			If "Enable All STM-0s" is set to "0"
			If the appropriate "E2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E2 byte, within the "outbound" STM-1 signal. More specifically, this value will be loaded into the E2 byte position, within STM-0 # 1 (within the outbound STM-1 signal).
			If Bit 5 (E2 Insert Method) within the Transmit STM-0 Section – SONET Transmit Control Register – Byte 1 (Address Location = 0xN902) is set to "1", then the Transmit STM-0 SOH Processor block will load the contents of this register into the "E2" byte-field, within each outbound STM-1 frame.
		, o ^C	If "Enable All STM-0s" is set to "1"
	(or princ	In this mode, these register bit permit the user to have direct READ/WRITE access of the "STM-0 E2 Byte shadow" register; that is being pointed at by the "E2 Pointer[1:0]" value.
	Auct	31,5	These register bits are ignored if Bit 5 (E2 Byte Insert Method) is set to "0".
	The progressing the and the	and the second	<u> </u>



Table 558: Transmit STM-0 Section – J0 Byte Value Register (Address Location= 0xN94B; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	Transmit_J0_Value[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
0	0	0	0	0	0	0	0				

BIT NUMBER	Nаме	Түре	DESCRIPTION			
7 – 0	Transmit_J0_Value[7:0]	R/W	Transmit J0 Value Byte:			
			 These READ/WRITE bits permit a user to specify the value of the J0 byte, that will be transmitted via the Section Overhead, within the very next STM-1 Frame. Note: This register is only valid if the Transmit STM-0 SOH Processor block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STM-1 frame. The user accomplishes this by setting Bits 1 and 0 (J0_TYPE), within the Transmit STM-0 Section – J0 Byte Control Register (Address Location= 0xN94F) to "1, 0". 			

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Table 559: Transmit STM-0 Section – Transmit Section Trace Message Control Register (Address Location= 0xN94F; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused					ection Trace Length[1:0]		ection Trace Source[1:0]
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	Түре		DESCRIPTION
7 – 4	Unused	R/O		
3-2	Transmit Section Trace Message Length[1:0]	R/W	These two READ/M the Section Trace block will repeated between the conter	(in terms of bytes)
1 – 0	Transmit Section Trace Message Source[1:0]	R/W	These two READ/V of the "outbound" S J0 byte channel w below.	Frace Message Source[1:0]: VRITE bit-fields permit the user to specify the source Section Trace message that will be Sectioned via the ithin the outbound STM-1 data-stream, as depicted Resulting Source of the Section Trace Message.
	1.8	and	00	Fixed Value: The Transmit STM-0 SOH Processor block will automatically set the J0 Byte, in each "outbound" STM-1 frame to the value "0x01".
			01	The "Transmit Section Trace Message Buffer". The Transmit STM-0 SOH Processor block will read out the contents within the Transmit Section Trace Message Buffer, and will transmit this message to the remote LTE. The "Transmit STM-0 SOH Processor block - Transmit Section Trace Message Buffer" Memory is located at Address Location 0x1B00 through 0x1B3F.
			10	From the "Transmit J0 Value[7:0]" Register. In this setting, the Transmit STM-0 SOH Processor



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	block will read out the contents of the "Transmit J0 Byte Value[7:0]" Register (Address Location= 0xN94B), and will insert this value into the J0 byte- position within each outbound STM-1 frame.
11	From the "TxSOH" Input pin (pin F8).
	In this configuration setting, the Transmit STM-0 SOH Processor block will externally accept the contents of the "Section Trace Message" via the "TxSOH Input Port" and it will Section this message (via the J0 byte-channel) to the remote LTE.

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Table 560: Transmit STM-0 Section – Serial Port Control Register (Address Location= 0xN953; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		TxSOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxSOH_CLOCK_SPEED[7:0]	R/W	TxSOHClk Output Clock Signal Speed:These READ/WRITE bit-fields permits the user to specify thefrequency of the "TxSOHClk output clock signal.The formula that relates the contents of these register bits tothe "TxSOHClk" frequency is presented below.FREQ = 19.44 /[20 (TxSOH_CLOCK_SPEED + 1)Note: For STM-1/STM-1 applications, the frequency of the
			TXSOHCIk output signal must be in the range of 0.6075MHz to 9.72MHz

Note: For STM-1/STA TASOHCIA out 0.6075MHz to 0.6075MHz to 0.6075MHz to 0.6075MHz to 0.6075MHz to 0.6075MHz to



1.15 TRANSMIT STM-0 POH PROCESSOR BLOCK REGISTERS

Table 561: Transmit STM-0 Path – SONET Control Register – Byte 1 (Address Location= 0xN982; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 4	Unused	R/O	.5 0
3	Z5 Byte	R/W	Z5 Byte Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit STM- 0 POH Processor block to use either the contents within the "Transmit STM- 0 Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte in the outbound STM-1c SPE data-stream, as described below.
			0 – Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound STM-1c SPE.
			1 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the 25 byte position within each outbound STM-1c SPE.
			Note: The Address Location of the Transmit STM-0 POH Processor Block Transmit Z5 Byte Value Register is 0xN9B3
2	Z4 Byte	R/W	Z4 Byte Insertion Type:
		sertion Type	This READ/WRITE bit-field permits the user to configure the Transmit STM- D POH Processor block to use either the contents within the "Transmit STM- 0 Path – Transmit Z4 Byte Value" Register or the TxPOH input pin as the source for the Z4 byte, in the outbound STM-1c SPE data-stream, as described below.
	The	13 M2	 Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit Z4 Byte Value" Register into the Z4 byte position within each outbound STM-1c SPE.
		an	1 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the "TxPOH" input port) and to insert this data into the Z4 byte position within each outbound STM-1c SPE.
			Note: The address location of the Transmit STM-0 POH Processor block -Transmit Z4 Byte Value Register is 0xN9AF
1	Z3 Byte	R/W	Z3 Byte Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit STM- 0 POH Processor block to use either the contents within the "Transmit STM- 0 Path – Transmit Z3 Byte Value" Register or the TxPOH input pin as the source for the Z3 byte, in the outbound STM-1c SPE data-stream, as described below.
			0 – Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound STM-1c SPE.
			1 - Configures the Transmit STM-0 POH Processor block to accept

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			externally supplied data (via the "TxPOH" input port) and to insert this data into the Z3 byte position within each outbound STM-1c SPE. Note: The Address Location of the Transmit STM-0 POH Processor block - Transmit Z3 Byte Value Register is 0xN9AB
0	H4 Byte Insertion Type	R/W	H4 Byte Insertion Type: This READ/WRITE bit-field permits the user to configure the Transmit STM- 0 POH Processor block to use either the contents within the "Transmit STM- 0 Path – Transmit H4 Byte Value" Register or the TxPOH input pin as the source for the H4 byte, in the outbound STM-1c SPE data-stream, as described below.
			0 – Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound STM-1c SPE.
			1 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound STM-1c SPE.
			Note: The Address Location of the Transmit STM-0 POH Processor block -Transmit H4 Byte Value Register is 0xN9A7

Address Location of the Transmit H4 Byte Value Red



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Table 562: Transmit STM-0 Path – SONET Control Register – Byte 0 (Address Location= 0xN983; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F2 Byte Insertion Type	HP-REI Type			· -	C2 Byte Insertion Type	Unused	Transmit AIS- P Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7	F2 Byte	R/W	F2 Byte Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to use either the contents within the "Transmit STM-0 Path – Transmit F2 Byte Value" Register or the TxPOH input pin as the source for the F2 byte, in the outbound STM-1c SPE data-stream, as described below.
			0 – Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit F2 Byte Value" Register into the F2 byte position within each outbound STM-1c SPE.
			1 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound STM-1c SPE.
			Note: The Address Location of the Transmit STM-0 POH Processor block - Transmit F2 Byte Value Register is 0xN9A3
6 - 5	HP-REI Insertion	R/W	HP-REI Insertion Type[1:0]:
	Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit STM-0 POH Processor block to use one of the three following sources for the HP REI bit fields (e.g., bits 1 through 4, within the G1 byte) within each outbound STM-1c SPE.
		api ST	From the corresponding Receive STM-1c POH Processor block (e.g., the Transmit STM-0 POH Processor block will set the HP-REI bit-fields to the appropriate value, based upon the number of B3 byte errors that the Receive STM1c POH Processor block detects and flags, within its incoming STM-1c SPE data-stream).
	The sta		From the "Transmit G1 Byte Value" Register. In this case, the Transmit STM- O POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit STM-0 POH Processor block – Transmit G1 Byte Value" Register into the HP-REI bit-fields within each outbound STM-1c SPE.
			• From the "TPOH" input pin. In this case, the Transmit STM-0 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the HP-REI bit-fields within each outbound STM-1c SPE.
			00/11 – Configures the Transmit STM-0 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the Receive STM-1c POH Processor block detects and flags within the incoming STM-1c data-stream.
			01 – Configures the Transmit STM-0 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STM-0 POH Processor block - Transmit G1 Byte Value" register.
			10 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the HP-REI bit-positions within each outbound STM-1c SPE.
			Note: The address location of the Transmit STM-0 POH Processor block -



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			Transmit G1 Byte Value Register is 0xN99F
4 - 3	HP-RDI	R/W	HP-RDI Insertion Type[1:0]:
	Insertion Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit STM-0 POH Processor block to use one of the three following sources for the HP-RDI bit-fields (e.g., bits 5 through 7, within the G1 byte) within each outbound STM-1c SPE.
			• From the corresponding Receive STM-1c POH Processor block (e g., the Transmit STM-0 POH Processor block will set the HP-RDI bit-fields to the appropriate value, based upon which defect conditions are being declared by the Receive STM-1c POH Processor block, within its incoming STM-1c SPE data-stream).
			• From the "Transmit G1 Byte Value" Register. In this case, the Transmit STM- 0 POH Processor block will insert the content of bits 2 through 0 within the "Transmit STM-0 POH Processor block – Transmit G1 Byte Value" Register into the HP-RDI bit-fields within each outbound STM-10 SPE.
			• From the "TPOH" input pin. In this case, the Transmit STM-0 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the HP-RDI bit-fields within each outbound STM-1c SPE.
			00/11 – Configures the Transmit STM POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the defects conditions that the Receive STM-1c POH Processor block is currently declaring within the incoming STM-1c data-stream.
			01 – Configures the Transmit STM-0 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STM-0 POH Processor block - Transmit G1 Byte Value" register.
			10 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the HP-RDI bit-positions within each outbound STM-1c SPE.
			Note: The address location of the Transmit STM-0 POH Processor block - Transmit G1 Byte Value Register is 0xN99F
2	C2 Byte Insertion Type	R/W	C2 Byte Insertion Type:
	постоптуре	oro	This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to use either the contents within the "Transmit STM-0 Path – Transmit C2 Byte Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound STM-1c SPE data-stream, as described below.
	~	6,2	0 – Configures the Transmit STM-0 POH Processor block to insert the contents within the "Transmit STM-0 Path – Transmit C2 Byte Value" Register into the C2 byte-position within each outbound STM-1c SPE.
		2	1 – Configures the Transmit STM-0 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the C2 byte position within each outbound STM-1c SPE.
			Note: The address location of the Transmit STM-0 POH Processor block - Transmit C2 Byte Value Register is 0xN99B
1	Unused	R/O	
0	Transmit	R/W	Transmit AIS-P Enable:
	AIS-P Enable		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to (via software control) transmit the AIS-P indicator to the remote PTE.
			If this feature is enabled, then the Transmit STM-0 POH Processor block will automatically set the H1, H2, H3 and all the "outbound" STM-1c SPE bytes to an "All Ones" pattern, prior to routing this data to the Transmit STM-1 SOH



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Processor block.
0 – Configures the Transmit STM-0 POH Processor block to NOT transmit the AIS-P indicator to the remote PTE. In this case, the Transmit STM-0 POH Processor block will transmit "normal" traffic to the remote PTE.
1 – Configures the Transmit STM-0 POH Processor block to transmit the AIS-P indicator to the remote PTE.

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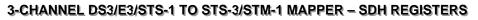




Table 563: Transmit STM-0 Path – Transmitter J1 Byte Value Register (Address Location= 0xN993; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_J1_Byte[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION			
7 - 0 Transmit J1 B Value[7:0]	Transmit J1 Byte	R/W	Transmit J1 Byte Value:			
	value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound STM-1c SPE.			
			If the user configures the Transmit STM-0 POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each "outbound" STM-1c SPE. This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Insertion Method) within the "Transmit STM-0 Path – SONET Path J1 Byte Control Register" register.			
			Note: The Address Location of the Transmit STM-0 Path – SONET J1 Byte Control Register is 0xN9BB			
		STM-1				

Table 564: Transmit STM-0 Path – Transmitter B3 Byte Error Mask Register (Address Location= 0xN997; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/WO	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER		Түре	DESCRIPTION
7 - 0	Transmit B3 Byte Error_Mask[7:0]	arrw	 Transmit B3 Byte Error Mask[7:0]: This READ/WRITE bit-field permits the user to insert errors into the B3 byte within each "outbound" STM-1c SPE, prior to transmission to the Transmit STM-1 SOH Processor block. The Transmit STM-0 POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte-position within each "outbound" STM-1c SPE. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. Note: For normal operation, the user should set this register to 0x00.



Table 565: Transmit STM-0 Path - Transmit C2 Byte Value Register (Address Location= 0xN99B; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_C2_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit C2 Byte Value[7:0]	R/W	 Transmit C2 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound STM-1c SPE. If the user configures the Transmit STM-0 POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" STM-1c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 0" register. Note: The Address Location of the Transmit STM-0 Path – SONET
			Control Register – Byte 0" Register is 0xN983

Ø Table 566: Transmit STM-0 Path - Transmit G1 Byte Value Register (Address Location= 0xN99F; where N ranges in value from 5 to 7) . Jo _ ol , (

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Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_G1_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER		TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	BRW and ma	 Transmit G1 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the contents of the HP-RDI and HP-REI bit-fields, within each G1 byte in the "outbound" STM-1c SPE. If the users sets "HP-REI_Insertion_Type[1:0]" and "HP-RDI_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the HP-REI and the HP-RDI bit-fields (within each G1 byte of the "outbound" STM-1c SPE) will be dictated by the contents of this register. <i>Note:</i> 1. The "HP-REI_Insertion_Type[1:0]" and "HP-RDI_Insertion_Type[1:0]" bit-fields are located in the "Transmit STM-0 Path – SONET Control Register – Byte 0" Register. 2. The Address Location of the Transmit STM-0 Path – SONET Control Register - Byte 0" Register is 0xN983

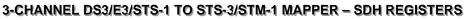




Table 567: Transmit STM-0 Path - Transmit F2 Byte Value Register (Address Location= 0xN9A3; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit F2 Byte	R/W	Transmit F2 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound STM-1c SPE.
			If the user configures the Transmit STM-0 POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" STM-1c SPE.
			This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 0" register.
			Note: The Address Location of the Transmit STM-0 Path – SONET Control Register is 0xN983

vè Table 568: Transmit STM-0 Path – Transmit H4 Byte Value Register (Address Location= 0xN9A7; where N ranges in value from 5 to 7) 0 C C

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Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit H4_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0 🗸	00	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Туре	DESCRIPTION
Віт N UMBER 7 - 0	NAME Transmit H4 Byte Value[7:0]		DESCRIPTION Transmit H4 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound STM-1c SPE. If the user configures the Transmit STM-0 POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" STM-1c SPE. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 1" register.
			Note: The Address Location for the "Transmit STM-0 Path – SONET Control Register – Byte 1" register is 0xN982



Table 569: Transmit STM-0 Path – Transmit Z3 Byte Value Register (Address Location= 0xN9AB; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit Z3 Byte	R/W	Transmit Z3 Byte Value:
	Value[7:0]		 These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound STM-1c SPE. If the user configures the Transmit STM-0 POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" STM-1c SPE. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 1" register. Note: The Address Location for the "Transmit STM-0 Path – SONET Control Register – Byte 1" register – Byte 1" register is 0xN982
			s per BS

Table 570: Transmit STM-0 Path – Transmit Z4 Byte Value Register (Address Location= 0xN9AF; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Brt 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit_Z4_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	00	\$ \$	0	0	0	0		

BIT NUMBER		TYRE	DESCRIPTION
7 - 0	Transmit Z4 Byte	R/W	Transmit Z4 Byte Value:
	Value[70]	These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound STM-1c SPE.	
		0	If the user configures the Transmit STM-0 POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" STM-1c SPE.
		This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 0" register.	
			Note: The Address Location of the Transmit STM-0 Path – SONET Control Register – Byte 0" Register is 0xN982

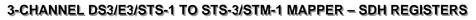




Table 571: Transmit STM-0 Path – Transmit Z5 Byte Value Register (Address Location= 0xN9B3; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 0	Transmit Z5 Byte	R/W	Transmit Z5 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound STM-1c SPE.
			If the user configures the Transmit STM-0 POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" STM-1c SPE.
			This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit STM-0 Path – SONET Control Register – Byte 0" register.
			Note: The Address Docation of the Transmit STM-0 Path – SONET Control Register – Byte 0" register is 0xN982
	the	produ data	Note: The Address Location of the Transmit STM-0 Path – SONET Control Register – Byte 0" register is 0xN982



Table 572: Transmit STM-0 Path – Transmit Path Control Register (Address Location= 0xN9B7; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	 Pointer Force: This READ/WRITE bit-field permits the user to load the values contained within the "Transmit STM-0 POH Arbitrary H1 Pointer Byte" and "Transmit STM-0 POH Arbitrary H2 Pointer Byte" registers into the H1 and H2 bytes (within the outbound STM-1c data stream). Note: The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes, Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition. 0 - Configures the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to Transmit STM-0/STM-1 data with normal and correct H1 and H2 bytes. 1 - Configures the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STM- 1c/STM 1 data stream) with the values in the "Transmit STM-0 POH Arbitrary H1 and H2 Pointer Byte" registers. Note: 1 - The Address Location of the Transmit STM-0 Arbitrary H1 Pointer Byte
4	Check Stuff	RAY	register is 0xN9BF 2. The Address Location of the Transmit STM-0 Arbitrary H2 Pointer Byte register is 0xN9C3
4	Check Stur	3100	This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods.
			0 – Disables this feature.
			In this mode, the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods.
			1 – Enables this feature.
			In this mode, the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.



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3	Insert Negative	R/W	Insert Negative Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to insert a negative-stuff into the outbound STM-1c/STM-1 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STM-0/STM-1 data stream).
			• The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on.
			Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2	Insert Positive	R/W	Insert Positive Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to insert a positive-stuff into the outbound STM-1c/STM-1 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STM-1c/STM-1 data-stream, immediately after the H3 byte position within the outbound STM-1c/STM-1 data stream).
			 The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event).
			 The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on.
		8	Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
1	Insert Continuous NDF Events	RAV	Insert Continuous NDF Events: This READ/WRITE bit-field permits the user configure the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STM-1c/STM-1 data stream.
		*	Note: As the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks insert the NDF event into the STM-0/STM-1 data stream, it will proceed to load in the contents of the "Transmit STM-0 POH Arbitrary H1 Pointer" and "Transmit STM-0 POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STM-1c/STM-1 data stream).
			0 – Configures the "Transmit STM-0 SOH and Transmit STM-1 POH Processor" blocks to not continuously insert NDF events into the "outbound" STM-1c/STM-1 data stream.
			1- Configures the "Transmit STM-0 SOH and Transmit STM-1 POH Processor" blocks to continuously insert NDF events into the "outbound" STM-1c/STM-1 data stream.
0	Insert Single	R/W	Insert Single NDF Event:
	NDF Event		This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH and Transmit STM-1 SOH Processor blocks to insert a New Data Flag



(NDF) pointer adjustment into the outbound STM-1c/STM-1 data stream.
Writing a "0" to "1" transition into this bit-field causes the following to happen.
• The "N" bits, within the H1 byte will set to the value "1001"
• The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit STM-0 POH – Arbitrary H1 Pointer" and "Transmit STM-0 POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3).
• Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on.
Note:
1. Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2. The Address Location of the Transmit STM-0 Arbitrary H1 Pointer Byte register is 0xN9BF
3. The Address Location of the Transmit STM-0 Arbitrary H2 Pointer Byte register is 0xN9C3

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Table 573: Transmit STM-0 Path – SONET Path J1 Byte Control Register (Address Location= 0xN9BB; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			Transmit Path Trace Message_Length[1:0]		Insertion_Method[1:0]		
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре		DESCRIPTION	
7 – 4	Unused	R/O			
3 - 2	Transmit Path Trace Message_Length[1:0]	R/W	V Transmit Path Message Length[1:0]: These READ/WRITE bit-fields permit the user to specify the length of J1 Trace Message, that the Transmit STM-0 POH Processor block transmit. The relationship between the content of these bit-fields and corresponding J1 Trace Message Length is presented below.		
			MSG LENGTH	Resulting V1 Trace Message Length	
			00	1 Byte	
			01	16 Bytes	
			10/11	64 Bytes	
1 - 0	Insertion_Method[1:0]	R/W	he/she will use to int relationship betwee	d[1:0]: bit-fields permit the user to specify the method t sert the J1 byte into the outbound STM-1c SPE. T en the contents of these bit-fields and the sertion Method is presented below.	Гhe
		, ct	J1 Insertion Method[1:0]	Resulting Insertion Method	
			000	Insert the value "0x00"	
	6	SUS	01	Insert from the J1 Trace Buffer	
	Thelat	andn	10	Insert from the "Transmit STM-0 Path – Transmit J1 Byte Value Register.	
		5	11	Insert via the "TxPOH_n" input port	



Table 574: Transmit STM-0 Path – Transmit Arbitrary H1 Pointer Register (Address Location= 0xN9BF; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
NDF Bits			SS	Bits	H1 Pointer Value		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	NDF Bits	R/W	NDF (New Data Flag) Bits:
			These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "transmit STM-0 Path – Transmit Path Control" Register.
			Note: The Address Location of the Transmit STM-0 Path – Transmit Path Control register is 0xN9B7
3 - 2	SS Bits	R/W	SS Bits
			These READ/WRITE bit fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STM-0 Path – Transmit Path Control" Register.
			1. The "SS" bits have no functional value, within the H1 byte.
			2. The Address Location of the Transmit STM-0 Path – Transmit Path Control register is 0xN9B7
1 - 0	H1 Pointer	R/W	H1 Pointer Value[1:0]:
	Value[1:0]	Ċ	These two READ/WRITE bit-fields, along with the constants of the "Transmit STMO Path – Transmit Arbitrary H2 Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the Pointer Word.
		ool	These two READ/WRITE bit-fields permit the user to define the value of the two most significant bits within the Pointer word.
	The	to d	Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STM-0 Path – Transmit Path Control" Register, the values of these two bits will be loaded into the two most significant bits within the Pointer Word.
		9	Note: The Address Location of the Transmit STM-0 Path – Transmit Path Control register is 0xN9B7

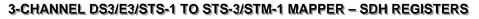




Table 575: Transmit STM-0 Path - Transmit Arbitrary H2 Pointer Register (Address Location= 0xN9C3; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

7 - 0 H2 Pointer R/W H2 Pointer Value[1:0]: Value[7:0] These sight DEADAVDITE his fields, slong with the constants of hits 1 as	BER NAME TYPE	DESCRIPTION
within the "Transmit STM-0 Path – Transmit Arbitrary H1 Pointer" Reg permit the user to provide the contents of the Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within Transmit STM-0 Path – Transmit Path Control" Register, the values of the	H2 Pointer Value[7:0] R/W H2 Pointer These eigh within the permit the these two eight least s Whenever Transmit S	Value[1:0]: READ/WRITE bit-fields, along with the constants of bits 1 and 0 Transmit STM-0 Path – Transmit Arbitrary H1 Pointer" Register ser to provide the contents of the Pointer Word. READ/WRITE bit-fields permit the user to define the value of the ignificant bits within the Pointer word. a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the M-0 Path – Transmit Path Control" Register, the values of these
Transmit STM-0 Path – Transmit Path Control" Register, the values of the eight bits will be loaded into the H2 byte, within the outbound STM-1c/ST data stream. Note: 1. The Address Location of the Transmit STM-0 Path – Transmit Arbitrary Pointer" register is 0xN9C3 2. The Address Location of the Transmit STM-0 Path – Transmit Path Corregister is 0xN9B7	eight bits w data stream Note: 1. The Add Pointer" reg 2. The Add	Il be loaded into the H2 byte, within the outbound STM-1c/STM-1 ress Location of the Transmit STM-0 Path – Transmit Arbitrary H1 ister is 0xN9C3 ress Location of the Transmit STM-0 Path – Transmit Path Control

Table 576: Transmit STM-0 Path - Transmit Current Pointer Byte Register - Byte 1 (Address Location= 0xN9C6; where N ranges in value from 5 tor) ´ X[©]

Віт 7	Віт 6	Віт 5	Bit 4	BIT 3	Віт 2	Віт 1	Віт 0
Unused						Tx_Pointer	r_High[1:0]
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0 0		0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused 🔨	R/0	N
1 - 0	Tx_Pointer_Hi gh[1:0]	R/O	 Transmit Pointer Word – High[1:0]: These two READ-ONLY bits, along with the contents of the "Transmit STM-0 Path – Transmit Current Pointer Byte Register – Byte 0" reflect the current value of the pointer (or offset of SPE within the STM-1c frame). These two bits contain the two most significant bits within the "10-bit pointer" word. Note: The Address Location of the Transmit STM-0 Path – Transmit Current Pointer Byte – Byte 0 register is 0xN9C7



Table 577: Transmit STM-0 Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0xN9C7; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	1	0	1	0	

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 – 0	Tx_Pointer_Lo	R/O	Transmit Pointer Word – Low[7:0]:
	w[7:0]		 These two READ-ONLY bits, along with the contents of the "Transmit STM-0 Path – Transmit Current Pointer Byte Register – Byte 1" reflect the current value of the pointer (or offset of SPE within the STM-1c frame). These two bits contain the eight least significant bits within the "10-bit pointer" word. Note: The Address Location of the Transmit STM-0 Path – Transmit Current Pointer Byte – Byte 0 register is 0xN9C6

ne Address Location Current Pointer Bre – Br

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Table 578: Transmit STM-0 Path – HP-RDI Control Register – Byte 2 (Address Location= 0xN9C9; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			PLM-P HP-RDI Code[2:0]			Transmit HP-RDI upon PLM-P	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	ΤΥΡΕ	DESCRIPTION
7 – 4	Unused	R/O	
3 - 1	PLM-P HP-RDI Code[2:0]	R/W	PLM-P (Path – Payload Mismatch) Defect – HP-RDI Code: These three READ/WRITE bit fields permit the user to specify the value that the Transmit STM-0 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within each "outbound" STM-1c SPE), whenever (and for the duration that) the Receive
			STM-1c POH Processor block detects and declares the PLM-P defect condition. Note: In order to enable this feature, the user must set Bit 0 (Transmit HP-RDI upon PLM-P) within this register to "1".
0	Transmit HP-RDI upon PLM-P	R/W	 Transmit the HP-RDI Indicator upon declaration of the PLM-P defect condition. This READ/WRITE Dit-field permits the user to configure the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STM-10 POH Processor block declares the PLM-P defect condition. 0 - Configures the Transmit STM-0 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-10 POH Processor block declares the PLM-P defect condition. 0 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 10 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 10 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 10 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 10 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 10 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 11 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 12 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 14 - Configures the Transmit STM-0 POH Processor block declares the PLM-P defect condition. 15 - Configures the Transmit STM-0 POH Processor block will transmit the HP-RDI indicator (in response to the Receive STM-10 POH Processor block declares the PLM-P defect condition). 16 - RDI bit-fields (within each outbound STM-10 SPE) to the contents within the "PLM-P HP-RDI Code[2:0]" bit-fields within this register.



Table 579: Transmit STM-0 Path – HP-RDI Control Register – Byte 1 (Address Location= 0xN9CA; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P HP-RDI Code[2:0]		Transmit HP-RDI upon TIM-P	HP-UNEQ HP-RDI Code[2:0]		Transmit HP-RDI upon HP-UNEQ		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	ΝΑΜΕ	Түре	DESCRIPTION
7 - 5	TIM-P HP-RDI Code[2:0]	R/W	TIM-P (Path – Trace Identification Mismatch) Defect – HP-RDI Code:
			These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STM-0 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within each "outbound" STM-1c SPE), whenever (and for the duration that) the Receive STM-1c POH Processor block detects and declares the TIM-P defect condition.
			Note: In order to enable this feature, the user must set Bit 4 (Transmit HP-RDI upon TIM-P) within this register to "1".
4	Transmit HP-RDI upon TIM-P	R/W	Transmit the HP-RDI Indicator upon declaration of the TIM-P defect condition
		pro	This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STM-1CPOH Processor block declares the TIM-P defect condition.
	NUS	o e	0 – Configures the Transmit STM-0 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the TIM-P defect condition.
	neproch	eet no	1 – Configures the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor blolck declares the TIM-P defect condition.
	The produce	•	NOTE: The Transmit STM-0 POH Processor block will transmit the HP-RDI indicator (in response to the Receive STM-1c POH Processor block declaring the TIM-P defect condition) by setting the HP-RDI bit-fields (within each outbound STM-1c SPE) to the contents within the "TIM-P HP-RDI Code[2:0]" bit-fields within this register.
3 - 1	HP-UNEQ HP-RDI	R/W	HP-UNEQ (Path – Unequipped) Defect – HP-RDI Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STM-0 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within each "outbound" STM-1c SPE), whenever (and for the duration that) the Receive STM-1c POH Processor block detects and declares the HP-UNEQ defect condition.
			Note: In order to enable this feature, the user must set Bit 0 (Transmit HP-RDI upon HP-UNEQ) within this register to "1".
0	Transmit HP-RDI upon	R/W	Transmit the HP-RDI indicator upon declaration of the HP-UNEQ

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HP-UNEQ	defect condition:
	This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STM-1c POH Processor block declares the HP-UNEQ defect condition.
	0 – Configures the Transmit STM-0 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the HP-UNEQ defect condition.
	1 – Configures the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the HP-UNEQ defect condition.
	NOTE: The Transmit STM-0 POH Processor block will transmit the HP-RDI indicator (in response to the Receive STM-1c POH Processor block declaring the HP-UNEQ defect condition) by setting the HP-RDI bit-fields (within each outbound STM-1c SPE) to the contents within the "HP-UNEQ HP-RDI Code[2:0]" bit-fields within this register.

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Table 580: Transmit STM-0 Path – HP-RDI Control Register – Byte 1 (Address Location= 0xN9CB; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
LOP-P HP-RDI Code[2:0]		Transmit HP- RDI upon LOP-P	AIS-P HP-RDI Code[2:0]			Transmit HP- RDI upon AIS-P	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 5	LOP-P HP-RDI Code[2:0]	R/W	LOP-P (Path – Loss of Pointer) Defect – HP-RDI Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STM-0 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within each "outbound" STM-1c SPE), whenever (and for the duration that) the Receive STM-1c POH Processor block detects and declares the LOP-P defect
			condition. Note: In order to enable this feature, the user must set Bit 4 (Transmit HP-RDI upon LOP-P) within this register to "1".
4	Transmit HP-RDI upon LOP-P	R/W	 Transmit the HP RDI Indicator upon declaration of the LOP-P defect condition: This READ/WRITE bit-field permits the user to configure the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STM-1c POH Processor block declares the LOP-P defect condition. 0 – Configures the Transmit STM-0 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STM-0 POH Processor block declares the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the LOP-P defect condition.
			Processor block declaring the LOP-P defect condition) by setting the HP-RDI bit-fields (within each outbound STM-1c SPE) to the contents within the "LOP-P HP-RDI Code[2:0]" bit-fields within this register.
3 - 1	AIS-P HP-RDI Code[2:0]	R/W	 AIS-P (Path – AIS) Defect – HP-RDI Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STM-0 POH Processor block will transmit, within the HP-RDI bit-fields of the G1 byte (within the "outbound" STM-1c SPE), whenever (and for the duration that) the Receive STM-1c POH Processor block detects and declares the AIS-P defect condition. Note: In order to enable this feature, the user must set Bit 0 (Transmit HP-RDI upon AIS-P) within this register to "1".
0	Transmit HP-RDI upon AIS-P	R/W	Transmit the HP-RDI Indicator upon declaration of the AIS-P defect condition: This READ/WRITE bit-field permits the user to configure the Transmit



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STM-0 POH Processor block to automatically transmit the HP-RDI Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STM-1c POH Processor block declares the AIS-P defect condition.
0 – Configures the Transmit STM-0 POH Processor block to NOT automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the AIS-P defect condition.
1 – Configures the Transmit STM-0 POH Processor block to automatically transmit the HP-RDI indicator whenever (and for the duration that) the Receive STM-1c POH Processor block declares the AIS-P defect condition.
NOTE: The Transmit STM-0 POH Processor block will transmit the HP-RDI indicator (in response to the Receive STM-1c POH Processor block declaring the AIS-P defect condition) by setting the HP-RDI bit-field (within each outbound STM-1c SPE) to the contents within the "AIS-P HP-RDI Code[2:0]" bit-fields within this register.



Table 581: Transmit STM-0 Path – Serial Port Control Register (Address Location= 0xN9CF; where N ranges in value from 5 to 7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				TxPOH Clock Speed [3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

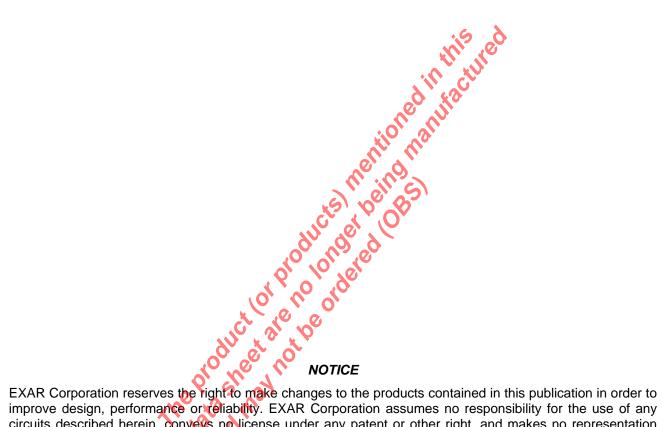
BIT NUMBER	Nаме	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 - 0	TxPOH Clock Speed [3:0]	R/W	TxPOHClk Output Clock Signal Speed: These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHClk output clock signal. The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below. FREQ = 19.44/[2 * (TxPOHCLCLOCK_SPEED + 1) Note: For STM-1/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz

.see: For STM-1/ST RxPOHCik outj to 9,72MHz

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NOTES:

REV. 2.0.0 – Added bit descriptions for bits 7, 6, 5 & 4 in register 0x011B.



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