GENERAL DESCRIPTION

The XR17C158[1] (158) is an octal Universal Asynchronous Receiver and Transmitter (UART). The device is designed to meet the 32-bit PCI Bus and high bandwidth requirement in communication systems. The global interrupt source register provides a complete interrupt status indication for all 8 channels to speed up interrupt parsing. Each UART has its own 16C550 compatible set of configuration registers, transmit and receive FIFOs of 64 bytes, fully programmable transmit and receive FIFO level triggers, transmit and receive FIFO level counters, automatic RTS/CTS or DTR/DSR hardware flow control with programmable hysteresis, automatic software (Xon/Xoff) flow control, IrDA (Infrared Data Association) encoder/decoder, 8 multi-purpose definable inputs/outputs, and a 16-bit general purpose timer/counter.

NOTE: 1 Covered by U.S. Patents #5,649,122 and #5,949,787

APPLICATIONS

- Remote Access Servers
- Ethernet Network to Serial Ports
- Network Management
- Factory Automation and Process Control
- Point-of-Sale Systems
- Multi-port RS-232/RS-422/RS-485 Cards

FEATURES

- High Performance Octal UART
- 32-bit PCI Bus Interface with EEPROM Interface
  - Interrupt Source Register for all 8 UARTs
  - Data Transfer in Byte, Word and Double-word
  - Read/Write Burst Operation
- Each UART Includes
  - 16C550 Compatible Registers
  - 64-byte Transmit and Receive FIFOs
  - Transmit and Receive FIFO Level Counters
  - Automatic RTS/CTS or DTR/DSR Flow Control
  - Automatic Xon/Xoff Software Flow Control
  - RS485 Half-duplex Control with Selectable Delay
  - Infrared (IrDA 1.0) Data Encoder/Decoder
  - Programmable Data Rate with Prescaler
  - Up to 6.25 Mbps Serial Data Rate
- Eight Multi-Purpose Inputs/outputs
- A General Purpose 16-bit Timer/Counter
- Sleep Mode with Automatic Wake-up
- 5V Operation (PCI Compliance)
- Same package and pinout as the XR17C154, XR17D154 and XR17D158
- 144-pin LQFP Package (20x20x1.4mm)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 1. BLOCK DIAGRAM

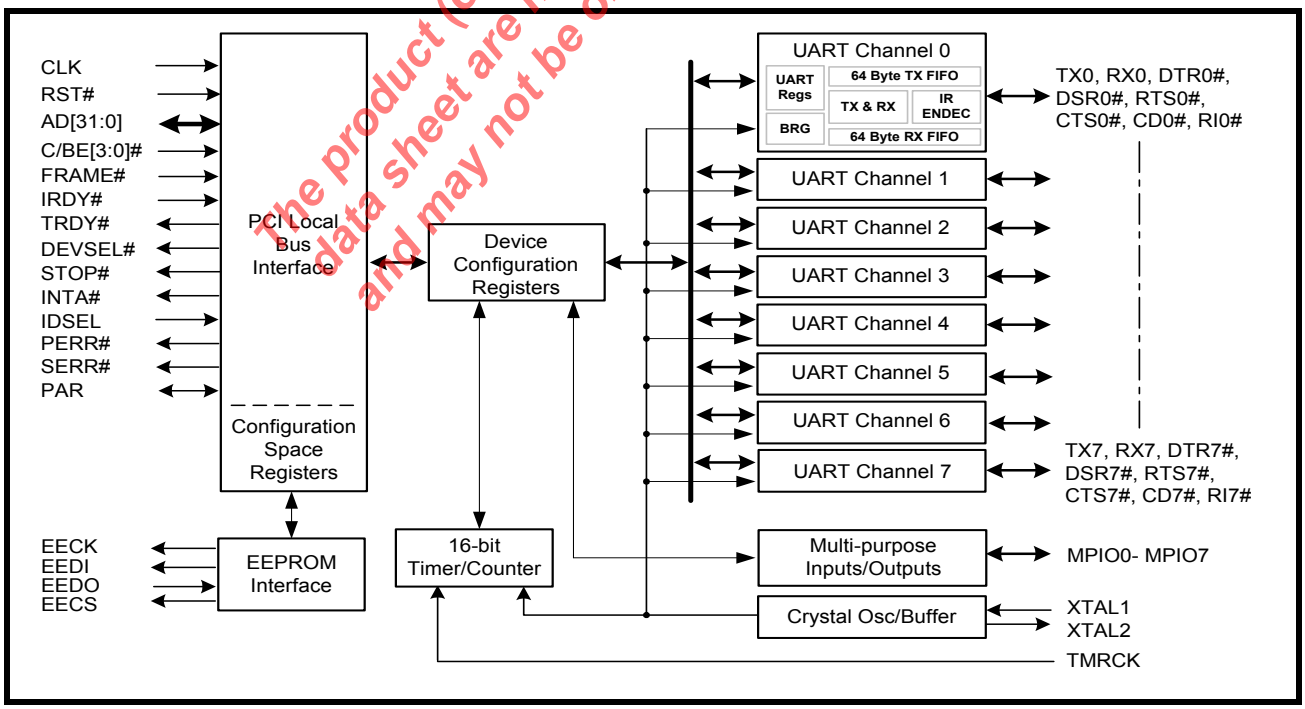
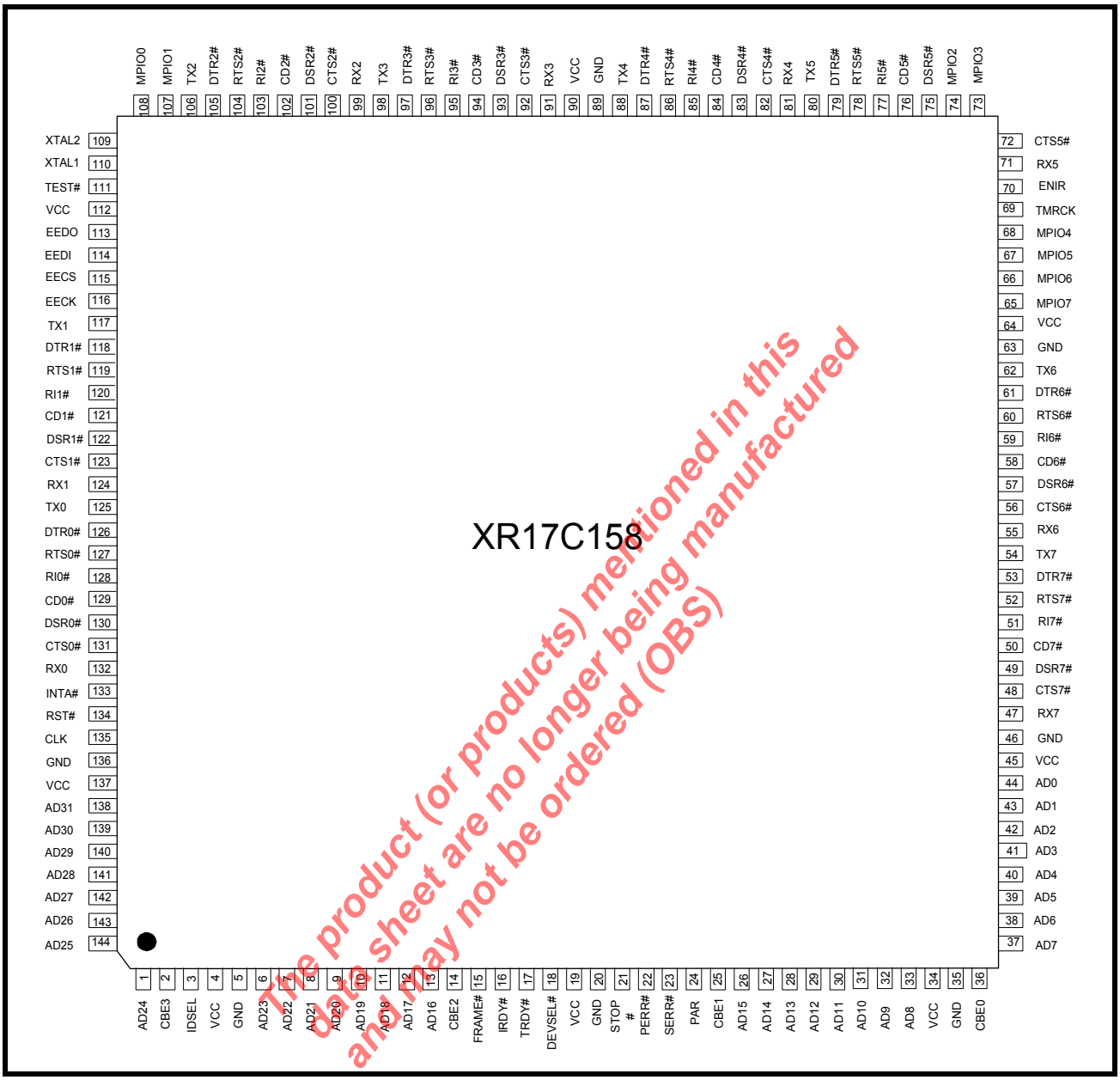


FIGURE 2. PIN OUT OF THE DEVICE



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
XR17C158CV	144-Lead LQFP	0°C to +70°C	Active
XR17C158IV	144-Lead LQFP	-40°C to +85°C	Active

PIN DESCRIPTIONS

Pin Description

NAME	PIN #	TYPE	DESCRIPTION
PCI LOCAL BUS INTERFACE			
RST#	134	I	Bus reset input (active low). It resets the PCI local bus configuration space registers, device configuration registers and UART channel registers to the default condition, see Table 19.
CLK	135	I	Bus clock input of up to 33.34MHz at 5V.
AD31-AD25, AD24, AD23-AD16, AD15-AD8, AD7-AD0	138-144, 1, 6-13, 26-33, 37-44	IO	Address data lines [31:0] (bidirectional).
FRAME#	15	I	Bus transaction cycle frame (active low). It indicates the beginning and duration of an access.
C/BE0#-C/BE3#	36,25,14,2	I	Bus Command/Byte Enable [3:0] (active low). This line is multiplexed for bus Command during the address phase and Byte Enables during the data phase.
IRDY#	16	I	Initiator Ready (active low). During a write, it indicates that valid data is present on data bus. During a read, it indicates the master is ready to accept data.
TRDY#	17	O	Target Ready (active low).
STOP#	21	O	Target request to stop current transaction (active low).
IDSEL	3	I	Initialization device select (active high).
DEVSEL#	18	O	Device select to the XR17C158 (active low).
INTA#	133	OD	Device interrupt from XR17C158 (open drain, active low).
PAR	24	IO	Parity is even across AD[31:0] and C/BE[3:0]# (bidirectional, active high).
PERR#	22	O	Data Parity error indicator, except for Special Cycle transactions (active low). Optional in bus target application.
SERR#	23	OD	System error indicator, Address parity or Data parity during Special Cycle transactions (open drain, active low). Optional in bus target application.
MODEM OR SERIAL I/O INTERFACE			
TX0	125	O	UART channel 0 Transmit Data or infrared transmit data.
RX0	132	I	UART channel 0 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS0#	127	O	UART channel 0 Request to Send or general purpose output (active low).
CTS0#	131	I	UART channel 0 Clear to Send or general purpose input (active low).
DTR0#	126	O	UART channel 0 Data Terminal Ready or general purpose output (active low).
DSR0#	130	I	UART channel 0 Data Set Ready or general purpose input (active low).
CD0#	129	I	UART channel 0 Carrier Detect or general purpose input (active low).
RI0#	128	I	UART channel 0 Ring Indicator or general purpose input (active low).
TX1	117	O	UART channel 1 Transmit Data or infrared transmit data.
RX1	124	I	UART channel 1 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses can be inverted internally prior the decoder by FCTR[4].
RTS1#	119	O	UART channel 1 Request to Send or general purpose output (active low).
CTS1#	123	I	UART channel 1 Clear to Send or general purpose input (active low).

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Pin Description

NAME	PIN #	TYPE	DESCRIPTION
DTR1#	118	O	UART channel 1 Data Terminal Ready or general purpose output (active low).
DSR1#	122	I	UART channel 1 Data Set Ready or general purpose input (active low).
CD1#	121	I	UART channel 1 Carrier Detect or general purpose input (active low).
RI1#	120	I	UART channel 1 Ring Indicator or general purpose input (active low).
TX2	106	O	UART channel 2 Transmit Data or infrared transmit data.
RX2	99	I	UART channel 2 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS2#	104	O	UART channel 2 Request to Send or general purpose output (active low).
CTS2#	100	I	UART channel 2 Clear to Send or general purpose input (active low).
DTR2#	105	O	UART channel 2 Data Terminal Ready or general purpose output (active low).
DSR2#	101	I	UART channel 2 Data Set Ready or general purpose input (active low).
CD2#	102	I	UART channel 2 Carrier Detect or general purpose input (active low).
RI2#	103	I	UART channel 2 Ring Indicator or general purpose input (active low).
TX3	98	O	UART channel 3 Transmit Data or infrared transmit data.
RX3	91	I	UART channel 3 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS3#	96	O	UART channel 3 Request to Send or general purpose output (active low).
CTS3#	92	I	UART channel 3 Clear to Send or general purpose input (active low).
DTR3#	97	O	UART channel 3 Data Terminal Ready or general purpose output (active low).
DSR3#	93	I	UART channel 3 Data Set Ready or general purpose input (active low).
CD3#	94	I	UART channel 3 Carrier Detect or general purpose input (active low).
RI3#	95	I	UART channel 3 Ring Indicator or general purpose input (active low).
TX4	88	O	UART channel 4 Transmit Data or infrared transmit data.
RX4	81	I	UART channel 4 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS4#	86	O	UART channel 4 Request to Send or general purpose output (active low).
CTS4#	82	I	UART channel 4 Clear to Send or general purpose input (active low).
DTR4#	87	O	UART channel 4 Data Terminal Ready or general purpose output (active low).
DSR4#	83	I	UART channel 4 Data Set Ready or general purpose input (active low).
CD4#	84	I	UART channel 4 Carrier Detect or general purpose input (active low).
RI4#	85	I	UART channel 4 Ring Indicator or general purpose input (active low).
TX5	80	O	UART channel 5 Transmit Data or infrared transmit data.
RX5	71	I	UART channel 5 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS5#	78	O	UART channel 5 Request to Send or general purpose output (active low).
CTS5#	72	I	UART channel 5 Clear to Send or general purpose input (active low).
DTR5#	79	O	UART channel 5 Data Terminal Ready or general purpose output (active low).
DSR5#	75	I	UART channel 5 Data Set Ready or general purpose input (active low).
CD5#	76	I	UART channel 5 Carrier Detect or general purpose input (active low).
RI5#	77	I	UART channel 5 Ring Indicator or general purpose input (active low).

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Pin Description

NAME	PIN #	TYPE	DESCRIPTION
TX6	62	O	UART channel 6 Transmit Data or infrared transmit data.
RX6	55	I	UART channel 6 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS6#	60	O	UART channel 6 Request to Send or general purpose output (active low).
CTS6#	56	I	UART channel 6 Clear to Send or general purpose input (active low).
DTR6#	61	O	UART channel 6 Data Terminal Ready or general purpose output (active low).
DSR6#	57	I	UART channel 6 Data Set Ready or general purpose input (active low).
CD6#	58	I	UART channel 6 Carrier Detect or general purpose input (active low).
RI6#	59	I	UART channel 6 Ring Indicator or general purpose input (active low).
TX7	54	O	UART channel 7 Transmit Data or infrared transmit data.
RX7	47	I	UART channel 7 Receive Data or infrared receive data. Normal RXD input idles HIGH. The infrared pulses typically idle LOW but can be inverted internally prior the decoder by FCTR[4].
RTS7#	52	O	UART channel 7 Request to Send or general purpose output (active low).
CTS7#	48	I	UART channel 7 Clear to Send or general purpose input (active low).
DTR7#	53	O	UART channel 7 Data Terminal Ready or general purpose output (active low).
DSR7#	49	I	UART channel 7 Data Set Ready or general purpose input (active low).
CD7#	50	I	UART channel 7 Carrier Detect or general purpose input (active low).
RI7#	51	I	UART channel 7 Ring Indicator or general purpose input (active low).
ANCILLARY SIGNALS			
MPIO0	108	I/O	Multi-purpose input/output 0. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT
MPIO1	107	I/O	Multi-purpose input/output 1. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO2	74	I/O	Multi-purpose input/output 2. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO3	73	I/O	Multi-purpose input/output 3. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO4	68	I/O	Multi-purpose input/output 4. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO5	67	I/O	Multi-purpose input/output 5. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO6	66	I/O	Multi-purpose input/output 6. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
MPIO7	65	I/O	Multi-purpose input/output 7. The function of this pin is defined thru the Configuration Register MPIOSEL, MPIOLVL, MPIOINV, MPIO3T and MPIOINT.
EECK	116	O	Serial clock to EEPROM. An internal clock of CLK divide by 256 is used for reading the vendor and sub-vendor ID during power up or reset. However, it can be manually clocked thru the Configuration Register REGB.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Pin Description

NAME	PIN #	TYPE	DESCRIPTION
EECS	115	O	Chip select to a EEPROM device like 93C46. It is manually selectable thru the Configuration Register REGB. Requires a pull-up 4.7K ohm resistor for external sensing of EEPROM during power up. See DAN112 for further details.
EEDI	114	O	Write data to EEPROM device. It is manually accessible thru the Configuration Register REGB.
EEDO	113	I	Read data from EEPROM device. It is manually accessible thru the Configuration Register REGB.
XTAL1	110	I	Crystal or external clock input.
XTAL2	109	O	Crystal or buffered clock output.
TMRCK	69	I	16-bit timer/counter external clock input.
ENIR	70	I	Infrared mode enable (active high). This pin is sampled during power up, following a hardware reset (RST#) or soft-reset (register RESET). It can be used to start up all 8 UARTs in the infrared mode. The sampled logic state is transferred to MCR bit-6 in the UART.
TEST#	111	I	Factory Test. Connect to VCC for normal operation.
VCC	4,19,34,45,64, 90,112,137		+5V power supply. For a pin-to-pin compatible device that operates at 3.3V, see the XR17D158.
GND	5,20,35,46,63, 89,136		Power supply common, ground.

NOTE: *Pin type: I=Input, O=Output, IO= Input/output, OD=Output Open Drain.*

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FUNCTIONAL DESCRIPTION

The XR17C158 (158) integrates the functions of 8 enhanced 16550 UARTs with the PCI Local Bus interface and a non-volatile memory interface for PCI bus's plug-and-play auto-configuration, a 16-bit timer/counter, 8 multi-purpose inputs/outputs, and an on-chip oscillator. The PCI local bus is a synchronous timing bus where all bus transactions are associated to the bus clock of up to 33.34MHz. The 158 supports 32-bit wide read and write data transfer operations including data burst mode through the PCI Local Bus interface. Read and write data operations may be in byte, word or double-word (DWORD) format. A single 32-bit interrupt status register provides interrupts status for all 8 UARTs, timer/counter, multipurpose inputs/outputs, and a special sleep wake up indicator. There are three sets of register in the device. First, the PCI local bus configuration registers for PCI auto configuration. A set of device configuration registers for overall control, 32-bit wide transmit and receive data transfer, and monitoring of the 8 UART channels. Lastly, each UART channel has its own 16550 UART compatible configuration register set for individual channel control, status, and byte wide data transfer.

Each UART has 64-byte FIFOs, automatic RTS/CTS or DTR/DSR hardware flow control with hysteresis control, automatic Xon/Xoff and special character software flow control, programmable transmit and receive FIFO trigger level, FIFO level counters, infrared encoder and decoder (IrDA ver. 1.0), programmable baud rate generator with a prescaler of 1X or 4X, and data rate up to 6.25 Mbps at 8X sampling clock. The XR17C158 bus timing and drive capability meets the PCI local bus specification revision 2.2 for 5 volt operation over the temperature range. For a pin-to-pin compatible part that can operate at 3.3V, see the XR17D158. The XR17C158 is available in a thin 144-pin LQFP (20x20x1.0mm) package in commercial and industrial temperature ranges.

PCI Local Bus Interface

This is the host interface and it meets the PCI Local Bus Specification revision 2.2 at 5V. The PCI local bus operations are synchronous meaning each transaction is associated to the bus clock. The XR17C158 can operate with the bus clock of up to a 33.34MHz. Data transfers operation can be formatted in 8-bit, 16-bit, 24-bit or 32-bit wide. With 32-bit data operations, it pushes the data transfer rate on the bus up to 132 MByte/sec. This increases the overall system's communication performance up to 16 times better than the 8-bit ISA bus. See PCI local bus specification revision 2.2 for bus operation details.

PCI Local Bus Configuration Space Registers

A set of PCI local bus configuration space register is provided. These registers provide the PCI local bus operating system with the card's vendor ID, device ID, sub-vendor ID, product model number, and resources and capabilities. The PCI local bus operating system collects this data from all the cards on the bus during the auto configuration phase that follows immediately after a power up or system reset/reboot. After it has sorted out all devices on the bus, it defines and download the operating conditions to the cards. One of the definitions is the base address loaded into the Base Address Register (BAR) where the card will be operating in the PCI local bus memory space.

EEPROM Interface

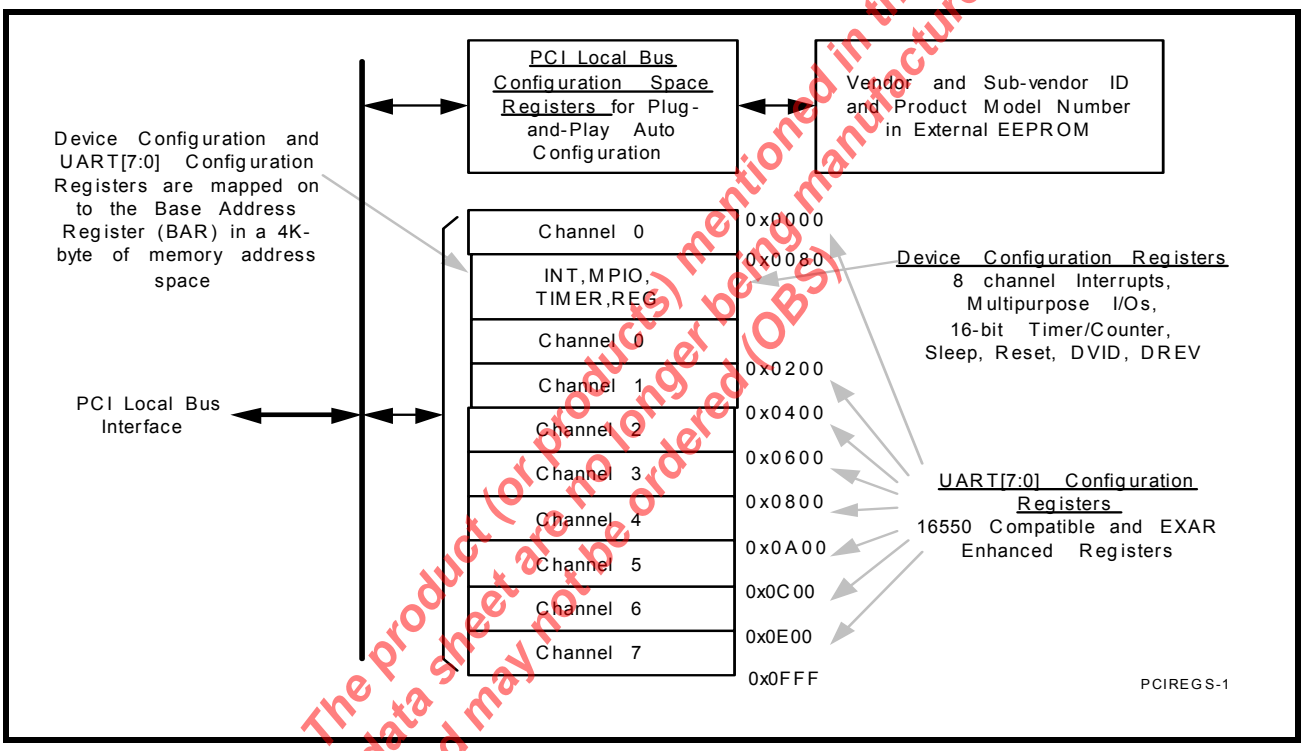
An external 93C46 EEPROM is only used to store the vendor's ID and model number, and the sub-vendor's ID and product model number. This information is only used with the plug-and-play auto configuration of the PCI local bus. These data provide automatic hardware installation onto the PCI bus. The EEPROM interface consists of 4 signals, EEDI, EEDO, EECS, and EECK. The EEPROM is not needed when auto configuration is not required in the application. However, If your design requires non-volatile memory for other purpose. It is possible to store and retrieve data on the EEPROM through a special PCI device configuration register. See application note DAN112 for its programming details.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

1.0 XR17C158 REGISTERS

The XR17C158 UART has three different sets of registers as shown in Figure 3. The PCI local bus configuration space registers are for plug-and-play auto-configuration when connecting the device to the PCI bus. This auto-configuration feature makes installation very easy into a PCI system and it is part of the PCI local bus specification. The second register set is the device configuration registers that are accessible directly from the PCI bus for programming general operating conditions of the device and monitoring the status of various functions. These registers are mapped into 4K of the PCI bus memory address space. These functions include all 8 channel UART's interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode, soft-reset, and device identification and revision. And lastly, each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. All 8 sets of channel registers are embedded inside the device configuration registers space, which provides faster access. The following paragraphs describe all 3 sets of registers in detail.

FIGURE 3. THE XR17C158 REGISTER SETS



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

1.1 PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

The PCI local bus configuration space registers are responsible for setting up the device's operating environment in the PCI local bus. The pre-defined operating parameters of the device is read by the PCI bus plug-and-play auto-configuration manager in the operating system. After the PCI bus has collected all data from every device/card on the bus, it defines and downloads the memory mapping information to each device/card about their individual operation memory address location and conditions. The operating memory mapped address location is downloaded into the Base Address Register (BAR) register, 0x10. The plug-and-play auto configuration feature is only available when an external 93C46 EEPROM is used. The EEPROM contains the device vendor and sub-vendor data required by the auto-configuration setup.

TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX)
0x00	31:16	RWR[1]	Device ID (Exar device ID number)	0x0158
	15:0	RWR[1]	Vendor ID (Exar) specified by PCISIG	0x13A8
0x04	31 30 29:28	RWC RWC RO	Parity error detected. Cleared by writing a logic 1. System error detected. Cleared by writing a logic 1. Unused	0000
	27	R-Reset	Target Abort. Set whenever 158 terminates with a target abort.	0
	26:25	RO	DEVSEL# timing.	00
	24	RO	Unemployments bus master error reporting bit	0
	23	RO	Fast back to back transactions are supported	1
	22:16	RO	Reserved Status bits	000 0000
	15:9,7, 5,4,3,2	RO	Command bits (reserved)	0x0000
	8	RWR	SERR# driver enable. Logic 1= enable driver and 0=disable driver	0
	6	RWR	Parity error enable. Logic 1= respond to parity error and 0=ignore	0
	1	RWR	Command controls a device's response to mem space accesses: Logic 0=disable mem space accesses, Logic 1= enable mem space accesses	0
	0	RO	Device's response to I/O space accesses is disabled. (Logic 0 = disable I/O space accesses)	0
0x08	31:8	RO	Class Code (Simple 550 Communication Controller).	0x070002
	7:0	RO	Revision ID (Exar device revision number)	Current Rev. value
0x0C	31:24	RO	BIST (Built-in Self Test)	0x00
	23:16	RO	Header Type (a single function device with one BAR)	0x00
	15:8	RO	Unimplemented Latency Timer (needed only for bus master)	0x00
	7:0	RO	Unimplemented Cache Line Size	0x00
0x10	31:12	RWR	Memory Base Address Register (BAR)	0x00
	11:0	RO	Claims a 4K address space for the memory mapped UARTs	0x000
0x14	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x18h	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x1C	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x20	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x24	31:0	RO	Unimplemented Base Address Register (returns zeros)	0x00000000
0x28	31:0	RO	Reserved	0x00000000

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TABLE 1: PCI LOCAL BUS CONFIGURATION SPACE REGISTERS

ADDRESS	BITS	TYPE	DESCRIPTION	RESET VALUE (HEX)
0x2C	31:16	RWR[1]	Subsystem ID (write from external EEPROM by customer)	0x0000
	15:0	RWR[1]	Subsystem Vendor ID (write from external EEPROM by customer)	0x0000
0x30	31:0	RO	Expansion ROM Base Address (Unimplemented)	0x00000000
0x34	31:0	RO	Reserved (returns zeros)	0x00000000
0x38	31:0	RO	Reserved (returns zeros)	0x00000000
0x3C	31:24	RO	Unimplemented MAXLAT	0x00
	23:16	RO	Unimplemented MINGNT	0x00
	15:8	RO	Interrupt Pin, use INTA#.	0x01
	7:0	RWR	Interrupt Line.	0xXX

NOTE: RWR[1]=Read/Write from external EEPROM. RWR=Read/Write from AD[31:0]. RO= Read Only. RWC=Read/Write-Clear.

1.2 Device Configuration Register Set

The device configuration registers and a special way to access each of the UART's transmit and receive data FIFOs are accessible directly from the PCI data bus. This provides easy programming of general operating parameters to the 158 UART and for monitoring the status of various functions. The registers occupy 4K of PCI bus memory address space. These addresses are offset onto the basic memory address, a value loaded into the Memory Base Address Register (BAR) in the PCI local bus configuration register set. These registers control or report on all 8 channel UARTs functions that include interrupt control and status, 16-bit general purpose timer control and status, multipurpose inputs/outputs control and status, sleep mode control, soft-reset control, and device identification and revision, and others.

The registers set is mapped into 8 address blocks where each UART channel occupies 512 bytes memory space for its own 16550 compatible configuration registers. The device configuration and control registers are embedded inside the UART channel zero's address space between 0x0080 to 0x0093. All these registers can be accessed in 8, 16, 24 or 32 bit width depending on the starting address given by the host at beginning of the bus cycle. Transmit and receive data may be loaded or unloaded in 8, 16, 24 or 32 bit format to the register's address. Every time a read or write operation is made to the transmit or receive register, its FIFO data pointer is automatically bumped to the next sequential data location either in byte, word or dword. One special case applies to the receive data unloading when reading the receive data together with its LSR register content. The host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

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TABLE 2: XR17C158 DEVICE CONFIGURATION REGISTERS

OFFSET ADDRESS	MEMORY SPACE	READ/WRITE	DATA WIDTH	COMMENT
0x000 - 0x00F	UART channel 0 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x010 - 0x07F	Reserved			
0x080 - 0x093	DEVICE CONFIG. REGISTERS	(Table 3)	8/16/24/32	
0x094 - 0x0FF	Reserved			
0x100 - 0x13F	UART 0 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x100 - 0x13F	UART 0 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x140 - 0x17F	Reserved			
0x180 - 0x1FF	UART 0 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0x200 - 0x20F	UART channel 1 Regs	(Table 11 & Table 12)	8/16//24/32	First 8 regs are 16550 compatible
0x210 - 0x2FF	Reserved			
0x300 - 0x33F	UART 1 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x300 - 0x33F	UART 1 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x340 - 0x37F	Reserved			
0x380 - 0x3FF	UART 1 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0x400 - 0x40F	UART channel 2 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x410 - 0x4FF	Reserved			
0x500 - 0x53F	UART 2 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x500 - 0x53F	UART 2 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x540 - 0x57F	Reserved			
0x580 - 0x5FF	UART 2 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0x600 - 0x60F	UART channel 3 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x610 - 0x6FF	Reserved			
0x700 - 0x73F	UART 3 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x700 - 0x73F	UART 3 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data

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TABLE 2: XR17C158 DEVICE CONFIGURATION REGISTERS

OFFSET ADDRESS	MEMORY SPACE	READ/WRITE	DATA WIDTH	COMMENT
0x740 - 0x77F	Reserved			
0x780 - 0x7FF	UART 3 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0x800 - 0x80F	UART channel 4 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0x810 - 0x8FF	Reserved			
0x900 - 0x93F	UART 4 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0x900 - 0x93F	UART 4 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0x940 - 0x97F	Reserved			
0x980 - 0x9FF	UART 4 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0xA00 - 0xA0F	UART channel 5 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0xA10 - 0xAFF	Reserved	ite		
0xB00 - 0xB3F	UART 5 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0xB00 - 0xB3F	UART 5 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0xB40 - 0xB7F	Reserved			
0xB80 - 0xBFF	UART 5 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0xC00 - 0xC0F	UART channel 6 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0xC10 - 0xCFF	Reserved			
0xD00 - 0xD3F	UART 6 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0xD00 - 0xD3F	UART 6 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data
0xD40 - 0xD7F	Reserved			
0xD80 - 0xDFF	UART 6 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR
0xE00 - 0xE0F	UART channel 7 Regs	(Table 11 & Table 12)	8/16/24/32	First 8 regs are 16550 compatible
0xE10 - 0xEFF	Reserved			
0xF00 - 0xF3F	UART 7 – Read FIFO	Read-Only	8/16/24/32	64 bytes of RX FIFO data
0xF00 - 0xF3F	UART 7 – Write FIFO	Write-Only	8/16/24/32	64 bytes of TX FIFO data

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 2: XR17C158 DEVICE CONFIGURATION REGISTERS

OFFSET ADDRESS	MEMORY SPACE	READ/WRITE	DATA WIDTH	COMMENT
0xF40 - 0xF7F	Reserved			
0xF80 - 0xFFF	UART 7 – Read FIFO with errors	Read-Only	16/32	64 bytes of RX FIFO data + LSR

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 3: DEVICE CONFIGURATION REGISTERS SHOWN IN BYTE ALIGNMENT

ADDRESS [A7:A0]	REGISTER	READ/WRITE COMMENT	RESET STATE
Ox080	INT0 [7:0]	Read-only Interrupt [7:0]	Bits 7-0 = 0x00
Ox081	INT1 [15:8]	Read-only	Bits 7-0 = 0x00
Ox082	INT2 [23:16]	Read-only	Bits 7-0 = 0x00
Ox083	INT3 [31:24]	Read-only	Bits 7-0 = 0x00
Ox084	TIMERCNTL	Read/Write Timer Control	Bits 7-0 = 0x00
Ox085	TIMER	Reserved	Bits 7-0 = 0x00
Ox086	TIMERLSB	Read/Write Timer LSB	Bits 7-0 = 0x00
Ox087	TIMERMSB	Read/Write Timer MSB	Bits 7-0 = 0x00
Ox088	8XMODE	Read/Write	Bits 7-0 = 0x00
Ox089	REGA	Reserved	Bits 7-0 = 0x00
Ox08A	RESET	Write-only Self clear bits after executing Reset	Bits 7-0 = 0x00
Ox08B	SLEEP	Read/Write Sleep mode	Bits 7-0 = 0x00
Ox08C	DREV	Read-only Device revision	Bits 7-0 = 0x09
Ox08D	DVID	Read-only Device identification	Bits 7-0 = 0x28
Ox08E	REGB	Write-only	Bits 7-0 = 0x00
Ox08F	MPIOINT	Read/Write MPIO interrupt mask	Bits 7-0 = 0x00
Ox090	MPIOLVL	Read/Write MPIO level control	Bits 7-0 = 0x00
Ox091	MPIO3T	Read/Write MPIO output control	Bits 7-0 = 0x00
Ox092	MPIOINV	Read/Write MPIO input polarity select	Bits 7-0 = 0x00
Ox093	MPIOSEL	Read/Write MPIO select	Bits 7-0 = 0xFF

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TABLE 4: DEVICE CONFIGURATION REGISTERS SHOWN IN DWORD ALIGNMENT

ADDRESS	REGISTER	BYTE 3 [31:24]	BYTE 2 [23:16]	BYTE 1 [15:8]	BYTE 0 [7:0]
0x080-083	INTERRUPT (read-only)	INT3	INT2	INT1	INT0
0x084-087	TIMER (read/write)	TIMERMSB	TIMERLSB	TIMER (reserved)	TIMERCNTL
0x088-08B	ANCILLARY1 (read/write)	SLEEP	RESET	REGA (reserved)	8XMODE
0x08C-08F	ANCILLARY2 (read-only)	MPIOINT	REGB	DVID	DREV
0x090-093	MPIO (read/write)	MPIOSEL	MPIOINV	MPIO3T	MPIOLVL

1.2.1 The Interrupt Status Register

The XR17C158 has a 32-bit wide register [INT0, INT1, INT2 and INT3] to provide interrupt information and supports two interrupt schemes. The first scheme is an 8-bit indicator representing all 8 channels with each bit representing each channel from 0 to 7. This permits the interrupt routine to quickly vector and serve that UART channel and determine the source(s) in each individual routines. INT0 bit-0 represents the interrupt status for UART channel 0 when its transmitter, receiver, line status, or modem port status requires service. Other bits in the INT0 register provide indication for the other channels with bit-7 representing UART channel 7 respectively.

The second scheme provides detail about the source of the interrupts for each UART channel. All the interrupts are encoded into a 3-bit code. This 3-bit code represents 7 interrupts corresponding to individual UART's transmitter, receiver, line status, modem port status. INT1, INT2 and INT3 registers provide the 24-bit interrupt status for all 8 channels. Bits 8, 9 and 10 representing channel 0 and bits 29, 30 and 31 representing channel 7 respectively. All 8 channel interrupts status are available with a single DWORD read operation. This feature allows the host to quickly vector and serve the interrupts, reducing service interval, hence, reducing the host bandwidth requirement. **Figure 4** shows the 4-byte interrupt register and its make up.

GLOBAL INTERRUPT REGISTER (DWORD) [default 0x00-00-00-00]

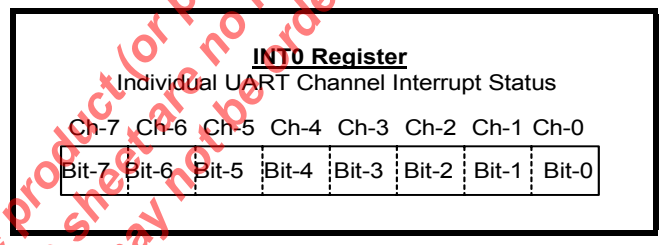
INT3 [31:24]	INT2 [23:16]	INT1 [15:8]	INT0 [7:0]

A special interrupt condition is generated by the 158 when it wakes up from sleep mode. This special interrupt is cleared by reading the INT0 register. If there are not any other interrupts pending, the value read from INT0 would be 0x00.

INT0 [7:0] Channel Interrupt Indicator

Each bit gives an indication of the channel that has requested for service. Bit-0 represents channel 0 and bit-7 indicates channel 7. Logic 1 indicates that a channel has called for service. The interrupt bit clears after reading the appropriate register of the interrupting channel register, see Interrupt Clearing section.

The INT0 register provides individual status for each channel



INT3, INT2 and INT1 [32:8]

Twenty four bit encoded interrupt indicator. Each channel's interrupt is encoded into 3 bits for receive, transmit, and status. Bits [10:8] represent channel 0 and go up to channel 7 with bits [31:29]. The 3 bit encoding and their priority order are shown below in **Table 5**. The Timer and MPIO interrupts are for the device and therefore they only exist within the channel 0 space (bits [10:8]) and not in any other channel.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 4. THE GLOBAL INTERRUPT REGISTER, INT0, INT1, INT2 AND INT3

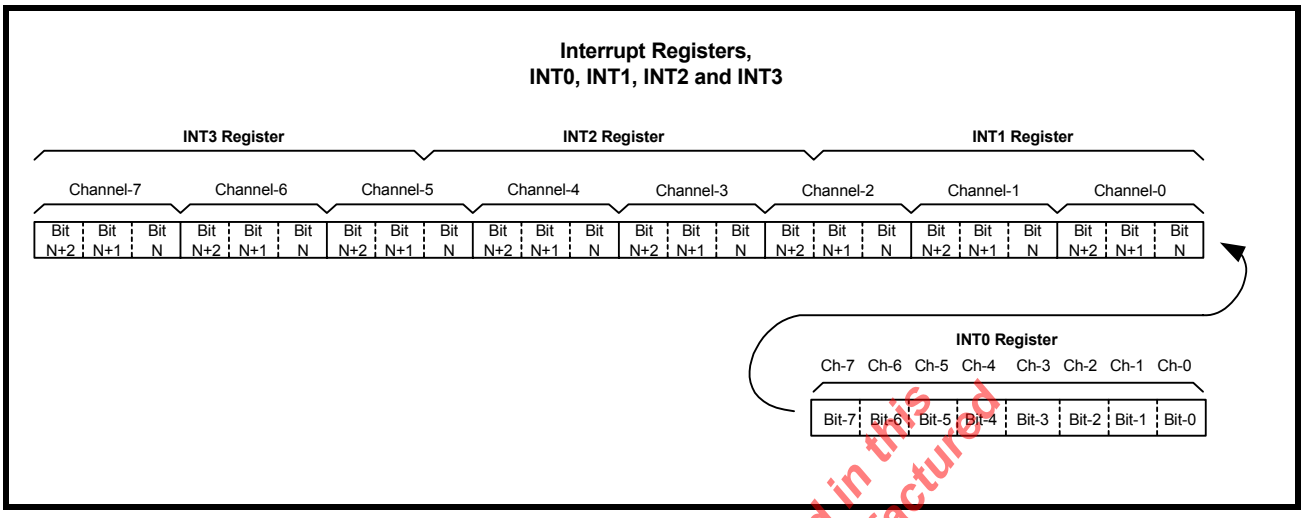


TABLE 5: UART CHANNEL [7:0] INTERRUPT SOURCE ENCODING

PRIORITY	BIT[N+2]	BIT[N+1]	BIT[N]	INTERRUPT SOURCE(S)
x	0	0	0	None
1	0	0	1	RXRDY and RX Line Status (logic OR of LSR[4:1])
2	0	1	0	RXRDY Time-out
3	0	1	1	TXRDY, THR or TSR (auto RS485 mode) empty
4	1	0	0	MSR, RTS/CTS or DTR/DSR delta or Xoff/Xon det. or special char. detected
5	1	0	1	Reserved.
6	1	1	0	MPIO pin(s). Available only within channel 0, reserved in other channels.
7	1	1	1	TIMER Time-out. Available only within channel 0, reserved in other channels.

TABLE 6: UART CHANNEL [7:0] INTERRUPT CLEARING

RXRDY is cleared by reading data in the RX FIFO until it falls below the trigger level.
RXRDY Time-out is cleared by reading data until the RX FIFO is empty.
RX Line Status interrupt clears after reading the LSR register.
TXRDY interrupt clears after reading ISR register that is in the UART channel register set.
Modem Status Register interrupt clears after reading MSR register that is in the UART channel register set.
RTS/CTS or DTR/DSR delta interrupt clears after reading MSR register that is in the UART channel register set.
Xoff/Xon interrupt clears after reading the ISR register that is in the UART channel register set.
Special character detect interrupt is cleared by a read to ISR or after the next character is received.
TIMER Time-out interrupt clears after reading the TIMERCNTL register that is in the Device Configuration register set.
MPIO interrupt clears after reading the MPIOLVL register that is in the Device Configuration register set.

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1.2.2 General Purpose 16-bit Timer/Counter [TIMERMSB, TIMELSB, TIMER, TIMECNTL] (DEFAULT 0xXX-XX-00-00)

A 16-bit down-count timer for general purpose timer or counter. Its clock source may be selected from internal crystal oscillator or externally on pin TMRCK. The timer can be set to be a single-shot for a one-time event or re-triggerable for continue interval. An interrupt may be generated in the Interrupt Register bits [10:8] when the timer times out. It is controlled through 4 configuration registers [TIMERCNTL, TIMER, TIMELSB, TIMERMSB]. These registers provide start/stop and re-triggerable or one-shot operation. The time-out output of the Timer can be set to generate an interrupt for system or event alarm.

FIGURE 5. TIMER/COUNTER CIRCUIT

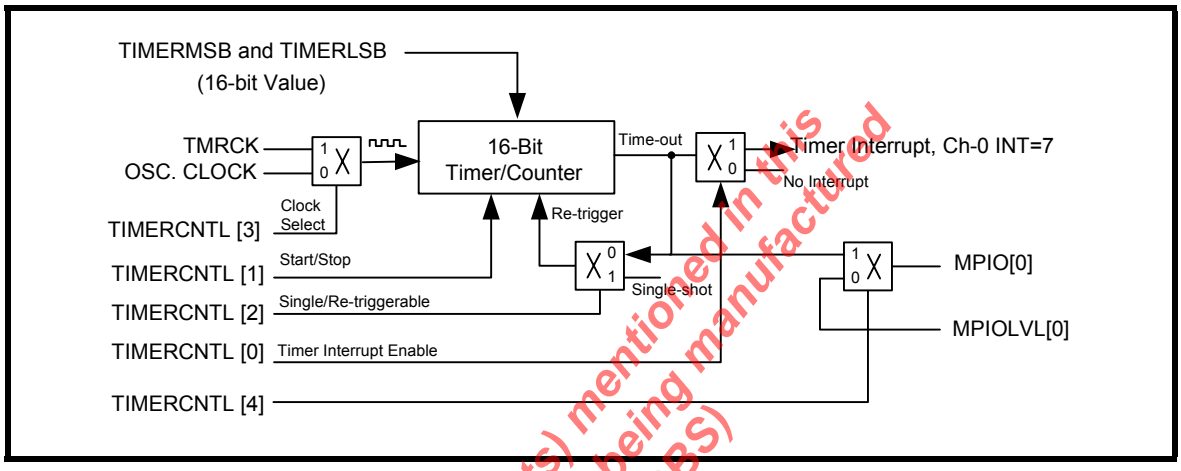


TABLE 7: TIMER CONTROL REGISTERS

TIMERCNTL [0]	Logic 0 (default) disables Timer-Counter interrupt and logic 1 enables the interrupt, reading the TIMERCNTL register clears the interrupt.
TIMERCNLT [1]	Logic 0 (default) stops/pauses the timer and logic 1 starts/re-starts the timer/counter.
TIMERCNTL [2]	Logic 0 (default) selects re-triggerable timer function and logic 1 selects one-shot (timer function).
TIMERCNTL [3]	Logic 0 (default) selects internal and logic one selects external clock to the timer/counter.
TIMERCNTL [4]	Routes the Timer-Counter interrupt to MPIO[0] if MPIOSEL[0]=0 for external event control.
TIMERCNTL [7:5]	Reserved (defaults to zero)

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

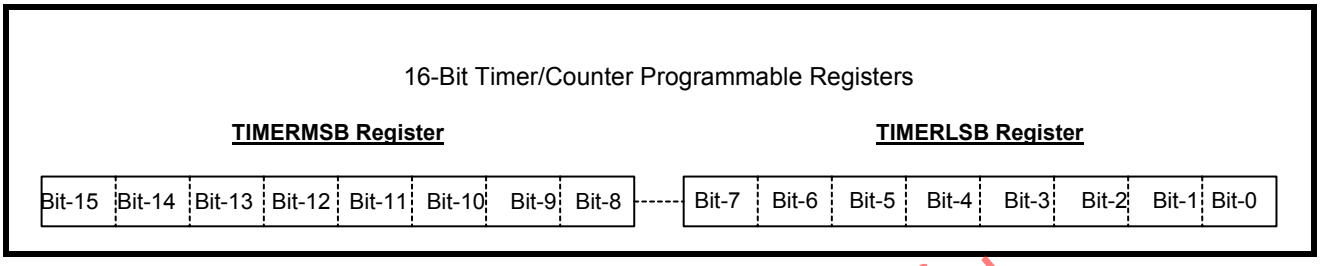
TIMERCNTL Register

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Rsvd	Rsvd	Rsvd	MPIO[0] Control	Clock Select	Single/ Re-trigger	Start/ Stop	INT Enable

TIMER [15:8] Reserved

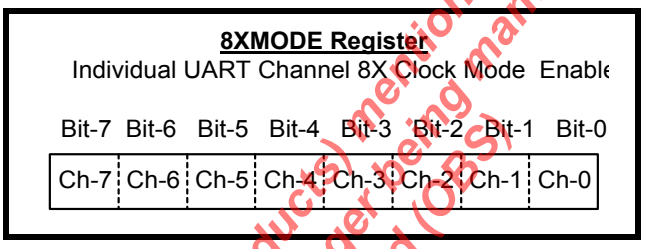
TIMERMSB [31:24] and TIMERLSB [23:16]

TIMERMSB and TIMERLSB form a 16-bit value. The least-significant bit of the timer is bit [0] of the TIMERLSB with most-significant-bit being bit [7] in TIMERMSB. Notice that these registers do not hold the current counter value when read. Reading the TIMERCNTL register will clear its interrupt. Default value is zero (timer disabled) upon powerup and reset.



1.2.3 8XMODE [7:0] (default 0x00)

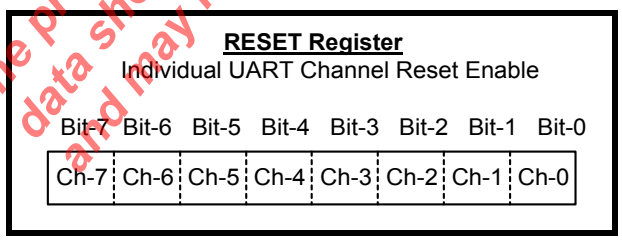
Each bit selects 8X or 16X sampling rate for that UART channel, bit-0 is channel 0. Logic 0 (default) selects normal 16X sampling and logic 1 selects 8X sampling rate. Transmit and receive data rates will double by selecting 8X sampling rate.



1.2.4 REGA [15:8] Reserved

1.2.5 RESET [23:16] (default 0x00)

The 8-bit Reset register [RESET] provides the software with the ability to reset the UART(s) when there is a need. Each bit is self-resetting after it is written a logic 1 to perform a reset to that channel. All registers in that channel will be reset to the default condition, see Table 19 for details. Bit-0 =1 resets UART channel 0 while bit-7=1 resets channel 7.



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1.2.6 SLEEP [31:24] - (default 0x00)

The 8-bit Sleep register enables each UART separately to enter Sleep mode. Sleep mode reduces power consumption when the system needs to put the UART(s) to idle. All of these conditions must be satisfied for the 158 to enter sleep mode:

- no interrupts pending (INT0 = 0x00)
- divisor is a non-zero value for all channels (ie. DLL = 0x1)
- sleep mode is enabled for all 8 channels (SLEEP = 0xFF)
- modem inputs for all channels are not toggling (MSR bits 0-3 = 0)
- RX input pins for all channels are idling HIGH

The 158 stops its crystal oscillator to conserve power in the sleep mode. User can check the XTAL2 pin for no clock output as an indication that the device has entered the sleep mode.

The 158 resumes normal operation by any of the following:

- a receive data start bit transition (HIGH to LOW) on the RX input of any channel
- a data byte is loaded to the transmitter, THR or FIFO, of any channel
- a change of logic state on any of the modem or general purpose serial inputs of any channel: CTS#, DSR#, CD#, RI#

If the 158 is awakened by any one of the above conditions, it will return to the sleep mode automatically after all interrupting conditions have been serviced and cleared. If the 158 is awakened by the modem inputs, a read to the MSR is required to reset the modem inputs. In any case, the sleep mode will not be entered while an interrupt is pending from any channel. The 158 will stay in the sleep mode of operation until it is disabled by setting Sleep = 0x00. The UART is ready after 32 crystal clocks to ensure full functionality. Also, a special interrupt is generated with an indication of no pending interrupt. Reading INT0 will clear this special interrupt. Logic 0 (default) disables the sleep mode and logic 1 enables the sleep mode for each channel. The crystal oscillator shuts down only when all 8 channels are in sleep mode.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

SLEEP Register
Individual UART Channel Sleep Enable

Ch-7	Ch-6	Ch-5	Ch-4	Ch-3	Ch-2	Ch-1	Ch-0
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

1.2.7 Device Identification and Revision

There are two internal registers that provide device identification and revision, DVID and DREV registers. The 8-bit content in the DVID register provides device identification. A return value of 0x28 from this register indicates the device is a XR17C158. The DREV register returns an 8-bit value of 0x01 for revision A with 0x02 equals to revision B and so forth. This information is very useful to the software driver for identifying which device it is communicating with and to keep up with revision changes.

DVID [15:8]

Device identification for the type of UART. The upper nibble indicates it is an XR17Cxxx series with lower nibble indicating the number of channels.

Examples:

XR17C158 or XR17D158 = 0x28

XR17C154 or XR17D154 = 0x24

XR17C152 or XR17D152 = 0x22

DREV [7:0]

Revision number of the XR17C158. A 0x01 represents "revision-A" with 0x02 for rev-B and so forth.

REGB [23:16] (default 0x00)

REGB register provides a control for simultaneous write to all 8 UARTs configuration register or individually. This is very useful for device initialization during power-up and reset routines. Also, the register provides a facility to interface to the non-volatile memory device such as a 93C46 EEPROM. In embedded applications, the user can use this facility to store proprietary data.

1.2.8 REGB Register

REGB[16](Read/Write)	Logic 0 (default) write to each UART configuration registers individually.
	Logic 1 enables simultaneous write to all 8 UARTs configuration register.
REGB[19:17]	Reserved
REGB[20] (Write-Only)	Control the EECK, clock, output (pin 116) on the EEPROM interface.
REGB[21] (Write-Only)	Control the EECS, chips select, output (pin 115) to the EEPROM device.
REGB[22] (Write-Only)	EEDI (pin 114) data input. Write data to the EEPROM device.
REGB[23] (Read-Only)	EEDO (pin 113) data output. Read data from the EEPROM device.

1.2.9 Multi-Purpose Inputs and Outputs

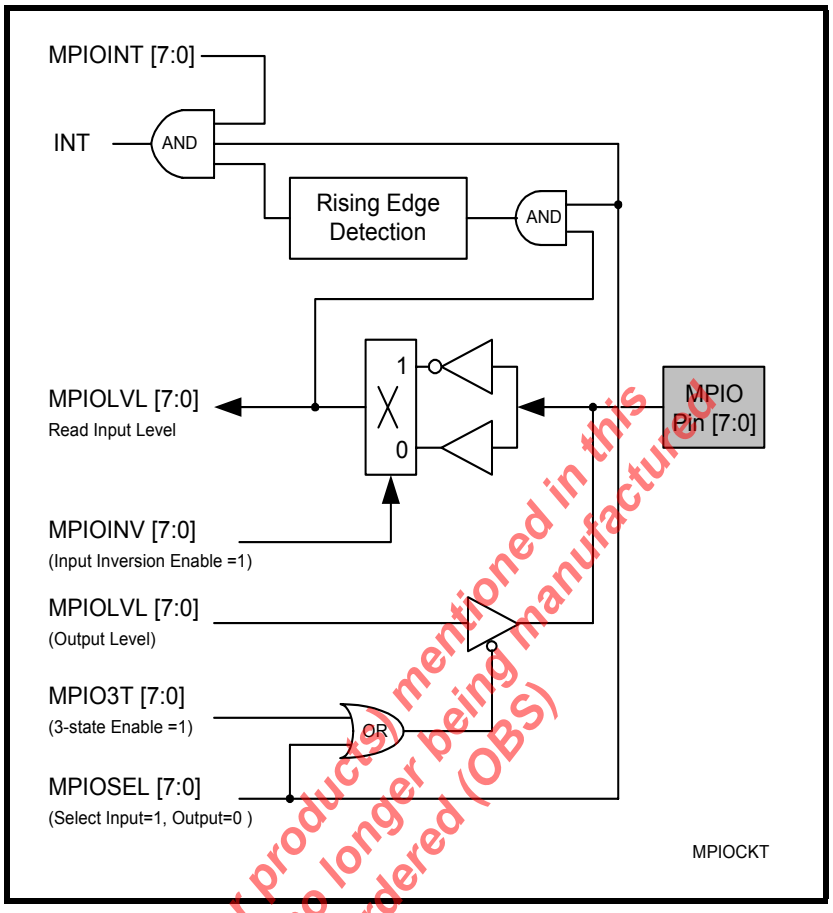
The 158 provides 8 multi-purpose inputs/outputs [MPIO7:0] for general use. Each pin can be programmed to be an input or output function. The input logic state can be set for normal or inverted level, and optionally set to generate an interrupt. The outputs can be set to be normal logic 1 or 0 state, or 3-state. Their functions and definitions are programmed through 5 registers: MPIOINT, MPIOLVL, MPIO3T, MPIOINV and MPIOSEL. If all 8 pins are set for inputs, all 8 interrupts would be OR'ed together. The OR'ed interrupt is reported in the channel 0 UART interrupt status (3-bit interrupt encoding, bits [10:8], in the global interrupt status register). SEE"THE INTERRUPT STATUS REGISTER" ON PAGE 15. The pins may also be programmed to be outputs and to the 3-state condition for signal sharing.

1.2.10 MPIO REGISTER

Bit 7 represents MPIO7 pin and bit 0 represents MPIO0 pin. There are 5 registers that select, control and monitor the 8 multipurpose inputs and outputs. **Figure 6** shows the internal circuitry.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 6. MULTIPURPOSE INPUT/OUTPUT INTERNAL CIRCUIT



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

MPIOINT [7:0] (default 0x00)

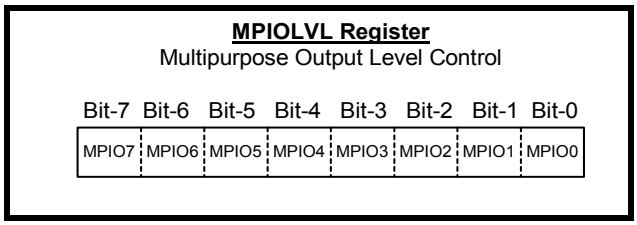
Enable multipurpose input pin interrupt. If the MPIO pin is selected by MPIOSEL as an input then bit-0 enables input pin 0 for interrupt, and bit-7 enables input pin 7. No interrupt is enable if the pin is selected to be an output. The interrupt is edge sensing and determined by MPIOINV and MPIOLVL registers. The MPIO interrupt clears after a read to register MPIOLVL. The combination of MPIOLVL and MPIOINV determines the interrupt being active low or active high, it's level trigger. Logic 0 (default) disables the pin's interrupt and logic 1 enables it.

MPIOINT Register
Multipurpose Input/Output Interrupt Enable

Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
MPIO7	MPIO6	MPIO5	MPIO4	MPIO3	MPIO2	MPIO1	MPIO0

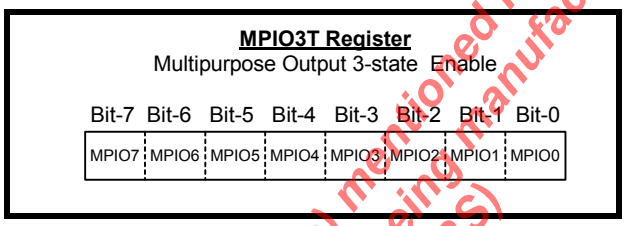
MPIOLVL [7:0] (default 0x00)

Output pin level control and input level status. The status of the input pin(s) is read on this register and output pins are controlled on this register. A logic 0 (default) sets the output to LOW and a logic 1 sets the output pin to HIGH. The MPIO interrupt will clear upon reading this register.



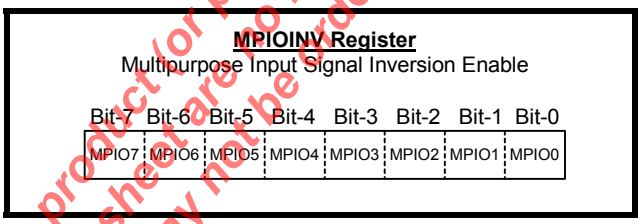
MPIO3T [7:0] (default 0x00)

Output pin tri-state control. A logic 0 (default) sets the output to active level per register MPIO3T setting, a logic 1 sets the output pin to tri-state.



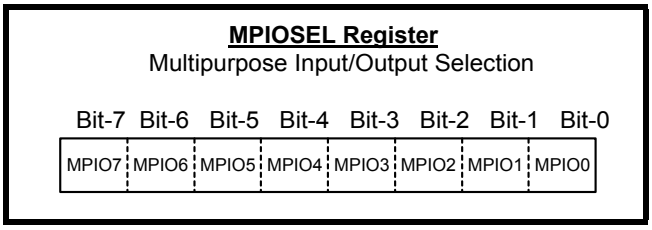
MPIOINV [7:0] (default 0x00)

Input inversion control. A logic 0 (default) does not invert the input pin logic. A logic 1 inverts the input logic level.



MPIOSEL [7:0] (default 0xFF)

Multipurpose input/output pin select. This register defines the functions of the pins. A logic 1 (default) defines the pin for input and a logic "0" for output.



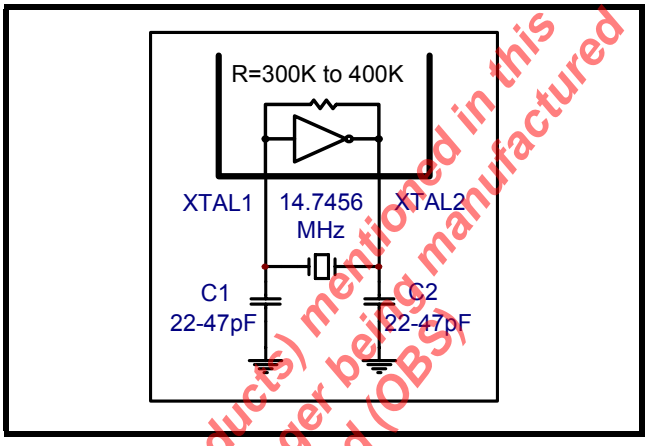
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

2.0 CRYSTAL OSCILLATOR / BUFFER

The 158 includes an on-chip oscillator (XTAL1 and XTAL2). The crystal oscillator provides the system clock to the Baud Rate Generators (BRG) in each of the 8 UARTs, the 16-bit general purpose timer/counter and internal logics. XTAL1 is the input to the oscillator or external clock buffer input with XTAL2 pin being the output. See Programmable Baud Rate Generator in the UART section for programming details.

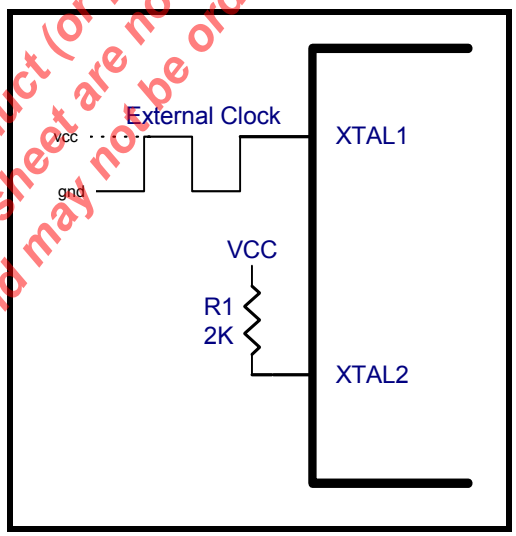
The on-chip oscillator is designed to use an industry standard microprocessor crystal (parallel resonant with 10-22 pF capacitance load, 100ppm) connected externally between the XTAL1 and XTAL2 pins (see **Figure 7**). Alternatively, an external clock can be connected to the XTAL1 pin to clock the internal 8 baud rate generators for standard or custom rates. However, for external clock frequencies greater than 24MHz, a 2K pull-up may be necessary on the XTAL2 output (see **Figure 8**). Typical oscillator connections are shown in **Figure 7**. For further reading on oscillator circuit please see application note DAN108 on EXAR's web site.

FIGURE 7. TYPICAL OSCILLATOR CONNECTIONS



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 8. EXTERNAL CLOCK CONNECTION FOR EXTENDED DATA RATE



3.0 TRANSMIT AND RECEIVE DATA

There are two methods to load transmit data and unload receive data from each UART channel. First, there is a transmit data register and receive data register for each UART channel in the device configuration register set to ease programming. These registers support 8, 16, 24 and 32 bits wide format. In the 32-bit format, it increases the data transfer rate on the PCI bus. Additionally, a special register location provides receive data byte with its associated error flags. This is a 16-bit or 32-bit read operation where the Line Status Register (LSR) content in the UART channel register is paired along with the data byte. This operation further facilitates data unloading with the error flags without having to read the LSR register separately. Furthermore, the XR17C158 supports PCI burst mode for read/write operation of up to 64 bytes of data.

The second method is through each UART channel's transmit holding register (THR) and receive holding register (RHR). The THR and RHR registers are 16550 compatible so their access is limited to 8-bit format. The software driver must separately read the LSR content for the associated error flags before reading the data byte.

3.1 DATA LOADING AND UNLOADING VIA 32-BIT PCI BURST TRANSFERS

The XR17C158 supports PCI Burst Read and PCI Burst Write transactions anywhere in the mapped memory region (except reserved areas). In addition, to utilize this feature fully, the device provides a separate memory location (apart from the 16550 register set) where the RX and the TX FIFO can be read from/written to, as shown in Table 2. The following is an extract from the table showing the burstable memory locations:

Channel N: (for channels 0 through 7) where M = 2N + 1

RX FIFO	:	0xM00 - 0xM3F (64 bytes)
TX FIFO	:	0xM00 - 0xM3F (64 bytes)
RX FIFO + status	:	0xM80 - 0xMFF (64 bytes data + 64 bytes status)

For example, the locations for channel 2 are:

Channel 2:

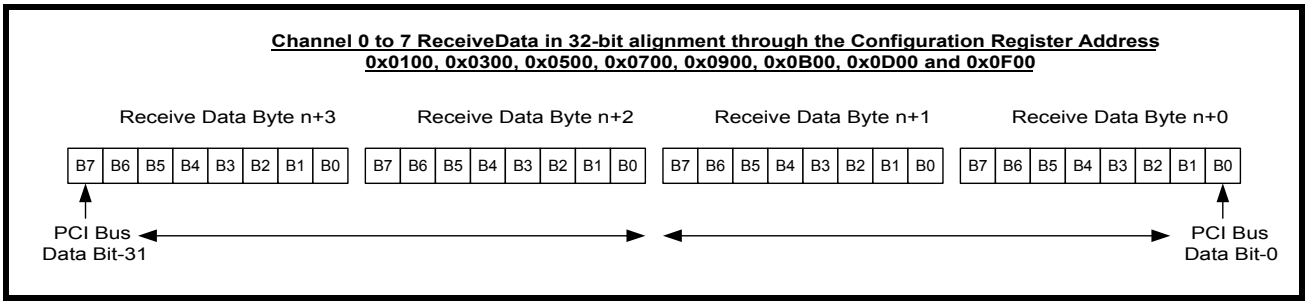
RX FIFO	:	0x500 - 0x53F (64 bytes)
TX FIFO	:	0x500 - 0x53F (64 bytes)
RX FIFO + status	:	0x580 - 0x5FF (64 bytes data + 64 bytes status)

3.1.1 Normal Rx FIFO Data Unloading at locations 0x100, 0x300, 0x500, 0x700, 0x900, 0xB00, 0xD00, and 0xF00

The RX FIFO data (up to the maximum 64 bytes) can be read out in a single burst 32-bit read operation (maximum 16 DWORD reads) at memory locations 0x100 (channel 0), 0x300 (channel 1), 0x500 (channel 2),....., 0xF00 (channel 7). This operation is at least 16 times faster than reading the data in 64 separate 8-bit memory reads of RHR register (0x000 for channel 0, 0x200 for channel 1, 0x400 for channel 2,....., 0xE00 for channel 7).

READ RX FIFO, WITH NO ERRORS	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Read n+0 to n+3	FIFO Data n+3	FIFO Data n+2	FIFO Data n+1	FIFO Data n+0
Read n+4 to n+7	FIFO Data n+7	FIFO Data n+6	FIFO Data n+5	FIFO Data n+4
Etc.				

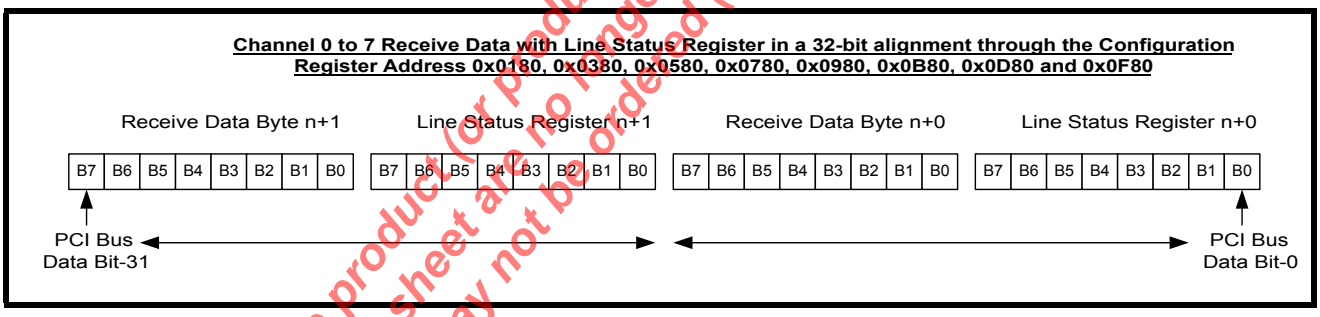
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)



3.1.2 Special Rx FIFO Data Unloading at locations 0x180, 0x380, 0x580, 0x780, 0x980, 0xB80, 0xD80, 0xF80

The XR17C158 also provides the same RX FIFO data along with the LSR status information of each byte side-by-side, at locations 0x180 (channel 0), 0x380 (channel 1), 0x580 (channel 2), ..., 0xF80 (channel 7). The entire RX data along with the status can be downloaded in a single PCI Burst Read operation of 32 DWORD reads. The Status and Data bytes must be read in 16 or 32 bits format to maintain data integrity. The following tables show this clearly.

READ RX FIFO, WITH LSR ERRORS	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Read n+0 to n+1	FIFO Data n+1	LSR n+1	FIFO Data n+0	LSR n+0
Read n+2 to n+3	FIFO Data n+3	LSR n+3	FIFO Data n+2	LSR n+2
Etc				

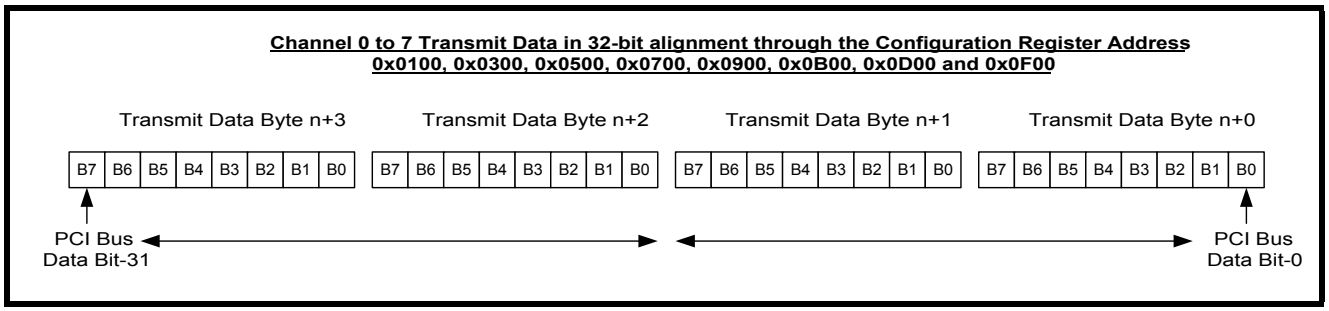


The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

3.1.3 Tx FIFO Data Loading at locations 0x100, 0x300, 0x500, 0x700, 0x900, 0xB00, 0xD00, 0xF00

The TX FIFO data (up to the maximum 64 bytes) can be loaded in a single burst 32-bit write operation (maximum 16 DWORD writes) at memory locations 0x100 (channel 0), 0x300 (channel 1), 0x500 (channel 2), ..., 0xD00 (channel 6) and 0xF00 (channel 7).

WRITE TX FIFO	BYTE 3	BYTE 2	BYTE 1	BYTE 0
Write n+0 to n+3	FIFO Data n+3	FIFO Data n+2	FIFO Data n+1	FIFO Data n+0
Write n+4 to n+7	FIFO Data n+7	FIFO Data n+6	FIFO Data n+5	FIFO Data n+4
Etc.				



3.2 FIFO DATA LOADING AND UNLOADING THROUGH THE UART CHANNEL REGISTERS, THR AND RHR IN 8-BIT FORMAT

The THR and RHR register address for channel 0 to channel 7 is shown in Table 8 below. The THR and RHR for each channel 0 to 7 are located sequentially at address 0x0000, 0x0200, 0x0400, 0x0600, 0x0800, 0x0A000, 0x0C00 and 0x0E00. Transmit data byte is loaded to the THR when writing to that address and receive data is unloaded from the RHR register when reading that address. Both THR and RHR registers are 16C550 compatible in 8-bit format, so each bus operation can only write or read in bytes.

TABLE 8: TRANSMIT AND RECEIVE DATA REGISTER IN BYTE FORMAT, 16C550 COMPATIBLE

THR and RHR Address Locations For CH0 to CH7 (16C550 Compatible)

CH0	0x000	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH0	0x000	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x200	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH1	0x200	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH2	0x400	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH2	0x400	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH3	0x600	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH3	0x600	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH4	0x800	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH4	0x800	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH5	0xA00	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH5	0xA00	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH6	0xC00	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH6	0xC00	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH7	0xE00	Write THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
CH7	0xE00	Read RHR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

THRRHR1

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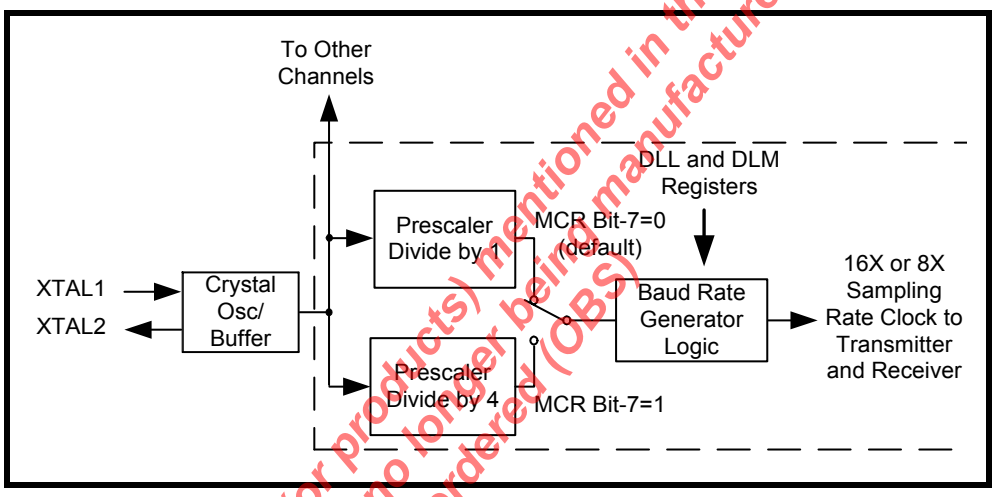
4.0 UART

There are 8 UARTs [channel 7:0] in the 158. Each has its own 64-byte of transmit and receive FIFOs, a set of 16550 compatible control and status registers, and a baud rate generator for individual channel data rate setting. Eight additional registers per UART were added for the EXAR enhanced features.

4.1 Programmable Baud Rate Generator

Each UART has its own Baud Rate Generator (BRG) with a prescaler for the transmitter and receiver. The prescaler is controlled by a software bit in the MCR register. The MCR register bit-7 sets the prescaler to divide the input crystal or external clock by 1 or 4. The output of the prescaler clocks to the BRG. The BRG further divides this clock by a programmable divisor between 1 and (2^{16} -1) to obtain a 16X or 8X sampling clock of the serial data rate. The sampling clock is used by the transmitter for data bit shifting and receiver for data sampling. The BRG divisor (DLL and DLM registers) defaults to a random value upon power up. Therefore, the BRG must be programmed during initialization to the operating data rate.

FIGURE 9. BAUD RATE GENERATOR



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Programming the Baud Rate Generator Registers DLM and DLL provides the capability for selecting the operating data rate. Table 9 shows the standard data rates available with a 14.7456 MHz crystal or external clock at 16X clock rate. At 8X sampling rate, these data rates would double. When using a non-standard data rate crystal or external clock, the divisor value can be calculated with the following equation(s).

divisor (decimal) = (XTAL1 clock frequency / prescaler) / (serial data rate x 16), **WITH 8XMODE [7:0] IS 0**

divisor (decimal) = (XTAL1 clock frequency / prescaler / (serial data rate x 8), **WITH 8XMODE [7:0] IS 1**

TABLE 9: TYPICAL DATA RATES WITH A 14.7456 MHZ CRYSTAL OR EXTERNAL CLOCK AT 16X SAMPLING

OUTPUT Data Rate MCR Bit-7=1	OUTPUT Data Rate MCR Bit-7=0	DIVISOR FOR 16x Clock (Decimal)	DIVISOR FOR 16x Clock (HEX)	DLM PROGRAM VALUE (HEX)	DLL PROGRAM VALUE (HEX)	DATA RATE ERROR (%)
100	400	2304	900	09	00	0
600	2400	384	180	01	80	0
1200	4800	192	C0	00	C0	0
2400	9600	96	60	00	60	0
4800	19.2k	48	30	00	30	0
9600	38.4k	24	18	00	18	0
19.2k	76.8k	12	0C	00	0C	0
38.4k	153.6k	6	06	00	06	0
57.6k	230.4k	4	04	00	04	0
115.2k	460.8k	2	02	00	02	0
230.4k	921.6k	1	01	00	01	0

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4.2 Transmitter

The transmitter section comprises of a 64 bytes of FIFO, a byte-wide Transmit Holding Register (THR) and an 8-bit Transmit Shift Register (TSR). THR receives a data byte from the host (non-FIFO mode) or a data byte from the FIFO when the FIFO is enabled by FCR bit-0. TSR shifts out every data bit with the 16X or 8X internal clock. A bit time is 16 or 8 clock periods. The transmitter sends the start bit followed by the number of data bits, inserts the proper parity bit if enabled, and adds the stop bit(s). The status of the THR and TSR are reported in the Line Status Register (LSR bit-5 and bit-6).

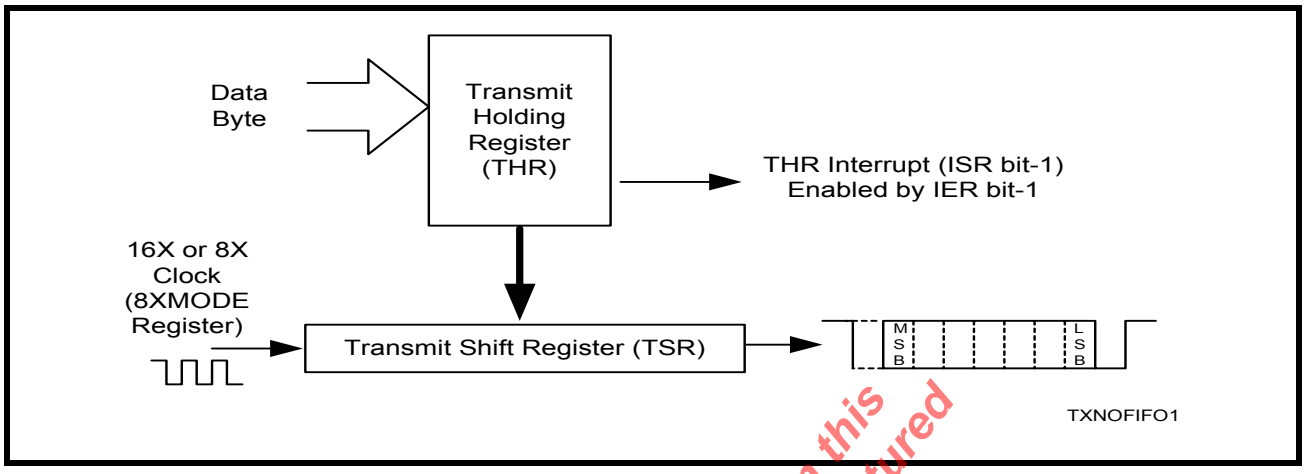
4.2.1 Transmit Holding Register (THR) - Write-Only

The transmit holding register is an 8-bit register providing a data interface to the host processor. The host writes transmit data byte to the THR to be converted into a serial data stream including start-bit, data bits, parity-bit and stop-bit(s). The least-significant-bit (bit-0) becomes the first data bit to go out. The THR is also the input register to the transmit FIFO of 64 bytes when FIFO operation is enabled by FCR bit-0. A THR empty interrupt can be generated when it is enabled in IER bit-1.

4.2.2 Transmitter Operation in non-FIFO mode

The host loads transmit data to THR one character at a time. The THR empty flag (LSR bit-5) is set when the data byte is transferred to TSR. THR flag can generate a transmit empty interrupt (ISR bit-1) when it is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty.

FIGURE 10. TRANSMITTER OPERATION IN NON-FIFO MODE



4.2.3 Transmitter Operation in FIFO mode

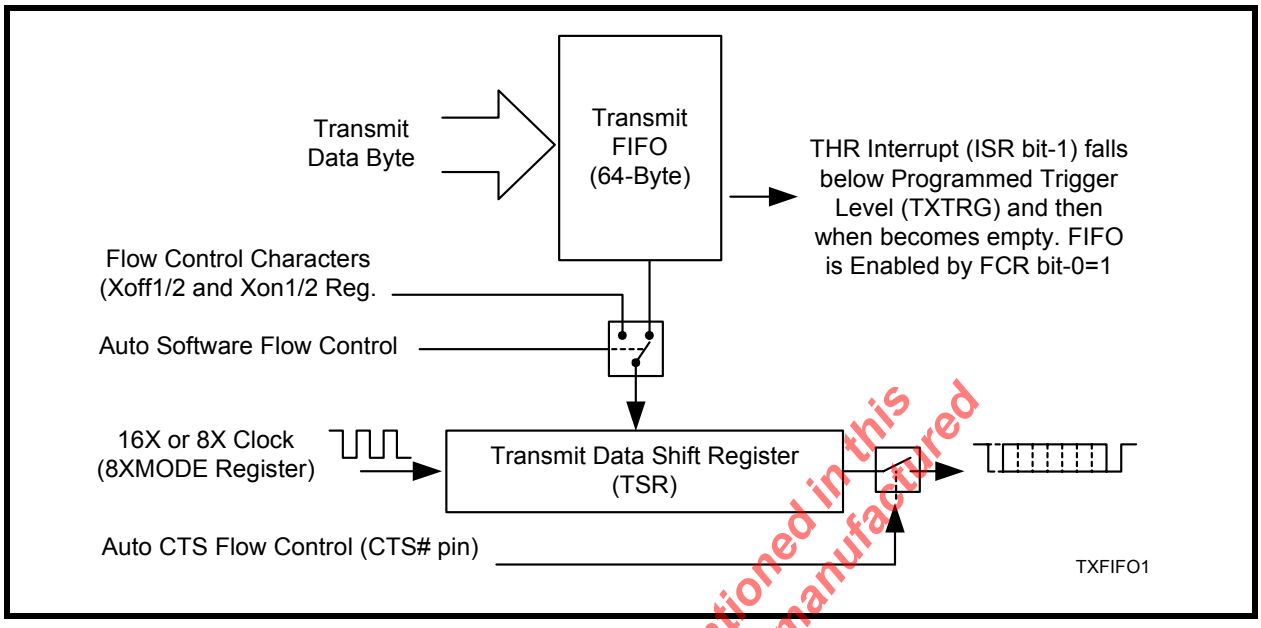
The host may fill the transmit FIFO with up to 64 bytes of transmit data. The THR empty flag (LSR bit-5) is set whenever the FIFO is empty. The transmit empty interrupt (ISR bit-1) is generated when the amount of data in the FIFO falls below its programmed trigger level (see TXTRG register) and when it empties. The transmit empty interrupt is enabled by IER bit-1. The TSR flag (LSR bit-6) is set when TSR becomes completely empty. Furthermore, with the RS485 half-duplex direction control enabled (FCTR bit-5=1) the source of the transmit empty interrupt changes to TSR empty instead of THR empty. This is to ensure the RTS# output is not changed until the last stop bit of the last character is shifted out.

4.2.4 Auto RS485 Operation

The auto RS485 half-duplex direction control changes the behavior of the transmitter when enabled by FCTR bit-5. While transmitting, the RTS# or DTR# signal is HIGH. The RTS# or DTR# signal changes from HIGH to LOW after a specified delay indicated in MSR[7:4] following the last stop bit of the last character that has been transmitted. This helps in turning around the transceiver to receive the remote station's response. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver. This delay prevents undesirable line signal disturbance that causes signal degradation. It also changes the transmitter empty interrupt to TSR empty instead of THR empty.

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FIGURE 11. TRANSMITTER OPERATION IN FIFO AND FLOW CONTROL MODE



4.3 Receiver

The receiver section contains an 8-bit Receive Shift Register (RSR) and Receive Holding Register (RHR). The RSR uses the 16X or 8X clock for timing. It verifies and validates every bit on the incoming character in the middle of each data bit. On the falling edge of a start or false start bit, an internal receiver counter starts counting at the 16X or 8X clock rate. After 8 or 4 clocks the start bit period should be at the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. The rest of the data bits and stop bits are sampled and validated in this same manner to prevent false framing. If there were any error(s), they are reported in the LSR register bits 1-4. Upon unloading the receive data byte from RHR, the receive FIFO pointer is bumped and the error flags are immediately updated to reflect the status of the data byte in RHR register. RHR can generate a receive data ready interrupt upon receiving a character or delay until it reaches the FIFO trigger level. Furthermore, data delivery to the host is guaranteed by a receive data ready time-out function when receive data does not reach the receive FIFO trigger level. This time-out delay is 4 word lengths as defined by LCR[1:0] plus 12 bits time. The RHR interrupt is enabled by IER bit-0.

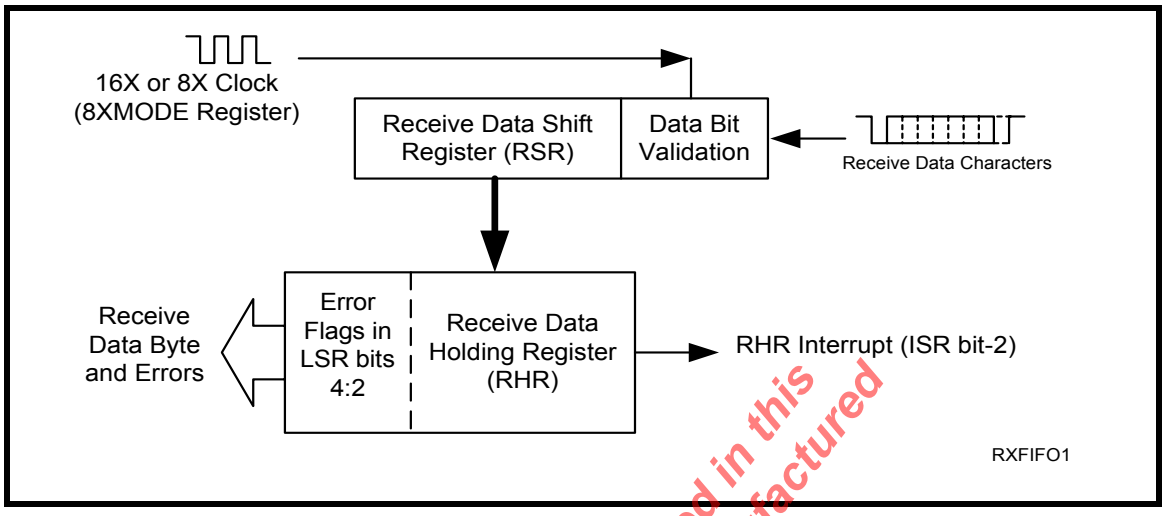
The product (or products) mentioned in this datasheet are no longer being manufactured and may not be ordered (OBS)

4.3.1 Receive Holding Register (RHR) - Read-Only

The receive holding register is an 8-bit register that holds a receive data byte from the receive shift register (RSR). It provides the receive data interface to the host processor. The host reads the receive data byte on this register whenever a data byte is transferred from the RSR. RHR also part of the receive FIFO of 64 bytes by 11-bit wide, 3 extra bits are for the error flags to be in LSR register. When the FIFO is enabled by FCR bit-0, it acts as the first-out register of the FIFO as new data are put over the first-in register. The receive FIFO pointer is bumped after the RHR register is read. Also, the error flags associated with the data byte are immediately updated onto the line status register (LSR) bits 1-4.

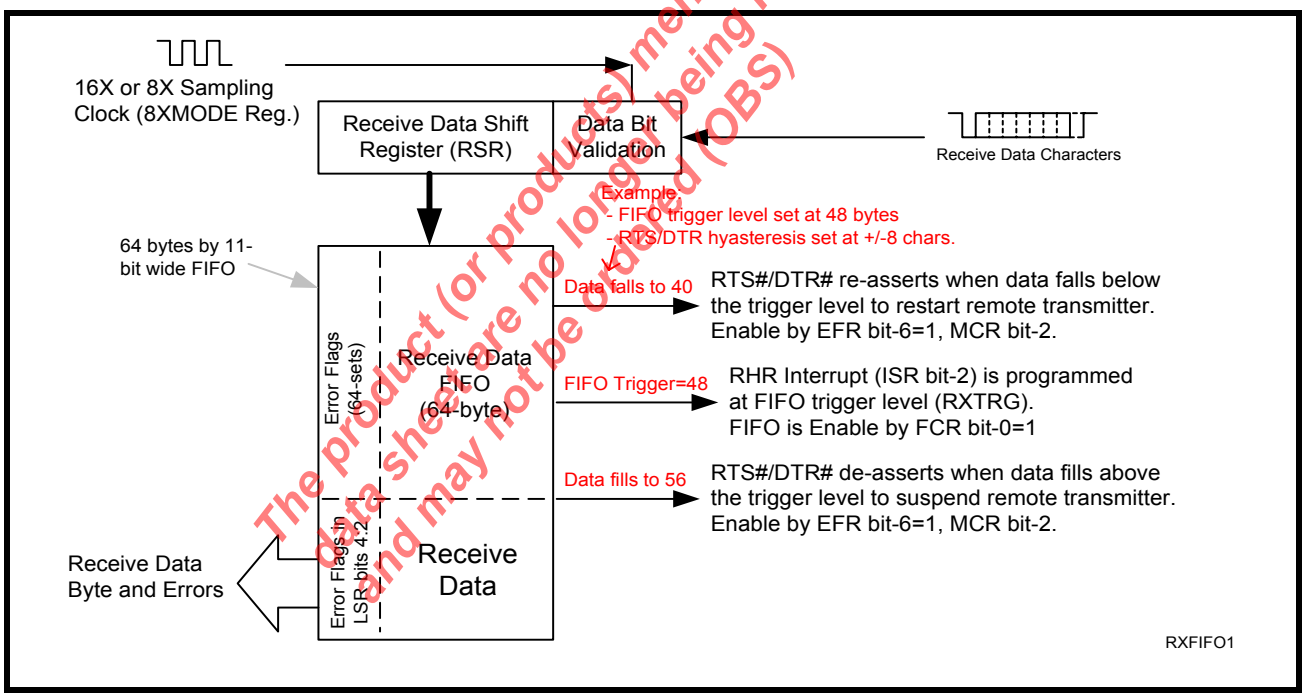
4.3.2 Receiver Operation in non-FIFO Mode

FIGURE 12. RECEIVER OPERATION IN NON-FIFO MODE



4.3.3 Receiver Operation in FIFO and Flow Control Mode

FIGURE 13. RECEIVER OPERATION IN FIFO AND FLOW CONTROL MODE



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4.4 Automatic Hardware (RTS/CTS or DTR/DSR) Flow Control Operation

Automatic hardware RTS/CTS or DTR/DSR flow control is used to prevent data overrun to the local receiver FIFO and remote receiver FIFO. The RTS#/DTR# output pin is used to request the remote unit to suspend/ restart data transmission while the CTS#/DSR# input pin is monitored to suspend/restart the local transmitter. The auto RTS/CTS or DTR/DSR flow control features are individually selected to fit specific application requirement and enabled through EFR bit-6 and 7 and MCR bit-2 for either RTS/CTS or DTR/DSR control signals.

TABLE 10: AUTO RTS/CTS OR DTR/DSR FLOW CONTROL SELECTION

MCR BIT-2	EFR BIT-7	EFR BIT-6	FLOW CONTROL SELECTION
0	1	X	Auto CTS Flow Control Enabled
0	X	1	Auto RTS Flow Control Enabled
1	1	X	Auto DSR Flow Control Enabled
1	X	1	Auto DTR Flow Control Enabled
X	0	0	No Flow Control

Auto RTS flow control must be started by asserting the RTS# output pin LOW (MCR bit-1 = 1). Similarly, Auto DTR flow control must be started by asserting the DTR# output pin LOW (MCR bit-0 = 1). Figure 14 shows in detail how automatic hardware flow control works.

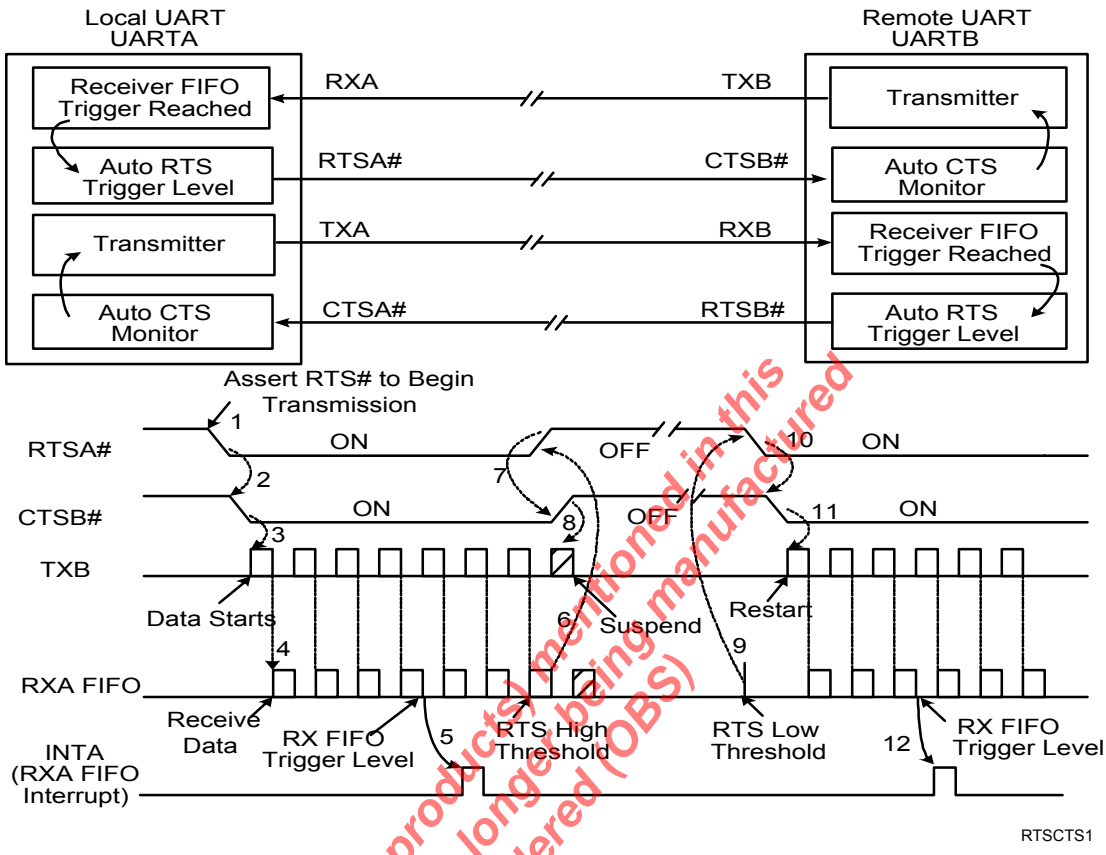
Two interrupts associated with auto RTS/CTS and DTR/DSR flow control have been added to give indication when RTS#/DTR# pin or CTS#/DSR# pin are de-asserted during operation. These interrupts are enabled by:

- Setting EFR bit-4 =1 to enable the shaded register bits
- Setting IER bit-7 will enable the CTS#/DSR# interrupt when these pins are de-asserted. The selection of CTS# or DSR# is selected via MCR bit-2. See Table 10 above for complete details.
- Setting IER bit-6 will enable the RTS#/DTR# interrupt when these pins are de-asserted. The selection of RTS# or DTR# is selected via MCR bit-2. See Table 10 above for complete details.

Automatic hardware flow control is selected by setting bits 6 (RTS) and 7 (CTS) of the EFR register to logic 1. If CTS# pin transitions from LOW to HIGH indicating a flow control request, ISR bit-5 will be set to logic 1, (if enabled via IER bit 6-7), and the UART will suspend TX transmissions as soon as the stop bit of the character in process is shifted out. Transmission is resumed after the CTS# input returns LOW, indicating more data may be sent.

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FIGURE 14. AUTO RTS/DTR AND CTS/DSR FLOW CONTROL OPERATION



The local UART (UARTA) starts data transfer by asserting -RTSA# (1). RTSA# is normally connected to CTSB# (2) of remote UART (UARTB). CTSB# allows its transmitter to send data (3). TXB data arrives and fills UARTA receive FIFO (4). When RXA data fills up to its receive FIFO trigger level, UARTA activates its RXA data ready interrupt (5) and continues to receive and put data into its FIFO. If interrupt service latency is long and data is not being unloaded, UARTA monitors its receive data fill level to match the upper threshold of RTS delay and de-assert RTSA# (6). CTSB# follows (7) and request UARTB transmitter to suspend data transfer. UARTB stops or finishes sending the data bits in its transmit shift register (8). When receive FIFO data in UARTA is unloaded to match the lower threshold of RTS delay (9), UARTA re-asserts RTSA# (10), CTSB# recognizes the change (11) and restarts its transmitter and data flow again until next receive FIFO trigger (12). This same event applies to the reverse direction when UARTA sends data to UARTB with RTSB# and CTSA# controlling the data flow.

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4.5 Infrared Mode

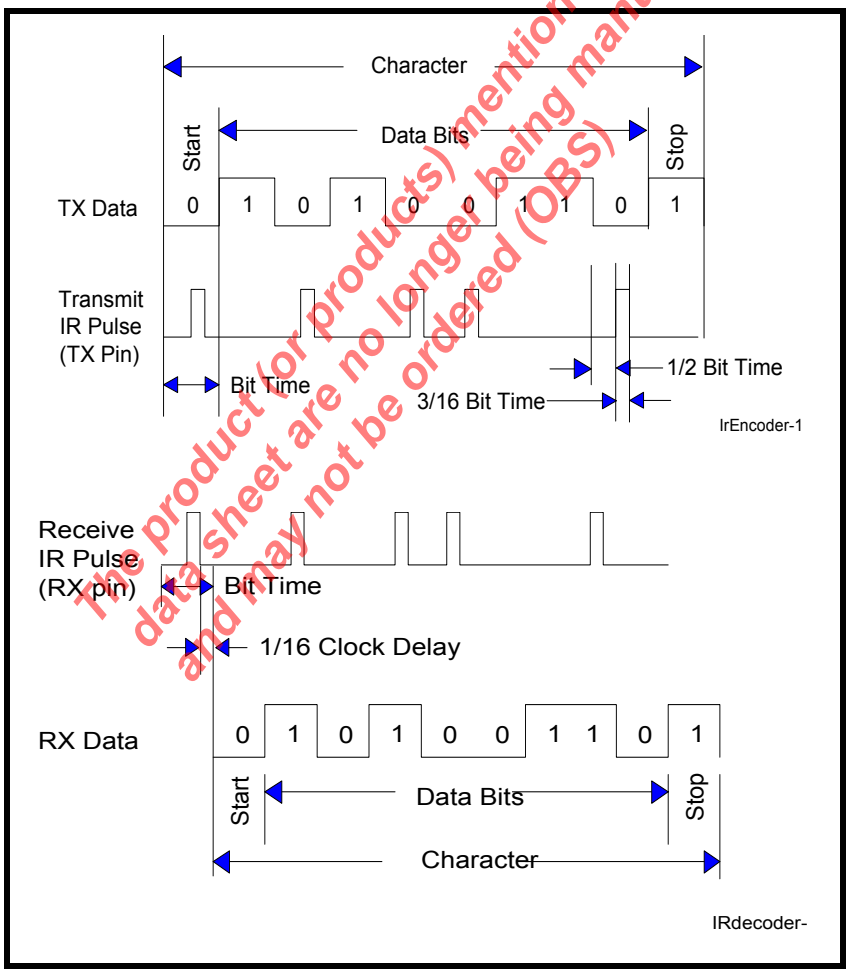
Each UART in the 158 includes the infrared encoder and decoder compatible to the IrDA (Infrared Data Association) version 1.0. The input pin ENIR conveniently activates all 8 UART channels to start up in the infrared mode. The ENIR pin is sampled when the RST# input is de-asserted. This global control pin enables the MCR bit-6 function in every UART channel register. After power up or a reset, the software can overwrite MCR bit-6 if so desired. ENIR and MCR bit-6 also disable its receiver while the transmitter is sending data. This prevents the echoed data from going to the receiver. The global activation ENIR pin prevents the infrared emitter from turning on and drawing large amount of current while the system is starting up. When the infrared feature is enabled, the transmit data outputs, TX[7:0], will idle LOW. Likewise, the RX [7:0] inputs assume an idling condition when it is LOW.

The infrared encoder sends out a 3/16 of a bit wide pulse for each “0” bit in the transmit data stream. This signal encoding reduces the on-time of the infrared LED, hence reduces the power consumption. See Figure 15 below.

The infrared decoder receives the input pulse from the infrared sensing diode on RX pin. Each time the decoder senses a light pulse, it returns a logic 0 to the data bit stream. The RX input signal may be inverted prior delivered to the input of the decoder via internal register setting. This option supports active low instead of normal active high pulse from some infrared modules on the market.

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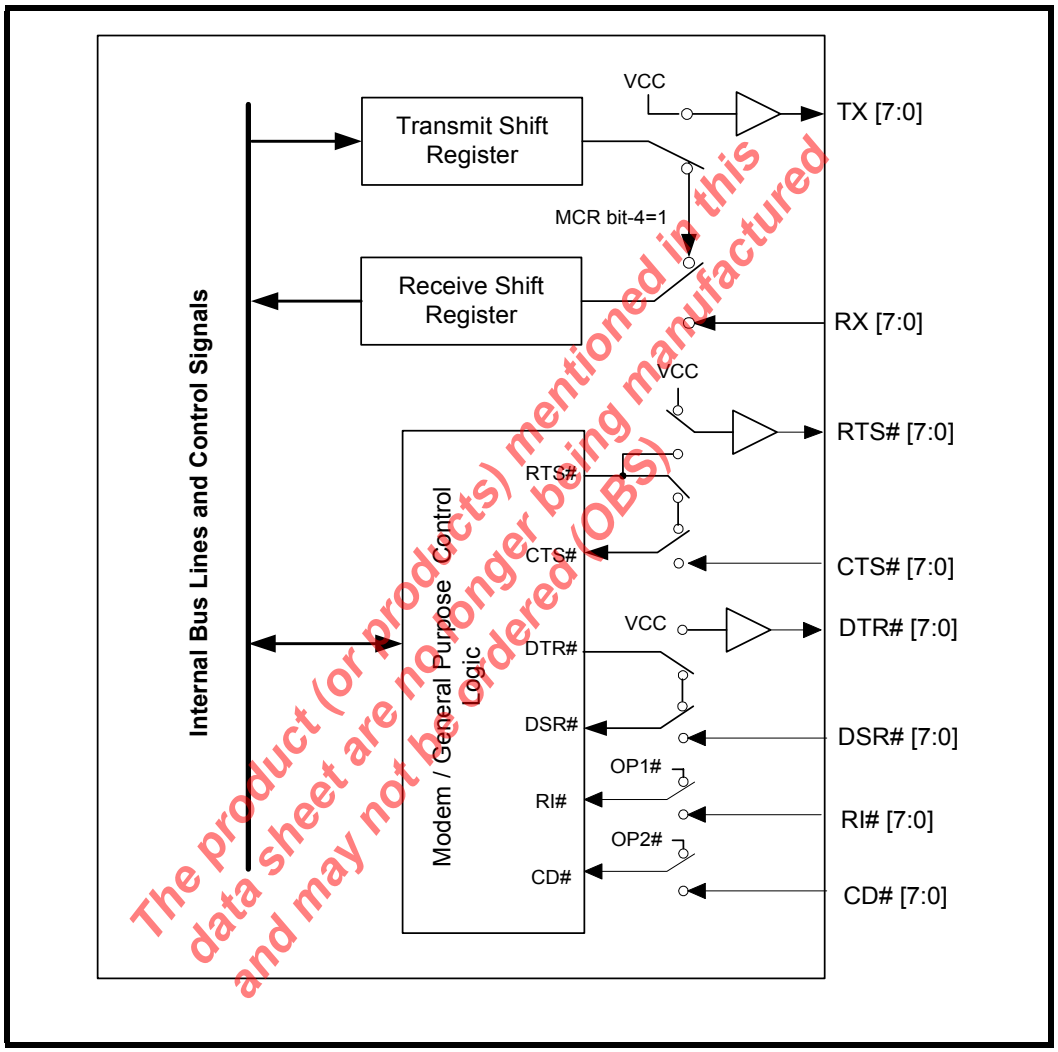
FIGURE 15. INFRARED TRANSMIT DATA ENCODING AND RECEIVE DATA DECODING



4.6 Internal Loopback

Each UART channel provides an internal loopback capability for system diagnostic. The internal loopback mode is enabled by setting MCR register bit-4 to logic 1. All regular UART functions operate normally. Figure 16 shows how the modem port signals are re-configured. Transmit data from the transmit shift register output is internally routed to the receive shift register input allowing the system to receive the same data that it was sending. The TX, RTS# and DTR# pins are held HIGH (idle or de-asserted state), and the CTS#, DSR# CD# and RI# inputs are ignored.

FIGURE 16. INTERNAL LOOP BACK



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4.7 UART CHANNEL CONFIGURATION REGISTERS AND ADDRESS DECODING

The 8 sets of UART configuration registers are decoded using address lines A8 to A11 as shown below. Address lines A0 to A3 select the 16 registers in each channel. The first 8 registers are 16550 compatible with EXAR enhanced feature registers located on the upper 8 addresses.

A11	A10	A9	A8	UART CHANNEL SELECTION
0	0	0	0	0
0	0	1	0	1
0	1	0	0	2
0	1	1	0	3
1	0	0	0	4
1	0	1	0	5
1	1	0	0	6
1	1	1	0	7

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.

TABLE 11: UART CHANNEL CONFIGURATION REGISTERS

ADDRESS				REGISTER	READ/WRITE	COMMENTS
A3	A2	A1	A0			
16550 COMPATIBLE REGISTERS						
0	0	0	0	RHR - Receive Holding Register	Read-only	LCR[7] = 0
0	0	0	0	THR - Transmit Holding Register	Write-only	LCR[7] = 0
0	0	0	0	DLL - Div Latch Low	Read/Write	LCR[7] = 1
0	0	0	1	DLM - Div Latch High	Read/Write	LCR[7] = 1
0	0	0	1	IER - Interrupt Enable Register	Read/Write	LCR[7] = 0
0	0	1	0	ISR - Interrupt Status Register	Read-only	
0	0	1	0	FCR - FIFO Control Register	Write-only	
0	0	1	1	LCR - Line Control Register	Read/Write	
0	1	0	0	MCR - Modem Control Register	Read/Write	
0	1	0	1	LSR - Line Status Register	Read-only	
0	1	1	0	MSR - Modem Status Register	Read-only	
0	1	1	0	RS485 Turn-Around Delay Register	Write-only	
0	1	1	1	SPR - Scratch Pad Register	Read/Write	
ENHANCED REGISTERS						
1	0	0	0	FCTR - Feature Control Register	Read/Write	
1	0	0	1	EFR - Enhanced Function Register	Read/Write	
1	0	1	0	TXCNT - Transmit FIFO Level Counter	Read-only	
1	0	1	0	TXTRG - Transmit FIFO Trigger Level	Write-only	
1	0	1	1	RXCNT - Receive FIFO Level Counter	Read-only	
1	0	1	1	RXTRG - Receive FIFO Trigger Level	Write-only	
1	1	0	0	Xoff-1 - Xoff Character 1	Write-only	
1	1	0	0	Xchar	Read-only	Xon,Xoff Rcvd. Flags
1	1	0	1	Xoff-2 - Xoff Character 2	Write-only	
1	1	1	0	Xon-1 - Xon Character 1	Write-only	
1	1	1	1	Xon-2 - Xon Character 2	Write-only	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED BY EFR BIT-4.

ADDRESS A3-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
0 0 0 0	RHR	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0 0	THR	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=0
0 0 0 0	DLL	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 0 1	DLM	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	LCR[7]=1
0 0 0 1	IER	R/W	0/ CTS/ DSR# Int. Enable	0/ RTS/ DTR# Int. Enable	0/ Xon/Xoff/ Sp. Char. Int. Enable	0	Modem Status Int. Enable	RX Line Status Int. Enable	TX Empty Int. Enable	RX Data Int. Enable	
0 0 1 0	ISR	R	FIFOs Enable	FIFOs Enable	0/ Delta-Flow Cntl	0/ Xoff/special char	INT Source Bit-3	INT Source Bit-2	INT Source Bit-1	INT Source Bit-0	
0 0 1 0	FCR	W	RX FIFO Trigger	RX FIFO Trigger	0/ TX FIFO Trigger	0/ TX FIFO Trigger	DMA Mode	TX FIFO Reset	RX FIFO Reset	FIFOs Enable	
0 0 1 1	LCR	R/W	Divisor Enable	Set TX Break	Set Parity	Even Parity	Parity Enable	Stop Bits	Word Length Bit-1	Word Length Bit-0	
0 1 0 0	MCR	R/W	0/ BRG Prescaler	0/ IR Enable	0/ XonAny	Internal Lopback Enable	(OP2)[1]	(OP1)[1] RTS/DTR Flow Sel	RTS# Pin Control	DTR# Pin Control	
0 1 0 1	LSR	R/W	RX FIFO ERROR	TSR Empty	THR Empty	RX Break	RX Fram-ing Error	RX Parity Error	RX Over-run	RX Data Ready	
0 1 1 0	MSR	R	CD	RI	DSR	CTS	Delta CD#	Delta RI#	Delta DSR#	Delta CTS#	
	MSR	W	RS485 DLY-3	RS485 DLY-2	RS485 DLY-1	RS485 DLY-0	Reserved	Reserved	Reserved	Reserved	
0 1 1 1	SPR	R/W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	User Data
1 0 0 0	FCTR	R/W	TRG Table Bit-1	TRG Table Bit-0	Auto RS485 Enable	Invert IR RX Input	RTS/DTR Hyst Bit-3	RTS/DTR Hyst Bit-2	RTS/DTR Hyst Bit-1	RTS/DTR Hyst Bit-0	
1 0 0 1	EFR	R/W	Auto CTS/DSR Enable	Auto RTS/DTR Enable	Special Char Select	Enable IER [7:5], ISR [5:4], FCR[5:4], MCR[7:5,2] MSR[7:4]	Software Flow Cntl Bit-3	Software Flow Cntl Bit-2	Software Flow Cntl Bit-1	Software Flow Cntl Bit-0	
1 0 1 0	TXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1 0	TXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1 1	RXCNT	R	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 0 1 1	RXTRG	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

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TABLE 12: UART CHANNEL CONFIGURATION REGISTERS DESCRIPTION. SHADED BITS ARE ENABLED BY EFR BIT-4.

ADDRESS A3-A0	REG NAME	READ/ WRITE	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	COMMENT
1 1 0 0	XCHAR	R	0	0	0	0	0	0	Xon Det. Indicator	Xoff Det. Indicator	Self-clear after read
1 1 0 0	XOFF1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 0 1	XOFF2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1 0	XON1	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	
1 1 1 1	XON2	W	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0	

NOTE: MCR bits 2 and 3 (OP1 and OP2 outputs) are not available in the XR17C158. They are present for 16C550 compatibility during Internal loopback, see Figure 16.

4.8 Registers

4.8.1 Receive Holding Register (RHR) - Read-Only

See "Section 4.3, Receiver" on page 30 for complete details.

4.8.2 Transmit Holding Register (THR) - Write-Only

See "Section 4.2, Transmitter" on page 28 for complete details.

4.8.3 Baud Rate Generator Divisors (DLL and DLM) - Read/Write

The Baud Rate Generator (BRG) is a 16-bit counter that generates the data rate for the transmitter and receiver. The baud rate is programmed through registers DLL and DLM which are only accessible when LCR bit-7 is set to logic 1. See "Section 4.1, Programmable Baud Rate Generator" on page 27 for more detail.

4.8.4 Interrupt Enable Register (IER) - Read/Write

The Interrupt Enable Register (IER) masks the interrupts from receive data ready, transmit empty, line status and modem status registers. These interrupts are reported in the Interrupt Status Register (ISR) register and also encoded in INT (INT0-INT3) register in the Device Configuration Registers.

IER VERSUS RECEIVE FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR bit-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the RHR interrupts (see ISR bits 3 and 4) status will reflect the following:

A. The receive data available interrupts are issued to the host when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B. FIFO level will be reflected in the ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C. The receive data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

IER VERSUS RECEIVE/TRANSMIT FIFO POLLED MODE OPERATION

When FCR BIT-0 equals a logic 1 for FIFO enable, resetting IER bits 0-3 enables the 158 in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A. LSR BIT-0 indicates there is data in RHR or RX FIFO.

B. LSR BIT-1 indicates an overrun error has occurred and that data in the FIFO may not be valid.

C. LSR BITS 2-4 provides the type of receive data errors encountered for the data byte in RHR, if any.

D. LSR BIT-5 indicates THR is empty.

E. LSR BIT-6 indicates when both the transmit FIFO and TSR are empty.

F. LSR BIT-7 indicates a data error in at least one character in the RX FIFO.

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IER[0]: RHR Interrupt Enable

The receive data ready interrupt will be issued when RHR has a data character in the non-FIFO mode or when the receive FIFO has reached the programmed trigger level in the FIFO mode. A receive data timeout interrupt will be issued in the FIFO mode when the receive FIFO has not reached the programmed trigger level and the RX input has been idle for 4 character + 12 bit times.

- Logic 0 = Disable the receive data ready interrupt (default).
- Logic 1 = Enable the receiver data ready interrupt.

IER[1]: THR Interrupt Enable

When Auto RS485 mode operation is disabled (FCTR bit-5 = 0), this interrupt is associated with bit-5 in the LSR register. An interrupt is issued whenever the THR becomes empty or when data in the FIFO falls below the programmed trigger level. When Auto RS485 mode operation is enabled (FCTR bit-5 = 1), this interrupt is associated with bit-6 in the LSR register. An interrupt is issued whenever the TX FIFO and the TSR becomes empty.

- Logic 0 = Disable Transmit Holding Register empty interrupt (default).
- Logic 1 = Enable Transmit Holding Register empty interrupt.

IER[2]: Receive Line Status Interrupt Enable

Any of LSR register bits 1, 2, 3 or 4 will generate an LSR interrupt immediately when a character received by the RX FIFO has an error.

- Logic 0 = Disable the receiver line status interrupt (default).
- Logic 1 = Enable the receiver line status interrupt.

IER[3]: Modem Status Interrupt Enable

- Logic 0 = Disable the modem status register interrupt (default).
- Logic 1 = Enable the modem status register interrupt.

IER[4]: Reserved

IER[5]: Xoff Interrupt Enable (requires EFR bit-4=1)

- Logic 0 = Disable the software flow control, receive Xoff interrupt (default).
- Logic 1 = Enable the software flow control, receive Xoff interrupt. See Software Flow Control section for details.

IER[6]: RTS#/DTR# Output Interrupt Enable (requires EFR bit-4=1)

The RTS# or DTR# output is selected via MCR bit-2. See Table 10 or MCR[2] for complete details.

- Logic 0 = Disable the RTS#/DTR# interrupt (default).
- Logic 1 = Enable the RTS#/DTR# interrupt. The UART issues an interrupt when the RTS#/DTR# pin makes a transition.

IER[7]: CTS# Input Interrupt Enable (requires EFR bit-4=1)

The CTS# or DSR# input is selected via MCR bit-2. See Table 10 or MCR[2] for complete details.

- Logic 0 = Disable the CTS#/DSR# interrupt (default).
- Logic 1 = Enable the CTS#/DSR# interrupt. The UART issues an interrupt when CTS# pin makes a transition.

4.8.5 Interrupt Status Register (ISR) - Read-Only

The UART provides multiple levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with six interrupt status bits. Performing a read cycle on the ISR will give the user the current highest pending interrupt level to be serviced with others queued up for next service. No other interrupts are acknowledged until the pending interrupt is serviced. The Interrupt Source Table, Table 13, shows the data values (bit 0-5) for the six prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Interrupt Generation:

- LSR is by any of the LSR bits 1, 2, 3 and 4.
- RXRDY is by RX trigger level.
- RXRDY Time-out is by the a 4-char plus 12 bits delay timer if the RX FIFO level is less than the RX trigger level.
- TXRDY is by LSR bit-5 (or bit-6 in auto RS485 control).
- MSR is by any of the MSR bits, 0, 1, 2 and 3.
- Receive Xon/Xoff/Special character is by detection of a Xon, Xoff or Special character.
- CTS#/DSR# is by a change of state on the input pin (from LOW to HIGH) with auto flow control enabled, EFR bit-7, and depending on selection of MCR bit-2.
- RTS#/DTR# is when its receiver changes the state of the output pin (from LOW to HIGH) during auto RTS/DTR flow control enabled by EFR bit-6 and selection of MCR bit-2.
- Wake-up Indicator: when the UART comes out of sleep mode.

Interrupt Clearing:

- LSR interrupt is cleared by a read to the LSR register.
- RXRDY is cleared by reading data until FIFO falls below the trigger level.
- RXRDY Time-out is cleared by reading data until the RX FIFO is empty.
- TXRDY interrupt is cleared by a read to the ISR register.
- MSR interrupt is cleared by a read to the MSR register.
- Xon or Xoff character interrupt is cleared by a read to ISR register.
- Special character interrupt is cleared by a read to ISR register or after the next character is received.
- RTS#/DTR# and CTS#/DSR# status change interrupts are cleared by a read to the MSR register.
- Wake-up Indicator is cleared by a read to the INT0 register.

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TABLE 13: INTERRUPT SOURCE AND PRIORITY LEVEL

PRIORITY LEVEL	ISR REGISTER STATUS BITS						SOURCE OF THE INTERRUPT
	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0	
1	0	0	0	1	1	0	LSR (Receiver Line Status Register)
2	0	0	0	1	0	0	RXRDY (Received Data Ready)
3	0	0	1	1	0	0	RXRDY (Receive Data Time-out)
4	0	0	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
5	0	0	0	0	0	0	MSR (Modem Status Register)
6	0	1	0	0	0	0	RXRDY (Received Xon/Xoff or Special character)
7	1	0	0	0	0	0	CTS#/DSR#, RTS#/DTR# change of state
X	0	0	0	0	0	1	None (default)

ISR[0]: Interrupt Status

- Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
- Logic 1 = No interrupt pending (default condition).

ISR[3:1]: Interrupt Status

These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, 3 and 4 (See Interrupt Source Table 13).

ISR[4]: Xoff/Xon or Special Character Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-4 indicates that the receiver detected a data match of the Xoff character(s). If this is an Xoff/Xon interrupt, it can be cleared by a read to the ISR. Reading the XCHAR register will indicate which character (Xoff or Xon) was received last. If it is a special character interrupt, it can be cleared by reading ISR or it will automatically clear after the next character is received.

ISR[5]: RTS#/CTS# Interrupt Status

This bit is enabled when EFR bit-4 is set to a logic 1. ISR bit-5 indicates that the CTS# or RTS# has changed state from LOW to HIGH.

ISR[7:6]: FIFO Enable Status

These bits are set to a logic 0 when the FIFOs are disabled. They are set to a logic 1 when the FIFOs are enabled.

4.8.6 FIFO Control Register (FCR) - Write-Only

This register is used to enable the FIFOs, clear the FIFOs, set the transmit/receive FIFO trigger levels, and select the DMA mode (legacy term that refers to "block transfer mode"). The DMA and FIFO modes are defined as follows:

FCR[0]: TX and RX FIFO Enable

- Logic 0 = Disable the transmit and receive FIFO (default).
- Logic 1 = Enable the transmit and receive FIFOs. This bit must be set to logic 1 when other FCR bits are written or they will not be programmed.

FCR[1]: RX FIFO Reset

This bit is only active when FCR bit-0 is active.

- Logic 0 = No receive FIFO reset (default).
- Logic 1 = Reset the receive FIFO pointers and FIFO level counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[2]: TX FIFO Reset

This bit is only active when FCR bit-0 is active.

- Logic 0 = No transmit FIFO reset (default).
- Logic 1 = Reset the transmit FIFO pointers and FIFO level counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after resetting the FIFO.

FCR[3]: DMA Mode Select

This bit has no effect since TXRDY and RXRDY pins are not available in this device. It is provided for legacy software. DMA is a legacy term used for block transfer mode. DMA does not stand for "Direct Memory Access."

- Logic 0 = Set DMA to mode 0 (default).
- Logic 1 = Set DMA to mode 1.

FCR[5:4]: Transmit FIFO Trigger Select

(logic 0 = default, TX trigger level = 1)

The FCTR bits 6-7 are associated with these 2 bits by selecting one of the four tables. The 4 user selectable trigger levels in 4 tables are supported for compatibility reasons. These 2 bits set the trigger level for the transmit FIFO interrupt. The UART will issue a transmit interrupt when the number of characters in the FIFO falls below the selected trigger level, or when it gets empty in case that the FIFO did not get filled over the trigger level on last re-load. Table 14 below shows the selections. EFR bit-4 must be set to '1' before these bits can be accessed. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered. (OBS)

FCR[7:6]: Receive FIFO Trigger Select

(logic 0 = default, RX trigger level =1)

The FCTR Bits 6-7 are associated with these 2 bits. These 2 bits are used to set the trigger level for the receiver FIFO interrupt. Table 14 shows the complete selections. Note that the receiver and the transmitter cannot use different trigger tables. Whichever selection is made last applies to both the RX and TX side.

TABLE 14: TRANSMIT AND RECEIVE FIFO TRIGGER LEVEL SELECTION

TRIGGER TABLE	FCTR BIT-7	FCTR BIT-6	FCR BIT-7	FCR BIT-6	FCR BIT-5	FCR BIT-4	RECEIVE TRIGGER LEVEL	TRANSMIT TRIGGER LEVEL	COMPATIBILITY
Table A	0	0	0 0 1 1	0 1 0 1	0	0	1 (default) 4 8 14	1 (default)	16C550, 16C2550, 16C2552, 16C554, 16C580 compatible.
Table B	0	1	0 0 1 1	0 1 0 1	0 0 1 1	0 1 0 1	8 16 24 28	16 8 24 30	16C650A compatible.
Table C	1	0	0 0 1 1	0 1 0 1	0 0 1 1	0 1 0 1	8 16 56 60	8 16 32 56	16C654 compatible.
Table D	1	1	X	X	X	X	Programmable	Programmable	16C850, 16C2850, 16C2852, 16C854, 16C864, 16L2750, 16L2751, 16L2752 compatible.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

4.8.7 Line Control Register (LCR) - Read/Write

The Line Control Register is used to specify the asynchronous data communication format. The word or character length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR[1:0]: TX and RX Word Length Select

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	WORD LENGTH
0	0	5 (default)
0	1	6
1	0	7
1	1	8

LCR[2]: TX and RX Stop-bit Length Select

The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	WORD LENGTH	STOP BIT LENGTH (BIT TIME(S))
0	5,6,7,8	1 (default)
1	5	1-1/2
1	6,7,8	2

LCR[3]: TX and RX Parity Select

Parity or no parity can be selected via this bit. The parity bit is a simple way used in communications for data integrity check. See Table 15 for parity selection summary below.

- Logic 0 = No parity.
- Logic 1 = A parity bit is generated during the transmission while the receiver checks for parity error of the data character received.

LCR[4]: TX and RX Parity Select

If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.

- Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted character. The receiver must be programmed to check the same format (default).
- Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted character. The receiver must be programmed to check the same format.

LCR[5]: TX and RX Parity Select

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

- LCR BIT-5 = logic 0, parity is not forced (default).
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
- LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS).

TABLE 15: PARITY SELECTION

LCR BIT-5	LCR BIT-4	LCR BIT-3	PARITY SELECTION
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity to mark, “1”
1	1	1	Forced parity to space, “0”

LCR[6]: Transmit Break Enable

When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a “space", LOW state). This condition remains until disabled by setting LCR bit-6 to a logic 0.

- Logic 0 = No TX break condition (default).
- Logic 1 = Forces the transmitter output (TX) to a “space”, LOW, for alerting the remote receiver of a line break condition.

LCR[7]: Baud Rate Divisors Enable

Baud rate generator divisor (DLL/DLM) enable.

- Logic 0 = Data registers are selected (default).
- Logic 1 = Divisor latch registers are selected.

4.8.8 Modem Control Register (MCR) - Read/Write

The MCR register is used for controlling the modem interface signals or general purpose inputs/outputs.

MCR[0]: DTR# Pins

The DTR# pin may be used for automatic hardware flow control enabled by EFR bit-6 and MCR bit-2=1. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force DTR# output HIGH (default).
- Logic 1 = Force DTR# output LOW.

MCR[1]: RTS# Pins

The RTS# pin may be used for automatic hardware flow control by enabled by EFR bit-6 and MCR bit-2=0. If the modem interface is not used, this output may be used for general purpose.

- Logic 0 = Force RTS# output HIGH (default).
- Logic 1 = Force RTS# output LOW.

MCR[2]: DTR# or RTS# for Auto Flow Control

DTR# or RTS# auto hardware flow control select. This bit is in effect only when auto RTS/DTR is enabled by EFR bit-6. DTR# selection is associated with DSR# and RTS# is with CTS#.

- Logic 0 = Uses RTS# and CTS# pins for auto hardware flow control.
- Logic 1 = Uses DTR# and DSR# pins for auto hardware flow control.

MCR[3]: (OP2)

The OP2 output is not available in the XR17C158. It is present for 16C550 compatibility during internal loopback. See **Figure 16**. Logic 0 is default.

MCR[4]: Internal Loopback Enable

- Logic 0 = Disable internal loopback mode (default).
- Logic 1 = Enable internal loopback mode, see loopback section and **Figure 16**.

The product (or product(s) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

MCR[5]: Xon-Any Enable

- Logic 0 = Disable Xon-Any function (for 16C550 compatibility) (default).
- Logic 1 = Enable Xon-Any function. In this mode any RX character received will enable Xon, resume data transmission.

MCR[6]: Infrared Encoder/Decoder Enable

The state of this bit depends on the sampled logic level of pin ENIR during power up, following a hardware reset or a soft-reset. Afterward user can override this bit for desired operation.

- Logic 0 = Disable the infrared mode, operates in the normal serial character mode.
- Logic 1 = Enable infrared IrDA receive and transmit inputs/outputs. While in this mode, the TX/RX output/input are routed to the infrared encoder/decoder. The data input and output levels will conform to the IrDA infrared interface requirement. As such, while in this mode the infrared TX output will be a logic 0 during idle data conditions. FCTR bit-4 may be selected to invert the RX input signal level going to the decoder for infrared modules that provide rather an inverted output.

MCR[7]: Clock Prescaler Select

- Logic 0 = Divide by one. The input clock from the crystal or external clock is fed directly to the Programmable Baud Rate Generator without further modification, i.e., divide by one (default).
- Logic 1 = Divide by four. The prescaler divides the input clock from the crystal or external clock by four and feeds it to the Programmable Baud Rate Generator, hence, data rates become one-fourth.

4.8.9 Line Status Register (LSR) - Read/Only

This register provides the status of data transfers between the UART and the host. If IER bit-2 is set to a logic 1, an LSR interrupt will be generated immediately when any character in the RX FIFO has an error (parity, framing, overrun, break). Reading LSR will clear LSR bits 4-1.

LSR[0]: Receive Data Ready Indicator

- Logic 0 = No data in receive holding register or FIFO (default).
- Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR[1]: Receiver Overrun Flag

- Logic 0 = No overrun error (default).
- Logic 1 = Overrun error. A data overrun error condition occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the receive shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error. This bit is cleared after LSR is read.

LSR[2]: Receive Data Parity Error Tag

- Logic 0 = No parity error (default).
- Logic 1 = Parity error. The receive character in RHR does not have correct parity information and is suspect. This error is associated with the character available for reading in RHR. This bit is cleared after LSR is read.

LSR[3]: Receive Data Framing Error Tag

- Logic 0 = No framing error (default).
- Logic 1 = Framing error. The receive character did not have a valid stop bit(s). This error is associated with the character available for reading in RHR. This bit is cleared after LSR is read.

LSR[4]: Receive Break Tag

- Logic 0 = No break condition (default).
- Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO. This bit is cleared after LSR is read.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

LSR[5]: Transmit Holding Register Empty Flag

This bit is the Transmit Holding Register Empty indicator. This bit indicates that the transmitter is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the host when the THR interrupt enable is set. The THR bit is set to a logic 1 when the last data byte is transferred from the transmit holding register to the transmit shift register. The bit is reset to logic 0 concurrently with the data loading to the transmit holding register by the host. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR[6]: Transmit Shift Register Empty Flag

This bit is the Transmit Shift Register Empty indicator. This bit is set to a logic 1 whenever the transmitter goes idle. It is set to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR[7]: Receive FIFO Data Error Flag

- Logic 0 = No FIFO error (default).
- Logic 1 = An indicator for the sum of all error bits in the RX FIFO. At least one parity error, framing error or break indication is in the FIFO data. This bit clears when there is no more error(s) in the FIFO.

4.8.10 Modem Status Register (MSR) - Read-Only

This register provides the current state of the modem interface signals, or other peripheral device that the UART is connected. Lower four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a signal from the modem changes state. These bits may be used as general purpose inputs/outputs when they are not used with modem signals.

MSR[0]: Delta CTS# Input Flag

- Logic 0 = No change on CTS# input (default).
- Logic 1 = The CTS# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[1]: Delta DSR# Input Flag

- Logic 0 = No change on DSR# input (default).
- Logic 1 = The DSR# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[2]: Delta RI# Input Flag

- Logic 0 = No change on RI# input (default).
- Logic 1 = The RI# input has changed from a logic 0 to a logic 1, ending of the ringing signal. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[3]: Delta CD# Input Flag

- Logic 0 = No change on CD# input (default).
- Logic 1 = Indicates that the CD# input has changed state since the last time it was monitored. A modem status interrupt will be generated if MSR interrupt is enabled (IER bit-3).

MSR[4]: CTS Input Status

CTS# pin may function as automatic hardware flow control signal input if it is enabled and selected by Auto CTS (EFR bit-7) and RTS/CTS flow control select (MCR bit-2). Auto CTS flow control allows starting and stopping of local data transmissions based on the modem CTS# signal. A logic 1 on the CTS# pin will stop UART transmitter as soon as the current character has finished transmission, and a logic 0 will resume data transmission. If automatic hardware flow control is not used, MSR bit-4 bit is the compliment of the CTS# input. However in the loopback mode, this bit is equivalent to the RTS# bit in the MCR register. The CTS# input may be used as a general purpose input when the modem interface is not used.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

MSR[5]: DSR Input Status

This input may be used for auto DTR/DSR flow control function, see **"Section 4.4, Automatic Hardware (RTS/CTS or DTR/DSR) Flow Control Operation" on page 32** for complete details. If automatic hardware flow control is not used, this bit is the compliment of the DSR# input. In the loopback mode, this bit is equivalent to the DTR# bit in the MCR register. The DSR# input may be used as a general purpose input when the modem interface is not used.

MSR[6]: RI Input Status

This bit is the compliment of the RI# input. In the loopback mode this bit is equivalent to bit-2 in the MCR register. The RI# input may be used as a general purpose input when the modem interface is not used.

MSR[7]: CD Input Status

This bit is the compliment of the CD# input. In the loopback mode this bit is equivalent to bit-3 in the MCR register. The CD# input may be used as a general purpose input

4.8.11 Modem Status Register (MSR) - Write-Only

The upper four bits 4-7 of this register sets the delay in number of bits time for the auto RS485 turn around from transmit to receive.

MSR [7:4]

When Auto RS485 feature is enabled (FCTR bit-5=1) and RTS# output is connected to the enable input of a RS-485 transceiver. These 4 bits select from 0 to 15 bit-time delay after the end of the last stop-bit of the last transmitted character. This delay controls when to change the state of RTS# output. This delay is very useful in long-cable networks. Table 16 shows the selection. The bits are enabled by EFR bit-4.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 16: AUTO RS485 HALF-DUPLEX DIRECTION CONTROL DELAY FROM TRANSMIT-TO-RECEIVE

MSR[7]	MSR[6]	MSR[5]	MSR[4]	DELAY IN DATA BIT(S) TIME
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
9	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

4.8.12 SCRATCH PAD REGISTER (SPR) - Read/Write

This is an 8-bit general purpose register for the user to store temporary data. The content of this register is preserved during sleep mode but becomes 0xFF (default) after a reset or a power off-on cycle.

4.8.13 FEATURE CONTROL REGISTER (FCTR) - Read/Write

FCTR [3:0] - Auto RTS/DTR Flow Control Hysteresis Select

These bits select the auto RTS/DTR flow control hysteresis and only valid when TX and RX Trigger Table-D is selected (FCTR bit-6 and 7 are set to logic 1). The RTS/DTR hysteresis is referenced to the RX FIFO trigger level. After reset, these bits are set to logic 0 selecting the next FIFO trigger level for hardware flow control. Table 17 shows the 16 selectable hysteresis levels.

FCTR[4]: Infrared RX Input Logic Select

- Logic 0 = Select RX input as active high encoded IrDA data, normal, (default).
- Logic 1 = Select RX input as active low encoded IrDA data, inverted.

FCTR[5]: Auto RS485 Enable

Auto RS485 half duplex control enable/disable.

- Logic 0 = Standard ST16C550 mode. Transmitter generates an interrupt when transmit holding register (THR) becomes empty. Transmit Shift Register (TSR) may still be shifting data bit out.
- Logic 1 = Enable Auto RS485 half duplex direction control. RTS# output changes its logic level from HIGH to LOW when finished sending the last stop bit of the last character out of the TSR register. It changes back to HIGH from LOW when a data byte is loaded into the THR or transmit FIFO. The change to HIGH occurs prior sending the start-bit. It also changes the transmitter interrupt from transmit holding to transmit shift register (TSR) empty.

FCTR[7:6]: TX and RX FIFO Trigger Table Select

These 2 bits select the transmit and receive FIFO trigger level table A, B, C or D. When table A, B, or C is selected the auto RTS flow control trigger level is set to "next FIFO trigger level" for compatibility to ST16C550 and ST16C650 series. RTS#/DTR# triggers on the next level of the RX FIFO trigger level, in another word, one FIFO level above and one FIFO level below. See Table 14 for complete selection with FCR bit 4-5 and FCTR bit 6-7, i.e. if Table C is used on the receiver with RX FIFO trigger level set to 56 bytes, RTS/DTR# output will de-assert at 60 and re-assert at 16.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 17: 16 SELECTABLE HYSTERESIS LEVELS WHEN TRIGGER TABLE-D IS SELECTED

FCTR BIT-3	FCTR BIT-2	FCTR BIT-1	FCTR BIT-0	RTS/DTR HYSTERESIS (CHARACTERS)
0	0	0	0	0
0	0	0	1	± 4
0	0	1	0	± 6
0	0	1	1	± 8
0	1	0	0	± 8
0	1	0	1	± 16
0	1	1	0	± 24
0	1	1	1	± 32
1	1	0	0	± 12
1	1	0	1	± 20
1	1	1	0	± 28
1	1	1	1	± 36
1	0	0	0	± 40
1	0	0	1	± 44
1	0	1	0	± 48
1	0	1	1	± 52

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

4.8.14 Enhanced Feature Register (EFR) - Read/Write

Enhanced features are enabled or disabled using this register. Bits 0-3 provide single or dual consecutive character software flow control selection (see Table 18). When the Xon1 and Xon2 and Xoff1 and Xoff2 modes are selected, the double 8-bit words are concatenated into two sequential characters. Caution: note that whenever changing the TX or RX flow control bits, always reset all bits back to logic 0 (disable) before programming a new setting.

EFR[3:0]: Software Flow Control Select

Combinations of software flow control can be selected by programming these bits. See Table 18 for complete selections. The XOFF1/XOFF2 characters are transmitted approximately 2 character times after the RX FIFO level has reached the RX trigger level, irrespective of which trigger table is used (Trigger Tables A-D). The XON1/XON2 characters are transmitted when the RX FIFO level falls below the next lower trigger level for Trigger Tables A-C and they are transmitted when the RX FIFO level falls below the (RX trigger level - hysteresis level) for Trigger Table D. For example, if Trigger Table D is used with an RX trigger level of 56 and a hysteresis level of 16, the XON1/XON2 characters are sent when the RX FIFO level count falls below 40.

EFR[4]: Enhanced Function Bits Enable

Enhanced function control bit. This bit enables the functions in IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 to be modified. After modifying any enhanced bits, EFR bit-4 can be set to a logic 0 to latch the new values. This feature prevents legacy software from altering or overwriting the enhanced functions once set. Normally, it is recommended to leave it enabled, logic 1.

- Logic 0 = modification disable/latch enhanced features. IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are saved to retain the user settings. After a reset, the IER bits 4-7, ISR bits 4-5, FCR bits 4-5, and MCR bits 5-7 are set to a logic 0 to be compatible with the industry standard 16550 (default).
- Logic 1 = Enables the enhanced functions. When this bit is set to a logic 1 all enhanced features are enabled.

EFR[5]: Special Character Detect Enable

- Logic 0 = Special Character Detect Disabled (default).
- Logic 1 = Special Character Detect Enabled. The UART compares each incoming receive character with data in Xoff-2 register. If a match exists, the received data will be transferred to FIFO and ISR bit-4 will be set to indicate detection of the special character. Bit-0 corresponds with the LSB bit for the receive character. If flow control is set for comparing Xon1, Xoff1 (EFR [1:0]='10') then flow control and special character work normally. However, if flow control is set for comparing Xon2, Xoff2 (EFR[1:0]='01') then flow control works normally, but Xoff2 will not go to the FIFO, and will generate an Xoff interrupt and a special character interrupt.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 18: SOFTWARE FLOW CONTROL FUNCTIONS

TX S/W FLOW CONTROL		RX S/W FLOW CONTROL		
EFR BIT-3 CONT-3	EFR BIT-2 CONT-2	EFR BIT-1 CONT-1	EFR BIT-0 CONT-0	SOFTWARE FLOW CONTROL FUNCTIONS
0	0	X	X	No transmit flow control
0	1	X	X	Transmit Xon2, Xoff2
1	0	X	X	Transmit Xon1, Xoff1
1	1	X	X	Transmit Xon1 and Xon2, Xoff1 and Xoff2
X	X	0	0	No receive flow control
X	X	0	1	Receiver compares Xon2, Xoff2
X	X	1	0	Receiver compares Xon1, Xoff1
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2, Xoff1 and Xoff2
1	1	1	1	Transmit Xon1 and Xon2, Xoff1 and Xoff2 Receiver compares Xon1 and Xon2, Xoff1 and Xoff2

EFR[6]: Auto RTS or DTR Flow Control Enable

RTS#/DTR# output may be used for hardware flow control by setting EFR bit-6 to logic 1. When Auto RTS/DTR is selected, an interrupt will be generated when the receive FIFO is filled to the programmed trigger level and RTS#/DTR# will de-assert HIGH at the next upper trigger or selected hysteresis level. RTS#/DTR# will return LOW when FIFO data falls below the next lower trigger or selected hysteresis level (see FCTR bits 4-7). The RTS# or DTR# output must be asserted (LOW) before the auto RTS/DTR can take effect. The selection for RTS# or DTR# is through MCR bit-2. RTS/DTR# pin will function as a general purpose output when hardware flow control is disabled.

- Logic 0 = Automatic RTS/DTR flow control is disabled (default).
- Logic 1 = Enable Automatic RTS/DTR flow control.

EFR[7]: Auto CTS Flow Control Enable

Automatic CTS or DSR Flow Control.

- Logic 0 = Automatic CTS/DSR flow control is disabled (default).
- Logic 1 = Enable Automatic CTS/DSR flow control. Transmission stops when CTS#/DSR# pin de-asserts HIGH. Transmission resumes when CTS/DSR# pin returns LOW. The selection for CTS# or DSR# is through MCR bit-2.

4.8.15 TXCNT[7:0]: Transmit FIFO Level Counter - Read-Only

Transmit FIFO level byte count from 0x00 (zero) to 0x40 (64). This 8-bit register gives an indication of the number of characters in the transmit FIFO. The FIFO level Byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data loading to the transmit FIFO, which reduces CPU bandwidth requirements. Please see the Application Note DAN119 on Exar's website for a detailed discussion of FIFO level counters. Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.

4.8.16 TXTRG [7:0]: Transmit FIFO Trigger Level - Write-Only

An 8-bit value written to this register sets the TX FIFO trigger level from 0x00 (zero) to 0x40 (64). The TX FIFO trigger level generates an interrupt whenever the data level in the transmit FIFO falls below this preset trigger level.

4.8.17 RXCNT[7:0]: Receive FIFO Level Counter - Read-Only

Receive FIFO level byte count from 0x00 (zero) to 0x40 (64). It gives an indication of the number of characters in the receive FIFO. The FIFO level byte count register is read only. The user can take advantage of the FIFO level byte counter for faster data unloading from the receiver FIFO, which reduces CPU bandwidth requirements. Please see the Application Note DAN119 on Exar's website for a detailed discussion of FIFO level counters. Due to the dynamic nature of the FIFO counters, this register should be read until the same value is returned twice.

4.8.18 RXTRG[7:0]: Receive FIFO Trigger Level - Write-Only

An 8-bit value written to this register, sets the RX FIFO trigger level from 0x00 (zero) to 0x40 (64). The RX FIFO trigger level generates an interrupt whenever the receive FIFO level rises to this preset trigger level.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

TABLE 19: UART RESET CONDITIONS

REGISTERS	RESET STATE
DLL	Bits 7-0 = 0xXX
DLM	Bits 7-0 = 0xXX
RHR	Bits 7-0 = 0xXX
THR	Bits 7-0 = 0xXX
IER	Bits 7-0 = 0x00
FCR	Bits 7-0 = 0x00
ISR	Bits 7-0 = 0x01
LCR	Bits 7-0 = 0x00
MCR	Bits 7-0 = 0x00
LSR	Bits 7-0 = 0x60
MSR	Bits 3-0 = logic 0 Bits 7-4 = logic levels of the inputs
SPR	Bits 7-0 = 0xFF
FCTR	Bits 7-0 = 0x00
EFR	Bits 7-0 = 0x00
TXCNT	Bits 7-0 = 0x00
TXTRG	Bits 7-0 = 0x00
RXCNT	Bits 7-0 = 0x00
RXTRG	Bits 7-0 = 0x00
XCHAR	Bits 7-0 = 0x00
XON1	Bits 7-0 = 0x00
XON2	Bits 7-0 = 0x00
XOFF1	Bits 7-0 = 0x00
XOFF2	Bits 7-0 = 0x00
I/O SIGNALS	**RESET STATE**
TX[ch-7:0]	HIGH (if ENIR pin = LOW) LOW (if ENIR pin = HIGH)
RTS#[ch-7:0]	HIGH
DTR#[ch-7:0]	HIGH
EECK	LOW
EECS	LOW
EEDI	LOW

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5.0 PROGRAMMING EXAMPLES

These examples are for devices with top mark date codes of "GC YYWW" and older.

5.1 UNLOADING RECEIVE DATA USING THE SPECIAL RECEIVE FIFO DATA WITH STATUS

It is suggested that before starting to read the Special Receive FIFO Data with Status to unload data from any UART channel (address 0x180 for channel 0), do a dummy write to the Device ID (DVID) register in the Configuration Register of the device. The DVID register is a read-only register, so writing to it will not affect any of the settings of the UART. The Special Receive FIFO Data with Status register can then be read multiple times subsequently without any byte-swapping problem as long as no other register (except the Device ID register) is accessed in between data unload. If you must read or write to another register, make that dummy write to the DVID register again and continue with data unloading.

A step by step procedure describing the sequence for a target channel is shown below. From the receive data service routine:

- Do a dummy write to Device ID (DVID) register. Address 0x8D in BYTE alignment or address 0x8C in DWORD alignment.
- Read the data byte and its associated error status from 'Special Receive FIFO Data with Status' register of the target channel until done or empty when one of the LSR status byte bit-0=0.

NOTE: If you must do other Read/Write operations to other register(s) during data unloading, repeat steps 1 & 2 to continue unloading data plus status from the 'Special Receive FIFO Data with Status' register of the target channel.

Some Examples of using the Special Receive FIFO Data with Status:

EXAMPLE I: POLLING

.....
Read LSR
Write DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
.....

EXAMPLE 2: INTERRUPT SERVICE USING INTERRUPT INFORMATION IN DEVICE CONFIGURATION REGISTER SET

.....
Read Global Interrupt Register INT0 (address 0x080)
Read INT1 through INT3 registers to identify interrupting channel (address 0x081 through 0x083)
Write DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
.....

EXAMPLE 3: INTERRUPT SERVICE USING INTERRUPT INFORMATION IN INDIVIDUAL CHANNEL'S REGISTERS

.....
Read Global Interrupt Register INT0 (address 0x080)
Read ISR register of interrupting channel
Write DVID
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)*
Read Special Receive FIFO Data with Status (address 0x180 for channel 0, etc)
.....

* In case some other registers need to be accessed in between 'Special Receive FIFO Data with Status' reads, a 'Write DVID' instruction has to be inserted before resuming 'Special Receive FIFO Data with Status' read operation.

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ABSOLUTE MAXIMUM RATINGS

Power Supply Range	7 Volts
Voltage at Any Pin	-0.5 to 7V
Operating Temperature	-40° to +85° C
Storage Temperature	-65° to +150° C
Package Dissipation	500 mW
Thermal Resistance (20x20x1.4mm 144-LQFP)	theta-ja = 42, theta-jc = 8

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS FOR 5V SIGNALING

TA=0° to 70°C (-40° to +85°C for industrial grade package). VCC = 4.5 - 5.5V.

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITION	NOTES
V_{IL}	Input Low Voltage	-0.5	0.8	V		
V_{IH}	Input High Voltage	2.0	6.0	V		
V_{OL}	Output Low Voltage		0.55	V	Iout=6 mA	
V_{OH}	Output High Voltage	2.4		V	Iout=-2 mA	
I_{IL}	Input Low Leakage Current		-10	uA		
I_{IH}	Input High Leakage Current		10	uA		
I_{CL}	Input Clock Leakage		±10	uA		
C_{IN}	Input Pin Capacitance		10	pF		
C_{CLK}	CLK Pin Capacitance	5	12	pF		
C_{IDSEL}	IDSEL Pin Capacitance		8	pF		
I_{CC}	Power Supply Current		5	mA	PCI Bus CLK and Ext. Clock = 2MHz, all inputs at VCC or GND and all outputs are unloaded.	
I_{SLEEP}	Sleep Current		400	uA	All eight UARTs asleep. AD[31:0] at GND, all inputs at VCC or GND.	

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

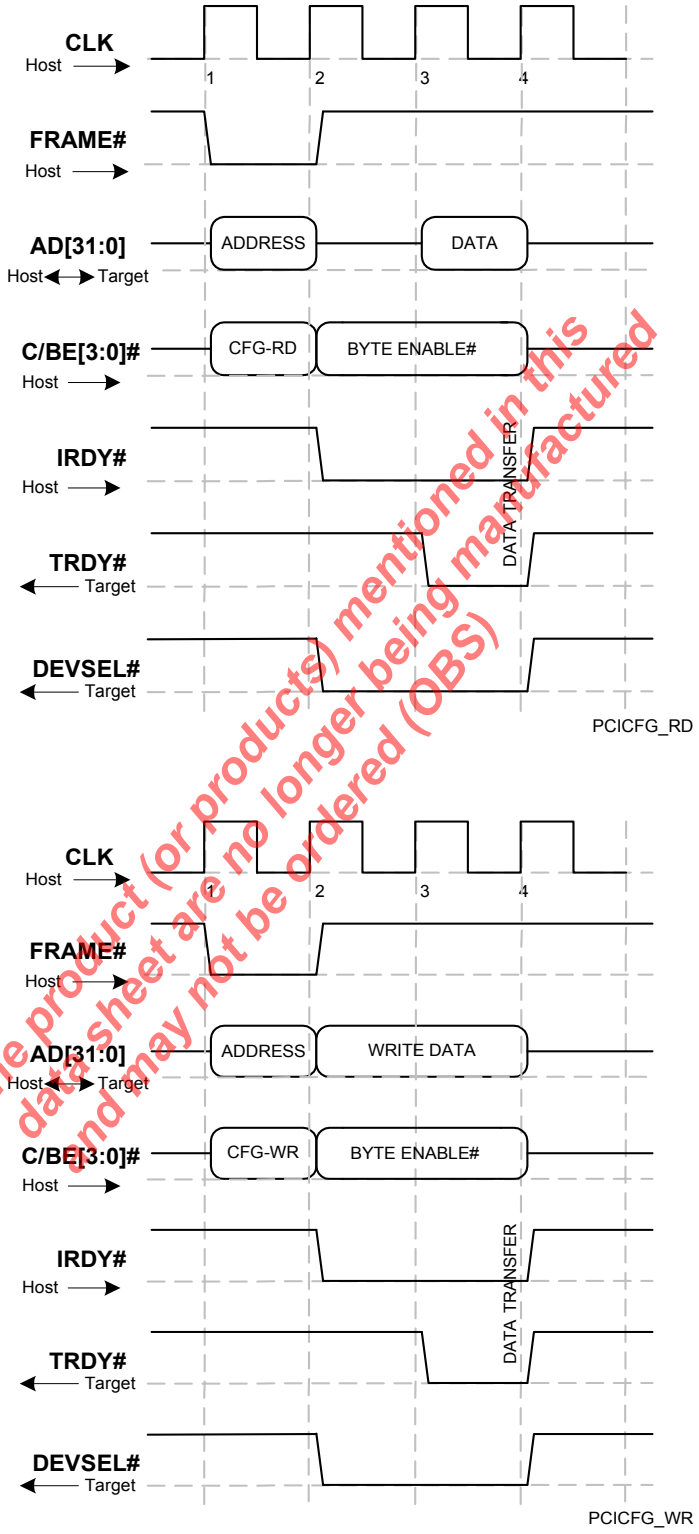
AC ELECTRICAL CHARACTERISTICS FOR 5V SIGNALING

TA=0^{o} to 70^{o}C (-40^{o} to +85^{o}C for industrial grade package). VCC = 4.5 - 5.5V.

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
XTAL1	UART Crystal Oscillator		24	MHz	
ECLK	External Clock		50	MHz	
$I_{OH(AC)}$	Switching Current High	-44		mA	0<Vout<1.4
$I_{OL(AC)}$	Switching Current Low	95		mA	Vout/0.023
$Slew_R$	Output Rise Slew Rate	1	4	V/ns	0.2Vcc - 0.6Vccload
$Slew_F$	Output Fall Slew Rate	1	4	V/ns	0.6Vcc - 0.2Vcc_{load}
T_{CYC}	CLK Cycle Time	30	∞	ns	PCI Bus Clock, CLK (33.34 MHz max)
T_{HI}	CLK High Time	11		ns	
T_{LO}	CLK Low Time	11		ns	
	CLK Slew Rate	1	4	V/ns	
T_{VAL}	CLK to Signal Valid Delay	2	11	ns	
T_{ON}	Float to Active Delay	2		ns	
T_{OFF}	Active to Float Delay		28	ns	
T_{SETUP}	Input Setup Time to CLK - bused signals	7		ns	
T_{HOLD}	Input Hold Time from CLK	0		ns	
T_{PRST}	RST# Active Time After Power Stable	1		ms	
$T_{CRST\#}$	RST# Active Time After CLK Stable	100		us	
	RST# Slew Rate	50		mV/ns	

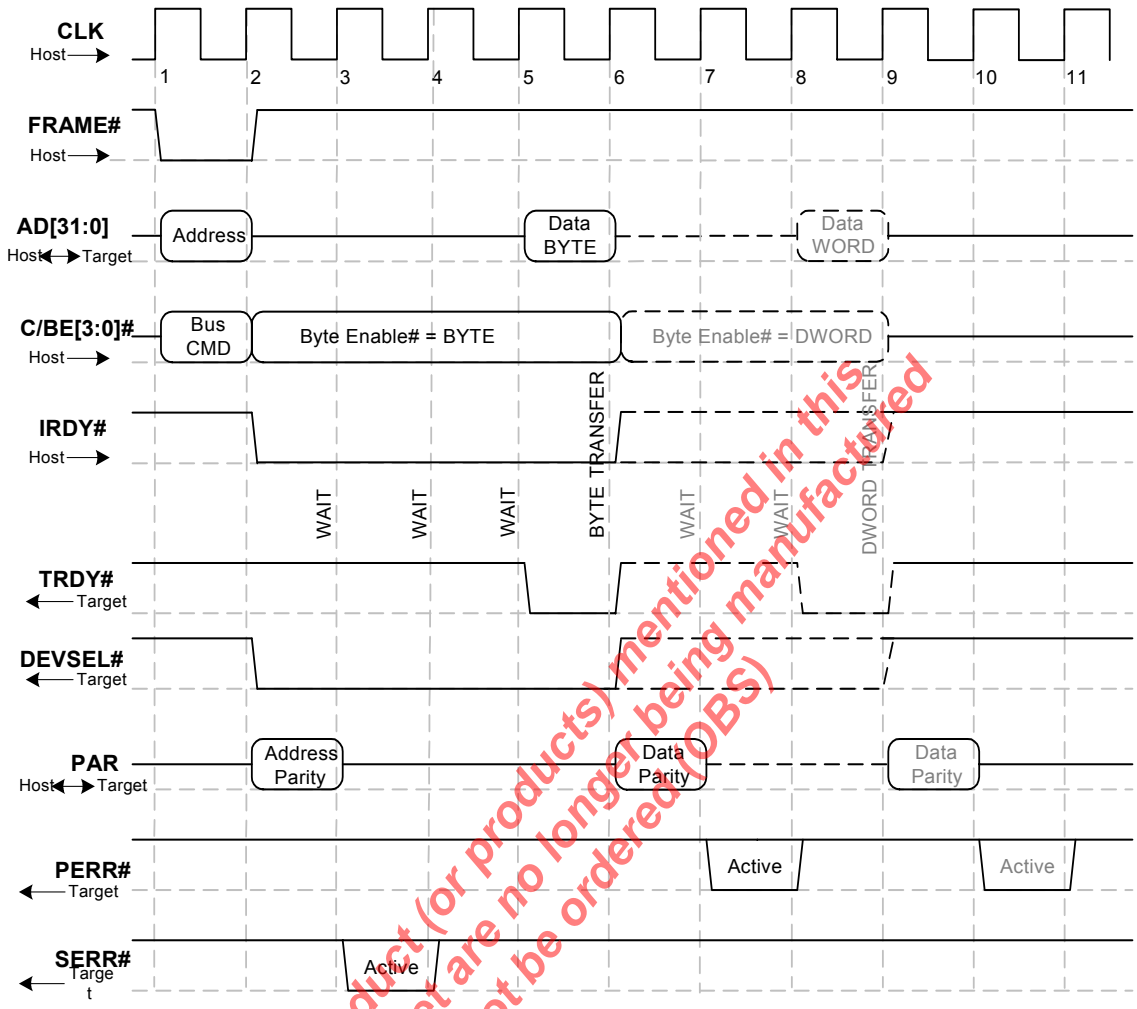
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 17. PCI BUS CONFIGURATION SPACE REGISTERS READ AND WRITE OPERATION



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

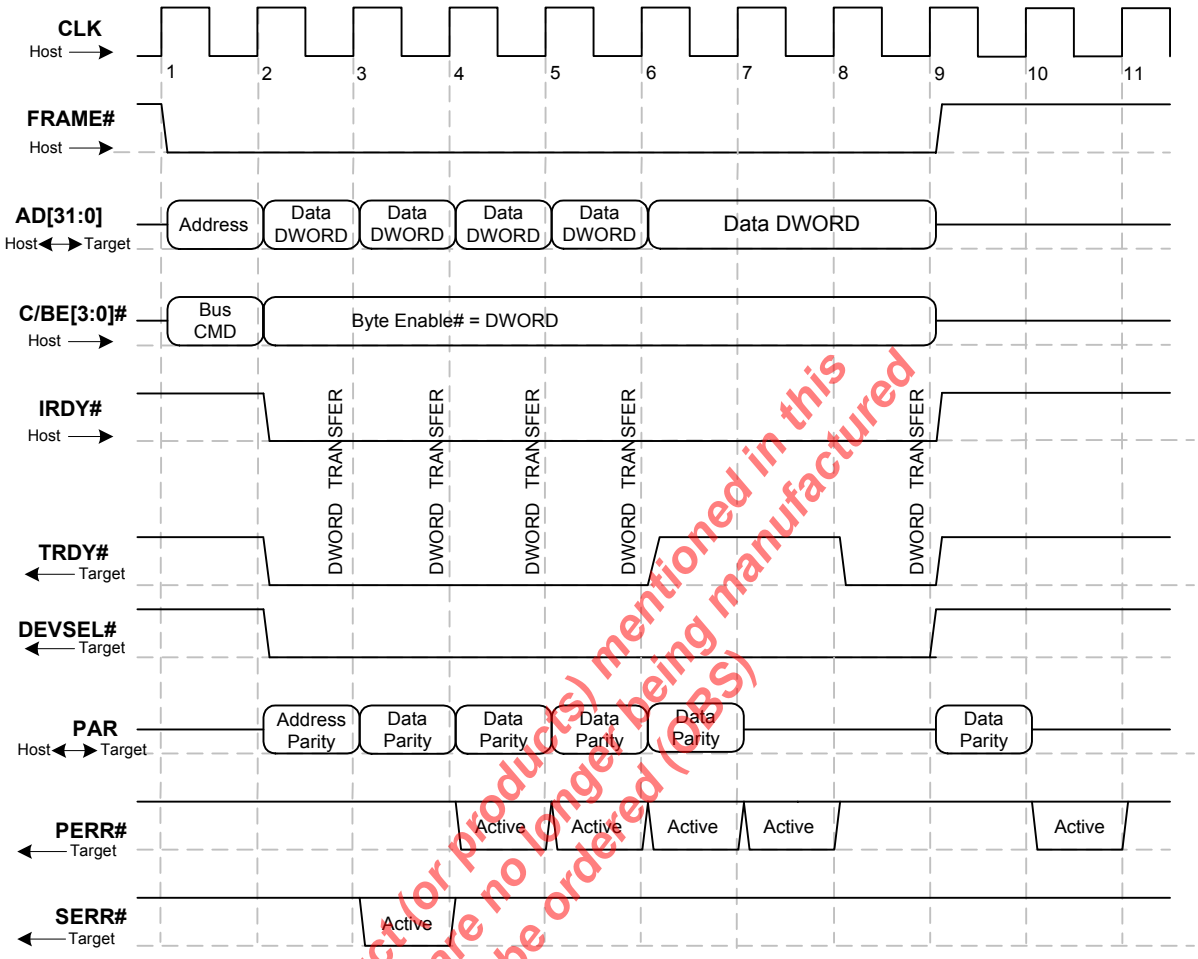
FIGURE 18. DEVICE CONFIGURATION AND UART REGISTERS READ OPERATION FOR A BYTE OR DWORD



Note: PERR# and SERR are optional in a bus target application.
Even Parity is on AD[31:0], C/BE[3:0]#, and PAR

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

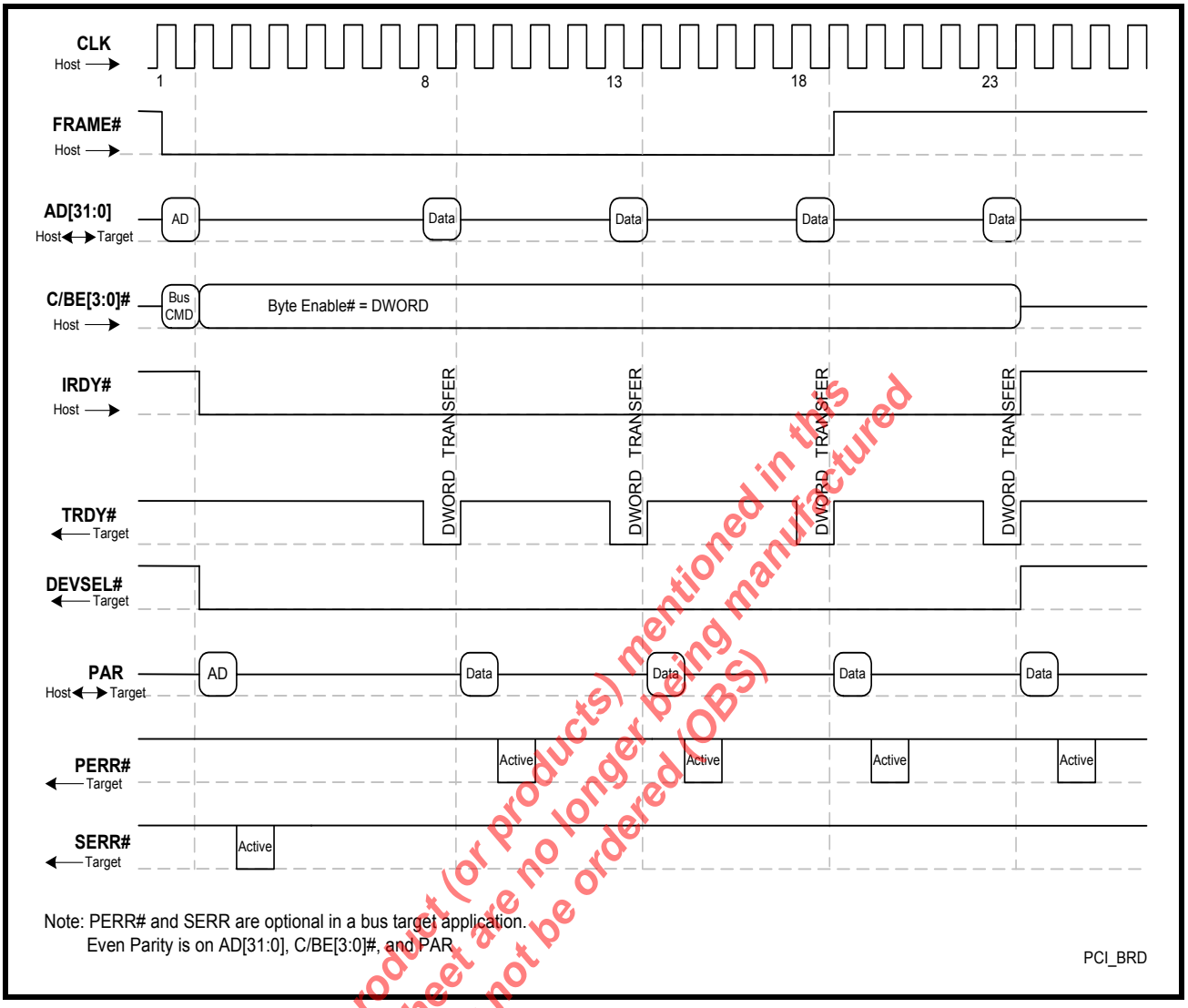
FIGURE 19. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND TRANSMIT DATA BURST WRITE OPERATION



Note: PERR# and SERR are optional in a bus target application.
Even Parity is on AD[31:0], C/BE[3:0]#, and PAR

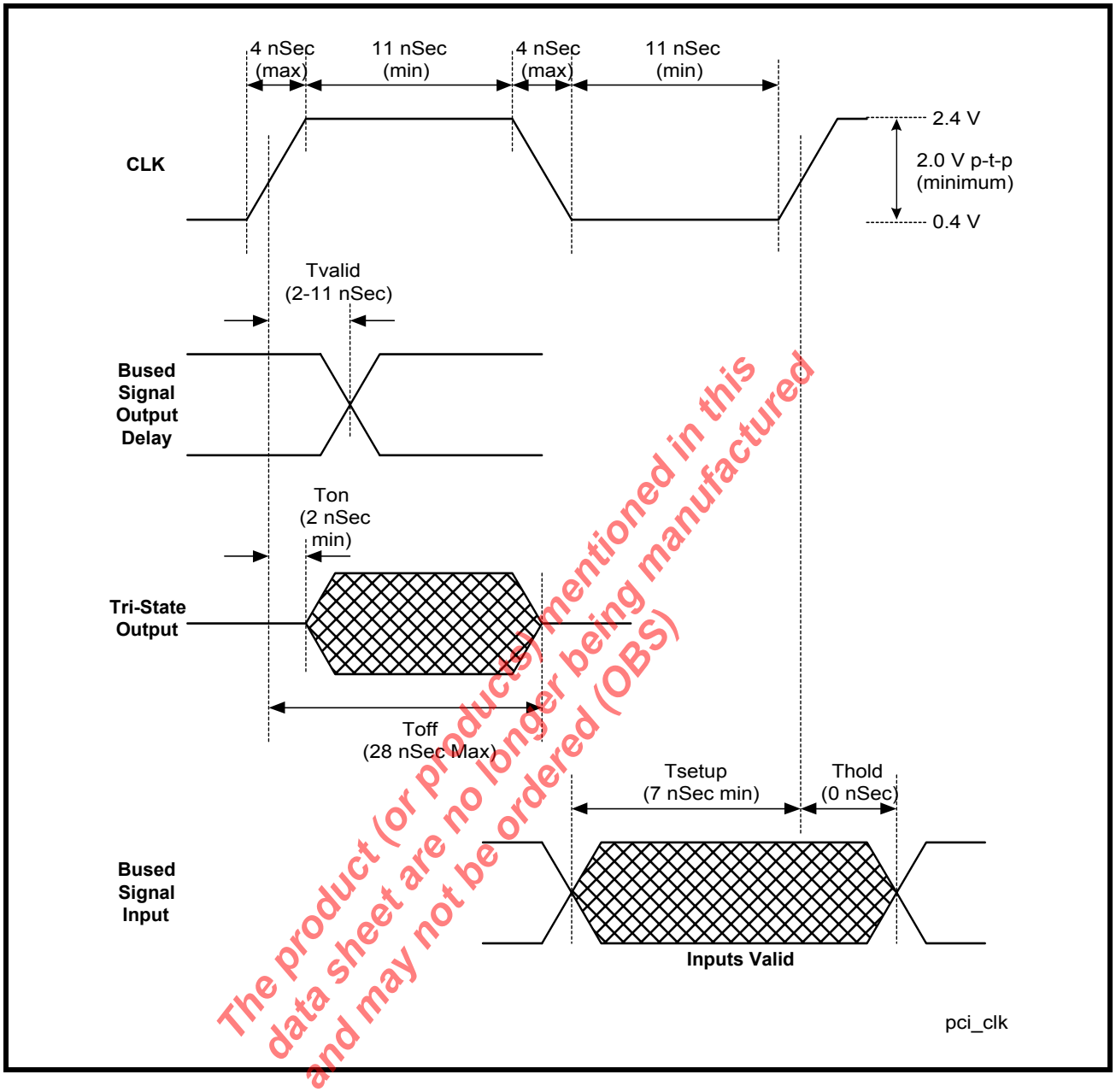
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 20. DEVICE CONFIGURATION REGISTERS, UART REGISTERS AND RECEIVE DATA BURST READ OPERATION



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 21. 5V PCI BUS CLOCK (DC TO 33MHZ)



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

FIGURE 22. TRANSMIT DATA INTERRUPT AT TRIGGER LEVEL

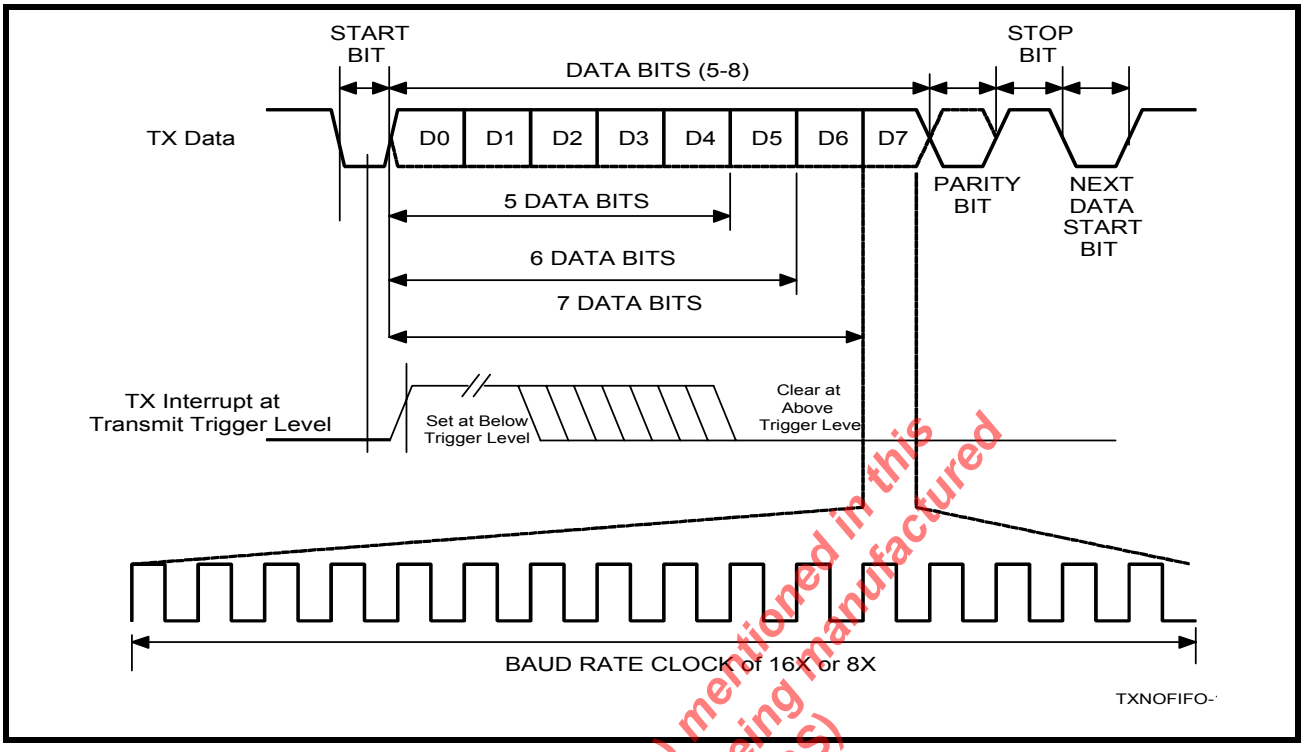
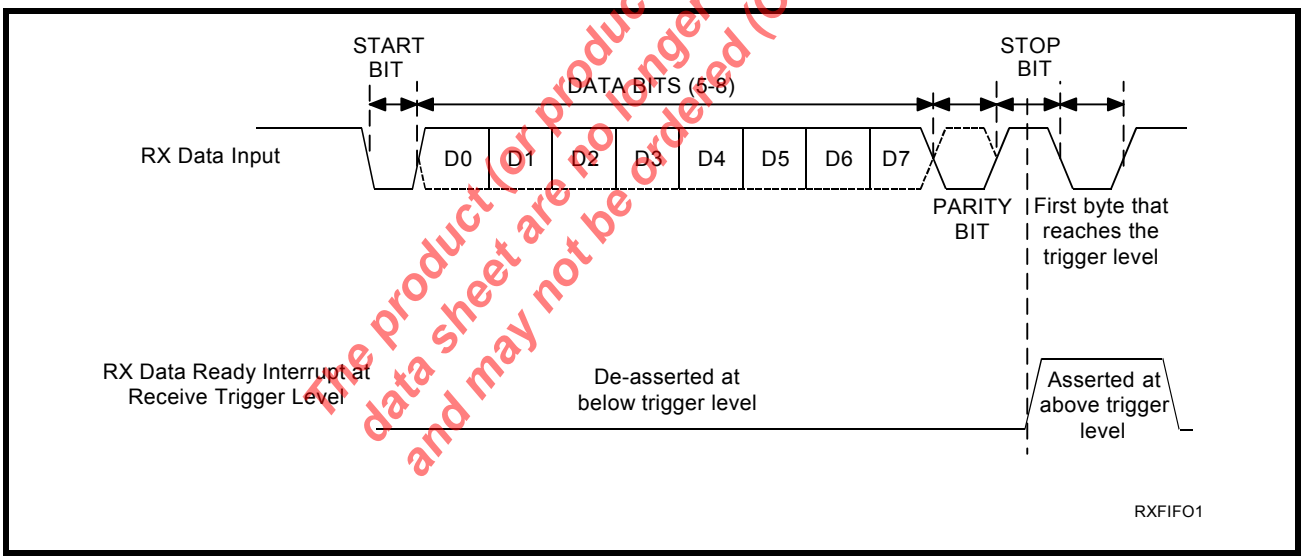


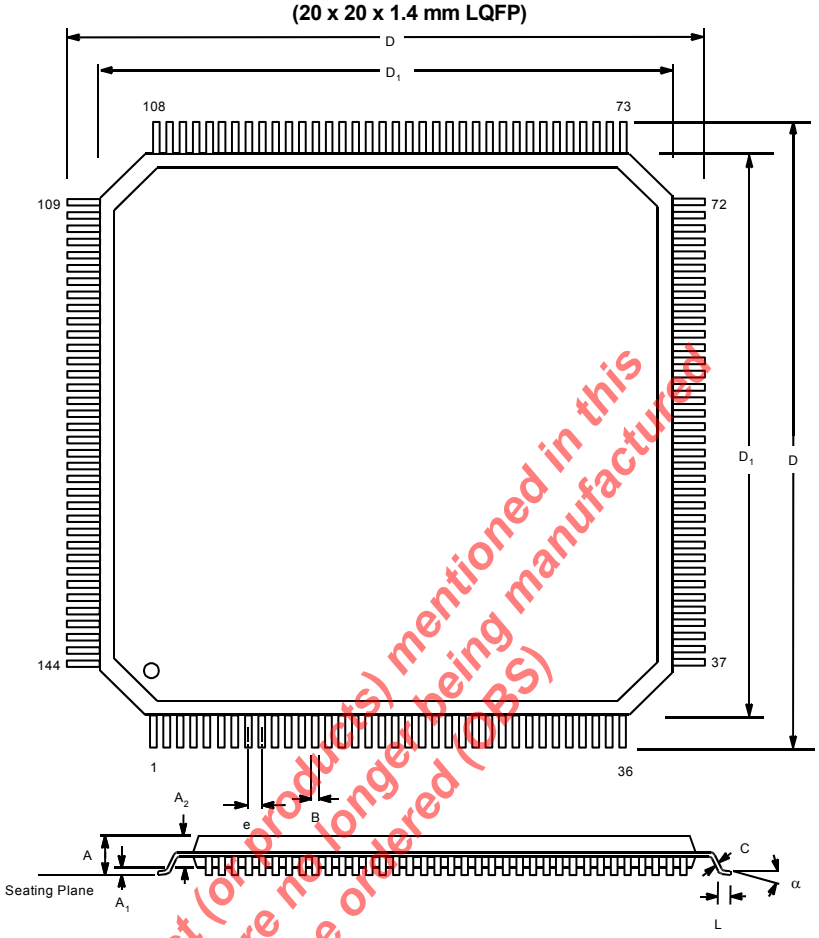
FIGURE 23. RECEIVE DATA READY INTERRUPT AT TRIGGER LEVEL



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

PACKAGE DIMENSIONS

144 LEAD LOW-PROFILE QUAD FLAT PACK
(20 x 20 x 1.4 mm LQFP)



The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

NOTE: *Note: The control dimension is the millimeter column*

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D1	0.783	0.791	19.90	20.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0×	7×	0×	7×

REVISION HISTORY

DATE	REVISION	DESCRIPTION
March 2000	Rev. 1.0.1	Preliminary
March 2001	Rev. 1.0.2	Corrected patent number, front page; reference to DAN112; corrected CTS#, DSR#, RI# and CD# in figure 11 internal loopback; shaded MCR bit-2 and EFR bit-4 in table 11; fixed "(ISR bit=1)" in figure 12; clarified MCR bits 2 and 6; update 5V electrical characteristics tables with Icc and Isleep current, and added 3.3V electrical characteristics tables
May 2001	Rev. 1.1.0	Deleted ICH and ICL from Electrical tables. Finalized and changed values in 3.3V Electrical table. Corrected spelling. Changed data sheet from Preliminary to Final.
June 2001	Rev. 1.1.1	Corrected VIH (2.0 to 2.4V) in DC Electrical Characteristics Tables.
August 2001	Rev. 1.1.2	Clarified EECS, PERR# & SERR# hardware pin descriptions, MSR Register and Software Flow Control Functions. Added Programming Examples to explain unloading receive data using the Special Receive FIFO Data with Status.
December 2001	Rev. 1.1.3	Changed V_{IL} max from 0.8 to 0.7V. Changed condition on ICC from CLK=50MHz to " PCIClk=2MHz, EXT Clock=2Mhz". Changed Condition on V_{OL} from Iout=6mA to 4mA. Changed Condition on V_{OH} from Iout=-2mA to -1mA.
May 2003	Rev 1.2.0	Changed to single column format. Added uarttechsupport e-mail address to last page.
September 2003	Rev 1.3.0	Added Device Status to Ordering Information. Clarified RS485 description. Added description for PCI Burst Read and PCI Burst Write. Added wake-up indicator to interrupt source table.
May 2004	Rev 1.4.0	Clarified pin descriptions- changed from using logic 1 and logic 0 to HIGH (VCC) and LOW (GND) for input and output pin descriptions. The XR17C158 is a 5V Only PCI Octal UART (removed 3.3V electrical characteristics). For a 3.3V PCI Octal UART, please see the XR17D158. The Device Revision Register (DREV) has been updated to 0x08 for devices with top mark date code "H2 YYWW".
November 2004	Rev 1.4.1	The Device Revision Register (DREV) has been updated to 0x09 for devices with top mark date code "I2 YYWW".
January 2005	Rev 1.4.2	The programming examples to unload data from the special RX FIFO + LSR data register were updated to use a dummy write to DVID instead of a dummy read to DVID to prevent the byte swapping in the devices with top mark date code of "GC YYWW" and older. SEE "PROGRAMMING EXAMPLES" ON PAGE 54.
August 2005	Rev 1.4.3	Updated the 1.4mm-thick Quad Flat Pack package description from "TQFP" to "LQFP" to be consistent with JEDEC and Industry norms.

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