A New Direction in Mixed-Signal

CLC2011, CLC4011

Low Power, Low Cost, Rail-to-Rail I/O Amplifiers

General Description

The CLC2011 (dual) and CLC4011 (quad) are ultra-low cost, low power, voltage feedback amplifiers. At 2.7V, the CLCx011 family uses only 136μA of supply current per amplifier and are designed to operate from a supply range of 2.5V to 5.5V (±1.25 to ±2.75). The input voltage range exceeds the negative and positive rails.

The CLCx011 family of amplifiers offer high bipolar performance at a low CMOS prices. They offer superior dynamic performance with 4.9MHz small signal bandwidths and 5.3V/μs slew rates. The combination of low power, high bandwidth, and rail-to-rail performance make the CLCx011 amplifiers well suited for battery-powered communication/computing systems.

FEATURES

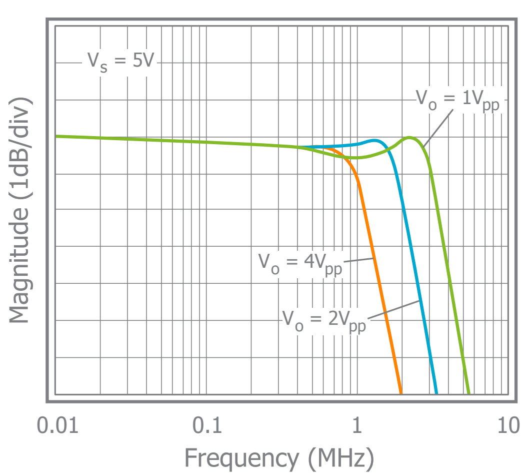
- 136μA supply current
- 4.9MHz bandwidth
- Output swings to within 20mV of either rail
- Input voltage range exceeds the rail by >250mV
- 5.3V/μs slew rate
- 21nV/√Hz input voltage noise
- ±35mA linear output current
- Fully specified at 2.7V and 5V supplies

APPLICATIONS

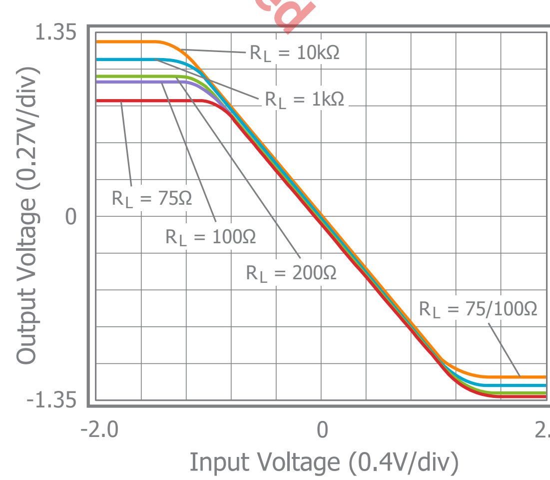
- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Notebooks and PDA's
- Signal conditioning
- Medical equipment
- Portable medical instrumentation

Ordering Information - back page

Large Signal Frequency Response



Output Swing vs. Load



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_S .... 0V to 6V

V_{IN} .... $-V_S$ - 0.5V to $+V_S$ +0.5V

Continuous Output Current........ -40mA to +40mA

Operating Conditions

Supply Voltage Range .... 2.5 to 5.5V

Operating Temperature Range .... -40°C to 125°C

Junction Temperature .... 150°C

Storage Temperature Range........ -65°C to 150°C

Lead Temperature (Soldering, 10s) .... 260°C

Package Thermal Resistance

θ_{JA} (SOIC-8) .... 150°C/W

θ_{JA} (MSOP-8) .... 200°C/W

θ_{JA} (SOIC-14) .... 90°C/W

θ_{JA} (TSSOP-14) .... 100°C/W

Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

CLC2011, CLC4011 (HBM) 2kV

ESD Rating for HBM (Human Body Model).

Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = R_g = 5kΩ, R_L = 10kΩ to V_S/2; G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.02V_{pp}		4.9		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		3.2		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		1.4		MHz
GBWP	Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		2.5		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		163		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		500		ns
OS	Overshoot	V_{OUT} = 1V step		<1		%
SR	Slew Rate	1V step		5.3		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		-72		dBc
HD3	3rd Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		-72		dBc
THD	Total Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		0.03		%
e_n	Input Voltage Noise	>10kHz		21		nV/√Hz
X_{TALK}	Crosstalk	Channel to Channel, V_{OUT} = 2V_{pp}, f = 10kHz		82		dB
		Channel to Channel, V_{OUT} = 2V_{pp}, f = 50kHz		74		dB
DC Performance						
V_{IO}	Input Offset Voltage			0.5		mV
d_{VIO}	Average Drift			5		µV/°C
I_B	Input Bias Current			90		nA
dI_B	Average Drift			32		pA/°C
PSRR	Power Supply Rejection Ratio	DC	55	83		dB
A_{OL}	Open Loop Gain	V_{OUT} = V_S / 2		90		dB
I_S	Supply Current	per channel		136		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		12		MΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common Mode Input Range			-0.25 to 2.95		V
CMRR	Common Mode Rejection Ratio	DC		81		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_S / 2		0.02 to 2.68		V
		R_L = 1kΩ to V_S / 2		0.05 to 2.63		V
		R_L = 200Ω to V_S / 2		0.11 to 2.52		V
I_{OUT}	Output Current			±30		mA

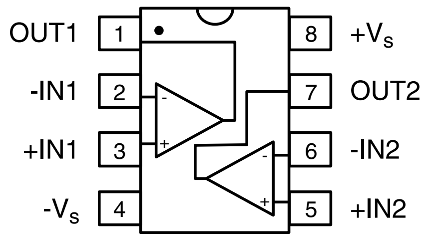
Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = R_g = 5kΩ, R_L = 10kΩ to V_S/2; G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.02V_{pp}		4.3		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		3.0		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		2.3		MHz
GBWP	Gain Bandwidth Product	G = +11, V_{OUT} = 0.2V_{pp}		2.5		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 1V step; (10% to 90%)		110		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		470		ns
OS	Overshoot	V_{OUT} = 1V step		<1		%
SR	Slew Rate	2V step		9		V/μs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		-73		dBc
HD3	3rd Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		-75		dBc
THD	Total Harmonic Distortion	10kHz, V_{OUT} = 1V_{pp}		0.03		%
e_n	Input Voltage Noise	>10kHz		22		nV/√Hz
X_{TALK}	Crosstalk	Channel to Channel, V_{OUT} = 2V_{pp}, f = 10kHz		82		dB
		Channel to Channel, V_{OUT} = 2V_{pp}, f = 50kHz		74		dB
DC Performance						
V_{IO}	Input Offset Voltage		-8	1.5	8	mV
d_{VIO}	Average Drift			15		μV/°C
I_B	Input Bias Current			90	450	nA
dI_B	Average Drift			40		pA/°C
PSRR	Power Supply Rejection Ratio	DC	55	85		dB
A_{OL}	Open Loop Gain	V_{OUT} = V_S / 2		80		dB
I_S	Supply Current	per channel		160	235	μA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		12		MΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common Mode Input Range			-0.25 to 5.25		V
CMRR	Common Mode Rejection Ratio	DC	58	80		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 10kΩ to V_S / 2	0.08 to 4.92	0.04 to 4.96		V
		R_L = 1kΩ to V_S / 2		0.07 to 4.9		V
		R_L = 200Ω to V_S / 2		0.14 to 4.67		V
I_{OUT}	Output Current			±35		mA

CLC2011 Pin Configurations

SOIC-8 / MSOP-8



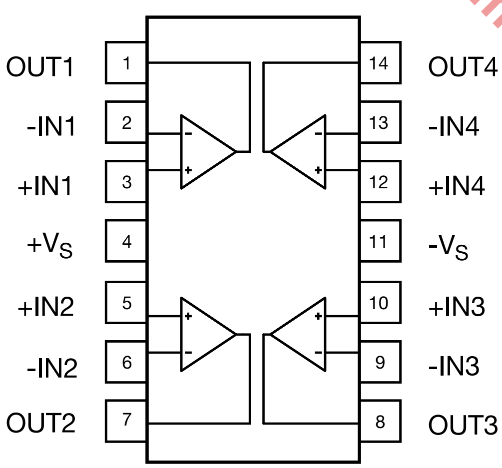
CLC2011 Pin Assignments

SOIC-8 / MSOP-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

CLC4011 Pin Configuration

SOIC-14 / TSSOP-14



CLC4011 Pin Assignments

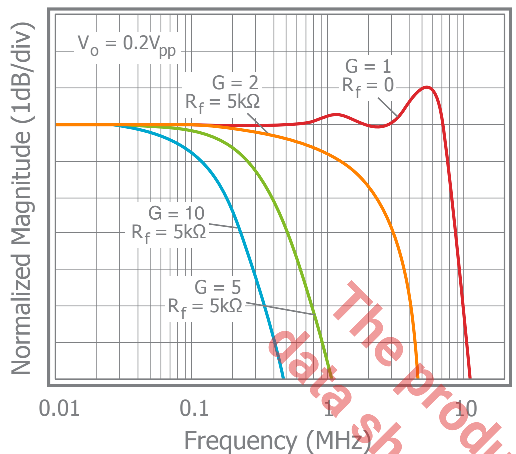
SOIC-14 / TSSOP-14

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$+V_S$	Positive supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative input, channel 3
10	+IN3	Positive input, channel 3
11	$-V_S$	Negative supply
12	+IN4	Positive input, channel 4
13	-IN4	Negative input, channel 4
14	OUT4	Output, channel 4

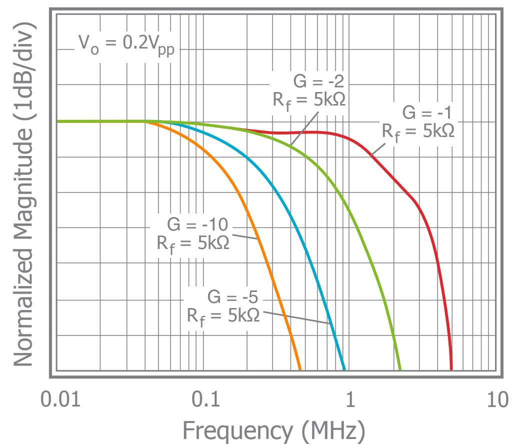
Typical Performance Characteristics

$T_A = 25°C$, $V_S = +2.7V$, $R_f = R_g = 5k\Omega$, $R_L = 10k\Omega$ to $V_S/2$; G = 2; unless otherwise noted.

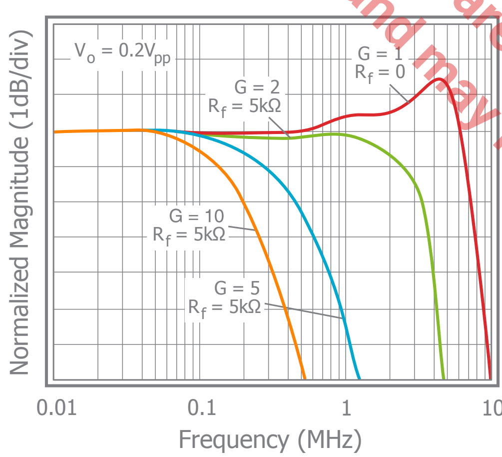
Non-Inverting Frequency Response at $V_S = 5V$



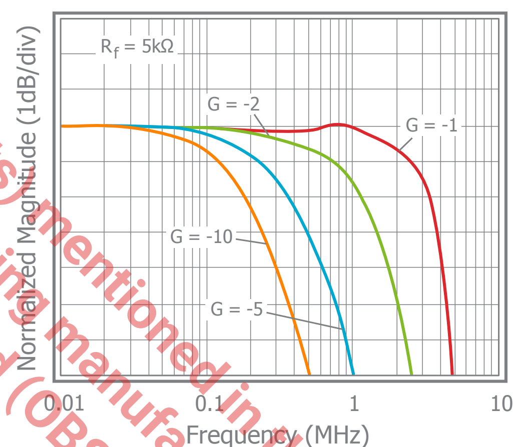
Inverting Frequency Response at $V_S = 5V$



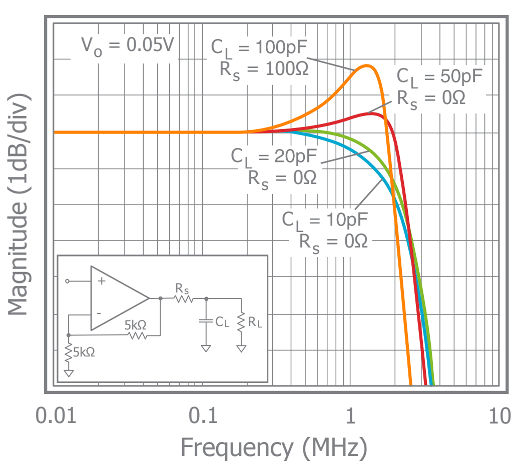
Non-Inverting Frequency Response at $V_S = 2.7V$



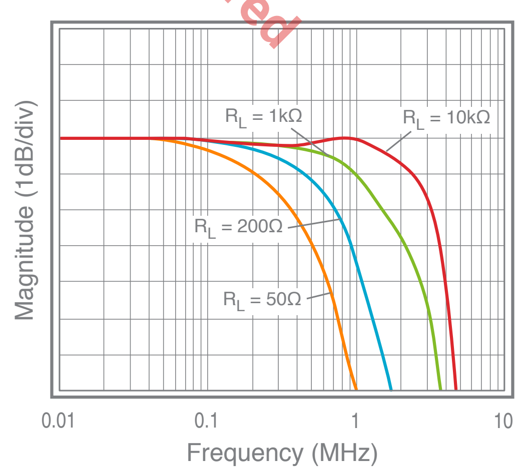
Inverting Frequency Response at $V_S = 2.7V$



Frequency Response vs C_L



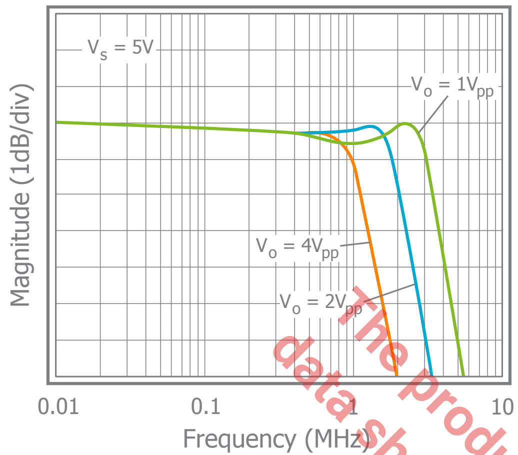
Frequency Response vs R_L



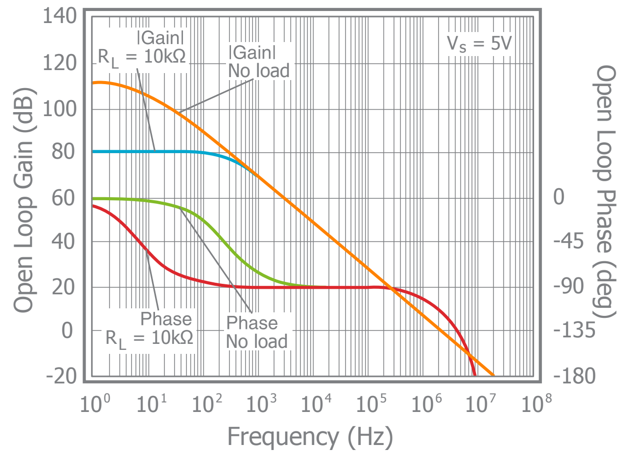
Typical Performance Characteristics

$T_A = 25°C$, $V_S = +2.7V$, $R_f = R_g = 5kΩ$, $R_L = 10kΩ$ to $V_S/2$; G = 2; unless otherwise noted.

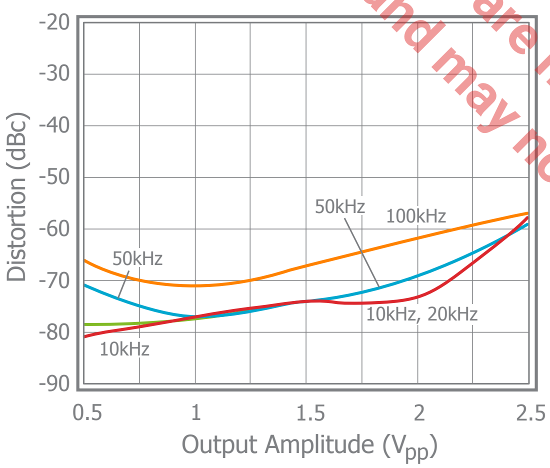
Frequency Response vs. V_{OUT}



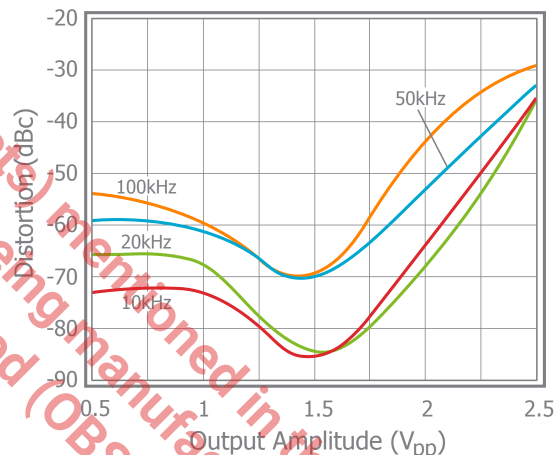
Open Loop Gain & Phase vs. Frequency



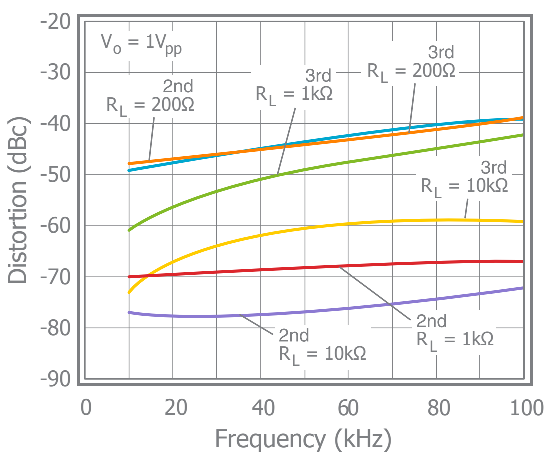
2nd Harmonic Distortion vs V_{OUT}



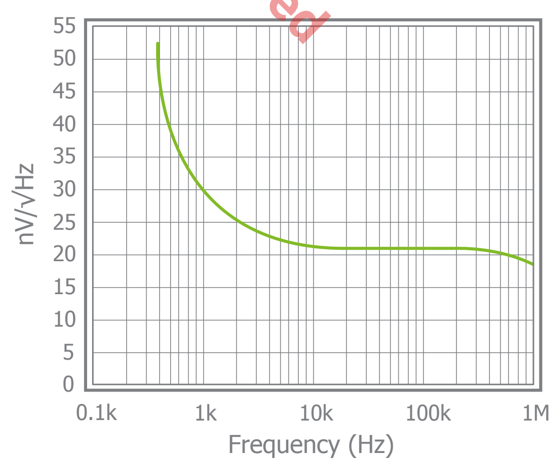
3rd Harmonic Distortion vs V_{OUT}



2nd & 3rd Harmonic Distortion at $V_S = 2.7V$



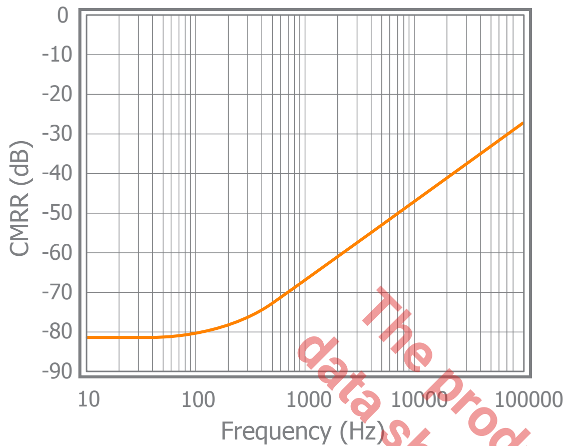
Input Voltage Noise



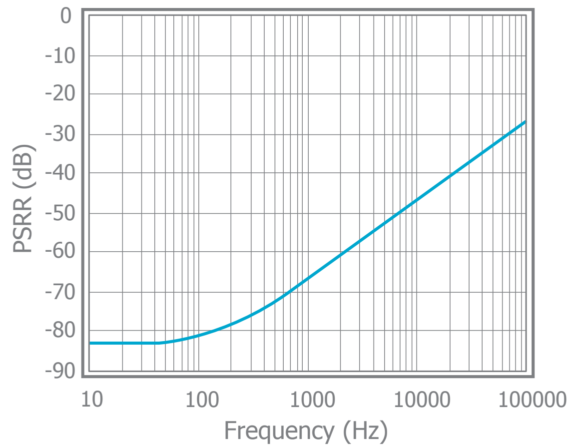
Typical Performance Characteristics

T_A = 25°C, V_S = +2.7V, R_f = R_g = 5kΩ, R_L = 10kΩ to V_S/2; G = 2; unless otherwise noted.

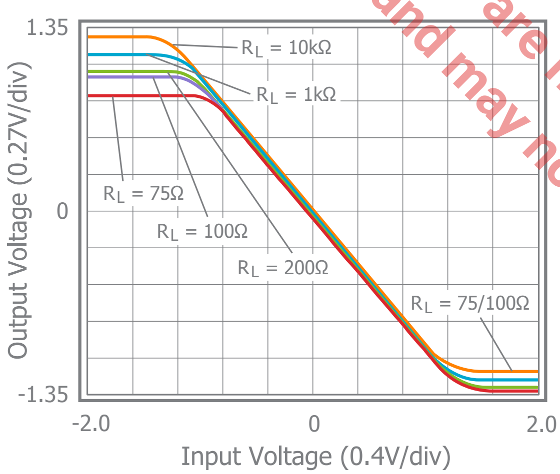
CMRR



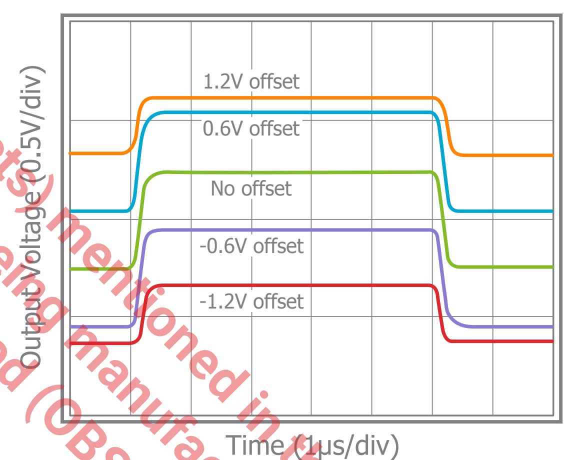
PSRR



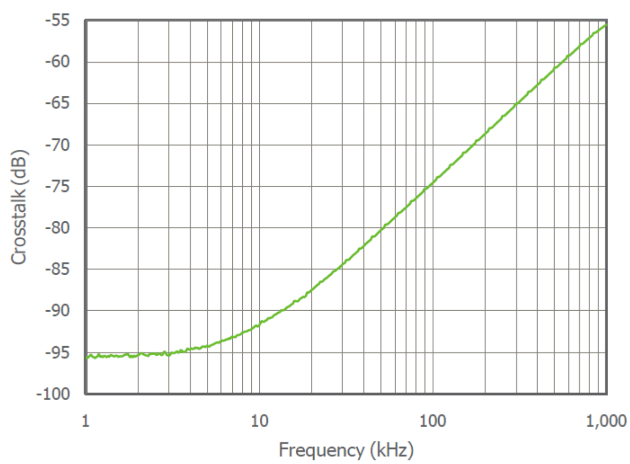
Output Swing vs. Load



Pulse Response vs. Common Mode Voltage



Crosstalk vs. Frequency



Application Information

General Description

The CLCx011 family of amplifiers are single supply, general purpose, voltage-feedback amplifiers. They are fabricated on a complimentary bipolar process, feature a rail-to-rail input and output, and are unity gain stable.

Basic Operation

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

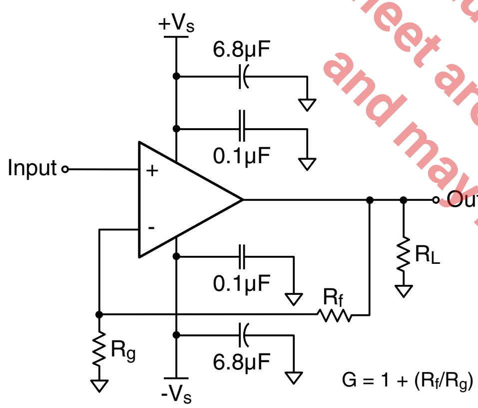


Figure 1: Typical Non-Inverting Gain Circuit

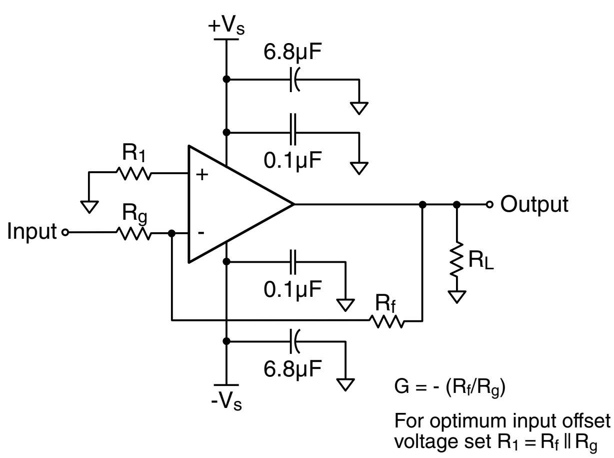


Figure 2: Typical Inverting Gain Circuit

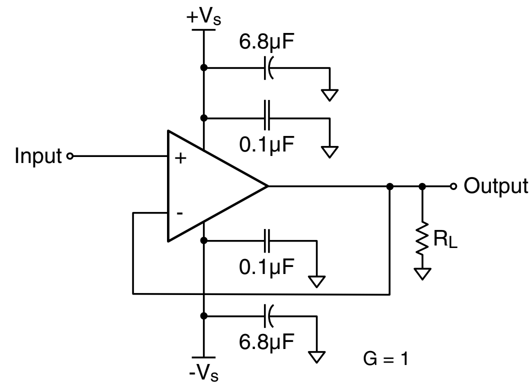


Figure 3: Unity Gain Circuit

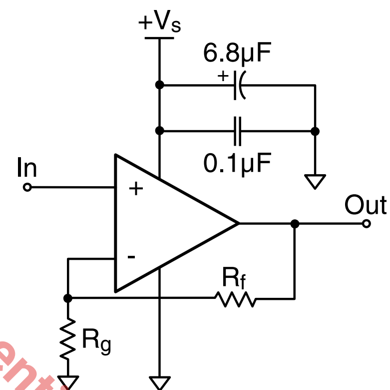


Figure 4: Single Supply Non-Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 10kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMSsupply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{load})_{RMS}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance, $Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{load})_{RMS} = V_{peak} / \sqrt{2}$$

$$(I_{load})_{RMS} = (V_{load})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{Dynamic} = (V_{S+} - V_{load})_{RMS} \times (I_{load})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC2011 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

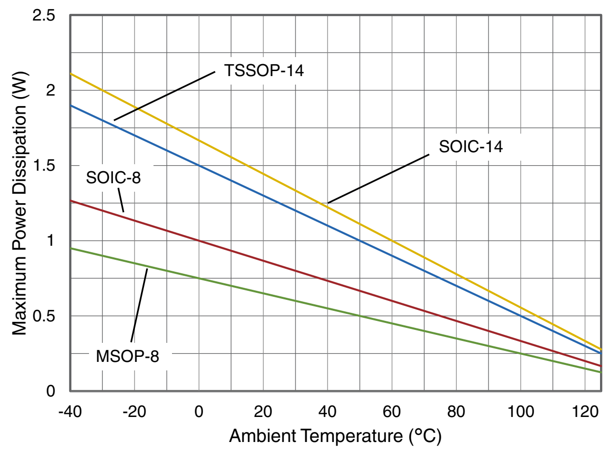


Figure 5. Maximum Power Derating

Input Common Mode Voltage

The common mode input range extends to 250mV below ground and to 250mV above Vs, in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition. If the absolute maximum input voltage (700mV beyond either rail) is exceeded, externally limit the input current to ±5mA as shown in Figure 6.

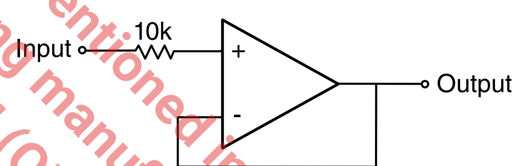


Figure 6. Circuit for Input Current Protection

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 7.

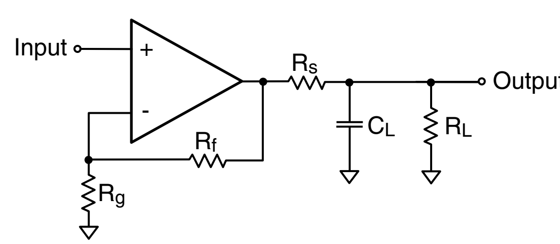


Figure 7. Addition of R_S for Driving Capacitive Loads

Table 1 provides the recommended R_S for various capacitive loads. The recommended R_S values result in approximately <1dB peaking in the frequency response. The Frequency Response vs. CL plot, on page 6, illustrates the response of the CLCx011.

C_L (pF)	R_S (Ω)	-3dB BW (MHz)
10pF	0	2.2
20pF	0	2.4
50pF	0	2.5
100pF	100	2

Table 1: Recommended R_S vs. C_L

For a given load capacitance, adjust R_S to optimize the tradeoff between settling time and bandwidth. In general, reducing R_S will increase bandwidth at the expense of additional overshoot and ringing.

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLCx011 will typically recover in less than 50ns from an overdrive condition. Figure 8 shows the CLC2011 in an overdriven condition.

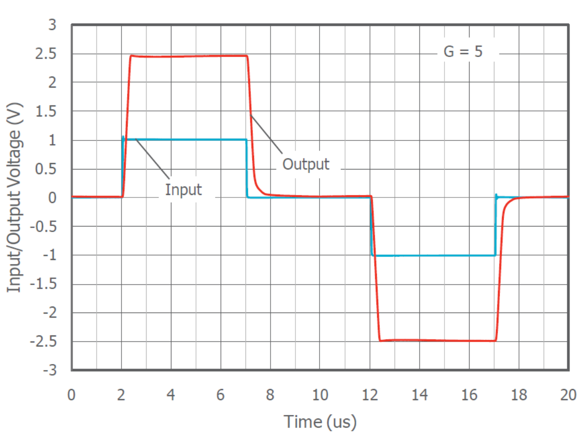


Figure 8: Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board #	Products
CEB006	CLC2011 in SOIC
CEB010	CLC2011 in MSOP
CEB019	CLC4011 in TSSOP
CEB018	CLC4011 in SOIC

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-16 These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

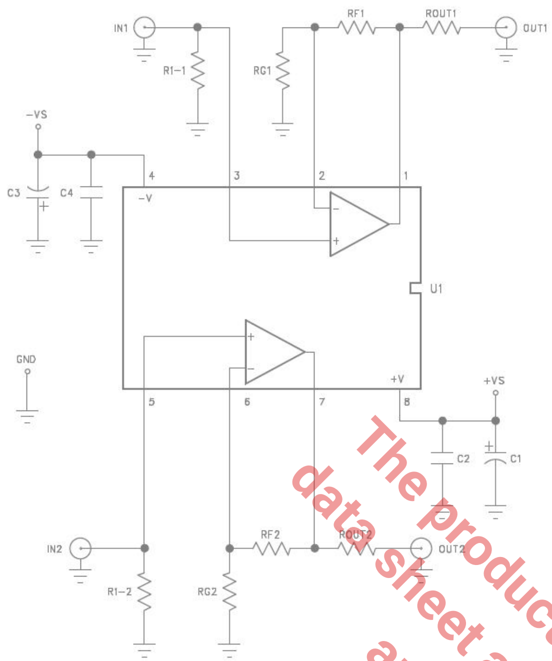


Figure 9. CEB006 & CEB010 Schematic

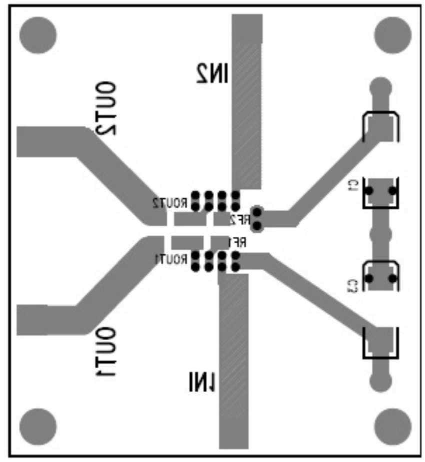


Figure 11. CEB006 Bottom View

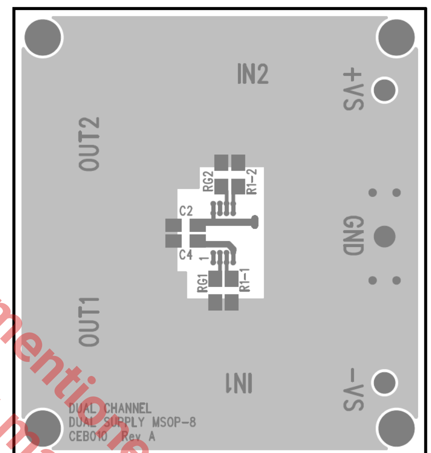


Figure 12. CEB010 Top View

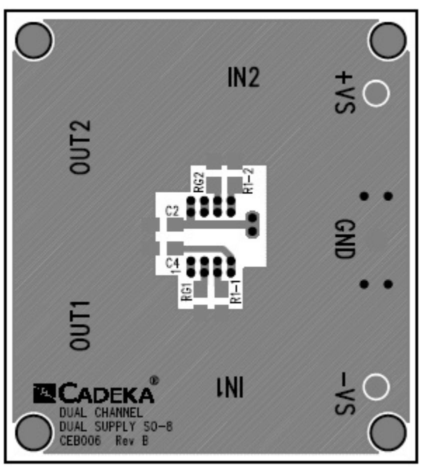


Figure 10. CEB006 Top View

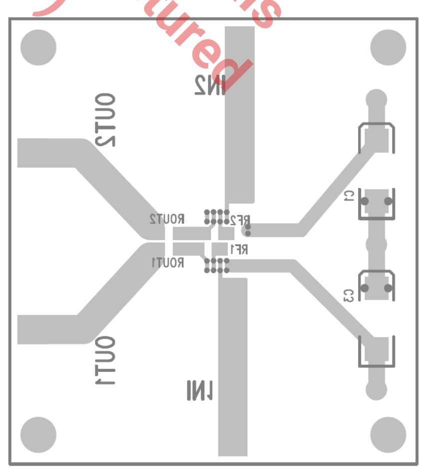


Figure 13. CEB010 Bottom View

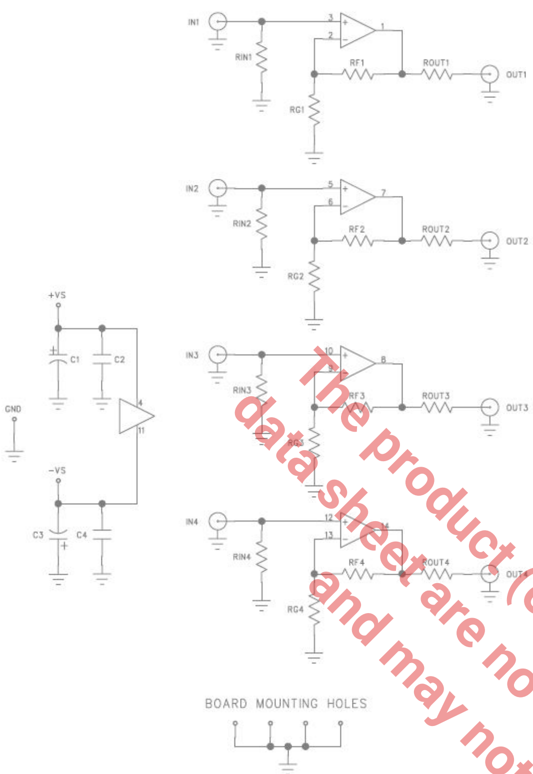


Figure 14. CEB018 Schematic

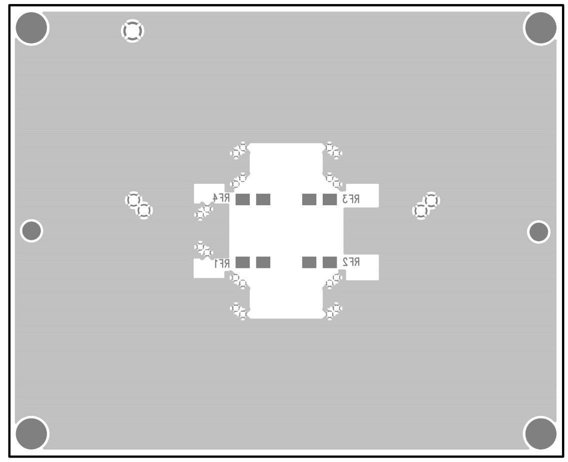


Figure 16. CEB018 Bottom View

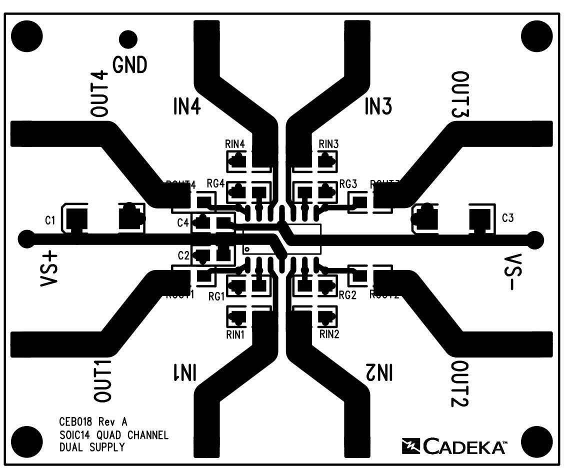
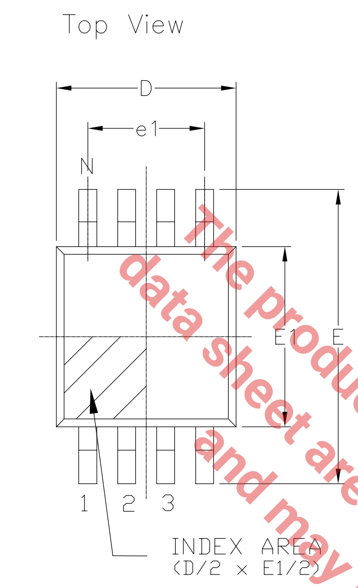


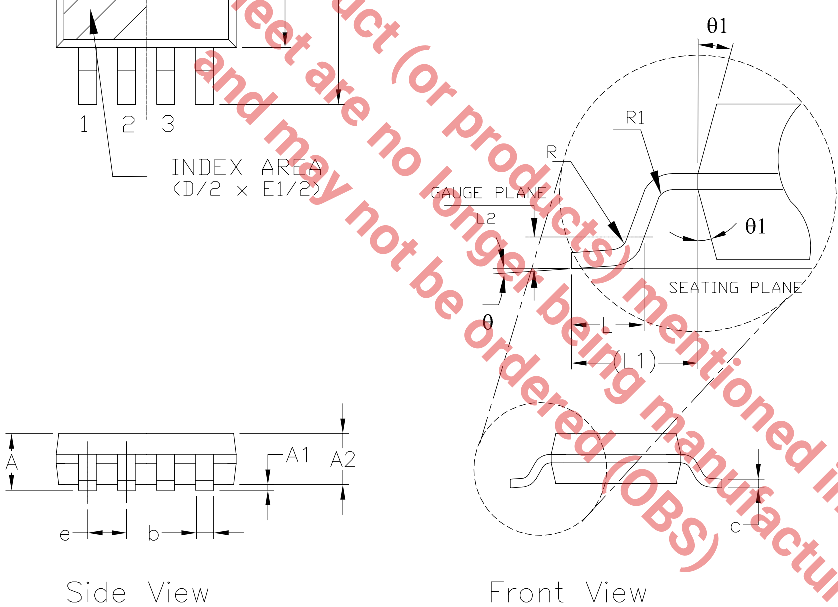
Figure 15. CEB018 Top View

Mechanical Dimensions

MSOP-8

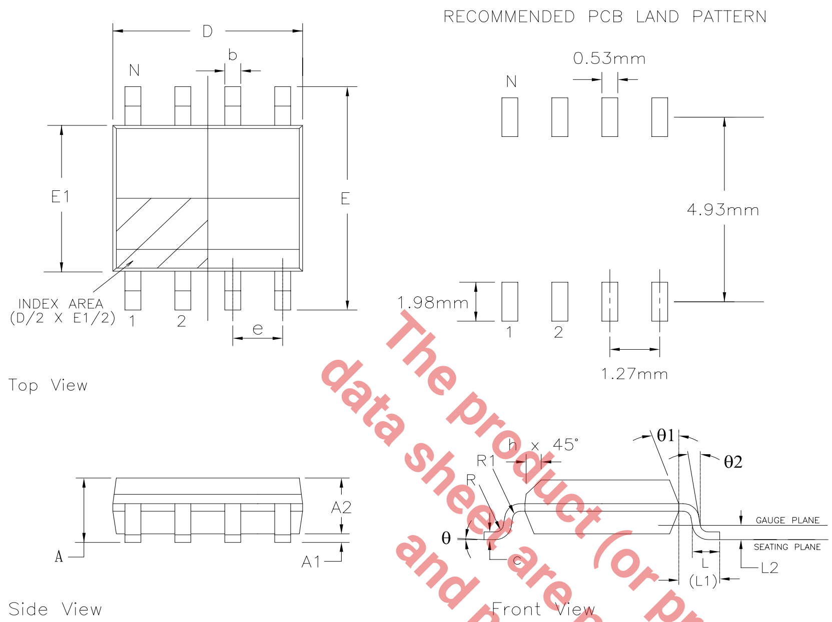
8 Pin MSOP JEDEC MO-187 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.15	0.000	—	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22	—	0.38	0.009	—	0.015
c	0.08	—	0.23	0.003	—	0.009
E	4.90 BSC			0.193 BSC		
E1	3.00 BSC			0.118 BSC		
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	0.95 REF			0.037 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
D	3.00 BSC			0.118 BSC		
N	8			8		





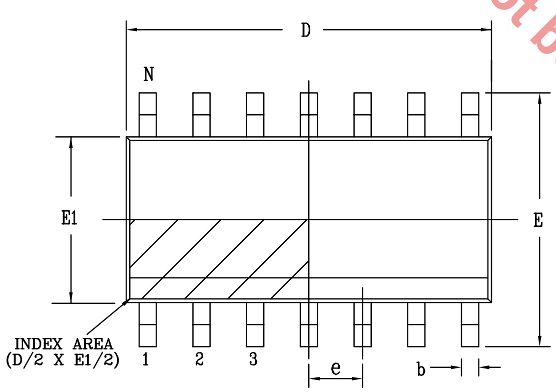
Mechanical Dimensions

SOIC-8 Package

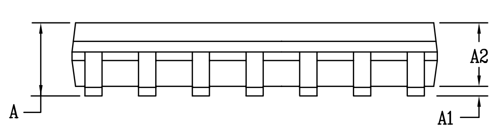


8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		

SOIC-14 Package



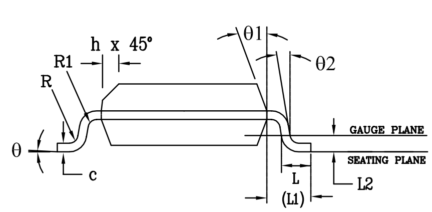
Top View



Side View

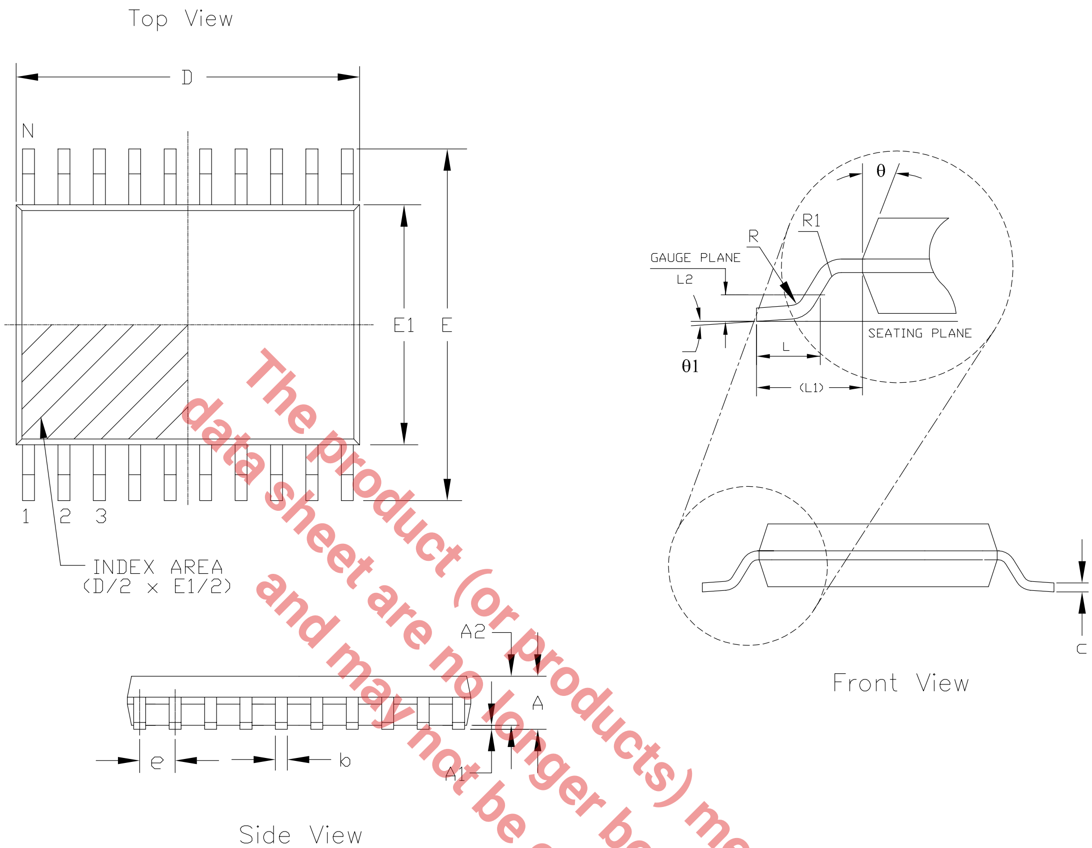
PACKAGE OUTLINE NSOIC .150" BODY JEDEC MS-012						
SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	SEE VARIATIONS					
N	SEE VARIATIONS					

VARIATION D							
VARIATIONS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)			N
	MIN	NOM	MAX	MIN	NOM	MAX	
AA	4.90 BSC			0.193 BSC			8
AB	8.65 BSC			0.341 BSC			14
AC	9.90 BSC			0.390 BSC			16



Front View

TSSOP-14 Package



14 Pin TSSOP JEDEC MO-153 Variation AB-1						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R	0.09	—	—	0.035	—	—
R1	0.09	—	—	0.035	—	—
θ	12° REF			12° REF		
θ1	0°	—	8°	0°	—	8°
D	4.90	5.00	5.10	0.193	0.197	0.200
N	14			14		

Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging
CLC2011 Ordering Information				
CLC2011ISO8X	SOIC-8	Yes	-40°C to +125°C	Tape & Reel
CLC2011ISO8MTR	SOIC-8	Yes	-40°C to +125°C	Mini Tape & Reel
CLC2011ISO8EVB	Evaluation Board	N/A	N/A	N/A
CLC2011IMP8X	MSOP-8	Yes	-40°C to +125°C	Tape & Reel
CLC2011IMP8MTR	MSOP-8	Yes	-40°C to +125°C	Mini Tape & Reel
CLC2011IMP8EVB	Evaluation Board	N/A	N/A	N/A
CLC4011 Ordering Information				
CLC4011ISO14X	SOIC-14	Yes	-40°C to +125°C	Tape & Reel
CLC4011ISO14MTR	SOIC-14	Yes	-40°C to +125°C	Mini Tape & Reel
CLC4011ISO14EVB	Evaluation Board	N/A	N/A	N/A
CLC4011ITP14X	TSSOP-14	Yes	-40°C to +125°C	Tape & Reel
CLC4011ITP14MTR	TSSOP-14	Yes	-40°C to +125°C	Mini Tape & Reel
CLC4011ITP14EVB	Evaluation Board	N/A	N/A	N/A

Moisture sensitivity level for all parts is MSL-1. Mini tape and reel quantity is 250.

Revision History

Revision	Date	Description
1D (ECN 1504-01)	January 19, 2015	Reformat into Exar data sheet template. Updated PODs and thermal resistance numbers. Updated ordering information table to include MTR and EVB part numbers. Increased operating temperature to +125°C.

For Further Assistance:

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