Data Sheet

COMLINEAR® CLC2058

Dual 4V to 36V Amplifier

FEATURES

- Unity gain stable
- 100dB voltage gain
- 5.5MHz gain bandwidth product
- 0.5MΩ input resistance
- 100dB power supply rejection ratio
- 95dB common mode rejection ratio
- 4V to 36V single supply voltage range
- ±2V to ±18V dual supply voltage range
- Gain and phase match between amps
- CLC2058: improved replacement for NJM4558 and MC1458
- CLC2058: Pb-free SOIC-8

APPLICATIONS

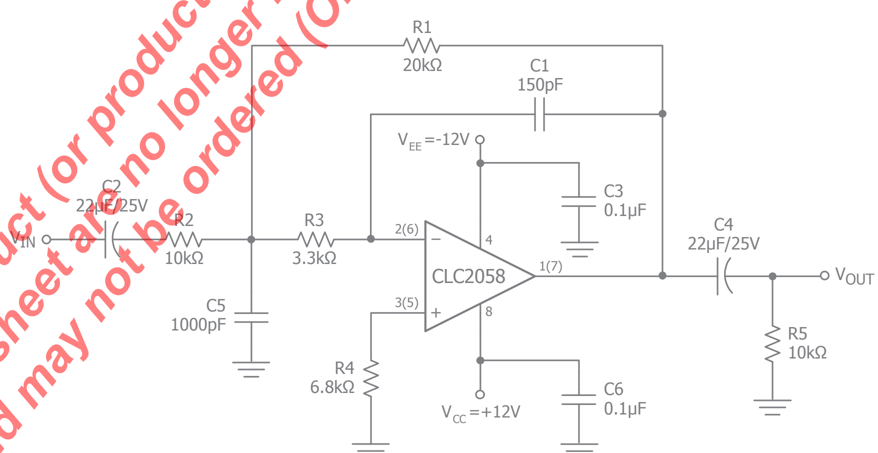
- Active Filters
- Audio Amplifiers
- Audio AC-3 Decoder Systems
- General purpose dual ampliifer

General Description

The COMLINEAR CLC2058 is a dual voltage feedback amplifier that is internally frequency compensated to provide unity gain stability. The CLC2058 offers 3.5MHz of bandwidth at a gain of 2. The CLC2058 also features high gain, low input voltage noise, high input resistance, and superb channel separation making it well suited for audio filter applications in set-top-boxes, DVD players, and televisions.

The COMLINEAR CLC2058 is designed to operate over a wide power supply voltage range, ±2V to ±18V (4V to 36V). It utilizes an industry standard dual amplifier pin-out and is available in a Pb-free, RoHS compliant SOIC-8 package.

Typical Application - 2nd Order Low-Pass Audio Filter

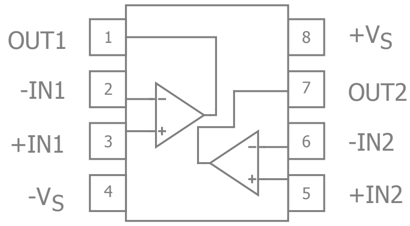


Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC2058ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

CLC2058 Pin Configuration



CLC2058 Pin Description

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	40 (±20)	V
Differential Input Voltage		60 (±30)	V
Input Voltage		30 (±15)	V
Power Dissipation (T_A = 25°C) - SOIC-8		500	mW

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
SOIC-8		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	4 (±2)		36 (±18)	V

Electrical Characteristics

T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, R_f = R_g =2kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}, V_S = 5V, R_f = 0		4.62		MHz
		G = +1, V_{OUT} = 0.2V_{pp}, V_S = 30V, R_f = 0		4.86		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}, V_S = 5V		3.49		MHz
		G = +1, V_{OUT} = 0.2V_{pp}, V_S = 30V		3.55		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 1V_{pp}, V_S = 5V		1.25		MHz
		G = +2, V_{OUT} = 2V_{pp}, V_S = 30V		0.74		MHz
GBWP	Gain-Bandwidth Product			5.5		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%), V_S = 5V		100		ns
		V_{OUT} = 0.2V step; (10% to 90%), V_S = 30V		98		ns
OS	Overshoot	V_{OUT} = 0.2V step		12		%
SR	Slew Rate	2V step, V_S = 5V		2.6		V/µs
		4V step, V_S = 30V		2.8		V/µs
Distortion/Noise Response						
THD+N	Total Harmonic Distortion plus Noise	V_{OUT} = 1V_{RMS}, f = 1kHz, G = 2, R_L = 10kΩ, V_S = 30V		0.002		%
e_n	Input Voltage Noise	> 1kHz, V_S = 5V		10		nV/√Hz
		> 1kHz, V_S = 30V		10		nV/√Hz
X_{TALK}	Crosstalk	Channel-to-channel, 500kHz		65		dB
DC Performance						
V_{IO}	Input Offset Voltage (1)	V_S = 5V to 30V		1	5	mV
I_b	Input Bias Current (1)	V_{CM} = 0V		70	400	nA
I_{OS}	Input Offset Current (1)	V_{CM} = 0V		10	100	nA
PSRR	Power Supply Rejection Ratio (1)	DC, R_S ≤ 10kΩ	80	100		dB
A_{OL}	Open-Loop Gain (1)	R_L = ≥2kΩ, V_{OUT} = 1V to 11V	85	100		dB
I_S	Supply Current (1)	Total, R_L = ∞		2.5	4.5	mA
Input Characteristics						
CMIR	Common Mode Input Range (1,3)	+V_S = 30V	±12			V
CMRR	Common Mode Rejection Ratio (1)	DC, R_S ≤ 10kΩ	70	95		dB
R_{IN}	Input Resistance			0.5		MΩ
Output Characteristics						
R_{OUT}	Output Resistance			45		Ω
V_{OUT}	Output Voltage Swing (1)	R_L = 2kΩ	±10	±13		V
		R_L = 10kΩ	±12	±14		V
I_{SOURCE}	Output Current, Sourcing	V_{IN+} = 1V, V_{IN-} = 0V, V_{OUT} = 2V		35		mA
I_{SINK}	Output Current, Sinking	V_{IN+} = 0V, V_{IN-} = 1V, V_{OUT} = 2V		60		mA

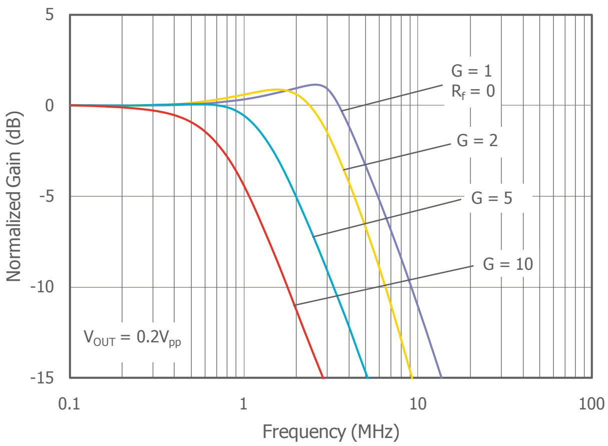
Notes:

1. 100% tested at 25°C at V_S = ±15V.

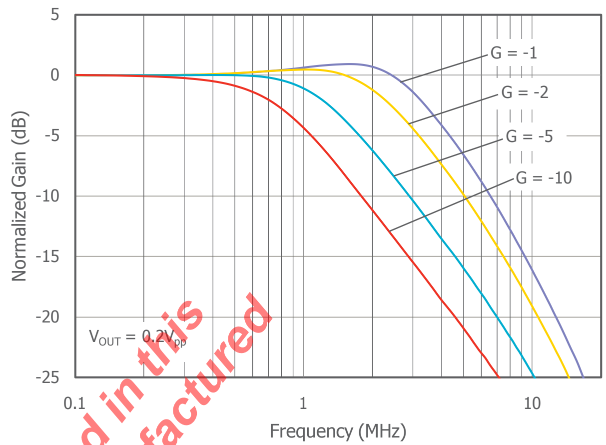
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, $R_f = R_g$ =2kΩ, R_L = 2kΩ to $V_S/2$, G = 2; unless otherwise noted.

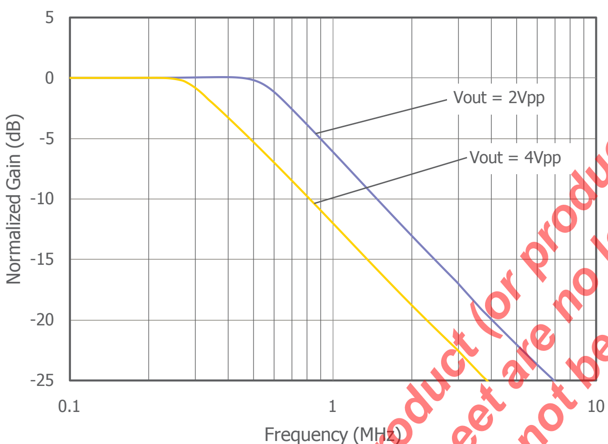
Non-Inverting Frequency Response



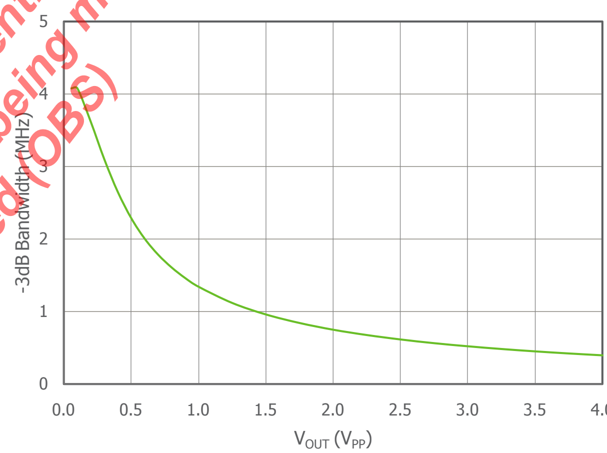
Inverting Frequency Response



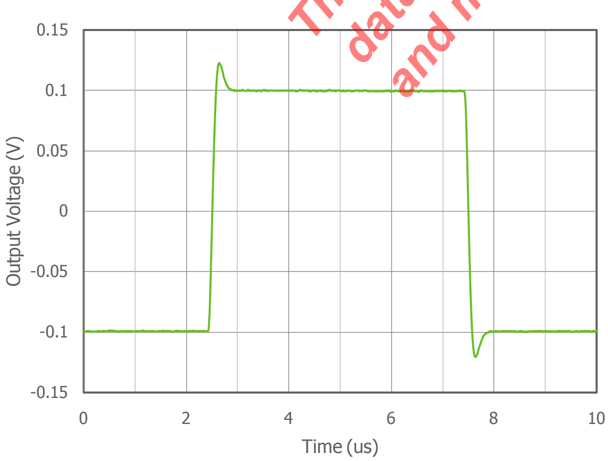
Large Signal Frequency Response



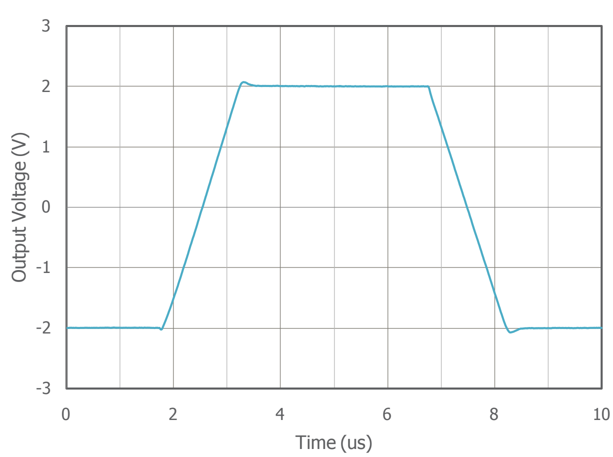
-3dB Bandwidth vs. V_{OUT}



Small Signal Pulse Response



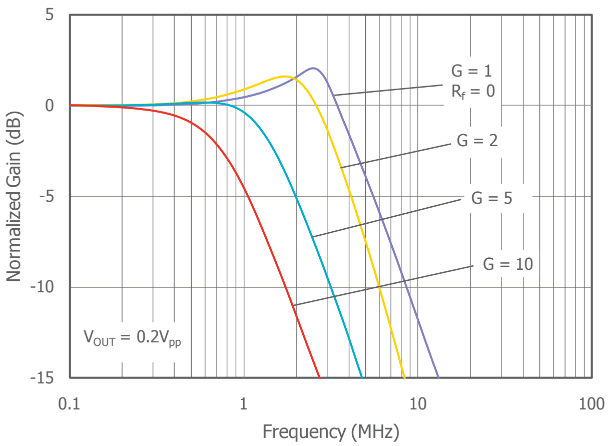
Large Signal Pulse Response



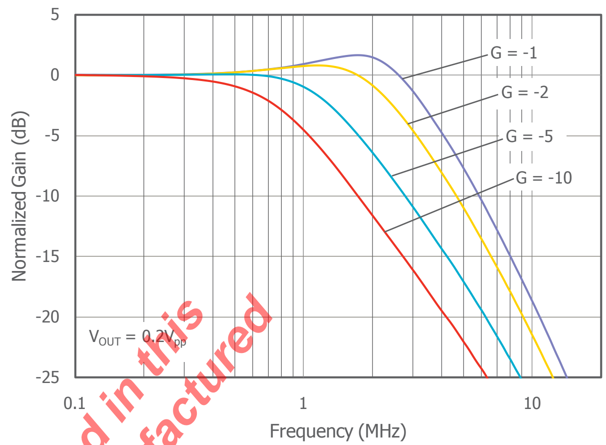
Typical Performance Characteristics

$T_A = 25°C$, $+V_S = +5V$, $-V_S = GND$, $R_f = R_g = 2k\Omega$, $R_L = 2k\Omega$ to $V_S/2$, $G = 2$; unless otherwise noted.

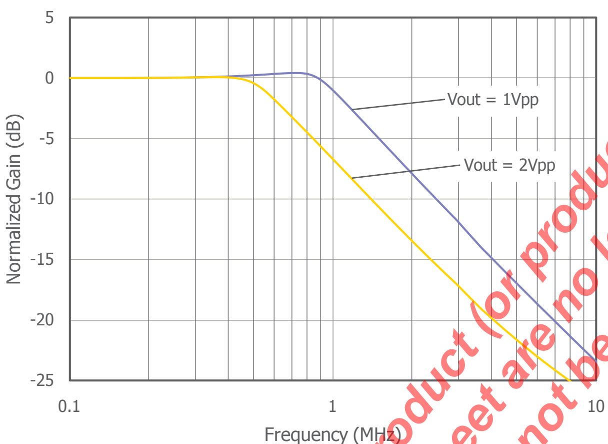
Non-Inverting Frequency Response



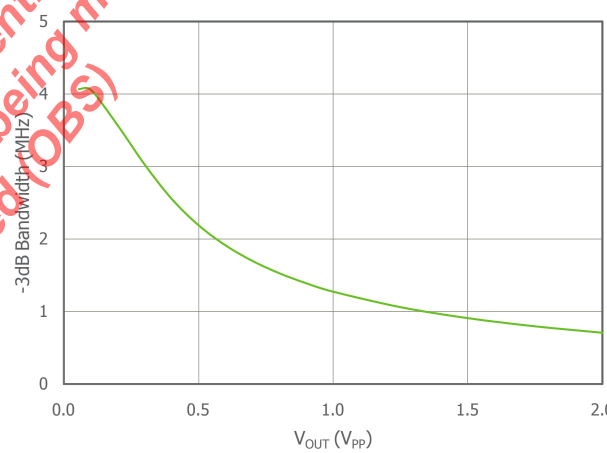
Inverting Frequency Response



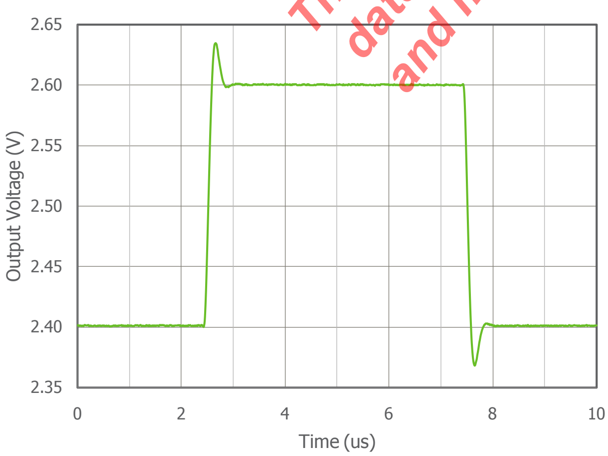
Large Signal Frequency Response



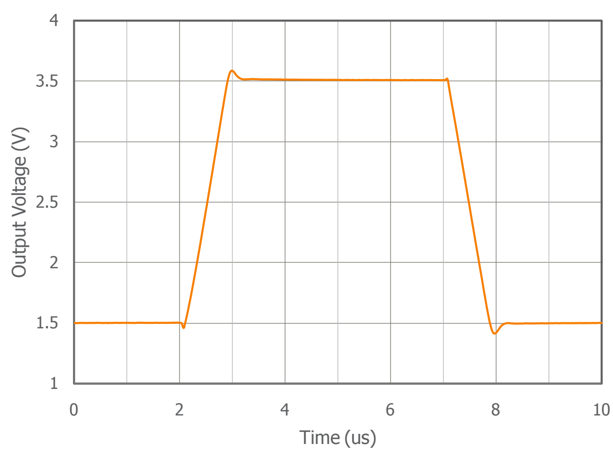
-3dB Bandwidth vs. V_{OUT}



Small Signal Pulse Response



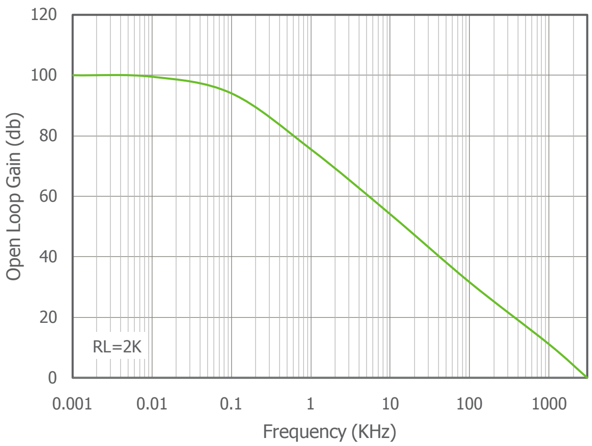
Large Signal Pulse Response



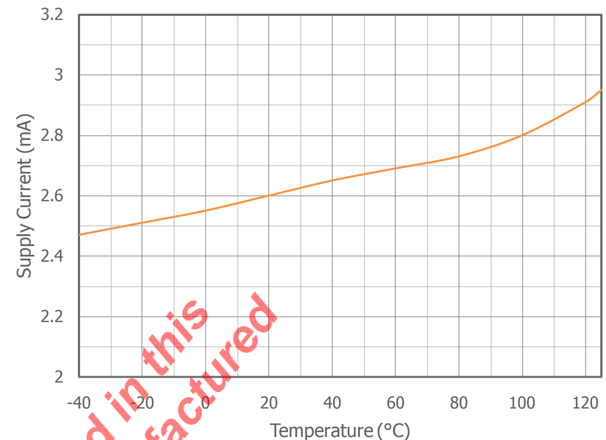
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, R_f = R_g =2kΩ, R_L = 2kΩ to $V_S/2$, G = 2; unless otherwise noted.

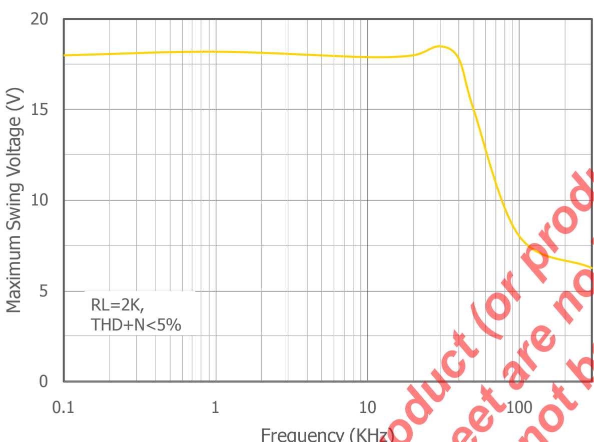
Open Loop Voltage Gain vs. Frequency



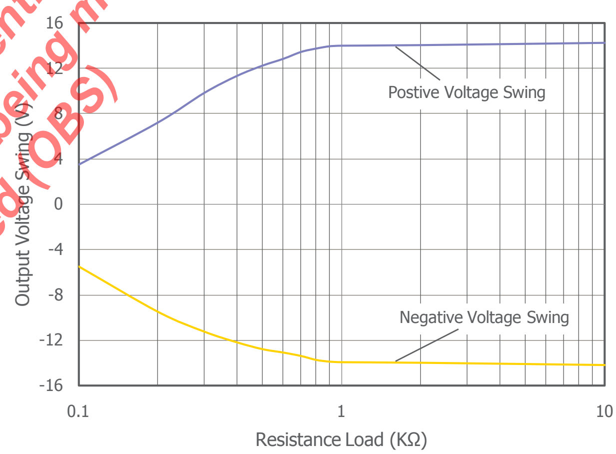
Supply Current vs. Temperature



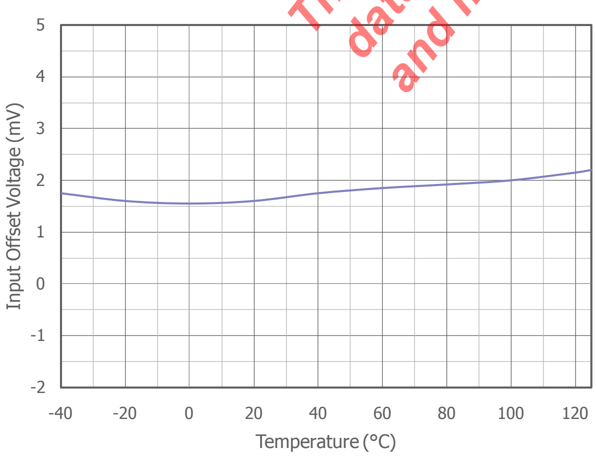
Maximum Output Voltage Swing vs. Frequency



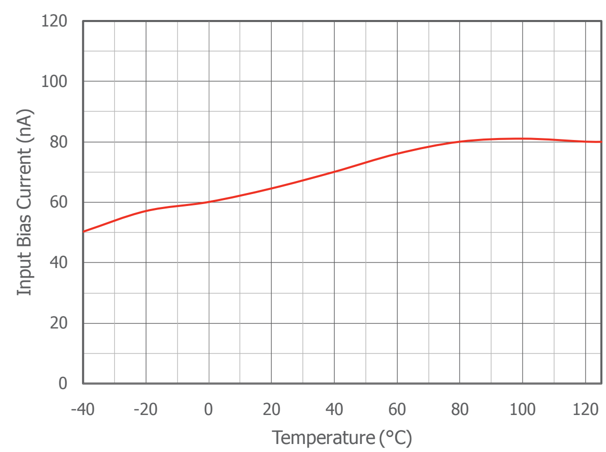
Maximum Output Voltage Swing vs. R_L



Input Offset Voltage vs. Temperature



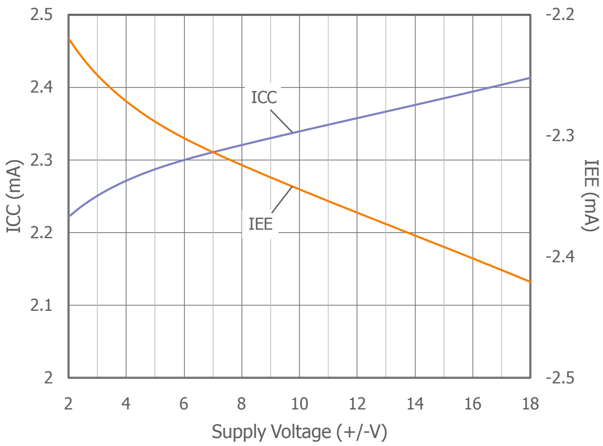
Input Bias Current vs. Temperature



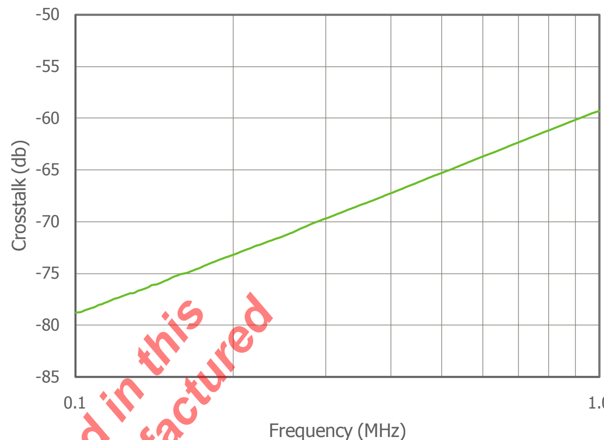
Typical Performance Characteristics

T_A = 25°C, $+V_S$ = +15V, $-V_S$ = -15V, R_f = R_g =2kΩ, R_L = 2kΩ to $V_S/2$, G = 2; unless otherwise noted.

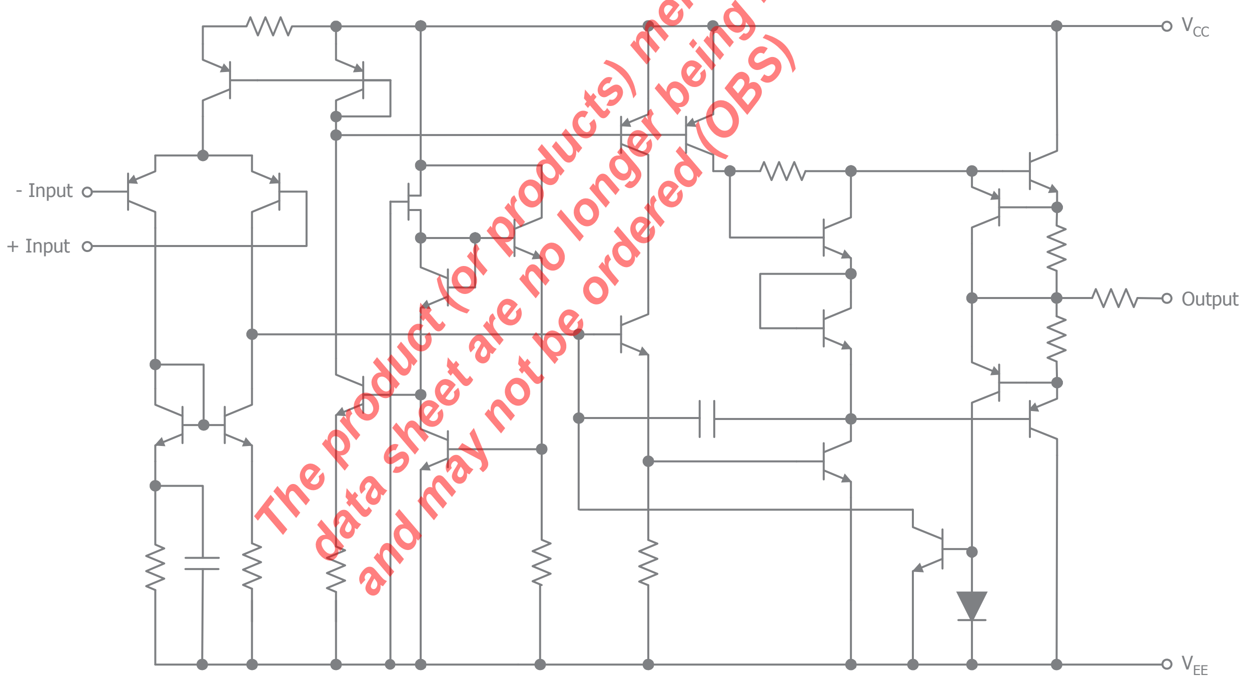
Supply Voltage vs. Supply Current



Crosstalk vs. Frequency



Functional Block Diagram



Application Information

Basic Operation

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations.

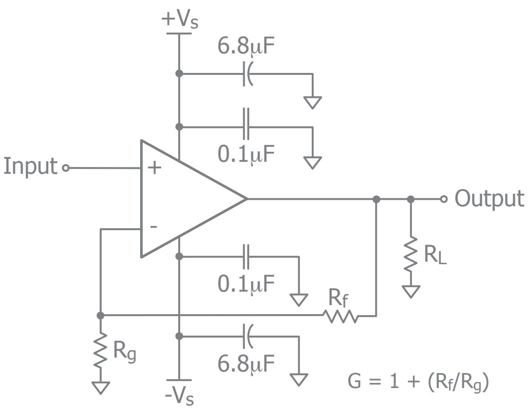


Figure 1. Typical Non-Inverting Gain Circuit

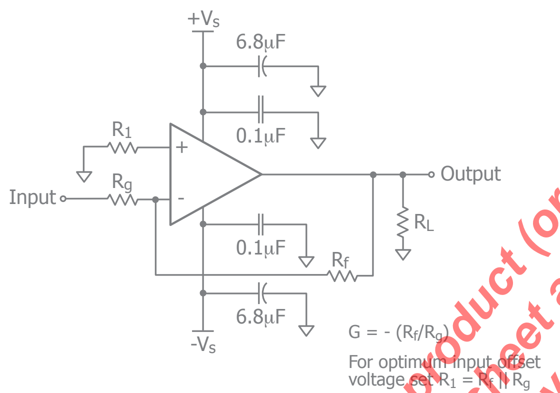


Figure 2. Typical Inverting Gain Circuit

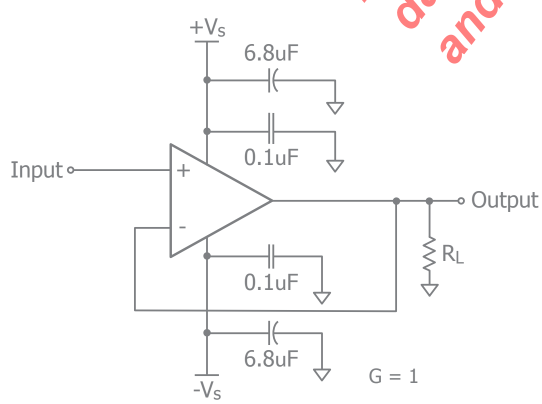


Figure 3. Unity Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2k ohm load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}{}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in figure 3 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$

$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

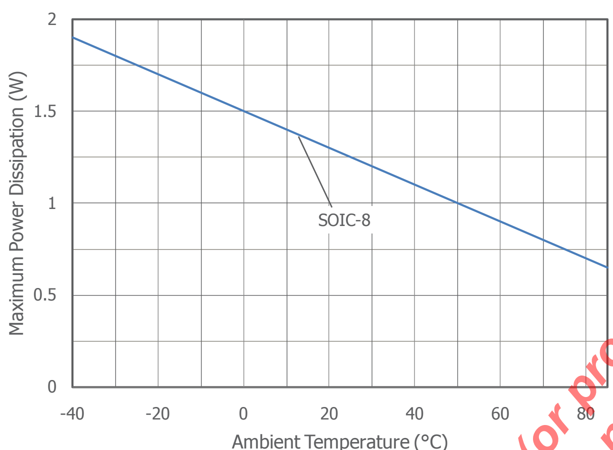


Figure 4. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 5.

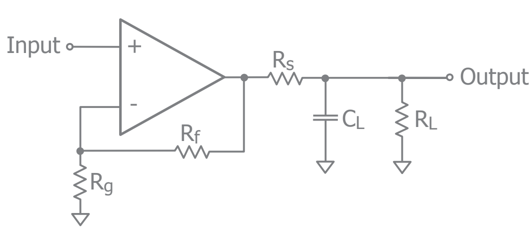


Figure 5. Addition of R_S for Driving Capacitive Loads

Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC2058 will typically recover in less than 30ns from an overdrive condition. Figure 6 shows the CLC2058 in an overdriven condition.

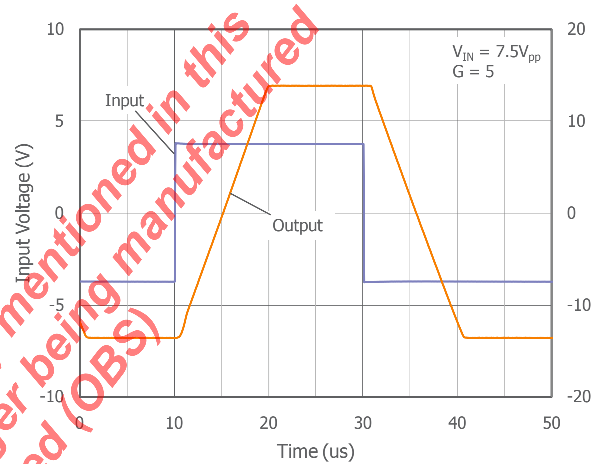


Figure 6. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.1μF ceramic capacitors for power supply decoupling
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.1μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB006	CLC2058

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 7-9. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.

2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

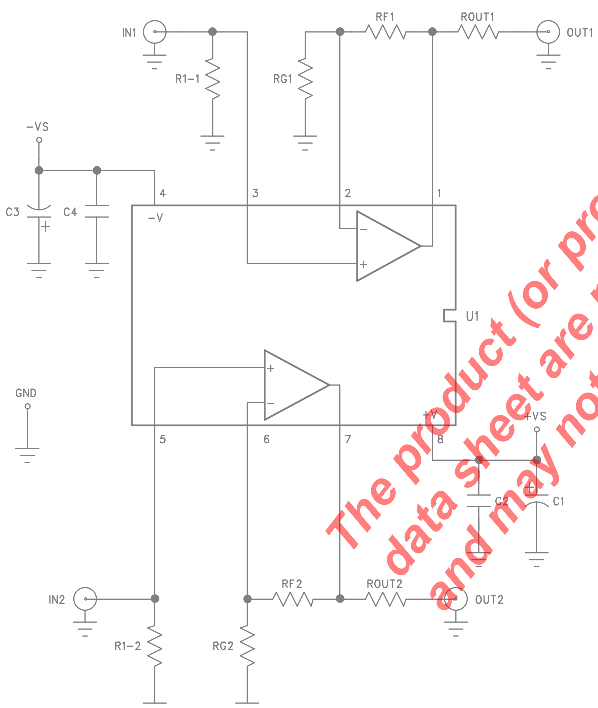


Figure 7. CEB006 Schematic

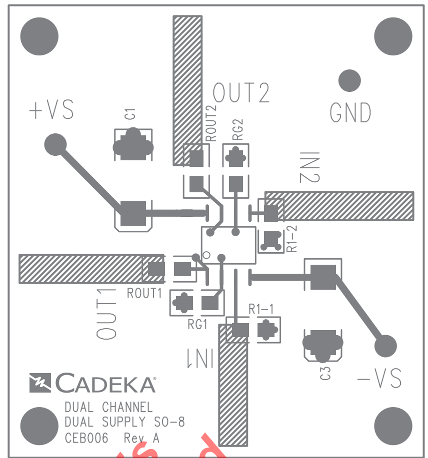


Figure 8. CEB006 Top View

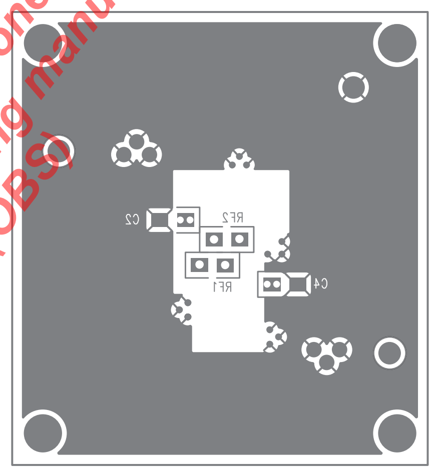


Figure 9. CEB006 Bottom View

Typical Applications

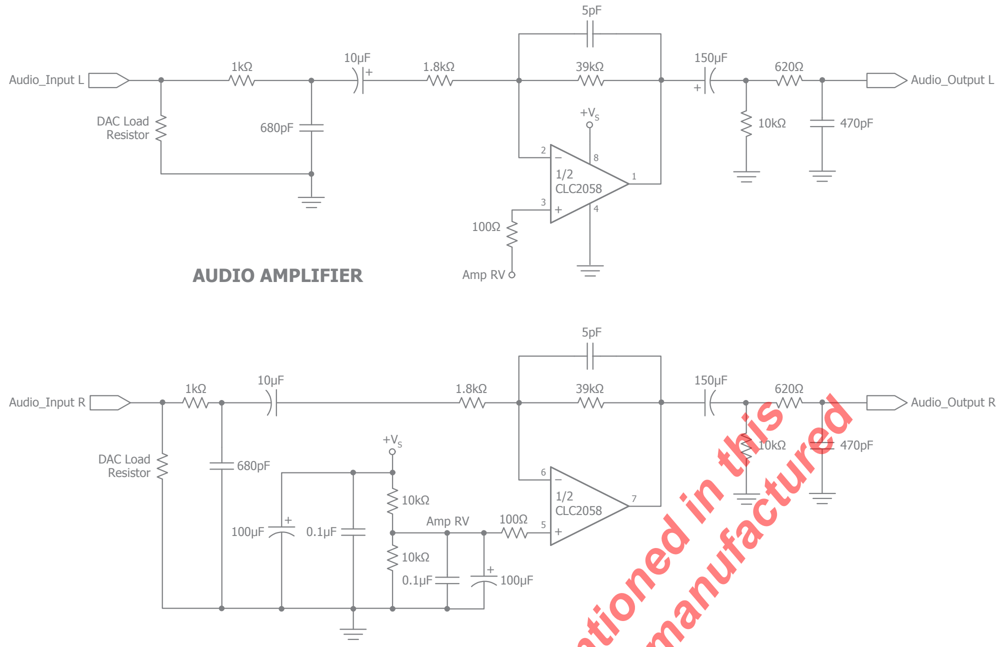


Figure 10: Typical Circuit for Filtering and Driving Audio in STB or DVD Player Applications

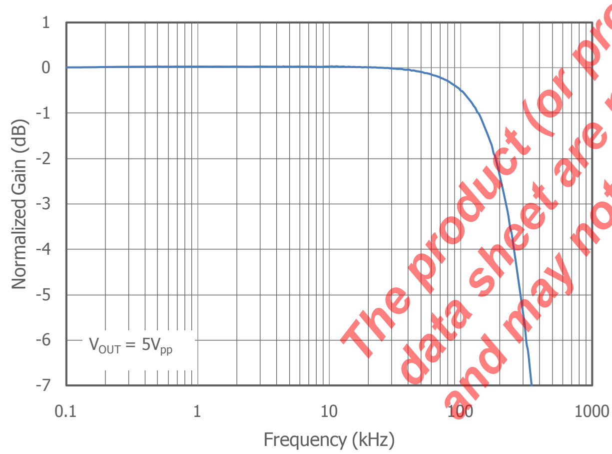


Figure 11: AC Reponse of Figure 10 (V_S=10V, R_L=630Ω)

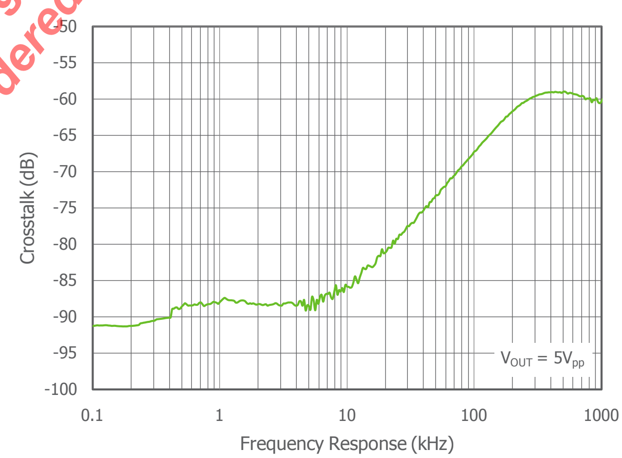
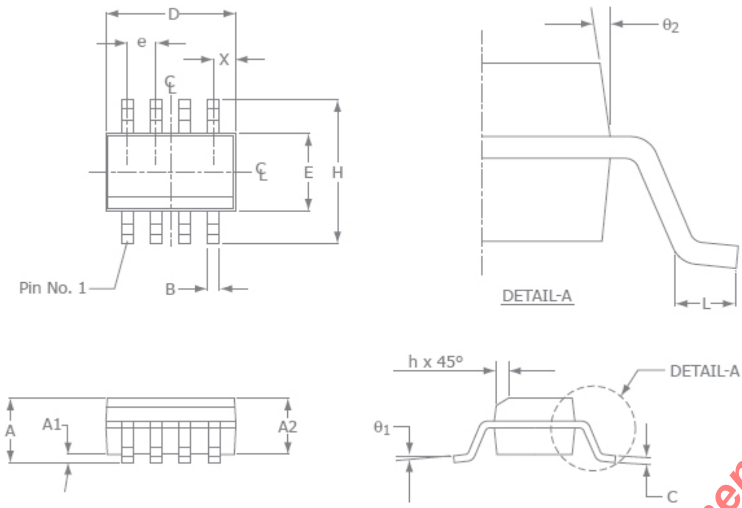


Figure 12: Cross-Talk Performance of Figure 10 (V_S=10V, R_L=630Ω)

Mechanical Dimensions

SOIC-8 Package



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ1	0°	8°
X	0.55 ref	
θ2	7° BSC	

NOTE:
1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For Further Assistance:

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A New Direction in Mixed-Signal