Data Sheet

CDK3405

8-bit, 180MSPS, Triple Video DAC

FEATURES

- 8-bit resolution, 180MSPS
- ±2.5% gain matching
- ±0.5% linearity error
- Sync and blank controls
- $1.0V_{pp}$ video into 37.5Ω or 75Ω load
- Internal bandgap voltage reference
- Low glitch energy
- Single +3.3V power supply

APPLICATIONS

- Video signal conversion
  - RGB
  - YC_BC_R
  - Composite, Y, C
- Multimedia systems
- Image processing
- PC Graphics

General Description

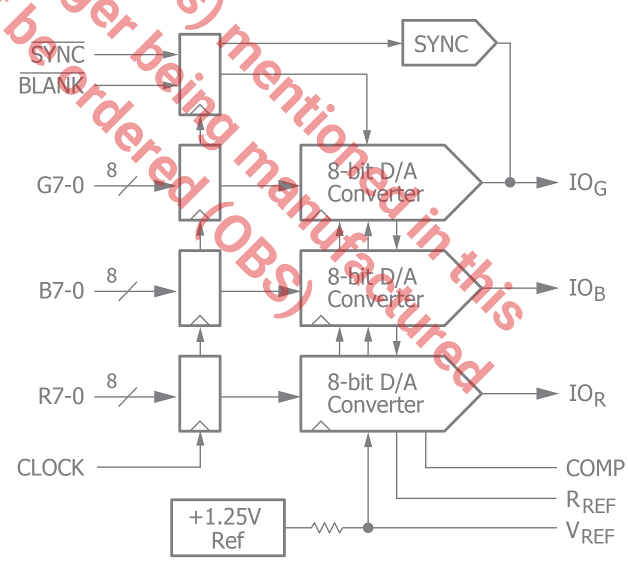
CDK3405 is a low-cost triple D/A converter that is tailored to fit graphics and video applications where speed is critical.

CMOS-level inputs are converted to analog current outputs that can drive 25-37.5Ω loads corresponding to doubly-terminated 50-75Ω loads. A sync current following $\overline{\text{SYNC}}$ input timing is added to the IO_G output. $\overline{\text{BLANK}}$ will override RGB inputs, setting IO_G, IO_B and IO_R currents to zero when $\overline{\text{BLANK}}$ = L. Although appropriate for many applications, the internal 1.25V reference voltage can be overridden by the V_{REF} input.

Few external components are required, just the current reference resistor, current output load resistors, bypass capacitors, and decoupling capacitors.

Package is a 48-lead TQFP. Fabrication technology is CMOS. Performance is guaranteed from -40°C to +125°C.

Block Diagram



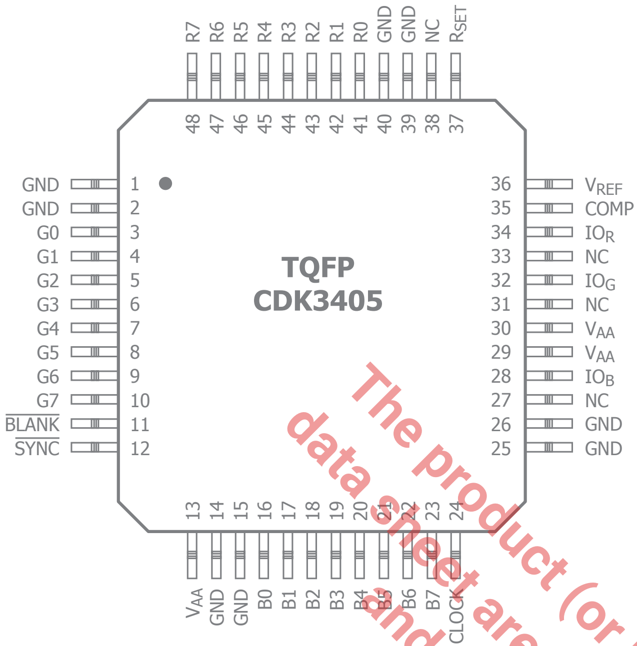
Ordering Information

Part Number	Package	Pb-Free	RoHS Compliant	Operating Temp Range	Packaging Method	Package Quantity
CDK3405CTQ48	TQFP-48	Yes	Yes	0°C to +70°C	Tray	250
CDK3405ATQ48	TQFP-48	Yes	Yes	-40°C to +125°C	Tray	250

Moisture sensitivity level for all parts is MSL-3.

Pin Configuration

TQFP-48



Pin Assignments

Pin No.	Pin Name	Description
Clock and Pixel I/O		
24	CLK	Clock Input
41-48	R7-0	Red Pixel Data Inputs
3-10	G7-0	Green Pixel Data Inputs
16-23	B7-0	Blue Pixel Data Inputs
Controls		
12	$\overline{\text{SYNC}}$	Sync Pulse Input
11	$\overline{\text{BLANK}}$	Blanking Input
Video Outputs		
34	IOR	Red Current Output
32	IOG	Green Current Output
28	IOB	Blue Current Output
Voltage Reference		
36	V_{REF}	Input for DACs or Voltage Reference Output (1.25V)
37	R_{SET}	Current-Setting Resistor
35	COMP	Compensation Capacitor
Power and Ground		
13, 29, 30	V_{AA}	Analog Power Supply
1, 2, 14, 15, 25, 26, 39, 40	GND	Ground
27, 31, 33	NC	No Connect

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

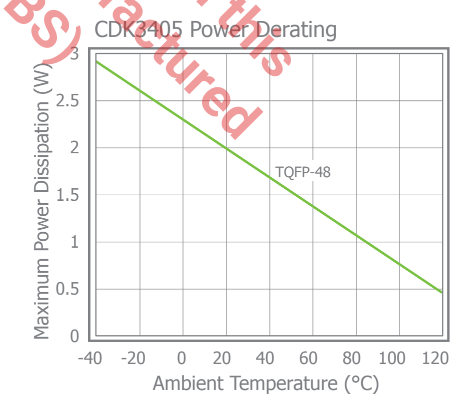
Parameter	Min	Max	Unit
Power Supply Voltage			
V_{AA} (Measured to GND)	-0.5	4.0	V
Digital Inputs			
Applied Voltage (measured to GND)[2]	-0.5	V_{AA} + 0.5	V
Forced Current[3,4]	-5.0	5.0	mA
Analog Inputs			
Applied Voltage (measured to GND)[2]	-0.5	V_{AA} + 0.5	V
Forced Current[3,4]	-10.0	10.0	mA
Analog Outputs			
Applied Voltage (measured to GND)[2]	-0.5	V_{AA} + 0.5	V
Forced Current[3,4]	-60.0	60.0	mA
Short Circuit Duration (single output in HIGH state to GND)		unlimited	sec

Reliability Information

Parameter	Min	Max	Unit
Temperature			
Operating, Ambient	-40	125	°C
Junction		150	°C
Lead Soldering (10 seconds)		300	°C
Vapor Phase Soldering (1 minute)		220	°C
Storage	-65	150	°C
Package Thermal Resistance (θ_{JA})	65		°C/W

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.



ESD Protection

Parameter	TQFP-48
Human Body Model (HBM)	TBD
Charged Device Model (CDM)	TBD

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{AA}	Power Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage, External	1.0	1.25	1.5	V
C_C	Compensation Capacitor		0.1		µF
R_L	Output Load		37.5		Ω
T_A	Ambient Temperature, Still Air	-40		+125	°C

Electrical Characteristics

(T_A = 25°C, V_{AA} =3.3V, V_{REF} = 1.25V, R_L = 37.5Ω, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Power Supply Current	T_A = 25°C (1)		80	85	mA
		T_A = -40°C to +125°C (2)			95	mA
PD	Total Power Dissipation(2)	T_A = -40°C to +125°C			300	mW
Digital Inputs						
V_{IH}	Input Voltage, HIGH (1)	T_A = -40°C to +125°C	2.5			V
V_{IL}	Input Voltage, LOW (1)	T_A = -40°C to +125°C			0.8	V
I_{IH}	Input Current, HIGH (1)	T_A = -40°C to +125°C	-1		1	μA
I_{IL}	Input Current, LOW (1)	T_A = -40°C to +125°C	-1		1	μA
C_I	Input Capacitance			4		pF
Analog Outputs						
	Output Current (1)				30	mA
R_O	Output Resistance			40		kΩ
C_O	Output Capacitance			7		pF
Reference Output						
V_{REF}	Reference Voltage Output (1)	T_A = -40°C to +125°C	1.135	1.25	1.365	V

Notes:

1. 100% tested at 25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

Switching Characteristics

(T_A = 25°C, V_{AA} =3.3V, V_{REF} = 1.25V, R_L = 37.5Ω, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clock Input						
	Conversion Rate (1)	T_A = -40°C to +125°C			180	MSPS
t_{PWH}	Pulse-width HIGH (2)	T_A = -40°C to +125°C	2			ns
t_{PWL}	Pulse-width LOW (2)	T_A = -40°C to +125°C	2			ns
Data Inputs						
t_S	Setup	T_A = 25°C (1)	1.5			ns
		T_A = -40°C to +125°C (2)	2			ns
t_H	Hold	T_A = 25°C (1)			0.6	ns
		T_A = -40°C to +125°C (2)			0.6	ns
Data Outputs, with 50Ω doubly terminated load						
t_D	Clock to Output Delay	T_A = -40°C to +125°C		1.6		ns
t_R	Output Risetime	T_A = -40°C to +125°C		0.6		ns
t_F	Output Falltime	T_A = -40°C to +125°C		0.4		ns
t_{SET}	Settling Time			2.5		ns
t_{SKEW}	Output Skew			0.3		ns

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

DC Performance

(T_A = 25°C, V_{AA} =3.3V, V_{REF} = 1.25V, R_L = 37.5Ω, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8			bits
INL	Integral Linearity Error	T_A = 25°C (1)	-0.5		0.5	LSB
		T_A = -40°C to +125°C (2)	-0.5		0.5	LSB
DNL	Differential Linearity Error	T_A = 25°C (1)	-0.5		0.5	LSB
		T_A = -40°C to +125°C (2)	-0.5		0.5	LSB
	Offset Error	T_A = -40°C to +125°C (2)			0.01	%FS
	Gain Matching Error	T_A = -40°C to +125°C (1)	-2.5		2.5	%FS
	Absolute Gain Error	T_A = -40°C to +125°C (1)	-3.5		3.5	%FS
	Full-Scale Output Current	T_A = 25°C (1)	18.0	18.7	19.4	mA
		T_A = -40°C to +125°C (2)	18.0	18.7	19.4	mA
		T_A = -40°C to +125°C , With internal reference. Trim RSET to calibrate full-scale current.		18.7		mA
PSRR	Power Supply Rejection Ratio	T_A = -40°C to +125°C (2)	-0.01	0	0.01	%/%

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

AC Performance

(T_A = 25°C, V_{AA} = 3.3V, V_{REF} = 1.25V, R_L = 37.5Ω, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Analog Outputs						
	Glitch Energy			20		pVsec
	DAC-to-DAC Crosstalk			30		dB
	Data Feedthrough			50		dB
	Clock Feedthrough			60		dB

Notes:

1. 100% production tested at +25°C.
2. Parameter is guaranteed (but not tested) by design and characterization data.

Table 1. Output Voltage vs. Input Code, $\overline{SYNC}$ and $\overline{BLANK}$, V_{REF} = 1.25V, R_{REF} = 348Ω, R_L = 37.5Ω

RGB7-0 (MSB...LSB)	BLUE AND RED			GREEN		
	$\overline{SYNC}$	$\overline{BLANK}$	V_{OUT} (V)	$\overline{SYNC}$	$\overline{BLANK}$	V_{OUT} (V)
1111 1111	1	1	0.700	1	1	1.007
1111 1111	0	1	0.700	0	1	0.700
1111 1110	1	1	0.697	1	1	1.004
1111 1101	1	1	0.695	1	1	1.001
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1000 0000	1	1	0.351	1	1	0.658
0111 1111	1	1	0.349	1	1	0.656
0111 1111	0	1	0.349	0	1	0.349
•	•	•	•	•	•	•
•	•	•	•	•	•	•
0000 0010	1	1	0.005	1	1	0.312
0000 0001	1	1	0.003	1	1	0.310
0000 0000	1	1	0.000	1	1	0.307
0000 0000	0	1	0.000	0	1	0.000
XXXX XXXX	1	0	0.000	1	0	0.307
XXXX XXXX	0	0	0.000	0	0	0.000

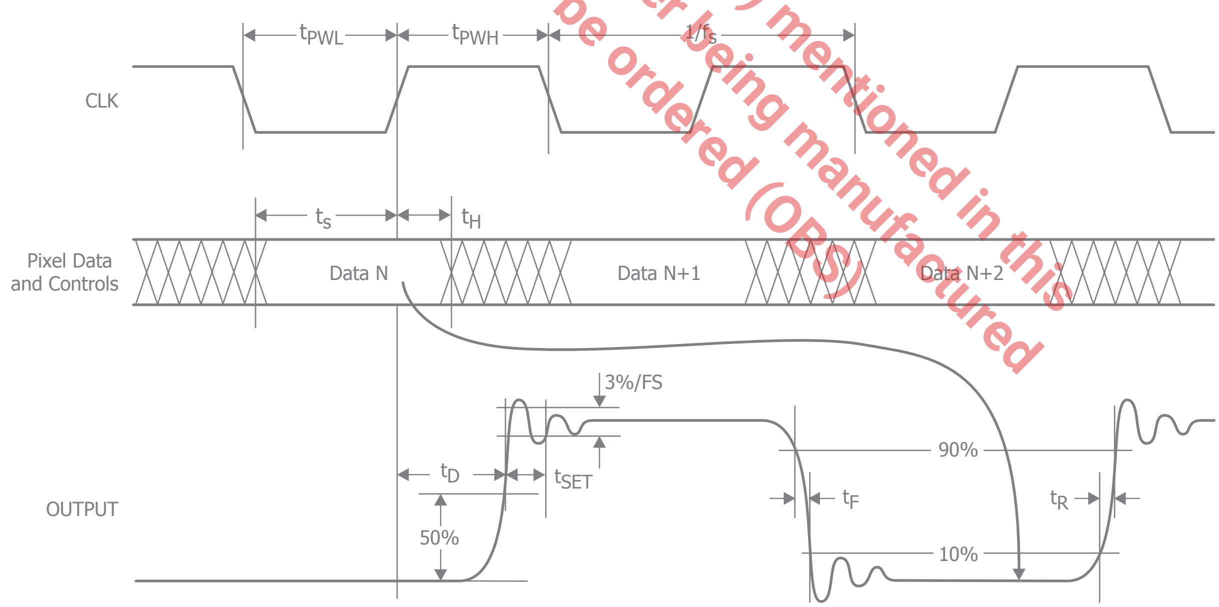


Figure 1. CDK3405 Timing Diagram

Functional Description

Within the CDK3405 are three identical 8-bit D/A converters, each with a current source output. External loads are required to convert the current to voltage outputs. Data inputs RGB7-0 are overridden by the $\overline{\text{BLANK}}$ input. $\overline{\text{SYNC}}$ = H activates, sync current from I_{OS} for sync-on-green video signals.

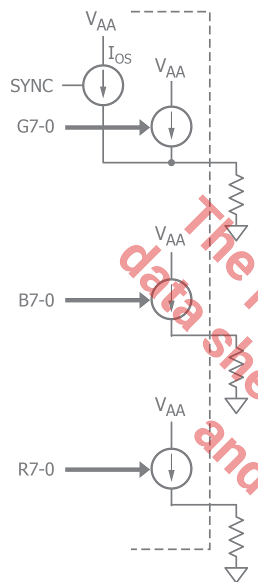


Figure 2. CDK3405 Current Source Structure

Digital Inputs

Incoming GBR data is regsitered on the rising edge of the clock input, CLK. Analog outputs follow the rising edge of CLK after a delay, t_{DO}.

Clock Input - CLK

Pixel data is registered on the rising edge of CLK. CLK should be driven by a dedicated buffer to avoid reflection induced jitter, overshoot, and undershoot.

Pixel Data Inputs - R7-0, B7-0, G7-0

RGB digital inputs are registered on the rising edge of CLK.

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$

$\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs control the output level (Figure 3 and Table 1, on the previous page) of the D/A converters during CRT retrace intervals. $\overline{\text{BLANK}}$ forces the D/A outputs to the blanking level while $\overline{\text{SYNC}}$ = L turns off a current source, I_{OS}, that is connected to the green D/A converter. $\overline{\text{SYNC}}$ = H adds a 112/256 fraction of full-scale current to the green output. $\overline{\text{SYNC}}$ = L extinguishes the sync current during the sync tip.

$\overline{\text{BLANK}}$ gates the D/A inputs. If $\overline{\text{BLANK}}$ = HIGH, the D/A inputs control the output currents to be added to the output blanking level. If $\overline{\text{BLANK}}$ = Low, data inputs and the pedestal are disabled.

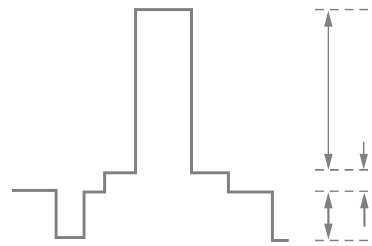


Figure 3. Normal Output Levels

Sync Pulse Input - $\overline{\text{SYNC}}$

Bringing $\overline{\text{SYNC}}$ LOW, disables a current source which superimposes a sync pulse on the IO_G output. $\overline{\text{SYNC}}$ and pixel data are registered on the rising edge of CLK. $\overline{\text{SYNC}}$ does not override any other data and should be used only during the blanking interval. If sync pulses are not required, $\overline{\text{SYNC}}$ should be connected to GND.

Blanking Input - $\overline{\text{BLANK}}$

When $\overline{\text{BLANK}}$ is LOW, pixel data inputs are ignored and the D/A converter outputs are driven to the blanking level. $\overline{\text{BLANK}}$ is registered on the rising edge of CLK.

D/A Outputs

Each D/A output is a current source from the V_{DDA} supply. Expressed in current units, the GBR transformation from data to current is as follows:

G = G7-0 & $\overline{\text{BLANK}}$ + $\overline{\text{SYNC}}$ * 112

B = B7-0 & $\overline{\text{BLANK}}$

R = R7-0 & $\overline{\text{BLANK}}$

Typical LSB current step is 73.2μA. To obtain a voltage output, a resistor must be connected to ground. Output voltage depends upon this external resistor, the reference voltage, and the value of the gain-setting resistor connected between R_{REF} and GND.

To implement a doubly-terminated 75Ω transmission line, a shunt 75Ω resistor should be placed adjacent to the analog output pin. With a terminated 75Ω line connected to the analog output, the load on the CDK3405 current source is 37.5Ω.

The CDK3405 may also be operated with a single 75Ω terminating resistor. To lower the output voltage swing to the desired range, the nominal value of the resistor on R_{REF} should be doubled.

R, G, and B Current Outputs - IO_R, IO_G, IO_B

Current source outputs can drive VESA VSIS, and RS-343A/SMPTE-170M compatible levels into doubly-terminated 75Ω lines. Sync pulses can be added to the green output. When $\overline{\text{SYNC}}$ is HIGH, the current added to IO_G is:

$IO_S = 2.33\ (V_{REF}/\ R_{REF})$

Current-Setting Resistor - R_{REF}

Full-scale output current of each D/A converter is determined by the value of the resistor connected between R_{REF} and GND. Nominal value of R_{REF} is found from:

$R_{REF} = 5.31\ (V_{REF}/I_{FS})$

where I_{FS} is the full-scale (white) output current (in amps) from the D/A converter (without sync). Sync is 0.439 * I_{FS}.

D/A full-scale (white) current may also be calculated from:

$I_{FS} = V_{FS}/R_L$

Where V_{FS} is the white voltage level and R_L is the total resistive load (Ω) on each D/A converter. V_{FS} is the blank to full-scale voltage.

Voltage Reference

Full scale current is a multiple of the current I_{SET} through an external resistor, R_{SET} connected between the R_{REF} pin and GND. Voltage across R_{SET} is the reference voltage, V_{REF}, which can be derived from either the 1.25 volt internal bandgap reference or an external voltage reference connected to V_{REF}. To minimize noise, a 0.1μF capacitor should be connected between V_{REF} and ground. I_{SET} is mirrored to each of the GBR output current sources. To minimize noise, a 0.1μF capacitor should be connected between the COMP pin and the analog supply voltage V_{AA}.

Voltage Reference Output/Input - V_{REF}

An internal voltage source of +1.25V is output on the V_{REF} pin. An external +1.25V reference may be applied to override the internal reference. Decoupling V_{REF} to GND with a 0.1μF ceramic capacitor is required.

Power and Ground

Required power is a single +3.3V supply. To minimize power supply induced noise, analog +3.3V should be connected to all three supply pins with 0.1μF and 0.01μF decoupling capacitors placed adjacent to each V_{AA} pin or pin pair.

The high slew-rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high-frequency components of the CLK signal, as well as the video output signal, the resulting data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance. All ground pins should be connected to a common solid ground plane for best performance.

Applications Dicussion

Figure 9 (on the following page) illustrates a typical CDK3405 interface circuit. In this example, an optional 1.2V bandgap reference is connected to the V_{REF} output, overriding the internal voltage reference source.

Grounding

It is important that the CDK3405 power supply is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit. The CDK3405 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages come from the system analog power source and all ground connections (GND) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor D/A conversion. Consider the following suggestions when doing the layout:

1. Keep the critical analog traces (V_{REF}, I_{REF}, COMP, IO_S, IO_R, IO_G) as short as possible and as far as possible from all digital signals. The CDK3405 should be located near the board edge, close to the analog out-put connectors.
2. The power plane for the CDK3405 should be separate from that which supplies the digital circuitry. A single power plane should be used for all of the V_{AA} pins. If the power supply for the CDK3405 is the same as that of the system's digital circuitry, power to the CDK3405 should be decoupled with 0.1µF and 0.01µF capacitors and isolated with a ferrite bead.
3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.
4. If the digital power supply has a dedicated power plane layer, it should not be placed under the CDK3405, the voltage reference, or the analog outputs. Capacitive coupling of digital power supply noise from this layer to the CDK3405 and its related analog circuitry can have an adverse effect on performance.
5. CLK should be handled carefully. Jitter and noise on this clock will degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

Improved Transisiton Times

Output shunt capacitance dominates slowing of output transition times, whereas series inductance causes a small amount of ringing that affects overshoot and settling time. With a doubly terminated 75Ω load, transition times can be improved by matching the capacitive impedance output of the CDK3405. Output capacitance can be matched with a 220nH inductor in series with the 75Ω source termination.

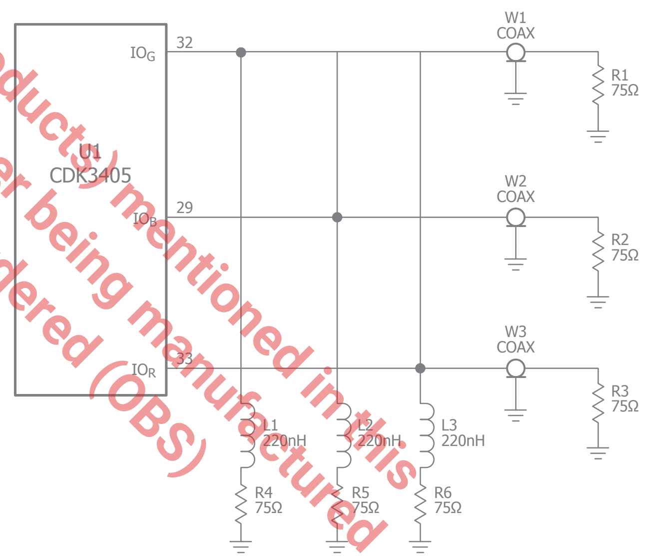


Figure 4. Schematic, Transition Time Sharpening Circuit

A 220nH inductor trims the performance of a 4ft cable, quite well. In Figures 5 through 8, the glitch at 12.5ns, is due to a reflection from the source. Not shown, are smaller glitches at 25 and 37.5ns, corresponding to secondary and tertiary reflections. Inductor values should be selected to match the length and type of the cable.

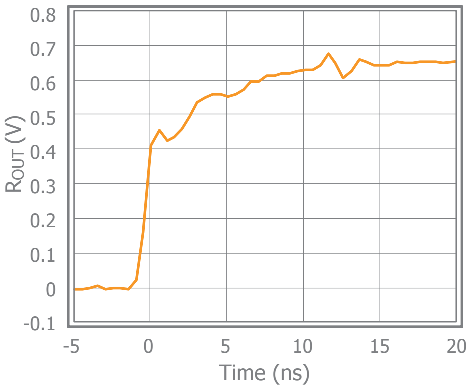


Figure 5. Unmatched t_R

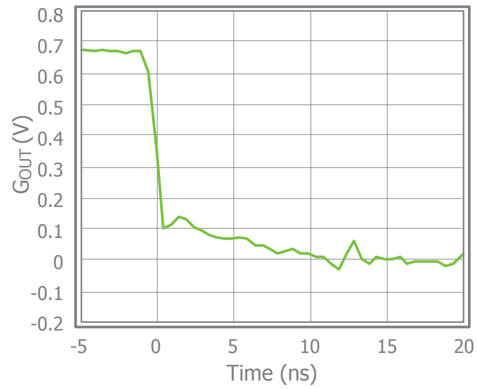


Figure 7. Unmatched t_F

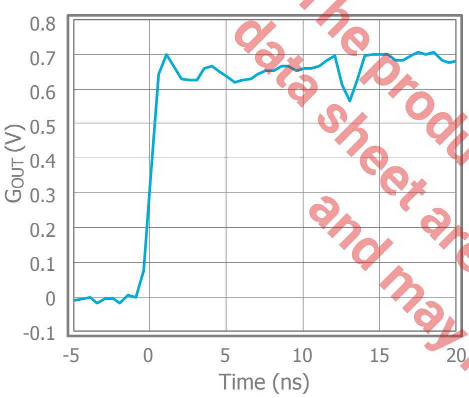


Figure 6. Matched t_R

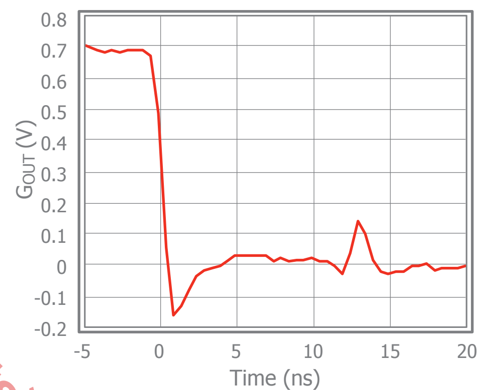


Figure 8. Matched t_F

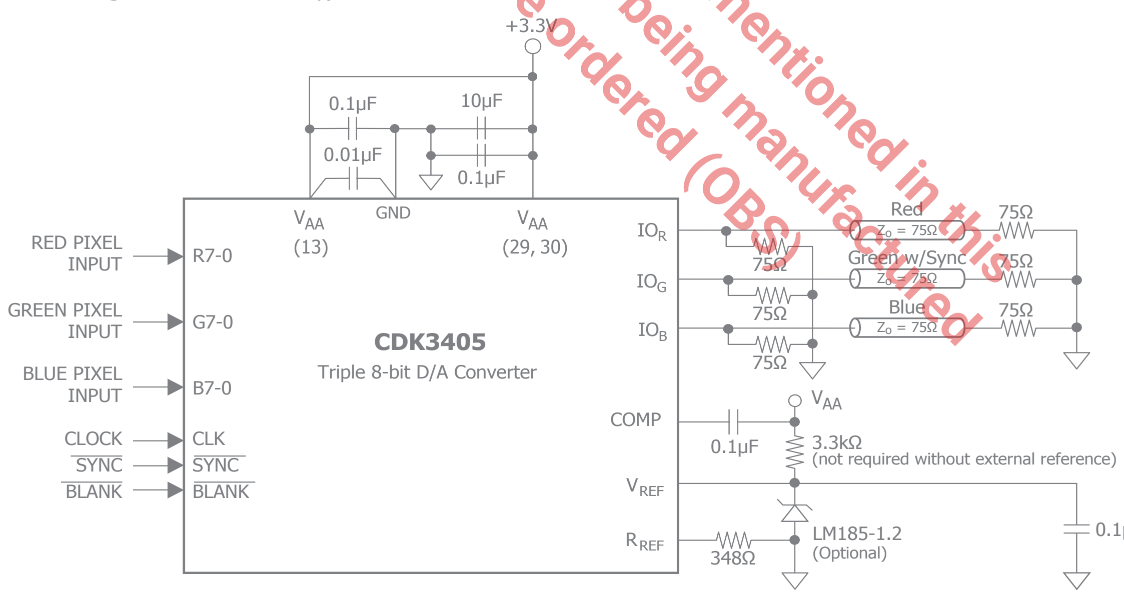


Figure 9. Typical Interface Circuit Diagram

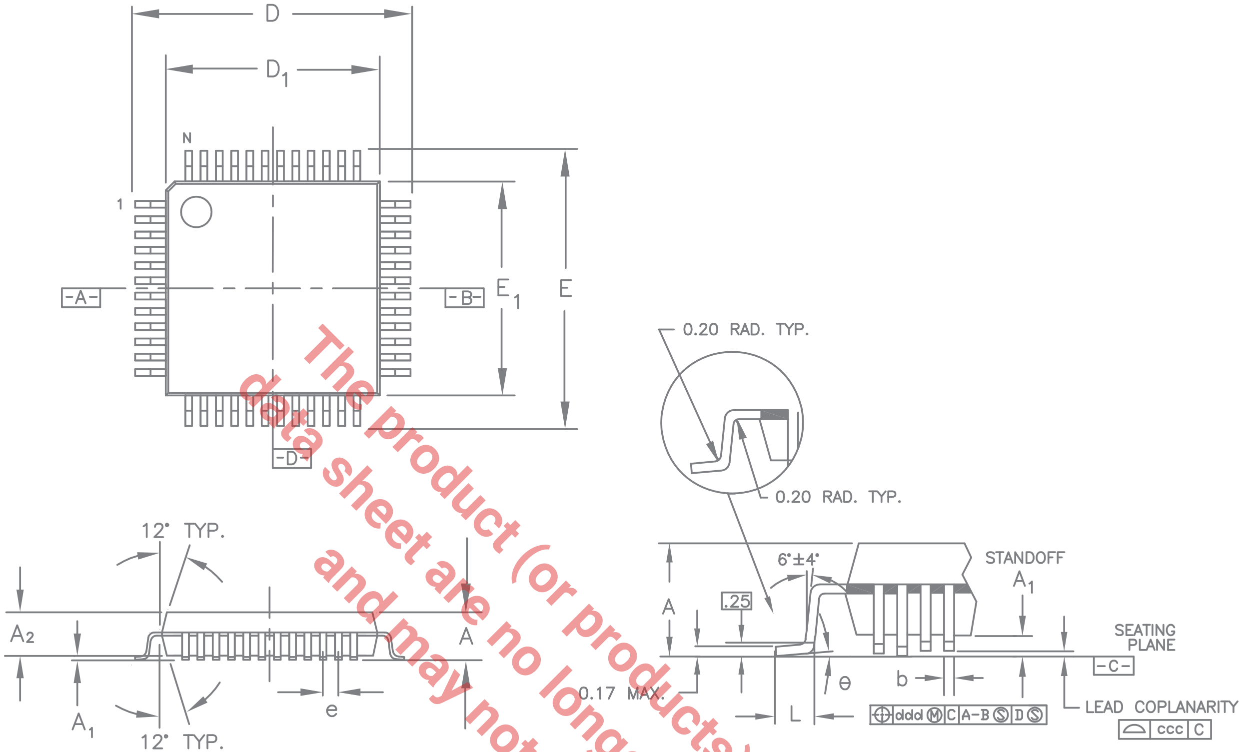
Evaluation boards are available (CEB3405), contact CADEKA for more information.

Related Products

- CDK3400/3401 Triple 10-bit 180MSPS DACs
- CDK3404 Triple 8-bit 180MSPS DAC

Mechanical Dimensions

TQFP-48 Package



LEAD COUNT		48L
DIMS.	TOL.	
A	MAX.	1.20
A_1	±.05	0.1
A_2	±.05	1.00
D	±.20	9.00
D_1	±.10	7.00
E	±.20	9.00
E_1	±.10	7.00
L	+.15/−.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°−7°
ddd	MAX.	.08
ccc	MAX.	.08
JEDEC REFERENCE DRAWING VARIATION DESIGNATOR		MS−026 ABC

NOTES.
1. All dimensions in mm.
2. Dimension shown are nominal with tolerances indicated.
3. Foot length 'L' is measured at gage plane 0.25mm above seating plane.
4. L/F: Eftec 64T Cu or equivalent, 0.127mm (0.005") thick

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A New Direction in Mixed-Signal